BCM8112
PRODUCT Brief

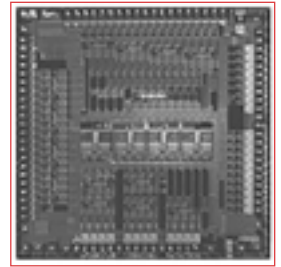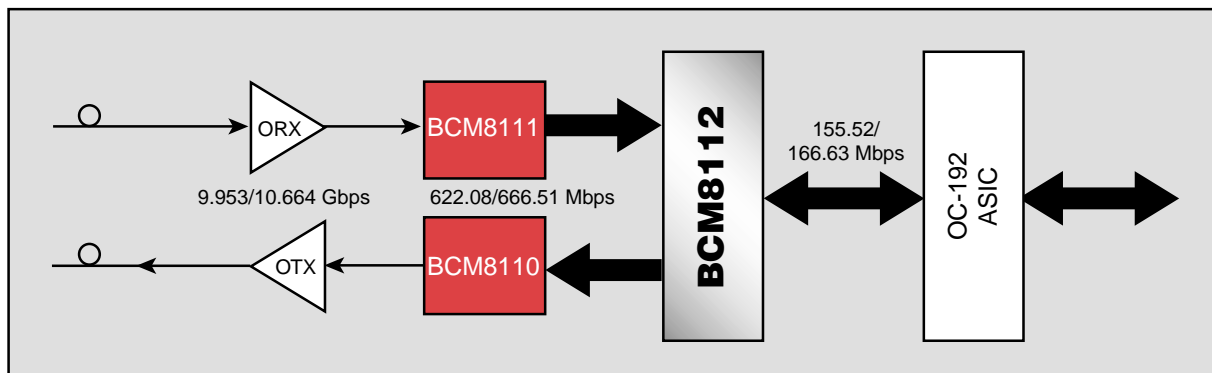**BROADCOM®**

16-BIT LVDS AND 64-BIT LVPECL INTERFACE

BCM8112 FEATURES

- **64:16 MUX with single-ended LVPECL 155.52/166.65-Mbps data inputs and LVDS 622.08/644.45-Mbps differential data outputs**
- **16:64 DEMUX with LVDS 622.08/644.45 Mbps differential data inputs and 155.52/166.65 Mbps series terminated logic (STL) single-ended data outputs**
- **On-chip 64 x 9 FIFO to eliminate system timing issues**
- **Core power supply: 1.8V**
- **I/O power supplies: 1.8V LVDS, 3.3V STL, and 3.3V CMOS**
- **Power consumption: 1700 mW typical**
- **Standard CMOS fabrication process**
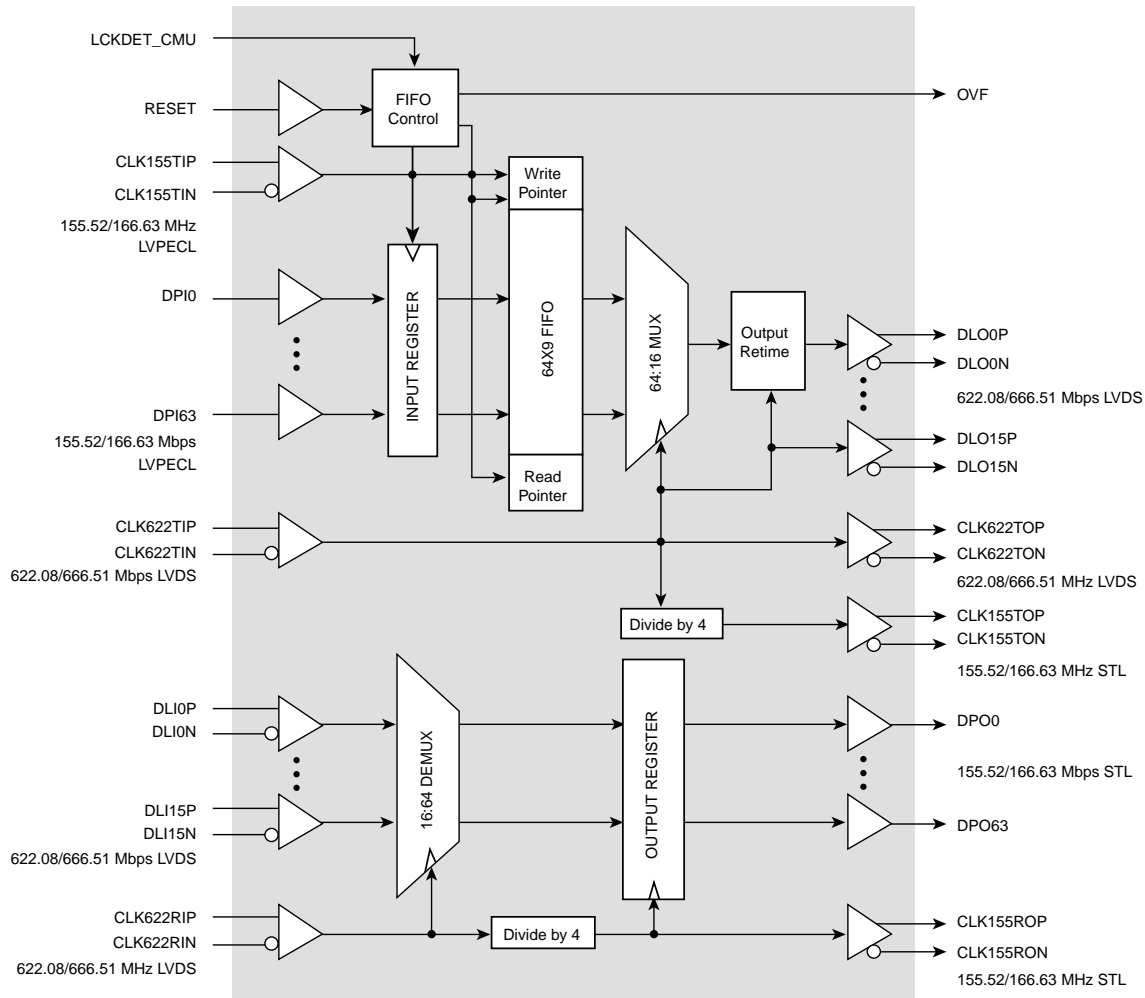- **452-pin BGA package**

SUMMARY OF BENEFITS

- **Compliant with industry standards such as: Optical Internetworking Forum (OIF), Telcordia, and ITU-T standards.**
- **High level of integration allows for higher port density solutions.**
- **CMOS-based device uses the most effective silicon economy of scale.**
- **Low power consumption eliminates the need for external cooling sources.**
- **Target applications:**
  - OC-192/STM-64 transmission equipment
  - SONET/SDH optical modules
  - ADD/DROP multiplexers
  - Digital cross-connects
  - ATM switch backbone
  - SONET test equipment
  - Terabit routers
  - Edge routers

Application Block Diagram

Interface Block Diagram

The **BCM8112** 16/64 LVDS/LVPECL interface is a fully integrated, 64:16 MUX and 16:64 DEMUX. The low-speed, 64-bit interface operates at 155.52/166.65 Mbps, and the high-speed, 16-bit interface operates at 622.08/644.45 Mbps. The 64-bit input interface is LVPECL, while the 64-bit output interface is STL. Both the 16-bit input and output interfaces are LVDS.

An on-chip 64 x 9 FIFO reduces any system timing issues. In OC-192 applications, this device can be used as an interface between a 64-bit LVPECL ASIC and 16-bit LVDS BCM8110/8111 OC-192 transmitter/receiver. The **BCM8112** comes in a 35 x 35 mm BGA package.

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