5-BIT PROGRAMMABLE SYNCHRONOUS BUCK CONTROLLER IC WITH TRIPLE LDO CONTROLLER

FEATURES

- Provides single chip solution for Vcore, GTL+, AGP bus, and 1.8V
- Automatic voltage selection for AGP slot V_{DDQ} supply
- Linear Regulator Controller On-Board for 1.8V
- Designed to meet Intel latest VRM specification for next generation microprocessors
- On-Board DAC programs the output voltage from 1.3V to 3.5V
- Linear Regulator Controller On-Board for 1.5V GTL+ Supply
- Loss-less Short Circuit Protection for all Outputs
- Synchronous operation allows maximum efficiency
- Patented architecture allows fixed frequency operation as well as 100% duty cycle during dynamic load
- Minimum Part Count
- Soft-Start
- High current totem pole driver for direct driving of the external Power MOSFET
- Power Good function monitors all outputs
- Over-Voltage Protection Circuitry Protects the switcher output and generates a Fault output

APPLICATIONS

- Total Power Solution for next generation Intel processor application

DESCRIPTION

The IRU3021M controller IC is specifically designed to meet Intel specification for next generation microprocessor applications requiring multiple on-board regulators. The IRU3021M provides a single chip controller IC for the Vcore, three LDO controllers, one with an automatic select pin that connects to the Type Detect pin of the AGP slot for the AGP V_{DDQ} supply, one for GTL+ and the other for the 1.8V chip set regulator as required for the next generation PC applications. The IRU3021M uses N-channel MOSFET as pass transistor for $V_{OUT}2(V_{DDQ})$, $V_{OUT}3(1.5V)$ and $V_{OUT}4(1.8V)$. No external resistor divider is necessary for any of the regulators. The switching regulator feature a patented topology that in combination with a few external components as shown in the typical application circuit, will provide well in excess of 20A of output current for an on-board DC/DC converter while automatically providing the right output voltage via the 5-bit internal DAC .The IRU3021M also features, loss-less current sensing for both switcher by using the $R_{DS(ON)}$ of the high-side power MOSFET as the sensing resistor, an output under-voltage shutdown that detects short circuit condition for the linear outputs and latches the system off, and a Power Good window comparator that switches its open collector output low when any one of the outputs is outside of a pre-programmed window.

TYPICAL APPLICATION

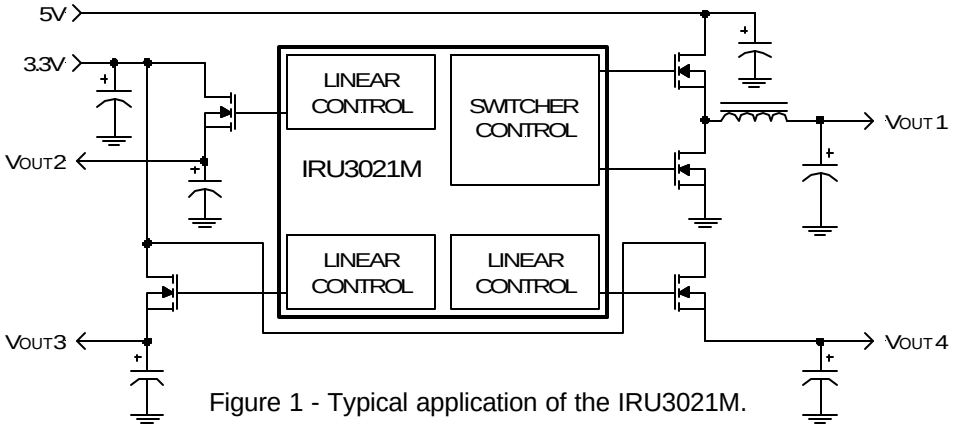


Figure 1 - Typical application of the IRU3021M.

PACKAGE ORDER INFORMATION

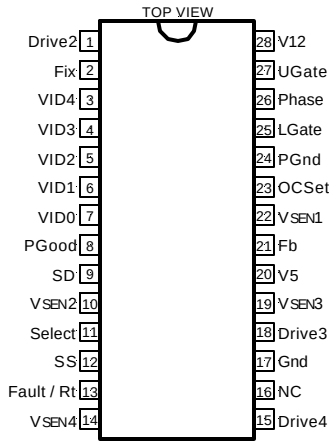
T_A (°C)	DEVICE	PACKAGE
0 To 70	IRU3021MCW	28-Pin Plastic SOIC WB

ABSOLUTE MAXIMUM RATINGS

V5 Supply Voltage 7V
V12 Supply Voltage 20V
Storage Temperature Range ..... -65°C To 150°C
Operating Junction Temperature Range ..... 0°C To 125°C

PACKAGE INFORMATION

28-PIN WIDE BODY PLASTIC SOIC (W)



θ_{JA} =80°C/W

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V12=12V, V5=5V and T_A=0 to 70°C. Typical values refer to T_A=25°C. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Supply UVLO Section						
UVLO Threshold-12V		Supply Ramping Up		10		V
UVLO Hysteresis-12V				0.6		V
UVLO Threshold-5V		Supply Ramping Up		4.4		V
UVLO Hysteresis-5V				0.3		V
Supply Current						
Operating Supply Current		V12 V5		6 30		mA
Switching Controllers; Vcore (V_{SEN}1) and AGP (V_{SEN}2)						
VID Section (Vcore only)						
DAC Output Voltage (Note 1)			0.99Vs	Vs	1.01Vs	V
DAC Output Line Regulation				0.1		%
DAC Output Temp Variation				0.5		%
VID Input LO					0.8	V
VID Input HI			2			V
VID Input Internal Pull-Up Resistor to V5				27		KΩ
V_{SEN}2 Voltage		Select <0.8V Select >2V		1.5 3.3		V

PARAMETER	SYM	TEST CONDITION	MIN	TYP	MAX	UNITS
Error Comparator Section						
Input Bias Current					2	µA
Input Offset Voltage			-2		+2	mV
Delay to Outout		V_{DIFF}=10mV			100	ns
Current Limit Section						
CS Threshold Set Current				200		µA
CS Comp Offset Voltage			-5		+5	mV
Hiccup Duty Cycle		Css=0.1µF		10		%
Output Drivers Section						
Rise Time		C_L=3000pF		70		ns
Fall Time		C_L=3000pF		70		ns
Dead Band Time Between High Side and Synch Drive (Vcore Switcher Only)		C_L=3000pF		200		ns
Oscillator Section (Internal)						
Osc Frequency		Rt=Open		217		KHz
1.8V Regulator (V_{SEN}4)						
V_{SEN} Voltage	V_O4	T_A=25°C, Drive4=V_{SEN}4		1.800		V
V_{SEN} Voltage				1.800		V
Input Bias Current					2	µA
Output Drive Current		V_{AUX} - V_{DRIVE}>0.6V	50			mA
1.5V Regulator (V_{SEN}3)						
V_{SEN} Voltage	V_O3	T_A=25°C, Drive3=V_{SEN}3		1.500		V
V_{SEN} Voltage				1.500		V
Input Bias Current					2	µA
Output Drive Current		V_{AUX} - V_{DRIVE}>0.6V	50			mA
Power Good Section						
V_{SEN}1 UV Lower Trip Point		V_{SEN}1 Ramping Down		0.90Vs		V
V_{SEN}1 UV Upper Trip Point		V_{SEN}1 Ramping Up		0.92Vs		V
V_{SEN}1 UV Hysterises				0.02Vs		V
V_{SEN}1 HV Upper Trip Point		V_{SEN}1 Ramping Up		1.10Vs		V
V_{SEN}1 HV Lower Trip Point		V_{SEN}1 Ramping Down		1.08Vs		V
V_{SEN}1 HV Hysterises				0.02Vs		V
V_{SEN}2 Trip Point		Select <0.8V Select >2V		1.100 2.560		V
V_{SEN}3 Trip Point		Fix=Gnd Fix=Open		0.920 1.320		V
V_{SEN}4 Trip Point		Fix=Gnd Fix=Open		0.920 1.140		V
Power Good Output LO		R_L=3mA		0.4		V
Power Good Output HI		R_L=5K, Pull-Up to 5V		4.8		V
Fault (Overvoltage) Section						
Core OV Upper Trip Point		V_{SEN}1 Ramping Up		1.17Vs		V
Core OV Lower Trip Point		V_{SEN}1 Ramping Down		1.15Vs		V
Fault Output HI		Io=3mA		10		V
Soft-Start Section						
Pull-Up Resistor to 5V		OCSet=0V, Phase=5V		20		µA

Note 1: Vs refers to the set point voltage given in Table 1.

D4	D3	D2	D1	D0	Vs
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00
0	0	0	0	0	2.05

D4	D3	D2	D1	D0	Vs
1	1	1	1	1	2.0
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

Table 1 - Set point voltage vs. VID codes.

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Drive2	This pin controls the gate of an external MOSFET for the AGP linear regulator.
2	Fix	Leaving this pin open provides fixed output voltages of the 1.5V and 1.8V for the #3 and #4 linear regulators. When this pin is grounded the reference to the linear regulators are set to 1.26V and therefore the output of the regulators can be programmed to any voltages above the 1.26V using: $V_{OUT}=1.26 \times (1 + R_{TOP}/R_{BOT})$ Where: R_{TOP} = Top resistor connected from the output to the V_{SENSE} pin. R_{BOT} = Bottom resistor connected from the V_{SENSE} pin to ground.
3	VID4	This pin selects a range of output voltages for the DAC. When in the LOW state the range is 1.3V to 2.05V and when it switches to HI state the range is 2.0V to 3.5V. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
4	VID3	MSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
5	VID2	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
6	VID1	Input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
7	VID0	LSB input to the DAC that programs the output voltage. This pin is TTL compatible that realizes a logic “1” as either HI or Open. When left open, this pin is pulled up internally by a 27KΩ resistor to 5V supply.
8	PGood	This pin is an open collector output that switches LO when any of the outputs are outside of the specified under-voltage trip point. It also switches low when $V_{SEN}1$ pin is more than 10% above the DAC voltage setting.

PIN#	PIN SYMBOL	PIN DESCRIPTION
9	SD	This pin provides shutdown for all the regulators. A TTL compatible, logic level high applied to this pin disables all the outputs and discharges the soft-start capacitor. The SD signal turns off the synchronous MOSFET allowing body diode to conduct and discharge the output capacitor.
10	$V_{SEN}2$	This pin provides the feedback for the AGP linear regulator. The Select pin when connected to the "Type Detect" pin of the AGP slot automatically selects the right voltage for the AGP V_{DDQ}.
11	Select	This pin provides automatic voltage selection for the AGP switching regulator. When it is pulled LO, the voltage is 1.5V and when left open or pulled to HI, the voltage is 3.3V.
12	SS	This pin provides the soft-start for all the regulators. An internal current source charges an external capacitor that is connected from this pin to ground which ramps up the outputs of the regulators, preventing the outputs from overshooting as well as limiting the input current. The second function of the Soft-Start cap is to provide long off time (HICCUP) for the synchronous MOSFET during current limiting.
13	Fault / Rt	This pin has dual function. It acts as an output of the over-voltage protection circuitry or it can be used to program the frequency using an external resistor. When used as a fault detector, if any of the switcher outputs exceed the OVP trip point, the Fault pin switches to 12V and the soft-start cap is discharged. If the Fault pin is to be connected to any external circuitry, it needs to be buffered.
14	$V_{SEN}4$	This pin provides the feedback for the linear regulator that its output drive is Drive4.
15	Drive4	This pin controls the gate of an external MOSFET for the 1.8V chip set linear regulator.
16	NC	This pin is not connected internally.
17	Gnd	This pin serves as the ground pin and must be connected directly to the ground plane.
18	Drive3	This pin controls the gate of an external transistor for the 1.5V GTL+ linear regulator.
19	$V_{SEN}3$	This pin provides the feedback for the linear regulator that its output drive is Drive3.
20	V5	5V supply voltage. A high frequency capacitor (0.1 to 1µF) must be placed close to this pin and connected from this pin to the ground plane for noise free operation.
21	Fb	This pin provides the feedback for the synchronous switching regulator. Typically this pin can be connected directly to the output of the switching regulator. However, a resistor divider is recommended to be connected from this pin to $V_{OUT}1$ and ground to adjust the output voltage for any drop in the output voltage that is caused by the trace resistance. The value of the resistor connected from $V_{OUT}1$ to Fb1 must be less than 1000Ω.
22	$V_{SEN}1$	This pin is internally connected to the under-voltage and over-voltage comparators sensing the Vcore status. It must be connected directly to the Vcore supply.
23	OCSet	This pin is connected to the Drain of the power MOSFET of the Core supply and it provides the positive sensing for the internal current sensing circuitry. An external resistor programs the current sense threshold depending on the R_{DS} of the power MOSFET. An external capacitor is placed in parallel with the programming resistor to provide high frequency noise filtering.
24	PGnd	This pin serves as the Power ground pin and must be connected directly to the ground plane close to the source of the synchronous MOSFET. A high frequency capacitor (typically 1µF) must be connected from V12 pin to this pin for noise free operation.
25	LGate	Output driver for the synchronous power MOSFET for the Core supply.
26	Phase	This pin is connected to the source of the power MOSFET for the Core supply and it provides the negative sensing for the internal current sensing circuitry.
27	UGate	Output driver for the high side power MOSFET for the Core supply.
28	V12	This pin is connected to the 12V supply and serves as the power Vcc pin for the output drivers. A high frequency capacitor (typically 1µF) must be placed close to this pin and PGnd pin and be connected directly from this pin to the ground plane for the noise free operation.

BLOCK DIAGRAM

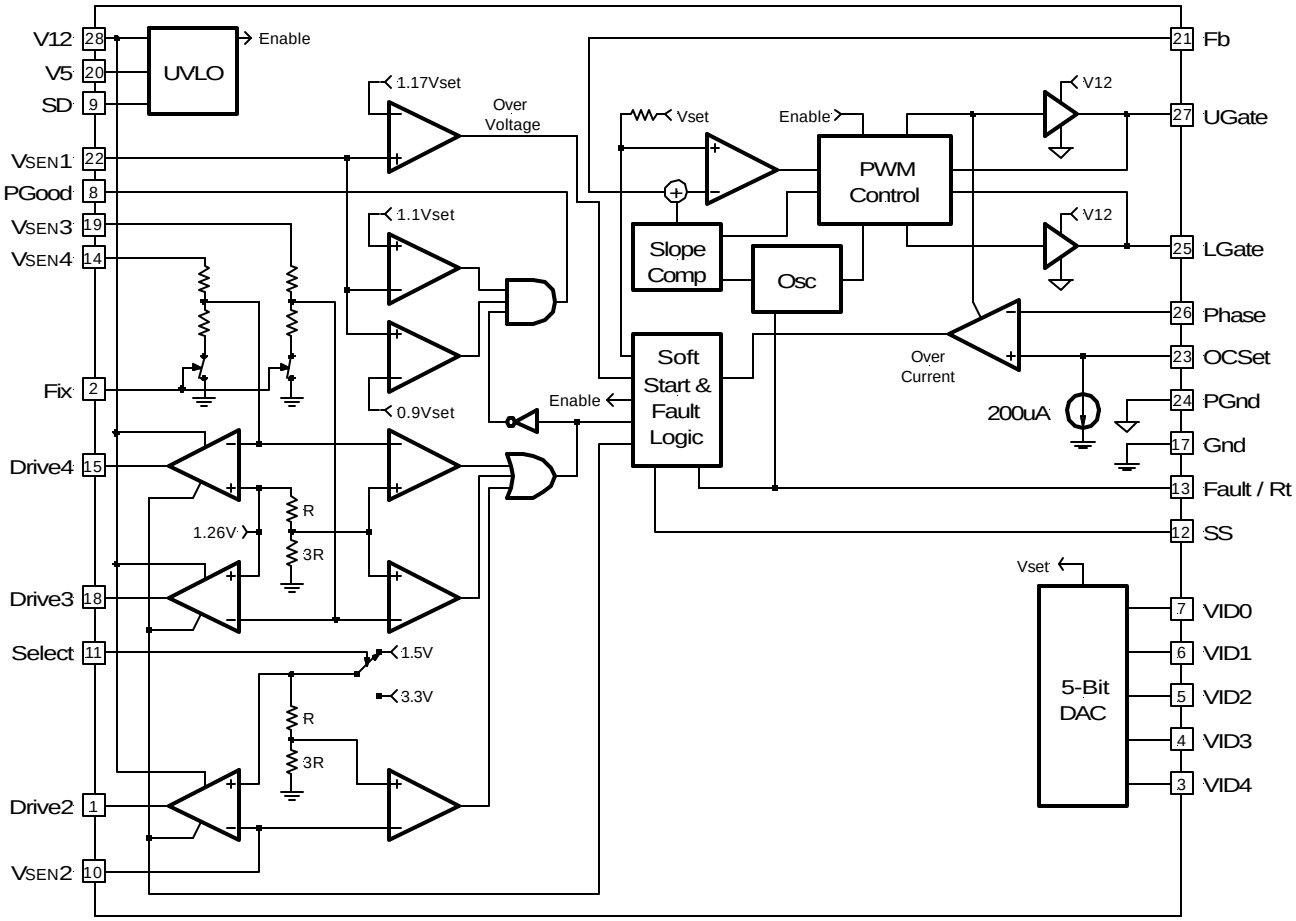


Figure 2 - Simplified block diagram of the IRU3021M.

TYPICAL APPLICATION

(Dual Layout with HIP6021)

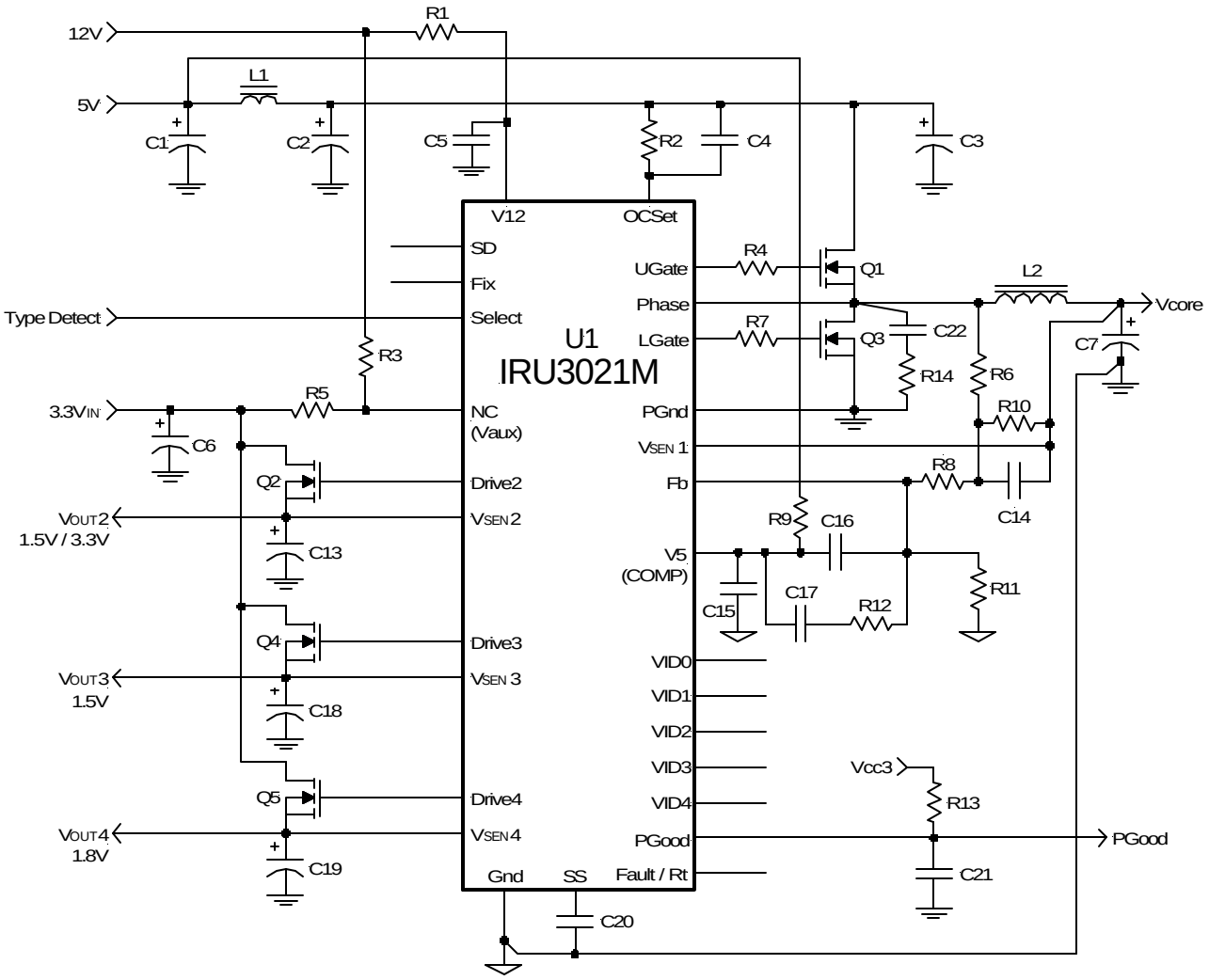


Figure 3 - Typical application of IRU3021M in a dual layout with HIP6021 for an on-board DC-DC converter providing power for the Vcore, GTL+, 1.8V chip set supply as well as auto select AGP supply for the next generation PC applications.

Part#	R3	R5	R9	R12	C15	C16	C17
HIP6021	O	S	O	V	O	V	V
IRU3021M	S	O	S	O	V	O	O

S - Short O - Open V - See IR or Harris parts list for the value

Table 2 - Dual layout component table.

IRU3021M APPLICATION PARTS LIST

Dual Layout with HIP6021

Ref Desig	Description	Qty	Part #	Manuf
Q1	MOSFET	1	IRL3103S, TO-263 package	IR
Q2	MOSFET	1	IRLR3103, TO-252 package	IR
Q3	MOSFET with Schottky	1	IRL3103D1S, TO-263 package	IR
Q4,5	MOSFET	2	IRLR024, TO-252 package	IR
L1	Inductor	1	L=1μH, 5052 core with 4 turns of 1.0mm wire	Micro Metal
L2	Inductor	1	L=2.7μH, 5052B core with 7 turns of 1.2mm wire	Micro Metal
C1	Capacitor, Electrolytic	1	10MV470GX, 470μF, 10V	Sanyo
C2,3	Capacitor, Electrolytic	2	10MV1200GX, 1200μF, 10V	Sanyo
C4	Capacitor, Ceramic	1	220pF, 0603	
C5	Capacitor, Ceramic	1	1μF, 0805	
C6,18	Capacitor, Electrolytic	2	6MV1000GX, 1000μF, 6.3V	Sanyo
C7	Capacitor, Electrolytic	6	6MV1500GX, 1500μF, 6.3V	Sanyo
C13,19	Capacitor, Electrolytic	1	6MV1500GX, 1500μF, 6.3V	Sanyo
C14,15	Capacitor, Ceramic	2	1μF, 0603	
C16,17	Capacitor, Ceramic	2	See Table 2, dual layout component 0603 × 2	
C20,21	Capacitor, Ceramic	2	0.1μF, 0603	
C22	Capacitor, Ceramic	1	1000pF, 0603	
R1	Resistor	1	10Ω, 5%, 0603	
R2	Resistor	1	3.3KΩ, 5%, 0603	
R3,5,12	Resistor	3	See Table 2, dual layout component 0603 × 3	
R4,7,14	Resistor	3	4.7Ω, 5%, 1206	
R6,8,10	Resistor	3	2.2KΩ, 1%, 0603	
R9	Resistor	1	0Ω, 0603	
R11	Resistor	1	220KΩ, 1%, 0603	
R13	Resistor	1	10KΩ, 5%, 0603	

International
IOR Rectifier

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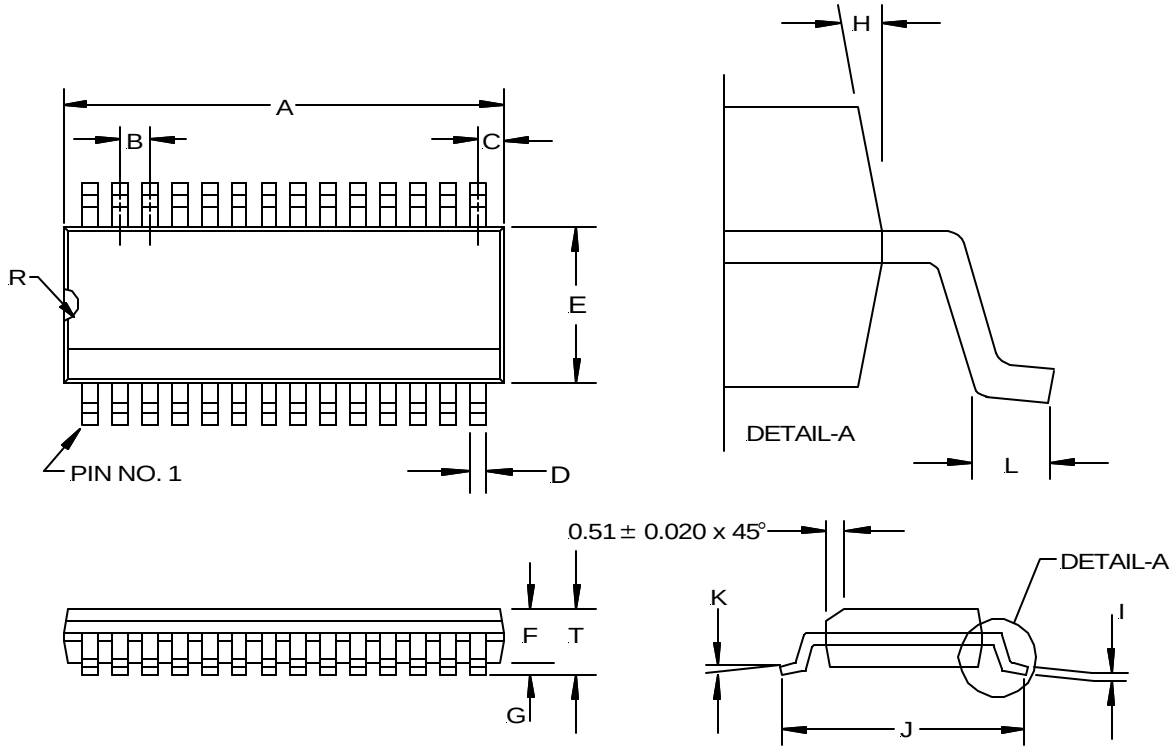
(W) SOIC Package
28-Pin Surface Mount, Wide Body

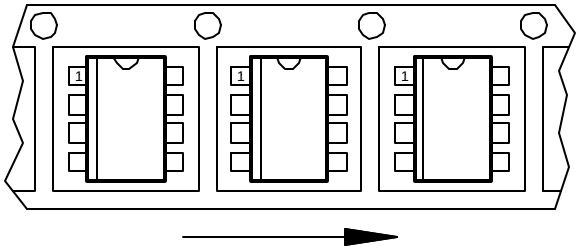


SYMBOL	28-PIN	
	MIN	MAX
A	17.73	17.93
B	1.27 BSC	
C	0.66 REF	
D	0.36	0.46
E	7.40	7.60
F	2.44	2.64
G	0.10	0.30
I	0.23	0.32
J	10.11	10.51
K	0°	8°
L	0.51	1.01
R	0.63	0.89
T	2.44	2.64

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.

PACKAGE SHIPMENT METHOD

PKG DESIG	PACKAGE DESCRIPTION	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Orientation
W	SOIC, Wide Body	28	27	1000	Fig A



Feed Direction
Figure A

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