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Single Synchronous Buck Pulse-Width Modulation (PWM) Controller

The ISL6520 makes simple work out of implementing a complete control and protection scheme for a DC/DC stepdown converter. Designed to drive N-Channel MOSFETs in a synchronous buck topology, the ISL6520 integrates the control, output adjustment, monitoring and protection functions into a single 8 Lead package.

The ISL6520 provides simple, single feedback loop, voltage-mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V, with a maximum tolerance of ±1.5% over-temperature and line voltage variations. A fixed frequency oscillator reduces design complexity, while balancing typical application cost and efficiency.

The error amplifier features a 15MHz gain-bandwidth product and 8V/μs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty cycles range from 0% to 100%.

Protection from over-current conditions is provided by monitoring the $r_{DS(ON)}$ of the upper MOSFET to inhibit PWM operation appropriately. This approach simplifies the implementation and improves efficiency by eliminating the need for a current sense resistor.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6520CB*	6520CB	0 to 70	8 Ld SOIC	M8.15
ISL6520CBZ* (Note)	6520 CBZ	0 to 70	8 Ld SOIC (Pb-free)	M8.15
ISL6520IB*	6520IB	-40 to 85	8 Ld SOIC	M8.15
ISL6520IBZ* (Note)	6520 IBZ	-40 to 85	8 Ld SOIC (Pb-free)	M8.15
ISL6520CR*	ISL 6520CR	0 to 70	16 Ld 4x4mm QFN	L16.4x4
ISL6520CRZ* (Note)	65 20CRZ	0 to 70	16 Ld 4x4mm QFN (Pb-free)	L16.4x4
ISL6520IR*	ISL 6520IR	-40 to 85	16 Ld 4x4mm QFN	L16.4x4
ISL6520IRZ* (Note)	65 20IRZ	-40 to 85	16 Ld 4x4mm QFN (Pb-free)	L16.4x4
ISL6520EVAL1		Evaluation Board		

* Add “-T” suffix for tape and reel.
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Operates from +5V Input
- 0.8V to V_{IN} Output Range
  - 0.8V Internal Reference
  - ±1.5% Over Line Voltage and Temperature
- Drives N-Channel MOSFETs
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Cycle
- Lossless, Programmable Over-Current Protection
  - Uses Upper MOSFET’s $r_{DS(on)}$
- Small Converter Size
  - 300kHz Fixed Frequency Oscillator
  - Internal Soft Start
  - 8 Ld SOIC or 16Ld 4mmx4mm QFN
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Power Supplies for Microprocessors
  - PCs
  - Embedded Controllers
- Subsystem Power Supplies
  - PCI/AGP/GTL+ Buses
  - ACPI Power Control
- Cable Modems, Set Top Boxes, and DSL Modems
- DSP and Core Communications Processor Supplies
- Memory Supplies
- Personal Computer Peripherals
- Industrial Power Supplies
- 5V-Input DC/DC Regulators
- Low-Voltage Distributed Power Supplies

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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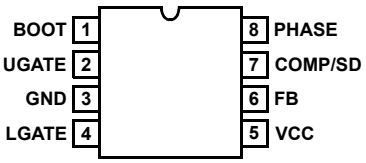
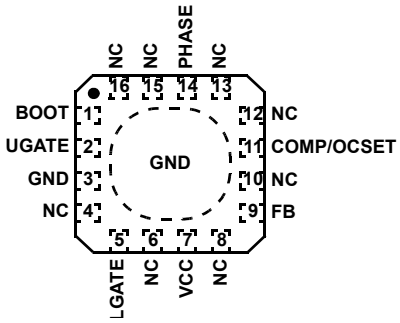
Pinouts

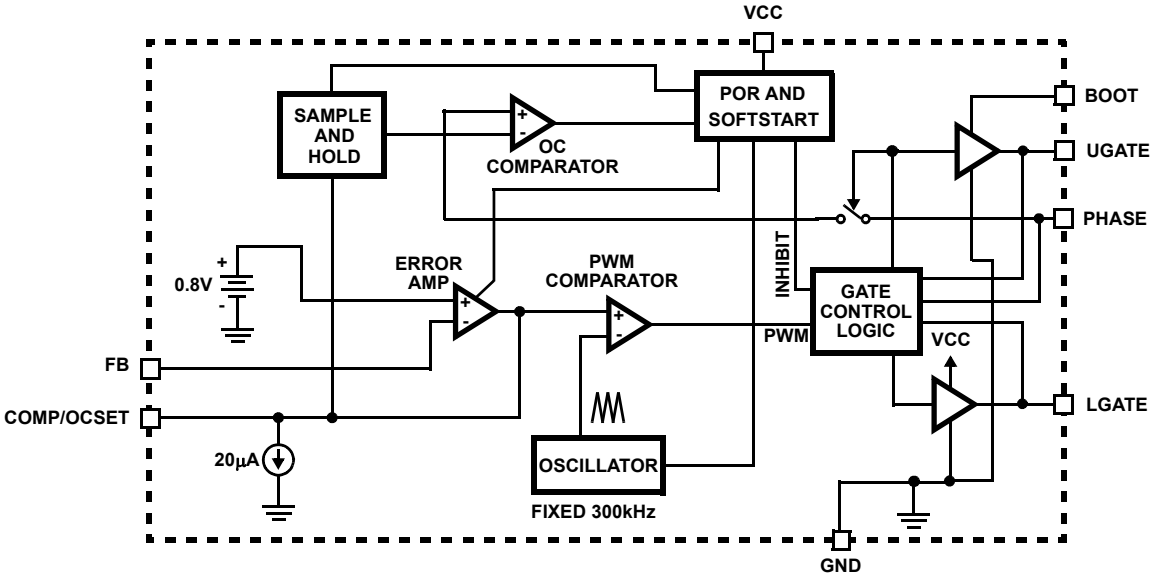
ISL6520
(8 LD SOIC)
TOP VIEW



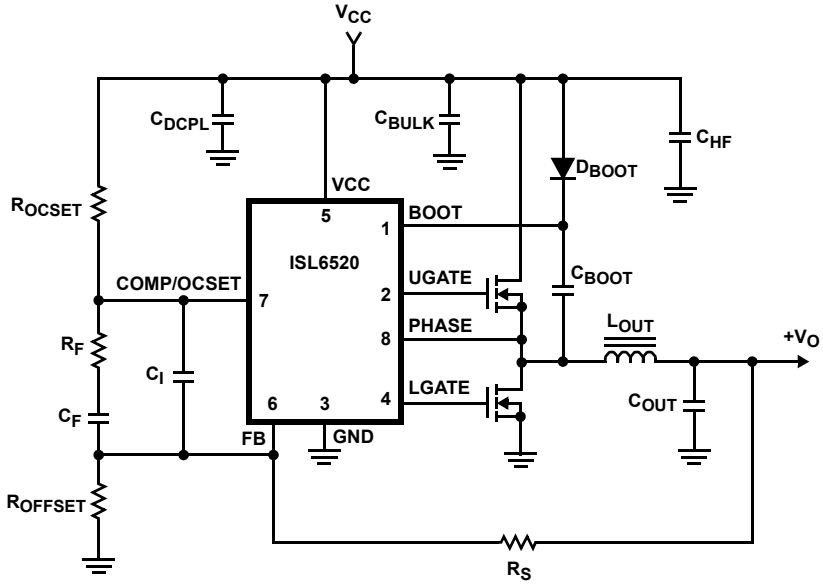
ISL6520
(16 LD QFN)
TOP VIEW



Block Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . +6.0V
Absolute Boot Voltage, V_{BOOT} . . . . . +15.0V
Upper Driver Supply Voltage, V_{BOOT} - V_{PHASE} . . . . . 7.0V (DC)
8.0V (<10ns Pulse Width, 10µJ)
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 2

Recommended Operating Conditions

Supply Voltage, VCC . . . . . +5V ±10%
Ambient Temperature Range - ISL6520C . . . . . 0°C to +70°C
Ambient Temperature Range - ISL6520I . . . . . -40°C to +85°C
Junction Temperature Range. . . . . -40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	95	N/A
QFN Package (Notes 2, 3).	45	7

Maximum Junction Temperature
(Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Maximum Lead Temperature
(Soldering 10s) . . . . . +300°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply	I_{VCC}	UGATE and LGATE Open	2.6	3.2	3.8	mA
POWER-ON RESET						
Rising VCC POR Threshold	POR		4.19	4.30	4.5	V
VCC POR Threshold Hysteresis			-	0.25	-	V
OSCILLATOR						
Frequency	f_{OSC}	ISL6520C, V_{CC} = 5V	250	300	340	kHz
		ISL6520I, V_{CC} = 5V	230	300	340	kHz
Ramp Amplitude	ΔV_{OSC}		-	1.5	-	V_{P-P}
REFERENCE						
Reference Voltage Tolerance		ISL6520C	-1.5	-	+1.5	%
		ISL6520I	-2.5		+2.5	%
Nominal Reference Voltage	V_{REF}		-	0.800	-	V
ERROR AMPLIFIER						
DC Gain		Guaranteed By Design	-	88	-	dB
Gain-Bandwidth Product	GBWP		-	15	-	MHz
Slew Rate	SR		-	8	-	V/µs
GATE DRIVERS						
Upper Gate Source Current	$I_{UGATE-SRC}$		-	-1	-	A
Upper Gate Sink Current	$I_{UGATE-SNK}$		-	1	-	A
Lower Gate Source Current	$I_{LGATE-SRC}$		-	-1	-	A
Lower Gate Sink Current	$I_{LGATE-SNK}$		-	2	-	A
PROTECTION / DISABLE						
OCSET Current Source	I_{OCSET}	ISL6520C	17	20	22	µA
		ISL6520I	14	20	24	µA
Disable Threshold	$V_{DISABLE}$		-	0.8	-	V

Functional Pin Description

VCC

This is the main bias supply for the ISL6520, as well as the lower MOSFET's gate. Connect a well-decoupled 5V supply to this pin.

FB

This pin is the inverting input of the internal error amplifier. Use this pin, in combination with the COMP/OCSET pin, to compensate the voltage-control feedback loop of the converter.

GND

This pin represents the signal and power ground for the IC. Tie this pin to the ground island/plane through the lowest impedance connection available.

PHASE

Connect this pin to the upper MOSFET source. This pin is used to monitor the voltage drop across the upper MOSFET for over-current protection. This pin is also monitored by the continuously adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.

UGATE

Connect this pin to the upper MOSFET's gate. This pin provides the PWM-controlled gate drive for the upper MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off. Do not insert any circuitry between this pin and the gate of the upper MOSFET, as it may interfere with the internal adaptive shoot-through protection circuitry and render it ineffective.

BOOT

This pin provides ground referenced bias voltage to the upper MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive a logic-level N-channel MOSFET.

COMP/OCSET

This is a multiplexed pin. During a short period of time following power-on reset (POR), this pin is used to determine the over-current threshold of the converter. Connect a resistor (R_{OCSET}) from this pin to the drain of the upper MOSFET (V_{CC}). R_{OCSET}, an internal 20µA current source (I_{OCSET}), and the upper MOSFET on-resistance ($r_{DS(ON)}$) set the converter over-current (OC) trip point according to the following equation:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}} \quad \text{(EQ. 1)}$$

Internal circuitry of the ISL6520 will not recognize a voltage drop across R_{OCSET} larger than 0.5V. Any voltage drop across R_{OCSET} that is greater than 0.5V will set the overcurrent trip point to:

$$I_{PEAK} = \frac{0.5V}{r_{DS(ON)}} \quad \text{(EQ. 2)}$$

An over-current trip cycles the soft-start function.

During soft-start, and all the time during normal converter operation, this pin represents the output of the error amplifier. Use this pin, in combination with the FB pin, to compensate the voltage-control feedback loop of the converter.

Pulling OCSET to a level below 0.8V will disable the controller. Disabling the ISL6520 causes the oscillator to stop, the LGATE and UGATE outputs to be held low, and the softstart circuitry to re-arm.

LGATE

Connect this pin to the lower MOSFET's gate. This pin provides the PWM-controlled gate drive for the lower MOSFET. This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off. Do not insert any circuitry between this pin and the gate of the lower MOSFET, as it may interfere with the internal adaptive shoot-through protection circuitry and render it ineffective.

Functional Description

Initialization

The ISL6520 automatically initializes upon receipt of power. The Power-On Reset (POR) function continually monitors the bias voltage at the VCC pin. The POR function initiates the Over-Current Protection (OCP) sampling and hold operation after the supply voltage exceeds its POR threshold. Upon completion of the OCP sampling and hold operation, the POR function initiates the Soft Start operation.

Over Current Protection

The over-current function protects the converter from a shorted output by using the upper MOSFET's on-resistance, $r_{DS(ON)}$, to monitor the current. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor.

The over-current function cycles the soft-start function in a hiccup mode to provide fault protection. A resistor (R_{OCSET}) programs the over-current trip level (see See "Typical Application" on page 2.).

Immediately following POR, the ISL6520 initiates the Over-Current Protection sampling and hold operation. First, the internal error amplifier is disabled. This allows an internal 20µA current sink to develop a voltage across R_{OCSET}. The ISL6520 then samples this voltage at the COMP pin. This sampled voltage, which is referenced to the VCC pin, is held internally as the Over-Current Set Point.

When the voltage across the upper MOSFET, which is also referenced to the VCC pin, exceeds the Over-Current Set Point, the over-current function initiates a soft-start sequence. Figure 1 shows the inductor current after a fault is introduced while running at 15A. The continuous fault causes the ISL6520 to go into a hiccup mode with a typical period of 25ms. The inductor current increases to 18A during the Soft

Start interval and causes an over-current trip. The converter dissipates very little power with this method. The measured input power for the conditions of Figure 1 is only 1.5W.

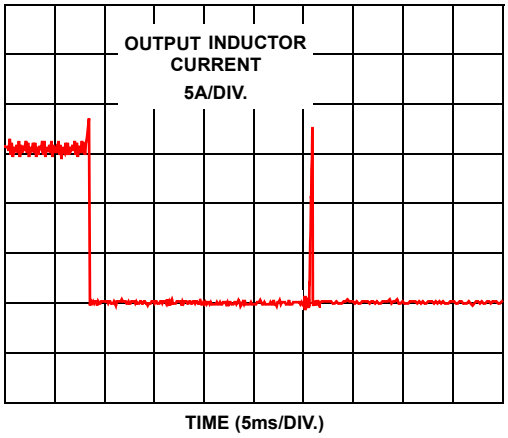


FIGURE 1. OVERCURRENT OPERATION

The over-current function will trip at a peak inductor current (I_{PEAK}) determined by:

$$I_{PEAK} = \frac{I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}} \quad \text{(EQ. 3)}$$

where I_{OCSET} is the internal OCSET current source (20µA typical). The OC trip point varies mainly due to the MOSFET's $r_{DS(ON)}$ variations. To avoid over-current tripping in the normal operating load range, find the R_{OCSET} resistor from the equation above with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. The minimum I_{OCSET} from the specification table.
3. Determine I_{PEAK} for $I_{PEAK} > I_{OUT(MAX)} + \frac{(\Delta I)}{2}$, where ΔI is the output inductor ripple current.

For an equation for the ripple current, see"Output Inductor Selection" on page 7.

Soft-Start

The POR function initiates the soft-start sequence after the overcurrent set point has been sampled. Soft-start clamps the error amplifier output (COMP pin) and reference input (non-inverting terminal of the error amp) to the internally generated Soft-Start voltage. Figure 2 shows a typical start up interval where the COMP/OCSET pin has been released from a grounded (system shutdown) state. Initially, the COMP/OCSET is used to sample the oversurrent setpoint by disabling the error amplifier and drawing 20µA through R_{OCSET}. Once the over-current level has been sampled, the soft start function is initiated. The clamp on the error amplifier (COMP/OCSET pin) initially controls the converter's output voltage during soft start. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates PHASE pulses of increasing width that charge the output capacitor(s). When the internally generated Soft-Start voltage exceeds the feedback (FB pin) voltage, the output voltage is in regulation. This method provides a rapid and controlled output voltage rise. The entire startup sequence typically take about 11ms.

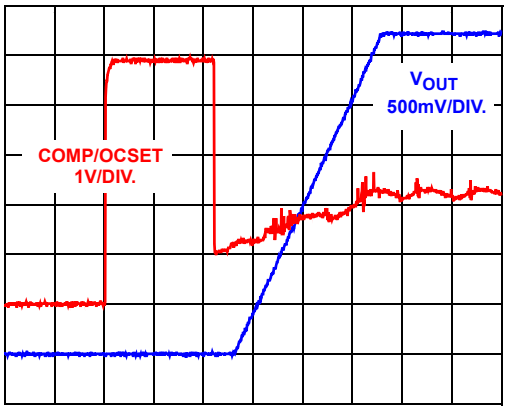


FIGURE 2. START UP SEQUENCE

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible, using ground plane construction or single point grounding.

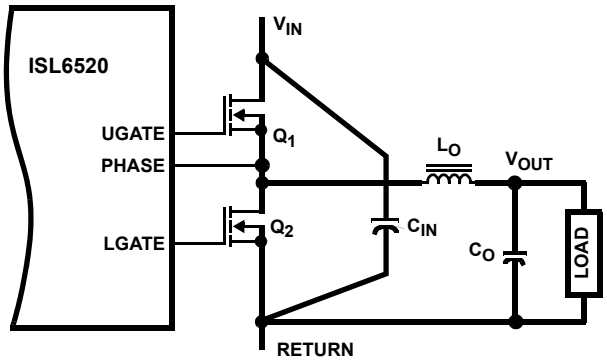


FIGURE 3. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 3 shows the critical power components of the converter. To minimize the voltage overshoot, the interconnecting wires indicated by heavy lines should be part of a ground or power plane in a printed circuit board. The components shown in Figure 3 should be located as close together as possible. Please note that the capacitors C_{IN} and C_O may each represent numerous physical capacitors. Locate the ISL6520 within 3 inches of the MOSFETs, Q_1 and Q_2. The circuit traces for the MOSFETs' gate and source connections from the ISL6520 must be sized to handle up to 1A peak current.

Figure 4 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the COMP/OCSET pin and locate the resistor, R_{OSCET} close to the COMP/OCSET pin because the internal current source is only 20µA. Provide local V_{CC} decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins. All components used for feedback compensation should be located as close to the IC a practical.

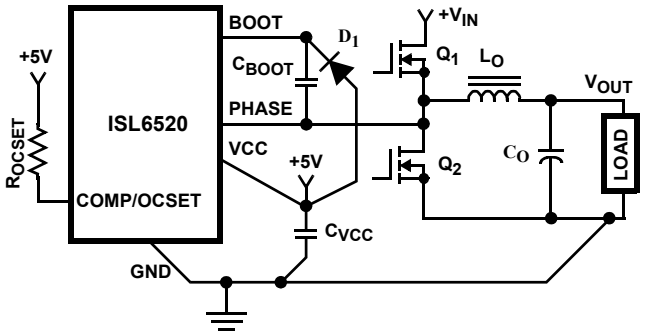


FIGURE 4. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

Feedback Compensation

Figure 5 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the Reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O).

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \times \sqrt{L_O \times C_O}} \qquad F_{ESR} = \frac{1}{2\pi \times ESR \times C_O} \qquad \text{(EQ. 4)}$$

The compensation network consists of the error amplifier (internal to the ISL6520) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 7. Use these guidelines for locating the poles and zeros of the compensation network:

1. Pick Gain (R_2/R_1) for desired converter bandwidth.
2. Place 1ST Zero Below Filter's Double Pole (~75% F_{LC}).
3. Place 2ND Zero at Filter's Double Pole.
4. Place 1ST Pole at the ESR Zero.
5. Place 2ND Pole at Half the Switching Frequency.
6. Check Gain against Error Amplifier's Open-Loop Gain.
7. Estimate Phase Margin - Repeat if Necessary.

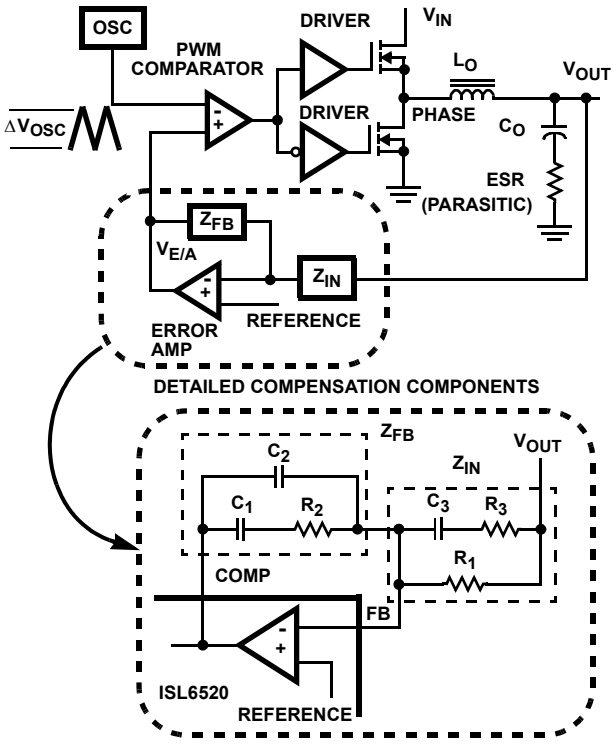


FIGURE 5. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$. This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \times R_2 \times C_1} \qquad F_{P1} = \frac{1}{2\pi \times R_2 \times \left(\frac{C_1 \times C_2}{C_1 + C_2}\right)}$$

$$F_{Z2} = \frac{1}{2\pi \times (R_1 + R_3) \times C_3} \qquad F_{P2} = \frac{1}{2\pi \times R_3 \times C_3} \qquad \text{(EQ. 5)}$$

Figure 6 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 6. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the graph of Figure 6 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45 degrees. Include worst case component variations when determining phase margin.

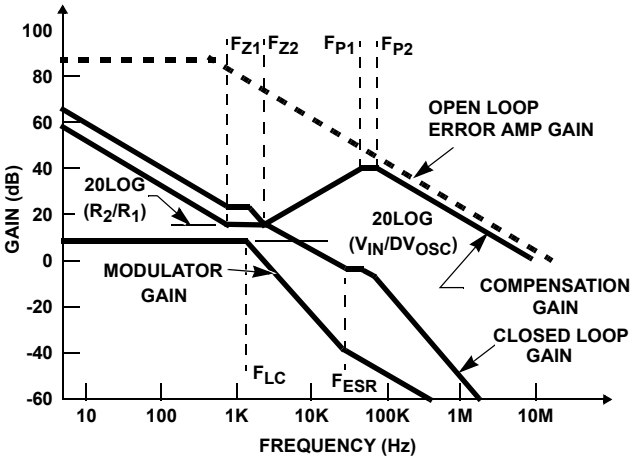


FIGURE 6. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

Component Selection Guidelines

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage and current are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{Fs \times L} \times \frac{V_{OUT}}{V_{IN}} \qquad \Delta V_{OUT} = \Delta I \times ESR \tag{EQ. 6}$$

Increasing the value of inductance reduces the ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the ISL6520 will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

The response time to a transient is different for the application of load and the removal of load. The following equations give the approximate response time interval for application and removal of a transient load:

$$t_{RISE} = \frac{L \times I_{TRAN}}{V_{IN} - V_{OUT}} \qquad t_{FALL} = \frac{L \times I_{TRAN}}{V_{OUT}} \tag{EQ. 7}$$

where: I_{TRAN} is the transient load current step, t_{RISE} is the response time to the application of load, and t_{FALL} is the response time to the removal of load. The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time Q_1 turns on. Place the small ceramic capacitors physically close to

the MOSFETs and between the drain of Q_1 and the source of Q_2.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

For a through hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

MOSFET Selection/Considerations

The ISL6520 requires two N-Channel power MOSFETs. These should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management requirements.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the upper MOSFET has switching losses, since the lower MOSFETs body diode or an external Schottky rectifier across the lower MOSFET clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage-current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are dissipated by the ISL6520 and don't heat the MOSFETs. However, large gate-charge increases the switching interval, t_{SW} which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = Io^2 \times r_{DS(ON)} \times D + \frac{1}{2} Io \times V_{IN} \times t_{SW} \times F_S$$

$$P_{LOWER} = Io^2 \times r_{DS(ON)} \times (1 - D)$$

Where: D is the duty cycle = V_{OUT} / V_{IN},
t_{SW} is the switching interval, and
F_S is the switching frequency.

(EQ. 8)

Given the reduced available gate bias voltage (5V), logic-level or sub-logic-level transistors should be used for both N-MOSFETs. Caution should be exercised with devices exhibiting very low $V_{GS(ON)}$ characteristics. The shoot-through protection present aboard the ISL6520 may be circumvented by these MOSFETs if they have large parasitic impedences and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on.

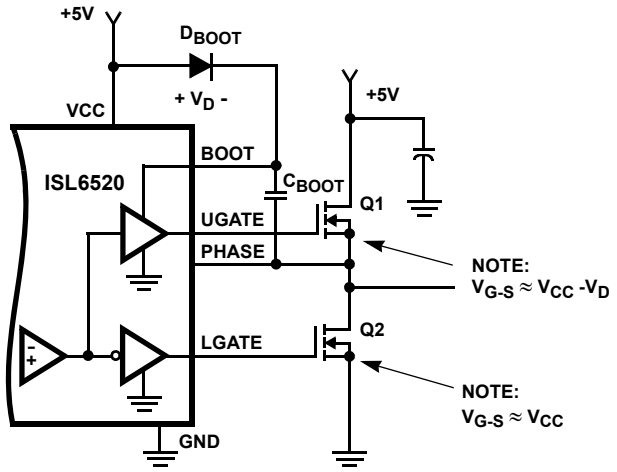
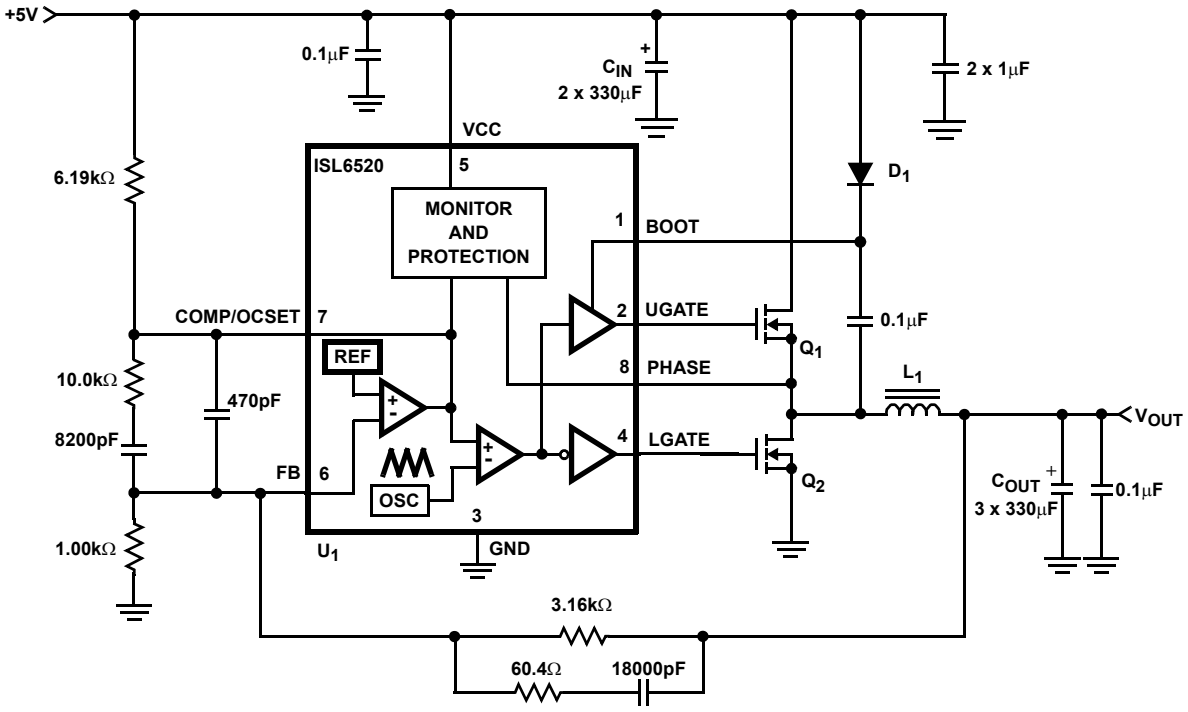


FIGURE 7. UPPER GATE DRIVE BOOTSTRAP

Figure 7 shows the upper gate drive (BOOT pin) supplied by a bootstrap circuit from V_{CC}. The boot capacitor, C_{BOOT}, develops a floating supply voltage referenced to the PHASE pin. The supply is refreshed to a voltage of V_{CC} less the boot diode drop (V_D) each time the lower MOSFET, Q_2, turns on.

ISL6520 DC/DC Converter Application Circuit

Figure 8 shows an application circuit of a DC/DC Converter. Detailed information on the circuit, including a complete Bill-of-Materials and circuit board description, can be found in Application Note AN9932.

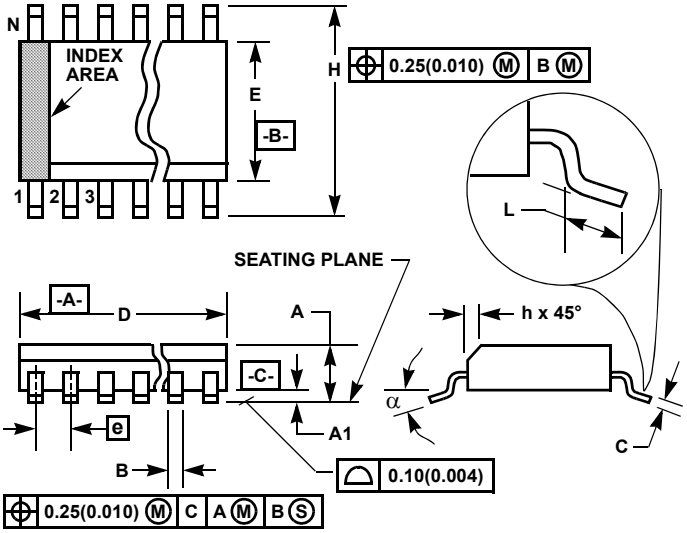


Component Selection Notes:

C_{IN} - Each 330mF 6.3WVDC, Sanyo 6TPB330M or Equivalent.
C_{OUT} - Each 330mF 6.3WVDC, Sanyo 6TPB330M or Equivalent.
D1 - 30mA Schottky Diode, MA732 or Equivalent
L_1 - 3.1µH Inductor, Panasonic P/N ETQ-P6F2ROLFA or Equivalent.
Q_1, Q_2 - Intersil MOSFET; HUF76143.

FIGURE 8. 5V to 3.3V 15A DC/DC CONVERTER

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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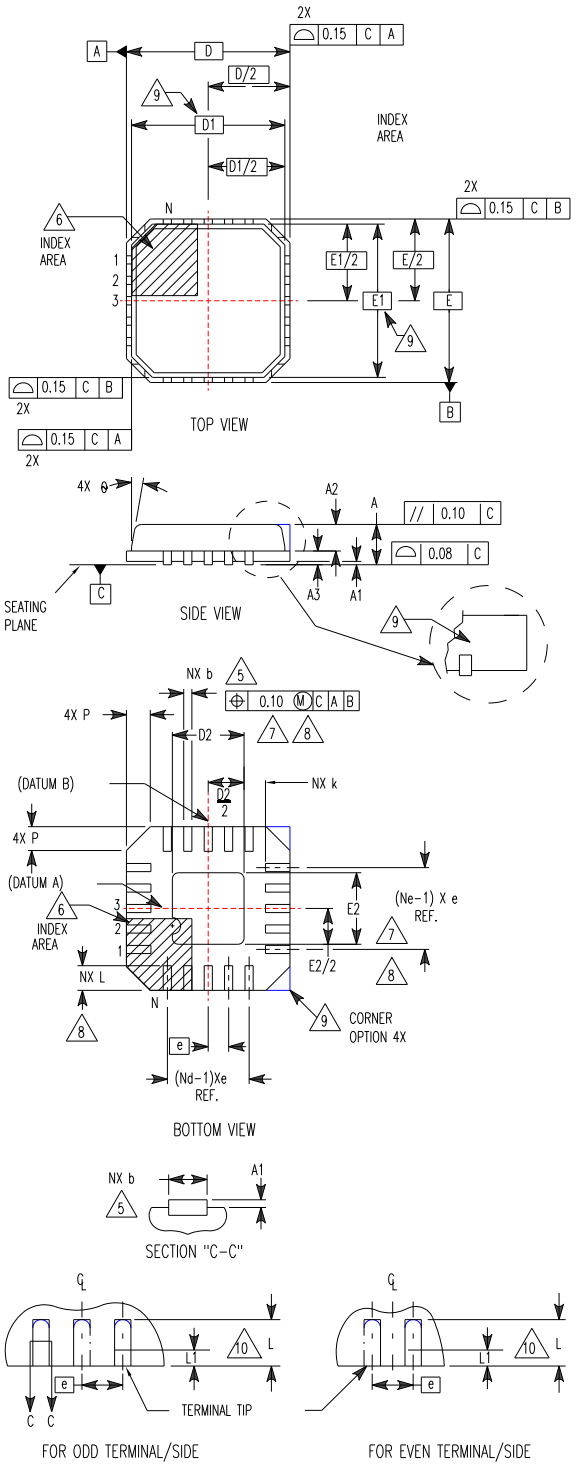
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

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