10/100BASE-TX/FX Octal-Φ™ Transceiver

GENERAL DESCRIPTION

The BCM5228 is an octal 10/100BASE-TX/FX transceiver targeted at Fast Ethernet switches. The device contains eight full-duplex 10BASE-T/100BASE-TX/FX Fast Ethernet transceivers, each of which perform all of the physical layer interface functions for 10BASE-T Ethernet on Category 3, 4 or 5 unshielded twisted pair (UTP) cable and 100BASE-TX Fast Ethernet on Category 5 UTP cable. 100BASE-FX is supported at each port through the use of external fiber optic transmit and receive devices.

The BCM5228 is a highly integrated solution combining digital adaptive equalizers, ADCs, phase locked loops, line drivers, encoders, decoders, and the required support circuitry into a single monolithic CMOS chip. The BCM5228 complies with the IEEE 802.3 specification, including the auto negotiation subsections.

The effective use of digital technology in the BCM5228 design results in robust performance over a broad range of operating scenarios. Problems inherent to mixed-signal implementations, such as analog offset and on-chip noise, are eliminated by employing field-proven digital adaptive equalization and digital clock recovery techniques.

FEATURES

- 10BASE-T/100BASE-TX/FX IEEE 802.3u compliant
- Single-chip octal physical interface-RMII to magnetics
- Reduced Media Independent Interface (RMII)
- Option - Serial Media Independent Interface (SMII)
- Option - Source Synchronous SMII (S3MII)
- Fully integrated digital adaptive equalizers
- 125-MHz clock generator and timing recovery
- On-chip multimode transmit waveshaping
- Edge-rate control eliminates external filters
- Integrated baseline wander correction
- HP Auto-MDIX
- Cable Length Indication
- Cable Noise Level Indication
- IEEE 802.3u-compliant auto negotiation
- Shared MII management interface up to 25 Mbps
- Serial LED status pins
- Programmable parallel LED pins
- Interrupt output capability
- Loopback mode for diagnostics
- IEEE 1149.1 (JTAG) and NAND chain ICT support
- Low-power dual-supply 2.5V/3.3V CMOS technology
- Compatible with 3.3V I/O
- 208 PQFP and 256 FPBGA packages
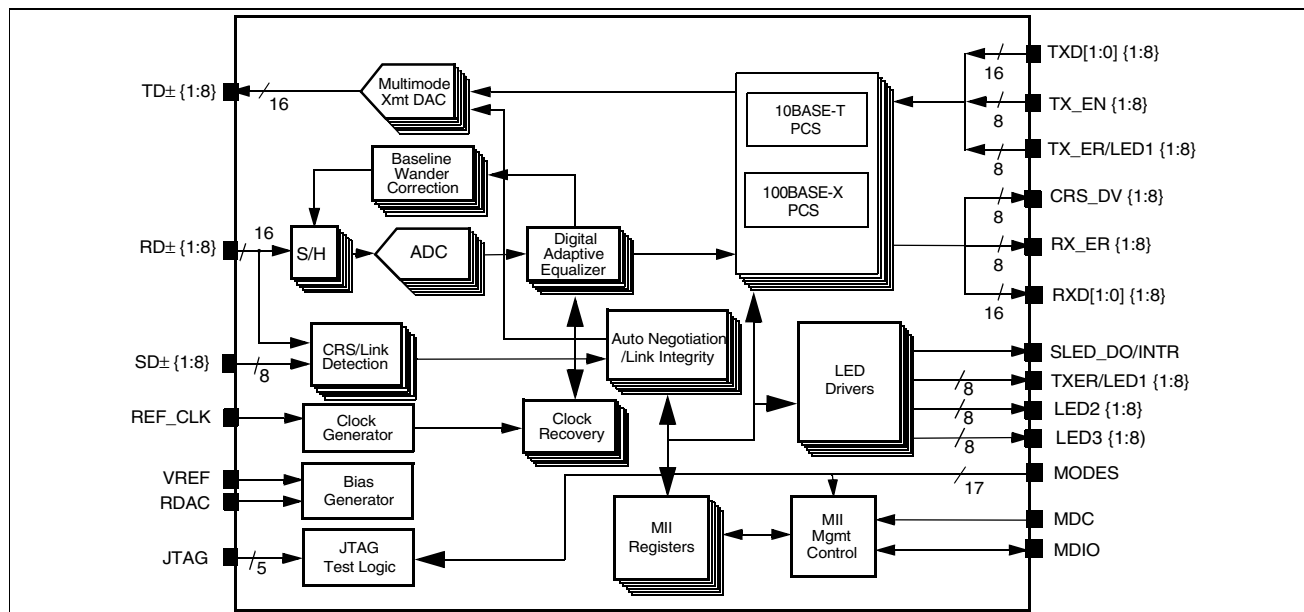
APPLICATIONS

- Fast Ethernet switches

Figure 1:   Functional Block Diagram

REVISION HISTORY

Revision	Date	Change Description
5228-DS01-R	11/24/99	Initial Release
5228-DS02-R	12/15/99	Added MDIX info to page 49. Minor editorial changes.
5228-DS03-R	09/01/00	• Correct several signal name inconsistencies. • Changed P14 from PLLVDDP to OVDD in Table 2, Figure 1, Figure 2, Figure 3, and Table 3. • Changed AGND from C05 to C06 in Table 3 on page 18. • Modified description for "100BASE-FX Mode" on page 24. • Changed "LED_CLK" to "SLED_CLK" for "Low-Cost Serial LED Mode" on page 26. • Changed address 1Ah bit 15 in Table 15 on page 33 from FDX LED Enable to Reserved. • Deleted FDX LED Enable bit description for Table 32 on page 52. • Added TX_ER parameter to Table 49 on page 64. • Added CRS_DV, RX_ER, and note 3 to Table 50 on page 65. • Changed SRD_Delay to SRX_Delay for Figure 8 on page 67. • Deleted reference to IVDD in Table 57 on page 70.

5228-DS04-R	03/15/01	• Added the following to list of FEATURES on Cover:
		  • Option - Source synchronous SMII (S3MII)
		  • HP Auto-MDIX
		  • Cable Length Indication
		  • Cable Noise Level Indication.
		• Following Table 32 on page 52, deleted from Interrupt Enable description "Bits 14 and 15 of this register are mutually exclusive. Only one may be set at a time."
		• In Table 49 on page 64, inserted TYP values for parameters TD± after TXEN Assert and TXD to TD± Steady State Delay.
		• In Table 50 on page 65, added TYP values for parameter CRS_DV Assert after RD±, CRS_DV Deassert after RD±; and CRS_DV Deassert after RD±, Valid EOP. Deleted last row (parameter RD± to CRS_DV Steady State Delay).
		• In Table 57 on page 70, added TYP and MAX values for Total Supply Current for AVDD, DVDD and OVDD pins.
		• Added Section 10 "Packaging Thermal Characteristics" on page 73.
		• Corrected specification of register 19h, bit 0 from "jabber detect" to "full-duplex indication."

5228-DS05-R	10/24/01	• Added ordering information; added minor table information updates.

TABLE OF CONTENTS

Broadcom Corporation

Broadcom Corporation

LIST OF FIGURES

LIST OF TABLES

Section 1: Functional Description

OVERVIEW

The BCM5228 is a single-chip device containing eight independent Fast Ethernet transceivers. Each transceiver performs all of the physical layer interface functions for 100BASE-TX full-duplex or half-duplex Ethernet on Category 5 unshielded twisted pair (UTP) cable and 10BASE-T full-duplex or half-duplex Ethernet on Category 3, 4 or 5 UTP cable. Each port may also be configured for 100BASE-FX full-duplex or half-duplex transmission over fiber optic cabling when paired with an external fiber optic line driver and receiver.

The chip performs 4B5B, MLT3, NRZI, and Manchester encoding and decoding, clock and data recovery, stream cipher scrambling/descrambling, digital adaptive equalization, line transmission, carrier sense and link integrity monitor, auto negotiation, and RMII and SMII management functions. The BCM5228 may be connected to a MAC through the RMII or SMII on one side and connected directly to the network media on the other side through isolation transformers for UTP modes, or through fiber optic transmitter/receiver components for FX mode. The BCM5228 is compliant with the IEEE 802.3 standard.

ENCODER/DECODER

In 100BASE-TX and 100BASE-FX modes, the BCM5228 transmits and receives a continuous data stream on twisted pair or fiber optic cable. When the RMII Transmit Enable is asserted, data from the transmit data pins is encoded into 5-bit code groups and inserted into the transmit data stream. The 4B5B encoding is shown in Table 1 on page 3. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. The transmitter repeatedly sends the idle code group between packets.

In TX mode, the encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multimode transmit DAC is used to drive the MLT3 data onto the twisted pair cable. In FX mode, the scrambling function is bypassed and the data is NRZI encoded. The multimode transmit DAC drives differential positive ECL (PECL) levels to an external fiber optic transmitter.

Following baseline wander correction, adaptive equalization, and clock recovery in TX mode, the receive data stream is converted from MLT3 to serial NRZI data. The NRZI data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

In FX mode, the receive data stream differential PECL levels are sampled from the fiber optic receiver. Baseline wander correction, adaptive equalization, and stream cipher descrambling functions are bypassed, and NRZI decoding is used instead of MLT3.

The 5-bit code groups are decoded into 4-bit data nibbles, as shown in Table 1 on page 3. The start-of-stream delimiter is replaced with preamble nibbles and the end-of-stream delimiter and idle codes are replaced with all zeros. The decoded data is driven onto the RMII/SMII receive data pins. When an invalid code group is detected in the data stream, the BCM5228 asserts the RMII/SMII RXER signal. The chip also asserts RXER for several other error conditions that improperly terminate the data stream. While RXER is asserted, the receive data pins are driven with a 01 for an invalid data reception and a 10 for a false carrier.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs pre-equalization for 100 meters of Category 3 cable.

Broadcom Corporation

LINK MONITOR

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor enters and remains in the Link Fail state where only idle codes are transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor enters the Link Pass state and the transmit and receive functions are enabled.

In 100BASE-FX mode, the external fiber optic receiver performs the signal energy detection function and communicates this information directly to the BCM5228 through the differential SD± pins.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD± pins for the presence of valid link pulses.

CARRIER SENSE

In DTE mode, the carrier sense and receive data valid signals are multiplexed on the same pin. The carrier sense is asserted asynchronously on the CRS_DV pin as soon as valid activity is detected in the receive data stream. Loss of carrier results in the deassertion of CRS_DV synchronous to the cycle of REF_CLK that presents the first di-bit of a nibble onto RXD. If the PHY has additional bits to be presented on RXD following the initial deassertion of CRS_DV, the PHY asserts CRS_DV on cycles of REF_CLK that present the second di-bit of each nibble, and deasserts CRS_DV on cycles of REF_CLK that present the first di-bit of each nibble. If carrier sense is asserted and a valid SSD is not detected immediately, RXER is asserted. A value of 2h (2 hex) is driven on the receive data pins to indicate false carrier sense.

In 10BASE-T mode, carrier sense is asserted asynchronously on the CRS pin when valid preamble activity is detected on the RD± input pins.

AUTO NEGOTIATION

The BCM5228 contains the ability to negotiate its mode of operation over the twisted pair link using the auto negotiation mechanism defined in the IEEE 802.3u specification. Auto negotiation may be enabled or disabled by hardware or software control. When the auto negotiation function is enabled, the BCM5228 automatically chooses its mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5228 can be configured to advertise 100BASE-TX full-duplex and/or half-duplex and 10BASE-T full-duplex and/or half-duplex. Each transceiver negotiates independently with its link partner and chooses the highest level of operation available for its own link.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes interzonal interference created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM5228 achieves an optimum signal to noise ratio by using a combination of feed-forward equalization and decision-feedback equalization. This powerful technique achieves a 100BASE-TX BER of less than 1×10^{-12} for transmission up to 100 meters on Category 5 twisted pair cable, even in harsh noise environments. The digital adaptive equalizers in the BCM5228 achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self adapting to any quality of cable or cable length. Because of transmit pre-equalization in 10BASE-T mode and complete lack of ISI in 100BASE-FX mode, the adaptive equalizer is bypassed in this mode of operation.

Broadcom Corporation

ADC

Each receive channel has its own 125-MHz analog to digital converter (ADC). The ADC samples the incoming data on the receive channel and produces a digital output. The output of the ADC is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low offset, high power supply noise rejection, fast settling time, and low bit error rate (BER).

DIGITAL CLOCK RECOVERY/GENERATOR

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clocks are locked to the 50-MHz clock input, while the receive clocks are locked to the incoming data streams. Clock recovery circuits optimized to MLT3, NRZI, and Manchester encoding schemes are included for use with each of the three different operating modes. The input data streams are sampled by the recovered clock from each port and fed synchronously to the respective digital adaptive equalizer.

BASELINE WANDER CORRECTION

A 100BASE-TX data stream is not always DC balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM5228 automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reducing the chance of a receive symbol error. The baseline wander correction circuit is not required, and is therefore bypassed, in 10BASE-T and 100BASE-FX operating modes

Table 1:   4B5B Encoding

Name	4b Code	5b Code	Meaning
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F

Broadcom Corporation

Table 1:   4B5B Encoding (Cont.)

Name	4b Code	5b Code	Meaning
I	0000*	11111	Idle
J	0101*	11000	Start-of-stream delimiter, part 1
K	0101*	10001	Start-of-stream delimiter, part 2
T	0000*	01101	End-of-stream delimiter, part 1
R	0000*	00111	End-of-stream delimiter, part 2
H	1000	00100	Transmit error (used to force signalling errors)
V	0111	00000	Invalid code
V	0111	00001	Invalid code
V	0111	00010	Invalid code
V	0111	00011	Invalid code
V	0111	00101	Invalid code
V	0111	00110	Invalid code
V	0111	01000	Invalid code
V	0111	01100	Invalid Code
V	0111	10000	Invalid Code
V	0111	11001	Invalid Code

* Treated as invalid code (mapped to 0111) when received in data field.

MULTIMODE TRANSMIT DAC

The multimode transmit digital to analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode, NRZI-coded symbols in 100BASE-FX mode and Manchester-coded symbols in 10BASE-T mode. It performs programmable edge-rate control in TX mode, which decreases unwanted high frequency signal components thus reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode; no filtering is performed in 100BASE-FX mode. The transmit DAC utilizes a current drive output which is well balanced and produces very low noise transmit signals. PECL voltage levels are produced with resistive terminations in 100BASE-FX mode.

STREAM CIPHER

In 100BASE-TX mode, the transmit data stream is scrambled in order to reduce radiated emissions on the twisted pair cable. The data is scrambled by *exclusive ORing* the NRZI signal with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range, and eliminating peaks at certain frequencies. Signal energy is spread further by using unique seeds to generate a different non-repeating sequence for each of the eight ports.

The receiver descrambles the incoming data stream by *exclusive ORing* it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler will "lock" to the scrambler state after detecting a sufficient number of consecutive idle code-groups. The receiver will not attempt to decode the data stream unless the descrambler is locked. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The receive data stream is expected

to contain inter-packet idle periods. If the descrambler does not detect enough idle codes within 724 microseconds, it becomes "unlocked", and the receive decoder is disabled. If the receiver is put into Token Ring mode (see bit 10, reg. 1Bh), the descrambler monitors the receiver for 5792 microseconds before unlocking. The descrambler is always forced into the unlocked state when a link failure condition is detected. Stream cipher scrambling/descrambling is not used in 100BASE-FX and 10BASE-T modes.

FAR-END FAULT

Auto negotiation provides a Remote Fault capability for detection of asymmetric link failures. Because auto negotiation is not available for 100BASE-FX, the BCM5228 implements the IEEE 802.3 standard Far-End Fault mechanism for the indication and detection of remote error conditions. If the Far-End Fault mechanism is enabled, a transceiver transmits the Far-End Fault indication whenever a receive channel failure is detected (signal detect is deasserted). Each transceiver also continuously monitors the receive channel when a valid signal is present (signal detect asserted). When its link partner is indicating a remote error, the transceiver forces its link monitor into the link fail state and set the Remote Fault bit in the RMII status register. The Far-End Fault mechanism is on by default in 100BASE-FX mode off by default in 100BASE-TX and 10BASE-T modes, and may be controlled by software after reset.

REDUCED MEDIA INDEPENDENT INTERFACE (RMII)

The interface in the BCM5228 is based on the low pin count (Reduced) Media Independent Interface (RMII) developed by the RMII Consortium. A copy of the specification can be found on the consortium Web site at: http://www.rmii-consort.com. The purpose of this interface is to provide a low-cost alternative to the IEEE 802.3u[2] Media Independent Interface (MII). The RMII is capable of supporting 10 megabit and 100 megabit data rates with a single clock, using independent 2-bit wide transmit and receive paths.

A single 50-MHz synchronous reference clock is used as a timing reference for all transmitters and receivers. By doubling the clock frequency relative to the MII, four pins are saved in the data path, which uses two lines into each transmitter and two lines out of each receiver, compared to four lines used in each direction in the MII. Since start-of-packet and end-of-packet timing information is preserved across the interface, the MAC is able to derive the COL signal from the receive and transmit data delimiters, saving another pin.

Transmit and receive clocks have been eliminated as well. All data transfers are synchronous with REF_CLK. This poses less of a challenge for the transmitter than it does for the receiver, which is now required to buffer output data in a FIFO until an edge of the REF_CLK is suitably aligned. The received data bits and the RX_DV signal are passed through the FIFO; the CRS_DV bit is not. It is asserted for the time the wire is receiving a frame. If the remote transmitter is idle, and no data need be passed from the receiver, status information can be made available by setting Bit 1 of Register 10h. Out-of-band signaling consists of 2 di-bit pairs immediately following the last di-bit pair of a received packet. The 2 di-bit pairs consist of "full-duplex, Link Speed - msb, lsb" and "RXER, FIFO Error - msb, lsb."

MII MANAGEMENT

Management of each transceiver within the BCM5228 remains the same as it was under the MII specification. Each PHY contains an independent set of MII management registers. They share a single MDC/MDIO serial interface. Each transceiver has a unique address and must be accessed individually. The common base address for the group of eight individual transceivers is defined by configuring the five external PHYAD address input pins.

SERIAL MEDIA INDEPENDENT INTERFACE (SMII)

The SMII is an alternative to both the MII and RMII. The objective is to reduce the number of pins required to interconnect the MAC and the PHY. This is accomplished by clocking data and control signals in and out of each PHY on a pair of pins at a rate of 125 MHz. The SMII mode is selected by pulling the SMII_EN pin high during power-on reset.

Data and control signals passing from the MAC to the PHY use the serial transmit (STX) line; data and control signals passing from the PHY to the MAC use the serial receive (SRX) line. All bit transfers are synchronous with clock (SCLK) at 125 MHz; frame synchronization is provided by a fourth line (SYNC), asserted at the beginning of each frame, which occurs every ten cycles of SCLK. Each PHY is provided with an STX and an SRX pair. Pins TXD0{x} and RXD0{x}, where x is the number of the specific PHY, are used to perform the STX and SRX functions.

The BCM5228 chip has a single SCLK and SYNC input that is common to all PHYs. Pins REF_CLK and SSYNC are used for these functions.

Receive data and control information are passed from the PHY to the MAC in ten bit frames. In 100 Mbps mode, each frame represents a new byte of data. In 10 Mbps mode, each byte of data is repeated ten times; the MAC can sample any one of every ten frames. Since the timing of data coming from a remote transmitter is not synchronized with the local SCLK or SYNC lines and may contain errors in frequency, a FIFO capable of storing 28 bits is provided in each receive path. The received data bits and the RX_DV signal are passed through the FIFO; the CRS bit is not. It is asserted for the time the wire is receiving a frame. If the remote transmitter is idle and no data need be passed from the receiver, status information becomes available.

Transmit data and control information are passed from the MAC to the PHY in ten bit frames, as in the receive path. In 100 Mbps mode, each frame represents a new byte of data. In 10 Mbps mode, each byte of data is repeated ten times; the PHY can transmit any one of every ten frames.

INTERRUPT MODE

The BCM5228 can be programmed to provide an interrupt output consisting of an OR of the eight interrupts, one from each PHY. The interrupt feature is disabled by default. The interrupt capability is enabled by setting MII register 1Ah, bit 14. The SLED_DO pin becomes the INTR# pin, when the SERIAL_EN is pulled low during power-up reset. If a serial LED mode is required, hardware interrupt can be obtained by wire ORing LED2{1:8} open drain outputs and programming LED2 to output interrupt by setting TXER/LED1{5:3} pins to a 5 during power-on reset. The status of each interrupt source is also reflected in Register 1Ah, bits 1, 2 and 3. The sources of interrupt are change in link, speed or full-duplex status. If any type of interrupt occurs, the Interrupt Status bit, Register 1Ah, bit 0 is set.

In addition, each transceiver has its own register controlling the interrupt function.

If the interrupt enable bit is set to 0, no status bits sets, and no interrupts are generated. If the interrupt enable bit is set to 1, the following conditions apply:

•   If mask status bits are to 0 and the interrupt mask is set to 1, status bits are set but no interrupts are generated.

•   If mask status bits are set to 0 and the interrupt mask is set to 0, status bits and interrupts are available.

•   If mask status bits are set to 1 and the interrupt mask is set to 0, no status bits and no interrupts are available.

Changes from active to inactive or vice versa causes an interrupt. Setting Register 1Ah, bit 8 high masks all interrupts, regardless of the settings of the individual mask bits.

Section 2: Hardware Signal Definition Table

Table 2:   Pin Definitions

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
Media Connections					
A12,B12	166,167	165,166	RD+{1}, RD-{1}		
A11,B11	178,177	173,172	RD+{2}, RD-{2}		
A08,B08	184,185	179,180	RD+{3}, RD-{3}		
A07,B07	196,195	198,197	RD+{4}, RD-{4}	I_A	**Receive Pair.** Differential data from the media is received on the RD± signal pair.
T06,R06	64,65	62,63	RD+{5}, RD-{5}		
T07,R07	76,75	81,80	RD+{6}, RD-{6}		
T10,R10	82,83	87,88	RD+{7}, RD-{7}		
T11,R11	94,93	95,94	RD+{8}, RD-{8}		
A13,B13	164,165	163,164	TD+{1}, TD-{1}		
A10,B10	180,179	175,174	TD+{2}, TD-{2}		
A09,B09	182,183	177,178	TD+{3}, TD-{3}		
A06,B06	198,197	200,199	TD+{4}, TD-{4}	O_A	**Transmit Pair.** Differential data is transmitted to the media on the TD± signal pair.
T05,R05	62,63	60,61	TD+{5}, TD-{5}		
T08,R08	78,77	83,82	TD+{6}, TD-{6}		
T09,R09	80,81	85,86	TD+{7}, TD-{7}		
T12,R12	96,95	97,96	TD+{8}, TD-{8}		
D12,E12	171,170		SD+{1}, SD-{1}		
D11,E11	173,174		SD+{2}, SD-{2}		**100BASE-FX Signal Detect.** Indicates signal
D08,E08	189,188		SD+{3}, SD-{3}		quality status on the fiber-optic link in 100BASE-
E07,D07	191,192		SD+{4}, SD-{4}	I_{PD}	FX mode. When the signal quality is good, the SD+ pin should be driven high relative to the SD–
N09,M09	69,68		SD+{5}, SD-{5}		pin. 100BASE-FX mode is disabled when both
N10,M10	71,72		SD+{6}, SD-{6}		pins are simultaneously pulled low or left
N11,M11	87,86		SD+{7}, SD-{7}		unconnected.
N12,M12	89,90		SD+{8}, SD-{8}		
Reduced Media Independent Interface (RMII)					
T15	99	100	REF_CLK	I	**Reference Clock Input.** This pin must be driven with a continuous 50-MHz clock in the RMII application and 125 MHz in the SMII application. It provides timing for CRS_DV, RXD1, RXD0, TX_EN, TXD1,TXD0, and RX_ER. Accuracy shall be ±50 ppm, with a duty cycle between 35% and 65% inclusive.

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output,
I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output,
O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = bias.
Bus naming convention: Pin label followed by {Port #}.

Table 2:   Pin Definitions (Cont.)

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
C03	4	4			**Transmit Enable.** In RMII mode,active high indicates that the MAC is presenting di-bits on TXD1,TXD0 for transmission. TX_EN is asserted synchronously with the first nibble of the preamble and remains asserted while all di-bits to be transmitted are presented to the RMII. TX_EN transitions synchronously with respect to REF_CLK.
B02	3	3			
B01	208	208			
A01	207	207	TX_EN{1:8}	I_{PD}	
T01	53	53			
R01	52	52			
P04	51	51			
P03	50	50			
D16	149	149	TXD1{1}		
E16	150	150	TXD0{1}		
F15	145	145	TXD1{2}		
F16	146	146	TXD0{2}		**Transmit Data Input.** In RMII mode, TXD1,TXD0 dibit wide data is input on these pins for transmission by the PHY. The data is synchronous with REF_CLK. TXD1 is the most significant bit. Values other than 00 on TXD1,TXD0 while TX_EN is deasserted are ignored by the PHY.
G15	139	139	TXD1{3}		
G16	140	140	TXD0{3}		
H15	135	135	TXD1{4}		
H16	136	136	TXD0{4}	I_{PD}	
J15	127	127	TXD1{5}		
J16	128	128	TXD0{5}		In SMII mode, the TXD0{1:8} form the STXD pins for each PHY.
K15	123	123	TXD1{6}		
K16	124	124	TXD0{6}		
L15	117	117	TXD1{7}		
L16	118	118	TXD0{7}		
M15	113	113	TXD1{8}		
M16	114	114	TXD0{8}		
A02	204	206			**Carrier Sense/Receive Data Valid.** In RMII mode, CRS_DV shall be asserted by the PHY when the medium is non-idle. The data on RXD1,RXD0 is considered valid once CRS_DV is asserted. During a false carrier event, CRS_DV shall remain asserted for the duration of carrier activity. CRS_DV is not synchronized with respect to REF_CLK.
A03	203	205			
B04	202	204			
A04	201	203	CRS_DV{1:8}	O_{3S}	
R03	59	57			
R02	58	56			
T03	57	55			
T02	56	54			

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = bias.
Bus naming convention: Pin label followed by {Port #}.

Table 2: Pin Definitions (Cont.)

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
D14	151	151	RXD1{1}		
D15	152	152	RXD0{1}		
E14	147	147	RXD1{2}		
E15	148	148	RXD0{2}		
F12	141	141	RXD1{3}		**Receive Data Outputs.** In RMII mode,
F13	142	142	RXD0{3}		RXD1,RXD0 data is output synchronous with
G12	137	137	RXD1{4}		REF_CLK. For each clock period in which
G14	138	138	RXD0{4}	O_{3S}	CRS_DV is asserted, RXD1,RXD0 transfers two bits of data from the PHY. RXD1 is the most
H12	129	129	RXD1{5}		significant bit.
H13	130	130	RXD0{5}		
J12	125	125	RXD1{6}		In SMII mode, the RXD0{1:8} form the SRXD
J14	126	126	RXD0{6}		pins for each PHY.
K12	119	119	RXD1{7}		
K13	120	120	RXD0{7}		
L12	115	115	RXD1{8}		
L14	116	116	RXD0{8}		
D02	8	8			
D01	7	7			**Receive Error Detected.** In RMII mode, RX_ER
C02	6	6			is asserted high for one or more REF_CLK
C01	5	5	RX_ER{1:8}	O_{3S}	periods to indicate that an error was detected somewhere in the frame presently being
N03	43	43			transferred from the PHY. RX_ER transitions
M01	42	42			synchronously with respect to REF_CLK.
M02	41	41			
L01	40	40			

Serial Media Independent Interface (SMII)

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
H01	23	23	SMII_EN/ SLED_CLK	I/O_{PU}	**SMII Enable.** Active high. An active high or being left unconnected during power-on reset selects the SMII mode, while an active low selects the RMII mode. **Serial LED clock.** After power-on reset, if Serial or Low-Cost Serial LED mode is enabled, this pin sources the clock for serial data SLED_DO. Refer to Section 5 "LED Modes" for details.
P15	105	105	SSYNC	I_{PD}	**SMII SYNC.** In SMII mode, this pin must be connected to a free running sync pulse occurring 1 of every 10 clock cycles. In RMII mode, this pin is NC (No Connect). Data and controls are transferred through TXD0 and RXD0 between respective MAC and PHY in default SMII mode. If source synchronous enable, SSMII_EN, is high, then SSYNC provides sync for TXD0 only and SMII_RSYNC from the BCM5228 provides sync for RXD0.

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = bias.
Bus naming convention: Pin label followed by {Port #}.

Table 2:   Pin Definitions (Cont.)

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
R15	103	103	SSMII_EN	I_{PD}	**SMII Source Synchronous (S3MII) Enable.** Active high. When S3MII is enabled, the BCM5228 provides a source synchronous receive clock (SMII_RXC) and a sync (SMII_RSYNC) for MAC to use. The BCM5228 uses SMII_TXC along with SSYNC to receive data from the MAC. Signals CRS_DV, TXER, TXEN, and RXER are not used when Source Synchronous mode is enabled.
R16	106	106	SMII_RXC	O_{3S}	**SMII Source Synchronous Receive Clock.** Optional 125-MHz clock in SMII mode for MAC use to clock in RXD0.
P16	107	107	SMII_RSYNC	O_{3S}	**SMII Source Synchronous SYNC.** In S3MII mode, this pin provides a source synchronous SYNC pulse for MAC to use for RXD0 if Source Synchronous is enabled.
T16	104	104	SMII_TXC	I_{PD}	**SMII Source Synchronous Transmit Clock.** 125-MHz clock in SMII mode for BCM5228 to clock in TXD0 if Source Synchronous is enabled.

Management Data I/O

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
J01	32	32	MDIO	I/O_{PU}	**Management Data I/O.** This serial input/output bit is used to read from and write to the RMII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
K01	31	31	MDC	I_{PD}	**Management Data Clock.** The MDC clock input must be provided to allow RMII management functions. Clock frequencies up to 25 MHz are supported.
G05 H05 H04 J05 J03	24 25 26 27 28	24 25 26 27 28	PHYAD{4:0}	I_{PD}	**PHY ADdress Selects.** These inputs set the base address for MII management PHY addresses. Also serve as test control inputs along with TESTEN to select the NAND-chain test mode.
H02	22	22	MASTERPHY/ SFRAME	I/O_{PD}	**Master PHY Address Mode.** Active high. This forces PHY address 0 to be a global write address for all PHYs within the BCM5228. An active high during power-on reset selects the master PHY address mode, while an active low or being left unconnected selects the normal address mode. **Serial LED Frame.** After power-on reset, this pin sources the serial LED frame output signal if serial LED mode is enabled.

Mode

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output,
I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output,
O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = bias.
Bus naming convention: Pin label followed by {Port #}.

Table 2:   Pin Definitions (Cont.)

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
C16	157	157	RESET#	I$_{PU}$	**Reset.** Active Low. Resets the BCM5228. Pin not included in NAND chain.
N15	109	109	F100	I$_{PU}$	**10/100 Mode Select.** When high and ANEN is low, all transceivers are forced to 100BASE-X operation. When low and ANEN is low, all transceivers are forced to 10BASE-T operation. When ANEN is high, F100 has no effect on the operation.
M13	108	108	ANEN	I$_{PU}$	**Auto Negotiation Enable.** Active high. When pulled high, auto negotiation begins immediately after reset. When low, auto negotiation is disabled after reset. Auto negotiation can be enabled under software control (Register 0, bit 12) if auto negotiation is enabled through hardware.
C15	156	156	FDXEN	I$_{PD}$	**Full-Duplex Mode Enable.** The FDXEN pin is logically ORed with an MII control bit to generate an internal full-duplex enable signal. When FDXEN is high, the BCM5228 may operate in full-duplex mode as determined by auto negotiation. When FDXEN is low, the internal control bit (Register 0, bit 8) determines the full-duplex operating mode. Initial value of the internal control bit is zero.
G01	19	19	TXER_EN	I/O$_{PU}$	**TXER Enable.** Active high. When pulled high during power-on reset, TXER[1:8]/LED1[1:8] pins become TXER[1:8] input. Otherwise they become LED1[1:8] output.
F05	20	20	MDIX_DIS	I/O$_{PD}$	**HP Auto-MDIX Disable.** Active high. When pulled high during reset, automatic TX cable swap detection function of the BCM5228 is disabled. Leave this pin unconnected for normal operation.
F04	17	17	TESTEN	I$_{PD}$	**Test Enable.** Active high test control input used along with PHYAD[4:0] to select the NAND-chain test mode. This test mode is latched when TESTEN is pulsed high, then low, with PHYAD[4:0]=10111. This pin is not included in the NAND chain and must be pulled low or left unconnected during normal operation.

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I$_A$ = analog input, O$_A$ = analog output,
I$_{PU}$ = digital input w/ internal pull-up, I$_{PD}$ = digital input w/ internal pull-down, O$_{OD}$ = open-drain output,
O$_{3S}$ = three-state output, I/O$_{PD}$ = bidirectional w/ internal pull-down, B = bias.
Bus naming convention: Pin label followed by {Port #}.

Table 2: Pin Definitions (Cont.)

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
LED					
G03	21	21	SERIAL_EN	I/O$_{PD}$	**Serial LED Enable.** Active high. Serial LED mode is enabled if this pin is high and the LC-SER_EN pin is low during power-on reset. Serial LED mode and Low-Cost Serial LED mode cannot be active at the same time. Refer to Section 5 "LED Modes" on page 25 for details.
G02	18	18	LC_SER_EN	I/O$_{PU}$	**Low-Cost Serial LED Enable.** Active high. Low-Cost Serial LED mode is enabled if this pin is high and SER_EN pin is high during power-on reset. Low-Cost Serial LED mode and Serial LED mode can not be active at the same time. See Section 5 "LED Modes" on page 25 for details.
K02	30	30	SLED_DO / INTR#	O$_{OD}$	**Serial LED Data.** Active low serial LED data. This pin becomes serial LED data output if SER_EN pin is high during power-on reset. See Section 5 "LED Modes" on page 25 for details. **PHY Interrupt.** Active low output. This pin becomes interrupt output if SER_EN pin is low during power-on reset.
F01 F02 E01 E02 P01 P02 N02 N01	12 11 10 9 47 46 45 44	12 11 10 9 47 46 45 44	TX_ER{1:8} LED1{1:8}	I/O$_{PD}$	**TXER[1:8].** Active high input. This pin becomes TXER input if TXER_EN pin is high during power-on reset. TXER function is typically used in HSTR application for transmitting halt codes. TXER[1:8] pins are sampled during power-on reset to set the default LED output for LED1, LED2 and LED3. See Section 5 "LED Modes" on page 25 for details. **LED1[1:8].** Active low output. This pin becomes LED1 output if TXER_EN pin is low during power-on reset. LED1 can be configured to output one of LINK, SPEED, ACTIVITY, FULL-DUPLEX, TRANSMIT, RECEIVE, INTERRUPT or COLLISION status. See Section 5 "LED Modes" on page 25 for details.
C04 E06 D05 C05 M07 N07 M06 N06		185 186 187 188 68 69 70 71	LED2{1:8}	O$_{OD}$	**LED2.** Active low. This pin can be configured to output one of SPEED, ACTIVITY, FULL-DUPLEX, TRANSMIT, RECEIVE, INTERRUPT, COLLISION, or LINK status. See Section 5 "LED Modes" on page 25 for details.

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I$_A$ = analog input, O$_A$ = analog output,
I$_{PU}$ = digital input w/ internal pull-up, I$_{PD}$ = digital input w/ internal pull-down, O$_{OD}$ = open-drain output,
O$_{3S}$ = three-state output, I/O$_{PD}$ = bidirectional w/ internal pull-down, B = bias.
Bus naming convention: Pin label followed by {Port #}.

Table 2:   Pin Definitions (Cont.)

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
D03		189			
B03		190			
E05		191			**LED3.** Active low. The function of this LED signal
D04		192	LED3{1:8}	O_{3S}	can be configured to output one of ACTIVITY,
M05		72			FULL-DUPLEX, LINK or SPEED status. Refer to
N04		73			Section 5 "LED Modes" on page 25 for details.
N05		74			
M04		75			
Bias					
A15	161	160	RDAC	B	**DAC Bias Resistor.** Adjusts the current level of each of the transmit DAC's. A resistor of 1.24 KΩ ±1% must be connected between the RDAC pin and AGND.
A14	162	161	VREF	B	**Voltage Reference.** Low-impedance bias pin driven by the internal band-gap voltage reference. This pin must be left unconnected during normal operation.
JTAG					
L02	37	37	TDI	I_{PU}	**Test Mode Select.** Serial data input to the JTAG TAP controller. Sampled on the rising edge of TCK. If unused, may be left unconnected.
L03	35	35	TMS	I_{PU}	**Test Data Input.** Single control input to the JTAG TAP controller used to traverse the test-logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected.
L05	36	36	TCK	I_{PU}	**Test Clock.** Clock input used to synchronize the JTAG TAP control and data transfers. If unused, may be left unconnected.
K04	33	33	TDO	O_{3S}	**Test Data Output.** Serial data output from the JTAG TAP Controller. Updated on the falling edge of TCK. Actively driven both high and low when enabled; high impedance otherwise.
K05	34	34	TRST#	I_{PU}	**Test Reset.** Asynchronous active-low reset input to the JTAG TAP Controller. Must be held low during power-up to insure the TAP Controller initializes to the test-logic-reset state. May be pulled low continuously when JTAG functions are not used. Must be held low for normal operation.
Power					
T14	101	102	PLLVDDC		**2.5V, Phase Locked Loop VDD Core (VDDC)**
R14	98	99	PLLGND		**Phase Locked Loop GND**
A16	160	159	BIASVDD		**2.5V, Bias VDD**

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output,
I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output,
O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = bias.
Bus naming convention: Pin label followed by {Port #}.

Broadcom Corporation

Table 2:   Pin Definitions (Cont.)

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
B16	163	162	BIASGND		**Bias GND**
A05	67	65			
C07	73	78			
C10	85	90			
C13	91	92	AVDD		**2.5V, Analog VDD**
P07	169	168			
P11	175	170			
T04	187	182			
T13	193	195			
B05		59			
B14	61	64			
B15	66	66			
C06	70	77			
C08	74	79			
C09	79	84			
C11	84	89			
C12	88	91			
D09	92	93			
D10	97	98	AGND		**Analog GND**
E09	168	167			
P05	172	169			
P06	176	171			
P08	181	176			
P09	186	181			
P10	190	183			
P12	194	194			
P13	199	196			
R04		201			
R13					
E04	2	2			
E13	15	15			
G04	48	48	DVDD		**2.5V, Digital Core VDD**
K14	111	111			
L04	132	132			
N13	154	154			
C14	1	1			
F03	14	14			
G06	49	49	DGND		**Digital Core GND**
J13	110	110			
M03	133	133			
N14	155	155			

= active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = bias.
Bus naming convention: Pin label followed by {Port #}.

Table 2: Pin Definitions (Cont.)

BCM5228B	BCM5228F	BCM5228U	Pin Label	I/o	Description
D06		13			
E03	13	16			
F14	16	39			
G13	39	67			
H03	100	101			
K03	121	121	OVDD		**3.3V, Digital Periphery (Output Buffer) VDD**
L13	122	122			
M14	143	143			
N08	144	144			
P14		184			
D13		38			
F06	38	58			
F07	60	76			
H11	112	112			
H14	131	131	OGND		**Digital Periphery (Output Buffer) GND**
J04	134	134			
L06	153	153			
L07	200	193			
N16		202			

 # = active low, I = digital input, O = digital output, I/O = bidirectional, I_A = analog input, O_A = analog output, I_{PU} = digital input w/ internal pull-up, I_{PD} = digital input w/ internal pull-down, O_{OD} = open-drain output, O_{3S} = three-state output, I/O_{PD} = bidirectional w/ internal pull-down, B = bias.
Bus naming convention: Pin label followed by {Port #}.

Section 3: Pinout Diagrams

Figure 1 provides the pinout diagram for the BCM5228F (FX Support).
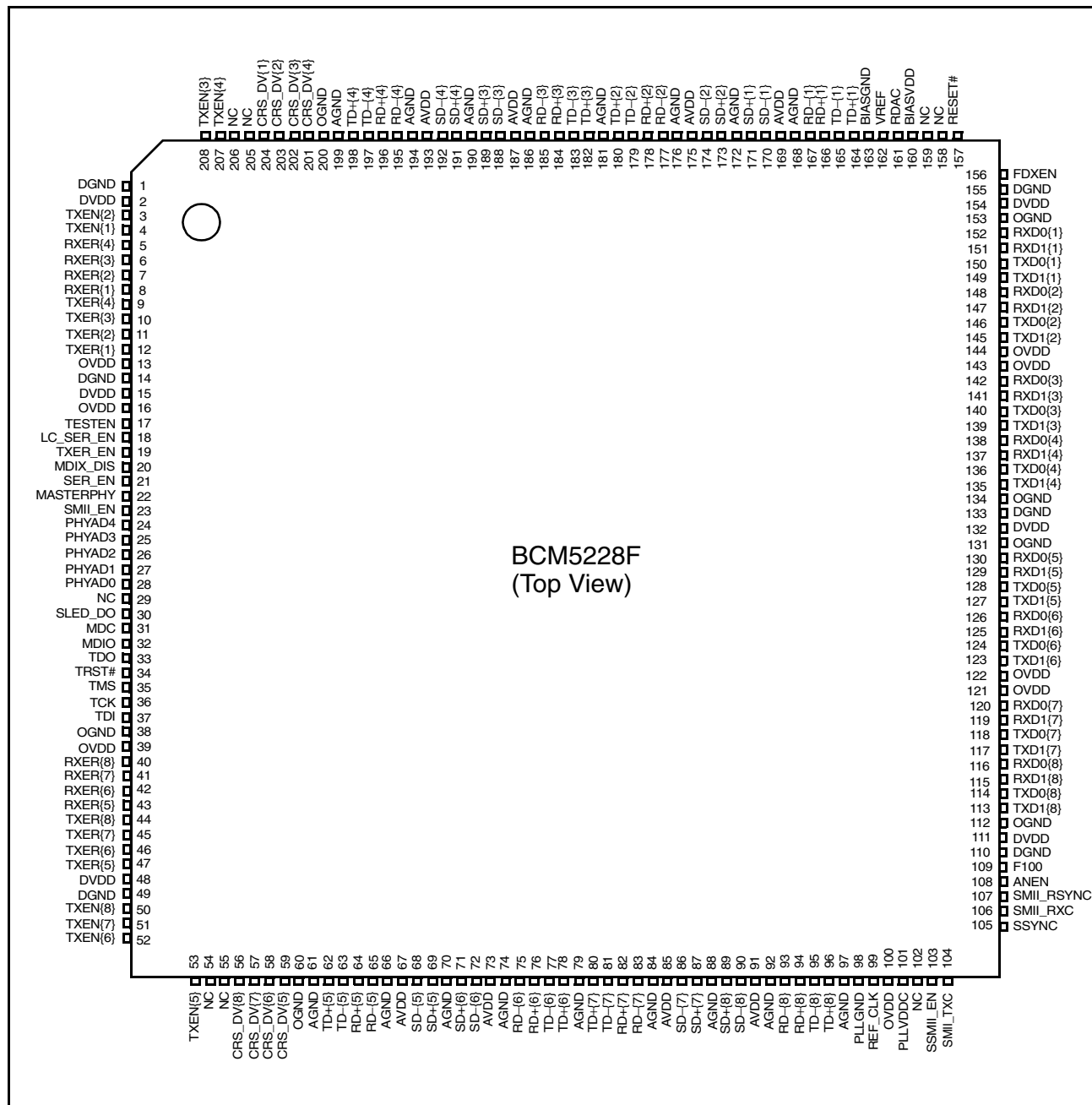
BCM5228F
(Top View)

Figure 1:   BCM5228F Pinout Diagram

Figure 2 provides the pinout diagram for the BCM5228U (UTP Support).
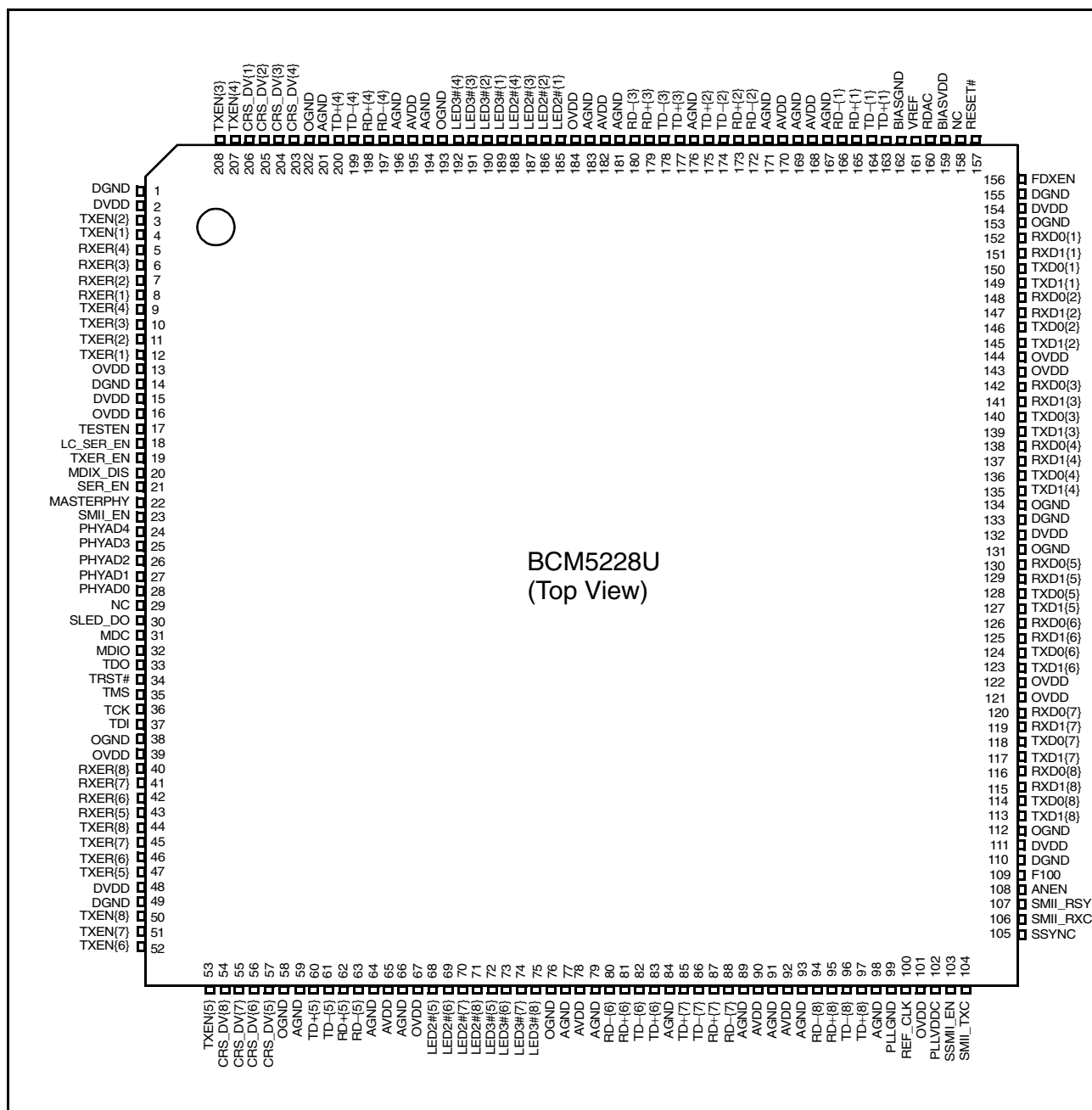
Figure 2:   BCM5228U Pinout Diagram

	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	
A	TXEN{4}	CRS_DV{1}	CRS_DV{2}	CRS_DV{4}	AVDD	TD+{4}	RD+{4}	RD+{3}	TD+{3}	TD+{2}	RD+{2}	RD+{1}	TD+{1}	VREF	RDAC	BIASVDD	A
B	TXEN{3}	TXEN{2}	LED3{2}	CRS_DV{3}	AGND	TD-{4}	RD-{4}	RD-{3}	TD-{3}	TD-{2}	RD-{2}	RD-{1}	TD-{1}	AGND	AGND	BIASGND	B
C	RXER{4}	RXER{3}	TXEN{1}	LED2{1}	LED2{4}	AGND	AVDD	AGND	AGND	AVDD	AGND	AGND	AVDD	DGND	FDXEN	RESET#	C
D	RXER{2}	RXER{1}	LED3{1}	LED3{4}	LED2{3}	OVDD	SD-{4}	SD+{3}	AGND	AGND	SD+{2}	SD+{1}	OGND	RXD1{1}	RXD0{1}	TXD1{1}	D
E	TX_ER{3}/LED1{3}	TX_ER{4}/LED1{4}	OVDD	DVDD	LED3{3}	LED2{2}	SD+{4}	SD-{3}	AGND	NC	SD-{2}	SD-{1}	DVDD	RXD1{2}	RXD0{2}	TXD0{1}	E
F	TX_ER{1}/LED1{1}	TX_ER{2}/LED1{2}	DGND	TESTEN	MDIX_DIS	OGND	OGND	TGND	TGND	TGND	TGND	RXD1{3}	RXD0{3}	OVDD	TXD1{2}	TXD0{2}	F
G	TXER_EN	LC_SER_EN	SERIAL_EN	DVDD	PHYAD4	DGND	TGND	TGND	TGND	TGND	TGND	RXD1{4}	OVDD	RXD0{4}	TXD1{3}	TXD0{3}	G
H	SMII_EN/SLED_CLK	MASTERPHY/SFRAME	OVDD	PHYAD2	PHYAD3	TGND	TGND	TGND	TGND	TGND	OGND	RXD1{5}	RXD0{5}	OGND	TXD1{4}	TXD0{4}	H
J	MDIO	NC	PHYAD0	OGND	PHYAD1	TGND	TGND	TGND	TGND	TGND	TGND	RXD1{6}	DGND	RXD0{6}	TXD1{5}	TXD0{5}	J
K	MDC	SLED_DO/INTR#	OVDD	TDO	TRST#	TGND	TGND	TGND	TGND	TGND	TGND	RXD1{7}	RXD0{7}	DVDD	TXD1{6}	TXD0{6}	K
L	RXER{8}	TDI	TMS	DVDD	TCK	OGND	OGND	TGND	TGND	TGND	TGND	RXD1{8}	OVDD	RXD0{8}	TXD1{7}	TXD0{7}	L
M	RXER{6}	RXER{7}	DGND	LED3{8}	LED3{5}	LED2{7}	LED2{5}	NC	SD-{5}	SD-{6}	SD-{7}	SD-{8}	ANEN	OVDD	TXD1{8}	TXD0{8}	M
N	TX_ER{8}/LED1{8}	TX_ER{7}/LED1{7}	RXER{5}	LED3{6}	LED3{7}	LED2{8}	LED2{6}	OVDD	SD+{5}	SD+{6}	SD+{7}	SD+{8}	DVDD	DGND	F100	OGND	N
P	TX_ER{5}/LED1{5}	TX_ER{6}/LED1{6}	TXEN{8}	TXEN{7}	AGND	AGND	AVDD	AGND	AGND	AGND	AVDD	AGND	AGND	OVDD	SSYNC	SMII_RSYNC	P
R	TXEN{6}	CRS_DV{6}	CRS_DV{5}	AGND	TD-{5}	RD-{5}	RD-{6}	TD-{6}	TD-{7}	RD-{7}	RD-{8}	TD-{8}	AGND	PLLGND	SSMII_EN	SMII_RXC	R
T	TXEN{5}	CRS_DV{8}	CRS_DV{7}	AVDD	TD+{5}	RD+{5}	RD+{6}	TD+{6}	TD+{7}	RD+{7}	RD+{8}	TD+{8}	AVDD	PLLVDDC	REF_CLK	SMII_TXC	T
	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	

Note: TGND balls are thermal grounds

Figure 3: BGA Pinout (Top View)

Table 3: BGA Ballout by Signal Name

Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
AGND	B05	CRS_DV{5}	R03	MASTERPHY/SFRAME	H02
AGND	B14	CRS_DV{6}	R02	MDC	K01
AGND	B15	CRS_DV{7}	T03	MDIO	J01
AGND	C06	CRS_DV{8}	T02	MDIX_DIS	F05

Table 3:   BGA Ballout by Signal Name (Cont.)

Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
AGND	C08	DGND	C14	NC	E10
AGND	C09	DGND	F03	NC	J02
AGND	C11	DGND	G06	NC	M08
AGND	C12	DGND	J13	OGND	D13
AGND	D09	DGND	M03	OGND	F06
AGND	D10	DGND	N14	OGND	F07
AGND	E09	DVDD	E04	OGND	H11
AGND	P05	DVDD	E13	OGND	H14
AGND	P06	DVDD	G04	OGND	J04
AGND	P08	DVDD	K14	OGND	L06
AGND	P09	DVDD	L04	OGND	L07
AGND	P10	DVDD	N13	OGND	N16
AGND	P12	F100	N15	OVDD	D06
AGND	P13	FDXEN	C15	OVDD	E03
AGND	R04	LC_SER_EN	G02	OVDD	F14
AGND	R13	LED2{1}	C04	OVDD	G13
ANEN	M13	LED2{2}	E06	OVDD	H03
AVDD	A05	LED2{3}	D05	OVDD	K03
AVDD	C07	LED2{4}	C05	OVDD	L13
AVDD	C10	LED2{5}	M07	OVDD	M14
AVDD	C13	LED2{6}	N07	OVDD	N08
AVDD	P07	LED2{7}	M06	OVDD	P14
AVDD	P11	LED2{8}	N06	PHYAD0	J03
AVDD	T04	LED3{1}	D03	PHYAD1	J05
AVDD	T13	LED3{2}	B03	PHYAD2	H04
BIASGND	B16	LED3{3}	E05	PHYAD3	H05
BIASVDD	A16	LED3{4}	D04	PHYAD4	G05
CRS_DV{1}	A02	LED3{5}	M05	PLLGND	R14
CRS_DV{2}	A03	LED3{6}	N04	PLLVDDC	T14
CRS_DV{3}	B04	LED3{7}	N05	RD-{1}	B12
CRS_DV{4}	A04	LED3{8}	M04	RD-{2}	B11
RD-{3}	B08	RXER{4}	C01	TD-{7}	R09
RD-{4}	B07	RXER{5}	N03	TD-{8}	R12
RD-{5}	R06	RXER{6}	M01	TD+{1}	A13
RD-{6}	R07	RXER{7}	M02	TD+{2}	A10
RD-{7}	R10	RXER{8}	L01	TD+{3}	A09

Broadcom Corporation

Table 3:   BGA Ballout by Signal Name (Cont.)

Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
RD-{8}	R11	SD-{1}	E12	TD+{4}	A06
RD+{1}	A12	SD-{2}	E11	TD+{5}	T05
RD+{2}	A11	SD-{3}	E08	TD+{6}	T08
RD+{3}	A08	SD-{4}	D07	TD+{7}	T09
RD+{4}	A07	SD-{5}	M09	TD+{8}	T12
RD+{5}	T06	SD-{6}	M10	TDI	L02
RD+{6}	T07	SD-{7}	M11	TDO	K04
RD+{7}	T10	SD-{8}	M12	TESTEN	F04
RD+{8}	T11	SD+{1}	D12	TGND	F08
RDAC	A15	SD+{2}	D11	TGND	F09
REF_CLK	T15	SD+{3}	D08	TGND	F10
RESET#	C16	SD+{4}	E07	TGND	F11
RXD0{1}	D15	SD+{5}	N09	TGND	G07
RXD0{2}	E15	SD+{6}	N10	TGND	G08
RXD0{3}	F13	SD+{7}	N11	TGND	G09
RXD0{4}	G14	SD+{8}	N12	TGND	G10
RXD0{5}	H13	SERIAL_EN	G03	TGND	G11
RXD0{6}	J14	SLED_DO/INTR#	K02	TGND	H06
RXD0{7}	K13	SMII_RSYNC	P16	TGND	H07
RXD0{8}	L14	SMII_RXC	R16	TGND	H08
RXD1{1}	D14	SMII_TXC	T16	TGND	H09
RXD1{2}	E14	SMII_EN/SLED_CLK	H01	TGND	H10
RXD1{3}	F12	SSMII_EN	R15	TGND	J06
RXD1{4}	G12	SSYNC	P15	TGND	J07
RXD1{5}	H12	TCK	L05	TGND	J08
RXD1{6}	J12	TD-{1}	B13	TGND	J09
RXD1{7}	K12	TD-{2}	B10	TGND	J10
RXD1{8}	L12	TD-{3}	B09	TGND	J11
RXER{1}	D02	TD-{4}	B06	TGND	K06
RXER{2}	D01	TD-{5}	R05	TGND	K07
RXER{3}	C02	TD-{6}	R08	TGND	K08
TGND	K09	TXD0{7}	L16	TXEN{6}	R01
TGND	K10	TXD0{8}	M16	TXEN{7}	P04
TGND	K11	TXD1{1}	D16	TXEN{8}	P03
TGND	L08	TXD1{2}	F15	TXER_EN	G01
TGND	L09	TXD1{3}	G15	TX_ER{1}/LED1{1}	F01

Broadcom Corporation

Table 3: BGA Ballout by Signal Name (Cont.)

Signal Name	Ball	Signal Name	Ball	Signal Name	Ball
TGND	L10	TXD1{4}	H15	TX_ER{2}/LED1{2}	F02
TGND	L11	TXD1{5}	J15	TX_ER{3}/LED1{3}	E01
TMS	L03	TXD1{6}	K15	TX_ER{4}/LED1{4}	E02
TRST#	K05	TXD1{7}	L15	TX_ER{5}/LED1{5}	P01
TXD0{1}	E16	TXD1{8}	M15	TX_ER{6}/LED1{6}	P02
TXD0{2}	F16	TXEN{1}	C03	TX_ER{7}/LED1{7}	N02
TXD0{3}	G16	TXEN{2}	B02	TX_ER{8}/LED1{8}	N01
TXD0{4}	H16	TXEN{3}	B01	VREF	A14
TXD0{5}	J16	TXEN{4}	A01		
TXD0{6}	K16	TXEN{5}	T01		

Broadcom Corporation

Section 4: Operational Description

RESETTING THE BCM5228

There are two ways to reset each transceiver in the BCM5228. A hardware reset pin has been provided which resets all internal nodes inside the chip to a known state. The reset pulse must be asserted for at least 2 microseconds. Hardware reset should always be applied to a BCM5228 after power-up.

Each transceiver in the BCM5228 also has an individual software reset capability. To perform software reset, a 1 must be written to bit 15 of the transceiver's MII Control Register (see MII Register Definitions). This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if a 0 is written to the MII Control Register reset bit.

ISOLATE MODE

Each transceiver in the BCM5228 may be isolated from the RMII. When a transceiver is put into isolate mode, all RMII inputs (TXD1,TXD0, TXEN, and TXER) are ignored, and all RMII outputs (CRS_DV, RXER, and RXD1,RXD0) are set at high impedance. Only the MII management pins (MDC, MDIO) operate normally. Upon resetting the chip, the isolate mode is off. Writing a 1 to bit 10 of the MII Control Register puts the transceiver into isolate mode. Writing a 0 to the same bit removes it from isolate mode.

LOOPBACK MODE

The loopback mode allows in-circuit testing of the BCM5228 chip. All packets sent in through the TXD pins are looped-back internally to the RXD pins, and are not sent out to the cable. Incoming packets on the cable are ignored.

The loopback mode may be entered by writing a 1 to bit 14 of the MII Control Register or by writing a 1 to bit 8 and bit 7 of shadow register 1Dh. In order to resume normal operation the bits must be 0.

Several function bypass modes are also supported which can provide a number of different combinations of feedback paths during loopback testing. These bypass modes include: bypass scrambler, bypass MLT3 encoder and bypass 4B5B encoder.

FULL-DUPLEX MODE

The BCM5228 supports full-duplex operation. While in full-duplex mode, a transceiver may simultaneously transmit and receive packets on the cable. By default, each transceiver in the BCM5228 powers up in half-duplex mode.

When auto negotiation is disabled, full-duplex operation can be enabled either by a pin (FDXEN) or by an MII register bit (Register 0' bit 8).

When auto negotiation is enabled in DTE mode, full-duplex capability is advertised by default but can be overridden by a write to the auto negotiation Advertisement Register (04h).

Broadcom Corporation

100BASE-FX MODE

Any of the BCM5228F transceivers may interface with an external 100BASE-FX fiber optic driver and receiver instead of the magnetics module used with twisted-pair cable. The differential transmit and receive data pairs will operate at PECL voltage levels instead of those required for twisted-pair transmission, if the termination scheme recommended in the application note is used. The data is encoded using two-level NRZI instead of three-level MLT3. The data stream is not scrambled for fiber-optic transmission. The stream cipher function is bypassed when 100BASE-FX mode is selected.

The external fiber optic receiver detects signal status and communicate it to the BCM5228B or BCM5228F through the SD± pins. In this mode, the internal signal detect function is bypassed. The 100BASE-FX mode is automatically selected whenever a valid differential signal is detected at the SD± input pins. Pulling both SD+ and SD- low simultaneously disables the 100BASE-FX mode.

10BASE-T MODE

The same magnetics module is used to interface the twisted-pair cable in 10BASE-T mode and in 100BASE-TX mode. The data is two-level Manchester coded instead of three-level MLT3 and no scrambling/descrambling or 4B5B coding is performed.

Data and clock rates are decreased by a factor of 10, with the RMII interface operating at 2.5 MHz.

PHY ADDRESS

Each transceiver in the BCM5228 has a unique PHY address for MII management. The PHY address is determined by the using the base address, which is input on the PHYAD[4:0] pins. The following shows the addressing of the eight PHYs.

PHY0 = PHYAD + 0, PHY1 = PHYAD + 1,... PHY7 = PHYAD + 7

Every time an MII write or read operation is executed, the transceiver compares the PHY address with its own PHY address definition. The operation is executed only when the addresses match.

Section 5: LED Modes

DESCRIPTION

The BCM5228 offers rich set of LED display outputs through serial and parallel LED modes. There are two serial LED modes available, Serial LED mode and Low-Cost Serial LED mode. The serial LED mode provides compatibility with few other Broadcom PHYs. Serial LED modes are selected by hardware only during power-on reset. When any serial LED mode is enabled global hardware interrupt feature is not available. However, if interrupt and a serial or a Low-Cost Serial LED mode is desired simultaneously, then a parallel LED can be programmed to provide on interrupt output per port and eight such interrupt can be ORed to obtain a global interrupt.

SERIAL LED MODE

Serial LED mode is enabled only by having SER_EN pin high and LC_SER_EN pin low during power-on reset. If serial LED mode is enabled then Low-Cost Serial LED mode and hardware global interrupt is disabled. In serial LED mode the BCM5228 sources a serial data stream, the associated clock, and a framing signal as follows:

Serial data stream, SLED_DO which is an active low bit stream containing 48 bits per frame.

Serial data clock, SLED_CLK which runs at approximately 2 MHz is used to clock out SLED_DO on the falling edge of this clock. SLED-DO is valid on the rising edge of this clock.

Framing pulse, SFRAME which is a logic high pulse occurring once every 48 SLED_DO bit times. SFRAME goes high coincident with bit 0 of port 1.

The BCM5228 provides two different serial LED stream depending on bit 14 of MII register 1Ah. When the serial LED mode is enabled by hardware, and no further action is taken, the Normal (default) LED stream is selected for SLED_DO. If Interrupt enable bit 14 of register 1Ah is set to a 1, then Interrupt LED stream is selected for SLED_DO. See Table 4 below for details.

Table 4:   Serial LED Mode Bit Framing

Option	Reg 1Ah	Serial Bit 5	Serial Bit 4	Serial Bit 3	Serial Bit 2	Serial Bit 1	Serial Bit 0
Normal	Bit 14 = 0	FDX	COL	Speed100	Link	Transmit	Receive
Interrupt	Bit 14 = 1	FDX	Global interrupt	Speed100	Link	Port interrupt	Activity

Note **A global interrupt indicates an interrupt from any of the eight PHYs as if they were ORed together. A port interrupt is provided on a per-PHY basis.**

Broadcom Corporation

LOW-COST SERIAL LED MODE

The Low-Cost Serial LED mode is enabled by pulling both LC_SER_EN pin and SER_EN pin high during power-on reset. When enabled, serial LED data stream, SLED_DO, is shifted out on the falling edge of SLED_CLK. SLED_DO is valid on the rising edge of this clock. The data is shifted in such a manner that the update of LEDs using a simple shift register that drive the display LEDs will not cause noticeable flicker in normal operation.

There are six banks, bank 1 through bank 6, associated with six LED outputs. Each bank has its own MII register bits that select LED a signal to output from that bank. Selected signal from each bank is shifted out on the LED_DO pin in the following order: Bank 1 for port 1 through port 8, Bank 2 for port 1 through port 8,…, and Bank 6 for port 1 through 8 for a total of 48 LED outputs. The Low-Cost Serial LED mode programmable banks are located in the MII shadow register 1Ah of port 2 and port 3. See Table 5, Table 6, Table 7, Table 8, Table 9 and Table 10 for programming details. The default LED outputs are SPEED, LINK, FULL-DUPLEX, ACTIVITY, SPEED, and LINK for bank 1 through bank 6 respectively.

Table 5:   Low-Cost Serial Mode Bank 1 LED Selection

MII Shadow Register 1Ah, PHY 3, Bits [2:0]	Value	LED Selection
SERIAL BANK 1 SELECT BITS[2:0]	0	Speed
	1	Activity
	2	Full-duplex
	3	Transmit
	4	Receive
	5	Interrupt
	6	Collision
	7	Link
Note: MII Shadow Register is accessed by setting MII Register 1Fh bit 7 to a 1.		

Table 6:   Low-Cost Serial Mode Bank 2 LED Selection

MII Shadow Register 1Ah, PHY 3, Bits [5:3]	Value	LED Selection
SERIAL LED BANK 2 SELECT BITS[2:0]	0	Link
	1	Speed
	2	Activity
	3	Full-duplex
	4	Transmit
	5	Receive
	6	Interrupt
	7	Collision
Note: MII Shadow Register is accessed by setting MII Register 1Fh bit 7 to a 1.		

Broadcom Corporation

Table 7:   Low-Cost Serial Mode Bank 3 LED Selection

MII Shadow Register 1Ah, PHY 3, Bits [8:6]	Value	LED Selection
Serial LED Bank 3 Select Bits[2:0]	0	Full-duplex
	1	Transmit
	2	Receive
	3	Interrupt
	4	Collision
	5	Link
	6	Speed
	7	Activity
Note: MII Shadow Register is accessed by setting MII Register 1Fh bit 7 to a 1.		

Table 8:   Low-Cost Serial Mode Bank 4 LED Selection

MII Shadow Register 1Ah, PHY 2, Bits [2:0]	Value	LED Selection
Serial LED Bank 4 Select Bits[2:0]	0	Activity
	1	Full-duplex
	2	Transmit
	3	Receive
	4	Interrupt
	5	Collision
	6	Link
	7	Speed
Note: MII Shadow Register is accessed by setting MII Register 1Fh bit 7 to a 1.		

Table 9: Low-Cost Serial Mode Bank 5 LED Selection

MII Shadow Register 1Ah, PHY 2, Bits [5:3]	Value	LED Selection
SERIAL LED BANK 5 SELECT BITS[2:0]	0	Speed
	1	Activity
	2	Full-duplex
	3	Transmit
	4	Receive
	5	Interrupt
	6	Collision
	7	Link

Note: MII Shadow Register is accessed by setting MII Register 1Fh bit 7 to a 1.

Table 10: Low-Cost Serial Mode Bank 6 LED Selection

MII Shadow Register 1Ah, PHY 2, Bits [8:6]	Value	LED Selection
SERIAL BANK 6 SELECT BITS[2:0]	0	Link
	1	Speed
	2	Activity
	3	Full-duplex
	4	Transmit
	5	Receive
	6	Interrupt
	7	Collision

Note: MII Shadow Register is accessed by setting MII Register 1Fh bit 7 to a 1.

PARALLEL LED MODE

The BCM5228U offers a parallel LED mode that is active all the time. There are 3 LED pins, LED1, LED2, and LED3 for each port each of which can be individually configured to output one of many LED signals. Configuration can be accomplished either by hardware or programming MII register bits. LED1 pins are shared with TXER. These pins can be configured to output LED1 if TXER_EN pin is pulled low during power-on reset.

For unmanaged system design using the BCM5228U, the parallel LED pins for each port can be programmed through hardware during power-on reset by pull-down or pull-up combinations of TXER/LED1 [1:8] pins. Pull-up and pull-down of these pins should be done using a series 4.7-KΩ resistor to OVDD or OGND respectively and LED drive and polarity should be such that the active low output on LED1 lights up the LED. LED2 and LED3 can be configured to output one of Link, Speed, Activity, Full-duplex, Transmit, Receive, Interrupt or Collision while LED3 can be configured to be one of Activity, Full-duplex, Link or Speed. Software configuration of LED1, LED2 and LED3 is accomplished through MII shadow register 1Ah, Phy 1, bits [7:0]. See Table 11, Table 12 and Table 13 for details. Because LED2{1:8} pins are open drain, they can be wire 0Red together and configured (by hardware during power-on reset or through software by setting bits in the MII shadow register) to provide global hardware interrupt when required.

Table 11:   Parallel LED Mode LED1 Selection

TXER[3:1]	MII Shadow Register 1Ah, PHY 1, Bits [2:0]	Value	LED1 Selection
POWER-ON LED1 SELECT BITS[2:0]	LED1 Select[2:0]	0	Link
		1	Speed
		2	Activity
		3	Full-duplex
		4	Transmit
		5	Receive
		6	Interrupt
		7	Collision
Note: MII Shadow Register is accessed by setting MII Register 1Fh bit 7 to a 1.			

Table 12:   Parallel LED Mode LED2 Selection

TXER [6:4]	MII Shadow Register 1Ah, PHY 1, Bits [5:3]	Value	LED2 Selection
POWER-ON RESET LED2 SELECT[2:0]	LED2 Select[2:0]	0	Speed
		1	Activity
		2	Full-duplex
		3	Transmit
		4	Receive
		5	Interrupt
		6	Collision
		7	Link
Note: MII Shadow Register is accessed by setting MII Register 1Fh bit 7 to a 1.			

Broadcom Corporation

Table 13:   Parallel LED Mode LED3 Selection

TXER [8:7]	MII Shadow Register 1Ah, PHY 1, Bits [7:6]	Value	LED3 Selection
POWER-ON RESET LED3 SELECT[1:0]	LED3 SELECT[1:0]	0	Activity
		1	Full-duplex
		2	Link
		3	Speed
Note: MII shadow register is accessed by setting MII Register 1Fh bit 7 to a 1.			

Section 6: Register Summary

MII MANAGEMENT INTERFACE: REGISTER PROGRAMMING

The BCM5228 fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers of each port are serially written-to and read from using a common set of MDIO and MDC pins. A single clock waveform must be provided to the BCM5228 at a rate of 0-25 MHz through the MDC pin. The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock. Every MII read or write instruction frame contains the following fields:

Table 14:   MII Management Frame Format

Operation	PRE	ST	OP	PHYAD	REGAD	TA	Data	Idle	Direction
Read	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Z Z	Driven to BCM5228 Driven by BCM5228
Write	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Z	Driven to BCM5228

Preamble (PRE). Thirty-two consecutive 1 bits must be sent through the MDIO pin to the BCM5228 to signal the beginning of an RMII instruction. Fewer than 32 1 bits causes the remainder of the instruction to be ignored.

Start of Frame (ST). A 01 pattern indicates that the start of the instruction follows.

Operation Code (OP). A Read instruction is indicated by 10, while a Write instruction is indicated by 01.

PHY Address (PHYAD). A 5-bit PHY address follows next, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple PHY chips. The BCM5228 supports a complete address space with PHYAD[4:0] input-pins used as the base address for selecting one of the eight transceivers.

Register Address (REGAD). A 5-bit Register Address follows, with the MSB transmitted first. The register map of the BCM5228, containing register addresses and bit definitions, are provided on the following pages.

Turnaround (TA). The next two bit times are used to avoid contention on the MDIO pin when a Read operation is performed. For a Write operation, 10 must be sent to the BCM5228 chip during these two bit times. For a Read operation, the MDIO pin must be placed into High-Impedance during these two bit times. The chip drives the MDIO pin to 0 during the second bit time.

Data. The last 16 bits of the frame are the actual data bits. For a Write operation, these bits are sent to the BCM5228, whereas, for a Read operation, these bits are driven by the BCM5228. In either case, the MSB is transmitted first. When writing to the BCM5228, the data field bits must be stable 10 nanoseconds before the rising edge of MDC, and must be held valid for 10 nanoseconds after the rising edge of MDC. When reading from the BCM5228, the data field bits are valid after the rising-edge of MDC until the next rising edge of MDC.

Idle. A high impedance state of the MDIO line. All tri-state drivers are disabled and the PHY's pull-up resistor pulls the MDIO line to logic 1. Note that at least one or more idle states are required between frames. Following are two examples of MII write and read instructions.

1. To put a transceiver with PHY address 00001 into Loopback mode, the following MII write instruction must be issued

1111 1111 1111 1111 1111 1111 1111 1111   0101 00001 00000 10 0100 0000 0000 0000 1...

2. To determine if a PHY is in the link pass state, the following MII read instruction must be issued

1111 1111 1111 1111 1111 1111 1111 1111   0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ 1...

Broadcom Corporation

For the MII read operation, the BCM5228 drives the MDIO line during the TA and Data fields (the last 17 bit times). A final 65th clock pulse must be sent to close the transaction and cause a write operation to take place.

MII REGISTER MAP SUMMARY

Table 15 contains the MII register summary for each port of the BCM5228. The register addresses are specified in hex form, and the name of register bits have been abbreviated. When writing to the reserved bits, always write a 0 value, and when reading from these bits, ignore the output value. Never write any value to an undefined register address. The reset value of the registers are shown in the Init column.

Table 15:   MII Register Map Summary

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Init
00h	Control	Soft Reset	Loop-back	Force100	Auto Neg Enable	Power Down	Isolate	Restart Auto Neg	Full Duplex	Coll-ision Test	Reserved							3000h
01h	Status	T4 Capable	TX FDX Capable	TX Capable	BT FDX Capable	10BT Capable	Reserved				MF pream supp-ress	Auto Neg comp	Remote Fault	Auto Neg Capable	Link Status	Jabber Detect	Extd Reg Capable	7809h
02h	PhyID High	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0040h
03h	PhyID Low	0	1	1	0	0	0	0	1	1	Model # 1	0	1	Revision # 0	0	0	0	61D0h
04h	Auto Neg Advertise	Next Page	Re-served	Remote Fault	Reserved Tech		Pause	Adv T4	Adv TX FDX	Adv TX	Adv BT FDX	Adv BT	Advertised Selector Field[4:0] 0	0	0	0	1	01E1h
05h	Link Partner Ability	LP Next Page	LP Acknow-ledge	LP Rem Fault	Reserved Tech		LP Pause	LP T4	LP TX FDX	LP TX	LP BT FDX	LP BT	Link Partner Selector Field [4:0]					0000h
06h	Auto Neg Expansion	Reserved											Par Det Fault	LP Next Pg Able	Next Pg Able	Page Recvd	LP Auto Neg Able	0004h
07h	Next Page	Next Page	Re-served	Message Page	Acknowledge2	Toggle	Message/Unformatted Code Field											2001h
08h	LP Next Page	Next Page	Re-served	Message Page	Acknowledge2	Toggle	Message/Unformatted Code Field											0000h
10h	100BASE-X Aux Control	Reserved		Trans Disable	Reserved		Bypass 4B5B Enc/Dec	Bypass Scram/De-scram	Bypass NRZI Enc/Dec	Bypass Rcv Sym Align	Base-line Wander Disable	FEF Enable	Reserved				Re-served	0000h
11h	100BASE-X Aux Status	Reserved			R/SMII Over Under Run		FX Mode	Locked	Current 100 Link Status	Current Remote Fault	Re-served	False Carrier De-tected	Bad ESD De-tected	RCV Error De-tected	Ex-tended RMII FIFOs	RMII Out of Band		0000h
12h	100BASE-X RCV Error Counter	Receive Error Counter[15:0]																0000h

Table 15: MII Register Map Summary (Cont.)

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Init
13h	100BASE-X False Carrier Counter	RMII/SMII Over-run/Under-run Counter[7:0]								False Carrier Sense Counter[7:0]								0000h
14h	100BASE-X Disconnect Counter	RMII/ SMII Fastrxd	RMII/ SMII Slowrxd	Reserved														0200h
15h	Reserved	Reserved																0300h
16h	Reserved	Reserved																0000h
17h	PTest	Reserved																0000h
18h	Auxiliary Control/ Status	Jabber Disable	Force Link	Reserved					TXDAC Power Mode	HSQ	LSQ	Edge Rate[1:0]		Auto Neg Enable Indi-cator	Force 100 Indi-cator	SP100 Indi-cator	FDX Indi-cator	003xh
19h	Auxiliary Status Summary	Auto Neg Com-plete	Auto Neg Com-plete Ack	AutoNeg Ack Detect	Auto Neg Ability Detect	Auto Neg Pause	Auto Neg HCD			Auto Neg Pardet Fault	LP Remote Fault	LP Page Rcvd	LP Auto Neg Able	SP100 Indi-cator	Link Status	Internal Auto Neg Enabled	Full-Duplex Indi-cation	0000h
1Ah	Interrupt	Re-served	INTR Enable	Reserved		FDX Mask	SPD Mask	Link Mask	INTR Mask	Reserved			Global Interrupt Status	FDX Change	SPD Change	Link Change	INTR Status	8F0xh
1Bh	Auxiliary Mode2	Reserved				10BT Dribble Correct	Token Ring Mode	HSTR FIFO Enable	Re-served	Block 10BT Echo Mode	Traffic Meter LED Mode	Activity LED Force On	Serial LED Enable	SQE Disable	Activity/ Link LED Enable	Qual Parallel Detect Mode	Re-served	008Ah
1Ch	10BASE-T Aux. Error & General Status	Reserved		MDIX Status	MDIX Manual Swap	HP Auto-MDIX Disable	Manch-str Code Err (BT)	EOF Err (BT)	Re-served	0	0	1	Re-served	Auto Neg Enable Indi-cator	Force 100 Indi-cator	SP100 Indi-cator	FDX Indi-cator	002xh
1Dh	Auxiliary Mode	Reserved				Reserved							Activity LED Force Inactive	Link LED Force Inactive	Re-served	Block TXEN Mode	Re-served	x000h
1Eh	Auxiliary Multi-PHY	HCD TX FDX	HC T4	HCD TX	HCD 10BT FDX	HCD 10BT	Reserved		Restart Auto Neg	Auto Neg Com-plete	Reserved	ACK Detect	Ability Detect	Super Isolate	Reserved		RXER Code Mode	0000h
1Fh	Broadcom Test	Reserved							Shadow Register Enable	Reserved								000Bh

Table 16: MII Shadow Register Map Summary (MII Register 1Fh, bit7 = 1)

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Init
18h	Reserved	Reserved																003Ah
1Ah	Auxiliary Mode 4 (PHY 1)	Reserved							MII LED Select enable	Parallel LED3 Select[1:0]		Parallel LED2 Select[2:0]			Parallel LED1 Select[2:0]			3000h
1Ah	Auxiliary Mode 4 (PHY 2)	Reserved							Serial Bank 6 Select[2:0]			Serial Bank 5 Select[2:0]			Serial Bank 4 Select[2:0]			3000h
1Ah	Auxiliary Mode 4 (PHY 3)	Reserved							Serial Bank 3 Select[2:0]			Serial Bank 2 Select[2:0]			Serial Bank 1 Select[2:0]			3000h
1Bh	Auxiliary Status 2	MLT3 Detect	Cable Length 100x[2:0]			ADC Peak Amplitude[5:0]						Reserved						0000h
1Ch	Auxiliary Status 3	Noise[7:0] (Root Mean Square error)								FLP Detect	NLP Detect	Link Break Timer Expire	Link Fail Timer Expire	FIFO Consumption[3:0]				0000h
1Dh	Auxiliary Mode 3	Reserved												FIFO Size Select[3:0]				0C04h
1Eh	Auxiliary Status4	Packet Length Counter[15:0]																0000h

MII CONTROL REGISTER

Table 17:   MII Control Register (Address 00d, 00h)

Bit	Name	R/W	Description	Default
15	Soft Reset	R/W (SC)	1 = PHY reset 0 = Normal operation	0
14	Loopback	R/W	1 = loopback mode 0 = Normal operation	0
13	Forced Speed Selection	R/W	1 = 100 megabits/second 0 = 10 megabits/second	1
12	Auto Negotiation Enable	R/W	1 = Auto negotiation enable 0 = Auto negotiation disable	1
11	Power Down	RO	0 = Normal operation	0
10	Isolate	R/W	1 = Electrically isolate PHY from RMII 0 = Normal operation	0
9	Restart Auto Negotiation	R/W (SC)	1 = Restart auto negotiation process 0 = Normal operation	0
8	Duplex Mode	R/W	1 = Full-duplex 0 = Half-duplex	0
7	Reserved	RO	Ignore when read	0
6:0	Reserved	RO	Ignore when read	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Soft Reset. To reset the BCM5228 by software control, a 1 must be written to bit 15 of the Control Register using an MII write operation. The bit clears itself after the reset process is complete, and need not be cleared using a second MII write. Writes to other Control Register bits will have no effect until the reset process is completed, which requires approximately 1 microsecond. Writing a 0 to this bit has no effect. Since this bit is self-clearing, after a few cycles from a write operation, it returns a 0 when read.

Loopback. The BCM5228 may be placed into loopback mode by writing a 1 to bit 14 of the Control Register. The loopback mode may be cleared by writing a 0 to bit 14 of the control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in software-controlled loopback mode, otherwise it returns a 0.

Forced Speed Selection. If auto negotiation is enabled, this bit has no effect on the speed selection. However, if auto negotiation is disabled by software control, the operating speed of the BCM5228 can be forced by writing the appropriate value to bit 13 of the Control Register. Writing a 1 to this bit forces 100BASE-X operation, while writing a 0 forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. In order to read the overall state of forced speed selection, including both hardware and software control, use bit 2of the Auxiliary Error and General Status Register, 1Ch.

Auto Negotiation Enable. Auto negotiation can be disabled by one of two methods: hardware or software control. If the ANEN input pin is driven to a logic 0, auto negotiation is disabled by hardware control. If bit 12 of the Control Register is written with a value of 0, auto negotiation is disabled by software control. When auto negotiation is disabled in this manner, writing a 1 to the same bit of the Control Register or resetting the chip re-enables auto negotiation. Writing to this bit has no effect when auto negotiation has been disabled by hardware control. When read, this bit returns the value most recently written to this location, or 1 if it has not been written since the last chip reset.

Power Down. The BCM5228 does not implement a low power mode.

Isolate. Each individual PHY may be isolated from its Media Independent Interface by writing a 1 to bit 10 of the Control Register. All RMII outputs is tri-stated and all RMII inputs are ignored. Because the MII management interface is still active, the isolate mode may be cleared by writing a 0 to bit 10 of the control register, or by resetting the chip. When this bit is read, it returns a 1 when the chip is in isolate mode, otherwise, it returns a 0.

Restart Auto Negotiation. Bit 9 of the Control Register is a self-clearing bit that allows the auto negotiation process to be restarted, regardless of the current status of the auto negotiation state machine. In order for this bit to have an effect, auto negotiation must be enabled. Writing a 1 to this bit restarts the auto negotiation, while writing a 0 to this bit has no effect. Since the bit is self-clearing after only a few cycles, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Auxiliary Multiple PHY Register.

Duplex Mode. By default, the BCM5228 powers up in half-duplex mode. The chip can be forced into full-duplex mode by writing a 1 to bit 8 of the Control Register while auto negotiation is disabled. Half-duplex mode can be resumed by writing a 0 to bit 8 of the Control Register, or by resetting the chip.

Reserved Bits. All reserved MII Register bits must be written as 0 at all times. Ignore the BCM5228 output when these bits are read.

Broadcom Corporation

MII STATUS REGISTER

Table 18: MII Status Register (Address 01d, 01h)

Bit	Name	R/W	Description	Default
15	100BASE-T4 Capability	RO	0 = Not 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX full-duplex capable	1
13	100BASE-TX Capability	RO	1 = 100BASE-TX half-duplex capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T full-duplex capable	1
11	10BASE-T Capability	RO	1 = 10BASE-T half-duplex capable	1
10:7	Reserved	RO	Ignore when read	0000
6	MF Preamble Suppression	R/W	1 = Preamble may be suppressed 0 = Preamble always required	0
5	Auto Negotiation Complete	RO	1 = Auto negotiation process completed 0 = Auto negotiation process not completed	0
4	Remote Fault	RO LH	1 = Far-End Fault condition detected 0 = No Far-End Fault condition detected	0
3	Auto Negotiation Capability	RO	1 = Auto negotiation capable 0 = Not auto negotiation capable	1
2	Link Status	RO LL	1 = Link is up (Link Pass state) 0 = Link is down (Link Fail state)	0
1	Jabber Detect	RO LH	1 = Jabber condition detected 0 = No Jabber condition detected	0
0	Extended Capability	RO	1 = Extended register capable	1

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

100BASE-T4 Capability. The BCM5228 is not capable of 100BASE-T4 operation, and returns a 0 when bit 15 of the status register is read.

100BASE-X Full-Duplex Capability. The BCM5228 is capable of 100BASE-X full-duplex operation, and returns a 1 when bit 14 of the Status Register is read.

100BASE-X Half-Duplex Capability. The BCM5228 is capable of 100BASE-X half-duplex operation, and returns a 1 when bit 13 of the Status Register is read.

10BASE-T Full-Duplex Capability. The BCM5228 is capable of 10BASE-T full-duplex operation, and returns a 1 when bit 12 of the Status Register is read.

10BASE-T Half-Duplex Capability. The BCM5228 is capable of 10BASE-T half-duplex operation, and returns a 1 when bit 11 of the Status Register is read.

Reserved Bits. Ignore the BCM5228 output when these bits are read.

MF Preamble Suppression. This bit is the only writable bit in the Status Register. Setting this bit to a 1 allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When preamble suppression is enabled, only two preamble bits are required between successive management commands, instead of the normal 32.

Auto Negotiation Complete. Bit 5 of the Status Register returns a 1 if the auto negotiation process has been completed and the contents of registers 4, 5 and 6 are valid.

Remote Fault. The PHY returns a 1 in bit 4 of the Status Register when its link partner has signalled a far-end fault condition. When a far-end fault occurs, the bit is latched at 1 and remains so until the register is read and the remote fault condition has been cleared; this only applies to the FX mode of operation.

Auto Negotiation Capability. The BCM5228 is capable of performing IEEE auto negotiation, and returns a 1 when bit 4 of the Status Register is read, regardless of whether or not the auto negotiation function has been disabled.

Link Status. The BCM5228 returns a 1 on bit 2 of the Status Register when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it returns 0. When a link failure occurs after the Link Pass state has been entered, the Link Status bit is latched at 0 and remains so until the bit is read. After the bit is read, it becomes 1 if the Link Pass state has been entered again.

Jabber Detect. 10BASE-T operation only. The BCM5228 returns a 1 on bit 1 of the Status Register if a jabber condition has been detected. After the bit is read, or if the chip is reset, it reverts to 0.

Extended Capability. The BCM5228 supports extended capability registers, and returns a 1 when bit 0 of the Status Register is read. Several extended registers have been implemented in the BCM5228, and their bit functions are defined later in this section.

PHY IDENTIFIER REGISTERS

Table 19: PHY Identifier Registers (Addresses 02d and 03d, 02h and 03h)

Bit	Name	R/W	Description	Value
15:0	MII Address 00010	RO	PHYID high	0040h
15:0	MII Address 00011	RO	PHYID low	XXXXh

Broadcom Corporation has been issued an Organizationally Unique Identifier (OUI) by the IEEE. It is a 24-bit number, 00-10-18, expressed as hex values. That number, along with the Broadcom Model Number for the BCM5228 part, 1Ch, and Broadcom Revision number, 00h, is placed into two MII Registers. The translation from OUI, Model Number and Revision Number to PHY Identifier Register occurs as follows:

PHYID High[15:0] = OUI[21:6]

PHYID Low[15:0] = OUI[5:0] + Model[5:0] + Rev[3:0]

Note **The two most significant bits of the OUI are not represented (OUI[23:22]).**

Figure 19 on page 39 shows the result of concatenating these values to form the MII Identifier Registers PHYID HIGH and PHYID LOW.

Broadcom Corporation

AUTO NEGOTIATION ADVERTISEMENT REGISTER

Table 20: Auto Negotiation Advertisement Register (Address 04d, 04h)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Next Page ability is enabled 0 = Next Page ability is disabled	0
14	Reserved	RO	Ignore when read	
13	Remote Fault	R/W	1 = Transmit Remote Fault	0
12:11	Reserved Technologies	RO	Ignore when read	00
10	Pause	R/W	1 = Pause operation for full-duplex	0
9	Advertise 100BASE-T4	R/W	1 = Advertise T4 capability 0 = Do not advertise T4 capability	0
8	Advertise 100BASE-X FDX	R/W	1 = Advertise 100BASE-X full-duplex 0 = Do not advertise 100BASE-X full-duplex	1
7	Advertise 100BASE-X	R/W	1 = Advertise 100BASE-X	1
6	Advertise 10BASE-T FDX	R/W	1 = Advertise 10BASE-T full-duplex 0 = Do not advertise 10BASE-T full-duplex	1
5	Advertise 10BASE-T	R/W	1 = Advertise 10BASE-T	1
4:0	Advertise Selector Field	R/W	Indicates 802.3	00001

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Next Page. The BCM5228 supports Next Page function.

Reserved Bits. Ignore output when read.

Remote Fault. Writing a 1 to bit 13 of the Advertisement Register causes a Remote Fault indicator to be sent to the Link Partner during auto negotiation. Writing a 0 to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it, or else 0, if no write has been completed since the last chip reset.

Reserved Technologies Bits. Ignore output when read.

Pause. Pause operation for full-duplex links. The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate pause capability to its Link Partner and has no effect on PHY operation.

Advertisement Bits. Bits 9:5 of the Advertisement Register allow the user to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the BCM5228. By writing a 1 to any of the bits, the corresponding ability is transmitted to the Link Partner. Writing a 0 to any bit causes the corresponding ability to be suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset.

Selector Field. Bits 4:0 of the Advertisement Register contain the value 00001, indicating that the chip belongs to the 802.3 class of PHY transceivers.

AUTO NEGOTIATION LINK PARTNER (LP) ABILITY REGISTER

Table 21:   Auto Negotiation Link Partner Ability Register (Address 05d, 05h)

Bit	Name	R/W	Description	Default
15	LP Next Page	RO	Link Partner next page bit	0
14	LP Acknowledge	RO	Link Partner acknowledge bit	0
13	LP Remote Fault	RO	Link Partner remote fault indicator	0
12:11	Reserved Technologies	RO	Ignore when read	000
10	LP Advertise Pause	RO	Link Partner has Pause capability	0
9	LP Advertise 100BASE-T4	RO	Link Partner has 100BASE-T4 capability	0
8	LP Advertise 100BASE-X FDX	RO	Link Partner has 100BASE-X FDX capability	0
7	LP Advertise 100BASE-X	RO	Link Partner has 100BASE-X capability	0
6	LP Advertise 10BASE-T FDX	RO	Link Partner has 10BASE-T FDX capability	0
5	LP Advertise 10BASE-T	RO	Link Partner has 10BASE-T capability	0
4:0	Link Partner Selector Field	RO	Link Partner selector field	00000

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Note that the values contained in the auto negotiation Link Partner Ability Register are only guaranteed to be valid once auto negotiation has successfully completed, as indicated by bit 5 of the MII Status Register.

LP Next Page. Bit 15 of the Link Partner Ability Register returns a value of 1 when the Link Partner implements the Next Page function and has Next Page information that it wants to transmit. The BCM5228 does not implement the Next Page function, and thus ignores the Next Page bit, except to copy it to this register.

LP Acknowledge. Bit 14 of the Link Partner Ability Register is used by auto negotiation to indicate that a device has successfully received its Link Partner's link code word.

LP Remote Fault. Bit 13 of the Link Partner Ability Register returns a value of 1 when the Link Partner signals that a remote fault has occurred. The BCM5228 simply copies the value to this register and does not act upon it.

Reserved Bits. Ignore when read.

LP Advertise Pause. Indicates that the Link Partner Pause bit is set.

LP Advertise Bits. Bits 9:5 of the Link Partner Ability Register reflect the abilities of the Link Partner. A 1 on any of these bits indicates that the Link Partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time auto negotiation is restarted or the BCM5228 is reset.

LP Selector Field. Bits 4:0 of the Link Partner Ability Register reflect the value of the Link Partner's selector field. These bits are cleared any time auto negotiation is restarted or the chip is reset.

AUTO NEGOTIATION EXPANSION REGISTER

Table 22:   Auto Negotiation Expansion Register (Address 06d, 06h)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Ignore when read	000h
4	Parallel Detection Fault	RO LH	1 = Parallel Detection Fault. 0 = No Parallel Detection Fault	0
3	Link Partner Next Page Able	RO	1 = Link Partner has Next Page capability 0 = Link Partner does not have Next Page	0
2	Next Page Able	RO	1 = Next Page able	1
1	Page Received	RO	1 = New page has been received 0 = New page has not been received	0
0	Link Partner Auto Negotiation Able	RO LH	1 = Link Partner has auto negotiation capability 0 = Link Partner does not have auto negotiation	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Reserved Bits. Ignore when read.

Parallel Detection Fault. Bit 4 of the auto negotiation Expansion Register is a read-only bit that gets latched high when a parallel detection fault occurs in the auto negotiation state machine. For further details, consult the IEEE standard. The bit is reset to 0 after the register is read, or when the chip is reset.

Link Partner Next Page Able. Bit 3 of the auto negotiation Expansion Register returns a 1 when the Link Partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability Register.

Next Page Able. The BCM5228 Returns 1 when bit 2 of the auto negotiation Expansion Register is read indicating that it has Next Page capabilities.

Page Received. Bit 1 of the auto negotiation Expansion Register is latched high when a new link code word is received from the Link Partner, checked, and acknowledged. It remains high until the register is read, or until the chip is reset.

Link Partner Auto Negotiation Able. Bit 0 of the auto negotiation Expansion Register returns a 1 when the Link Partner is known to have auto negotiation capability. Before any auto negotiation information is exchanged, or if the Link Partner does not comply with IEEE auto negotiation, the bit returns a value of 0.

AUTO NEGOTIATION NEXT PAGE REGISTER

Table 23:   Next Page Transmit Register (Address 07d, 07h)

Bit	Name	R/W	Description	Default
15	Next Page	R/W	1 = Additional Next Page(s) follows 0 = Last page	0
14	Reserved	R/W	Ignore when read	0
13	Message Page	R/W	1= Message page 0 = Unformatted page	1
12	Acknowledge 2	R/W	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted link code word 　　equalled logic zero 0 = Previous value of the transmitted Link Code Word 　　equalled logic one	0
10:0	Message/Unformatted Code Field	R/W		1

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Next Page. Indicates whether this is the last Next Page to be transmitted.

Message Page. Differentiates a Message Page from an unformatted page.

Acknowledge 2. Indicates that a device has the ability to comply with the message.

Toggle. Used by the arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field. An eleven-bit wide field, encoding 2048 possible messages.

Unformatted Code Field. An eleven-bit wide field, which may contain an arbitrary value.

AUTO NEGOTIATION LINK PARTNER (LP) NEXT PAGE TRANSMIT REGISTER

Table 24: Next Page Transmit Register (Address 08d, 08h)

Bit	Name	R/W	Description	Default
15	Next Page	RO	1 = Additional Next Page(s) follows 0 = Last page	0
14	Reserved	RO	Ignore when read	0
13	Message Page	RO	1= Message page 0 = Unformatted page	0
12	Acknowledge 2	RO	1 = Will comply with message 0 = Cannot comply with message	0
11	Toggle	RO	1 = Previous value of the transmitted Link Code Word equalled logic zero 0 = Previous value of the transmitted Link Code Word equalled logic one	0
10:0	Message/Unformatted Code Field	RO		0
R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s).				

Next Page. Indicates whether this is the last Next Page.

Message Page. Differentiates a Message Page from an unformatted page.

Acknowledge 2. Indicates that Link Partner has the ability to comply with the message.

Toggle. Used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange.

Message Code Field. An eleven-bit wide field, encoding 2048 possible messages.

Unformatted Code Field. An eleven-bit wide field, which may contain an arbitrary value.

100BASE-X AUXILIARY CONTROL REGISTER

Table 25:   100-BASE-X Auxiliary Control Register (Address 16d, 10h)

Bit	Name	R/W	Description	Default
15:14	Reserved		Write as 0, ignore on read	0
13	Transmit Disable	R/W	1 = Transmitter disabled in PHY 0 = Normal operation	0
12	Reserved	R/W	Write as 0, ignore when read	0
11	Reserved		Write as 0, ignore when read	0
10	Bypass 4B5B Encoder/Decoder	R/W	1 = Transmit and receive 5B codes over RMII pins 0 = Normal RMII	0
9	Bypass Scrambler/Descrambler	R/W	1 = Scrambler and descrambler disabled 0 = Scrambler and descrambler enabled	0
8	Bypass NRZI Encoder/Decoder	R/W	1 = NRZI encoder and decoder is disabled 0 = NRZI encoder and decoder is enabled	0
7	Bypass Receive Symbol Alignment	R/W	1 = 5B receive symbols not aligned 0 = Receive symbols aligned to 5B boundaries	0
6	Baseline Wander Correction Disable	R/W	1 = Baseline wander correction disabled 0 = Baseline wander correction enabled	0
5	FEF Enable	R/W	1 = Far-End Fault enabled. 0 = Far-End Fault disabled.	0
4:3	Reserved	R/W	Write as 0, ignore when read	0
2	Extended FIFO Enable	R/W	1 = Extended FIFO mode, 0 = Normal FIFO mode	0
1	RMII Out-of-Band Enable	R/W	1 = Enabled 0 = Disabled	0
0	Reserved	R/W	Write as 0, ignore when read	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Transmit Disable. The transmitter may be disabled by writing a 1 to bit 13 of MII Register 10h. The transmitter output (TD±) is forced into a high impedance state.

Bypass 4B5B Encoder/Decoder. The 4B5B encoder and decoder may be bypassed by writing a 1 to bit 10 of MII Register 10h. The transmitter sends 5B codes from the TXER and TXD1,TXD0 pins directly to the scrambler. TXEN must be active, and frame encapsulation (insertion of J/K and T/R codes) is not performed. The receiver places descrambled and aligned 5B codes onto the RXER, RXD1 and RXD0 pins. CRS is asserted when a valid frame is received.

Bypass Scrambler/Descrambler. The Stream Cipher function may be disabled by writing a 1 to bit 9 of MII Register 10h. The Stream Cipher function may be re-enabled by writing a 0 to this bit.

Bypass NRZI Encoder/Decoder. The NRZI encoder and decoder can be bypassed by writing a 1 to bit 8 of MII Register 10h, causing 3-level NRZI data to be transmitted and received on the cable. Normal operation (3-level NRZI encoding and decoding) may be re-enabled by writing a 0 to this bit.

Bypass Receive Symbol Alignment. Receive Symbol Alignment may be bypassed by writing a 1 to bit 7 of MII Register 10h. When used in conjunction with the bypass 4B5B encoder/decoder bit, unaligned 5B codes are placed directly on the RXER and RXD1, RXD0 pins.

Baseline Wander Correction Disable. The Baseline Wander Correction circuit may be disabled by writing a 1 to bit 6 of MII Register 10h. The BCM5228 corrects for baseline wander on the receive data signal when this bit is cleared.

FEF Enable. Controls the Far-End Fault mechanism associated with 100BASE-FX operation. A 1 enables the FEF function, and a 0 disables it.

Extended RMII/SMII FIFO Enable. Controls the Extended RMII/SMII FIFO mechanism.

RMII Out-of-Band Enable. Controls the RMII Out-of-Band mechanism within the RMII receive logic.

Reserved Bits. The Reserved bits of the 100BASE-X Auxiliary Control Register must be written as 0 at all times. Ignore the BCM5228 outputs when these bits are read.

Broadcom Corporation

100BASE-X AUXILIARY STATUS REGISTER

Table 26: 100BASE-X Auxiliary Status Register (Address 17d, 11h)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	Ignore when read	0
11	R/SMII Overrun/Underrun Detected	RO	1 = Error detected 0 = No error	0
10	FX Mode	RO	1 = 100BASE-FX mode 0 = 100BASE-TX or 10BASE-T mode	PIN
9	Locked	RO	1 = Descrambler locked 0 = Descrambler unlocked	0
8	Current 100BASE-X Link Status	RO	1 = Link pass 0 = Link fail	0
7	Remote Fault	RO	1 = Remote Fault detected 0 = No Remote Fault detected	0
6	Reserved	RO	Ignore when read	0
5	False Carrier Detected	RO LH	1 = False Carrier detected since last read 0 = No False Carrier since last read	0
4	Bad ESD Detected	RO LH	1 = ESD error detected since last read 0 = No ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit Error code received since last read 0 = No Transmit Error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock Error detected since last read 0 = No Lock Error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 Code Error detected since last read 0 = No MLT3 Code Error since last read	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

R/SMII Overrun/Underrun Error. The PHY returns a 1 in bit 11, when the RMII receive FIFO encounters an overrun or underrun condition.

FX Mode. Returns a value derived from the SD± input pins. Returns a 1 when SD± are driven with a valid differential signal level. Returns a 0 when both SD+ and SD- are simultaneously driven low.

Locked. The PHY returns a 1 in bit 9 when the descrambler is locked to the incoming data stream. Otherwise, it returns a 0.

Current 100BASE-X Link Status. The PHY returns a 1 in bit 8 when the 100BASE-X Link Status is good. Otherwise, it returns a 0.

Remote Fault. The PHY returns a 1 while its link partner is signalling a far-end fault condition. Otherwise, it returns a 0.

False Carrier Detected. The PHY returns a 1 in bit 5 of the extended status register if a false carrier has been detected since the last time this register was read. Otherwise, it returns a 0.

Bad ESD Detected. The PHY returns a 1 in bit 4 if an end-of-stream delimiter error has been detected since the last time this register was read. Otherwise, it returns a 0.

Receive Error Detected. The PHY returns a 1 in bit 3 if a packet was received with an invalid code since the last time this register was read. Otherwise, it returns a 0.

Transmit Error Detected. The PHY returns a 1 in bit 2 if a packet was received with a Transmit Error code since the last time this register was read. Otherwise, it returns a 0.

Lock Error Detected. The PHY returns a 1 in bit 1 if the descrambler has lost lock since the last time this register was read. Otherwise, it returns a 0.

MLT3 Code Error Detected. The PHY returns a 1 in bit 0 if an MLT3 coding error has been detected in the receive data stream since the last time this register was read. Otherwise it returns a 0.

100BASE-X RECEIVE ERROR COUNTER

Table 27:   100BASE-X Receive Error Counter (Address 18d, 12h)

Bit	Name	R/W	Description	Default
15:0	Receive Error Counter [15:0]	R/W	Number of Non-Collision packets with Receive Errors since last read	0000h

Receive Error Counter [15:0]. This counter increments each time the BCM5228 receives a non-collision packet containing at least one receive error. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting receive errors until cleared

100BASE-X FALSE CARRIER SENSE COUNTER

Table 28:   100BASE-X False Carrier Sense Counter (Address 19d, 13h)

Bit	Name	R/W	Description	Default
15:8	RMII/SMII Overrun/Underrun Counter [7:0]	R/W	Number of RMII Overruns/Underruns since last read	00h
7:0	False Carrier Sense Counter [7:0]	R/W	Number of False Carrier Sense events since last read	00h

RMII/SMII Overrun/Underrun Counter [7:0]. The RMII/SMII Overrun/Underrun Counter increments each time the BCM5228 detects an overrun or underrun of the RMII/SMII FIFOs. The counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting overrun/underrun errors until cleared.

False Carrier Sense Counter [7:0]. This counter increments each time the BCM5228 detects a false carrier on the receive input. This counter automatically clears itself when read. When the counter reaches its maximum value, FFh, it stops counting false carrier sense errors until cleared.

100BASE-X DISCONNECT COUNTER

Table 29:   100BASE-X Disconnect Counter

Bit	Name	R/W	Description	Default
15	RMII/SMII Fast RXD	R/O	1 = In extended FIFO mode, detect fast receive data 0 = Normal	0
14	RMII/SMII Slow RXD	R/O	0 = Normal 1 = In extended FIFO mode, detect slow receive data	0
13:8	Reserved	R/W	Write as 000010, ignore when read	000010
7:0	Reserved	R/W	Write as 00h, ignore when read	00h

> R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
> Use default values of reserved bit(s) when writing to reserved bit(s).

RMII/SMII Fast RXD. Extended FIFO operation only. Bit 15 of the Disconnect Counter Register indicates the FIFO state machine has detected fast receive data relative to the REF_CLK input.

RMII/SMII Slow RXD. Extended FIFO operation only. Bit 14 of the Disconnect Counter Register indicates the FIFO state machine has detected slow receive data relative to the REF_CLK input.

AUXILIARY CONTROL/STATUS REGISTER

Table 30:   Auxiliary Control/Status Register (Address 24d, 18h)

Bit	Name	R/W	Description	Default
15	Jabber Disable	R/W	1= Jabber function disabled in PHY 0 = Jabber function enabled in PHY	0
14	Link Disable	R/W	1= Link Integrity test disabled in PHY 0 = Link Integrity test is enabled in PHY	0
13:8	Reserved	RO	Ignore when read	000000
7:6	HSQ : LSQ	R/W	These two bits define the squelch mode of the 10BASE-T carrier sense mechanism: 00 = normal squelch 01 = low squelch 10 = high squelch 11 = not allowed	00
5:4	Edge Rate [1:0]	R/W	00 = 1 nanosecond 01 = 2 nanoseconds 10 = 3 nanoseconds 11 = 4 nanoseconds	11
3	Auto Negotiation Indicator	RO	1 = Auto negotiation activated 0 = Speed forced manually	1

> R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
> Use default values of reserved bit(s) when writing to reserved bit(s).

Table 30:　Auxiliary Control/Status Register (Address 24d, 18h) (Cont.)

Bit	Name	R/W	Description	Default
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-duplex Indication	RO	1 = Full-Duplex active 0 = Full-Duplex not active	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Jabber Disable. 10BASE-T operation only. Bit 15 of the Auxiliary Control Register allows the user to disable the Jabber Detect function, defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing a 1 to bit 15 of the Auxiliary Control Register, the Jabber Detect function is disabled. Writing a 0 to this bit or resetting the chip restores normal operation. Reading this bit returns the value of Jabber Detect disable.

Link Disable. Writing a 1 to bit 14 of the Auxiliary Control Register allows the user to disable the Link Integrity state machines, and place the BCM5228 into forced Link Pass status. Writing a 0 to this bit or resetting the chip restores the Link Integrity functions. Reading this bit returns the value of Link Integrity Disable.

HSQ and LSQ. Extend or decrease the squelch levels for detection of incoming 10BASE-T data packets. The default squelch levels implemented are those defined in the IEEE standard. The high- and low-squelch levels are useful for situations where the IEEE-prescribed levels are inadequate. The squelch levels are used by the CRS/LINK block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the BCM5228 to operate properly over longer cable lengths. Decreasing the squelch levels may be useful in situations where there is a high level of noise present on the cables. Reading these two bits returns the value of the squelch levels.

Edge Rate [1:0]. Control bits used to program the transmit DAC output Edge Rate in 100BASE-TX mode. These bits are logically ANDed with the ER [1:0] input pins to produce the internal edge-rate controls (Edge_Rate [1] AND ER [1], Edge_Rate [0] AND ER [0]).

Auto Negotiation Indicator. A read-only bit that indicates whether auto negotiation has been enabled or disabled on the BCM5228. A combination of a 1 in bit 12 of the Control Register and a logic 1 on the ANEN input pin is required to enable auto negotiation. When auto negotiation is disabled, bit 3 of the Auxiliary Control Register returns a 0. At all other times, it returns a 1.

Force100/10 Indication. A read-only bit that returns a value of 0 when one of following two cases is true:

- The ANEN pin is low *AND* the F100 pin is low, or
- Bit 12 of the Control Register has been written 0 *AND* bit 13 of the Control Register has been written 0.

When bit 8 of the Auxiliary Control Register is 0, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (auto negotiation is enabled), or the speed is forced to 100BASE-X.

Speed Indication. Bit 1 of the Auxiliary Control Register is a read-only bit that shows the true current operation speed of the BCM5228. A 1 bit indicates 100BASE-X operation, while a 0 indicates 10BASE-T. Note that while the auto negotiation exchange is performed, the BCM5228 is always operating at 10BASE-T speed.

Full-Duplex Indication. Bit 0 of the Auxiliary Control Register is a read-only bit that returns a 1 when the BCM5228 is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY STATUS SUMMARY REGISTER

Auxiliary Status Summary Register contains copies of redundant status bits found elsewhere within the MII register space.

Table 31:   Auxiliary Status Summary Register (Address 25d, 19h)

Bit	Name	R/W	Description	Default
15	Auto Negotiation Complete	RO	1 = Auto negotiation process completed	0
14	Auto Negotiation Complete Acknowledge	RO LH	1 = Auto negotiation completed acknowledge state	0
13	Auto Negotiation Acknowledge Detected	RO LH	1 = Auto negotiation acknowledge detected	0
12	Auto Negotiation Ability Detect	RO LH	1 = Auto negotiation for Link Partner ability	0
11	Auto Negotiation Pause	RO	BCM5228 & Link Partner Pause operation bit set	0
10:8	Auto Negotiation HCD	RO	000 = No highest common denominator 001 = 10BASE-T 010 = 10BASE-T full-duplex 011 = 100BASE-TX 100 = 100BASE-T4 101 = 100BASE-TX full-duplex 11x = undefined	000
7	Auto Negotiation Parallel Detection Fault	RO LH	1 = Parallel detection fault	0
6	Link Partner Remote Fault	RO	1 = Link Partner has signalled a far-end fault condition in FX mode	0
5	Link Partner Page Received	RO LH	1 = New Page has been received	0
4	Link Partner Auto Negotiation Able	RO	1 = Link Partner is auto negotiation capable	0
3	Speed Indicator	RO	1 = 100 megabits/second 0 = 10 megabits/second	0
2	Link Status	RO LL	1 = Link is up (link pass state)	0
1	Auto Negotiation Enabled	RO	1 = Auto negotiation enabled	1
0	Full-Duplex Indication	RO LL	1 = Full-Duplex active 0 = Full-Duplex not active	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Descriptions for each of these individual bits can be found associated with their primary register descriptions.

Broadcom Corporation

INTERRUPT REGISTER

Table 32:   Interrupt Register (Address 26d, 1Ah)

BIt	Name	R/W	Description	Default
15	Reserved	R/W	Ignore on read	1
14	INTR Enable	R/W	Interrupt enable	0
13:12	Reserved	RO	Ignore when read	00
11	FDX Mask	R/W	Full-duplex interrupt mask	1
10	SPD Mask	R/W	SPEED Interrupt mask	1
9	LINK Mask	R/W	LINK interrupt mask	1
8	INTR Mask	R/W	Master interrupt mask	1
7:5	Reserved	RO	Ignore when read	000
4	Global Interrupt Indicator	RO	1= Indicates an interrupt is present within the BCM5228	0
3	FDX Change	RO, LH	Duplex change interrupt	0
2	SPD Change	RO, LH	Speed change interrupt	0
1	LINK Change	RO, LH	Link change interrupt	0
0	INTR Status	RO, LH	Interrupt status	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Interrupt Enable. Setting this bit enables Interrupt mode. The state of this bit also affects which status signals are shifted out on the serial LED data in Serial LED mode. See Figure 4 on page 25 for details.

FDX Mask. When this bit is set, changes in duplex mode will not generate an interrupt.

SPD Mask. When this bit is set, changes in operating speed will not generate an interrupt.

Link Mask. When this bit is set, changes in Link status will not generate an interrupt.

Interrupt Mask. Master Interrupt Mask. When this bit is set, no interrupts will be generated, regardless of the state of the other mask bits.

Global Interrupt Indicator. A 1 indicates an Interrupt is present within the BCM5228.

FDX Change. A 1 indicates a change of Duplex status since last register read. Register read clears the bit.

SPD Change. A 1 indicates a change of Speed status since last register read. Register read clears the bit.

Link Change. A 1 indicates a change of Link status since last register read. Register read clears the bit.

Interrupt Status. Represents status of the INTR# pin. A 1 indicates that the interrupt mask is off and that one or more of the change bits are set. Register read clears the bit.

Broadcom Corporation

AUXILIARY MODE 2 REGISTER

Table 33:   Auxiliary Mode 2 Register (Address 27d, 1Bh)

Bit	Name	R/W	Description	Default
15:12	Reserved	RO	Ignore when read	0
11	10BT Dribble Bit Correct	R/W	1 = Enable, 0 = Disable	0
10	Token Ring Mode	R/W	1 = Enable, 0 = Disable	0
9	HSTR FIFO Enable	R/W	1 = Enable, 0 = Disable	0
8	Reserved	RO	Ignore when read	0
7	Block 10BT Echo Mode	R/W	1 = Enable, 0 = Disable	1
6	Traffic Meter LED Mode	R/W	1 = Enable, 0 = Disable	0
5	Activity LED Force On	R/W	1 = On, 0 = Normal operation	0
4	Reserved	R/W	Ignore when read	1
3	Reserved	R/W	Write as 1, ignore when read	1
2	Activity/Link LED Mode	R/W	1 = Enable, 0 = Disable	0
1	Qual Parallel Detect Mode	R/W	1 = Enable, 0 = Disable	1
0	Reserved	RO	Ignore when read	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

10BT Dribble Bit Correct. When enabled, the PHY will round-down to the nearest nibble when dribble bits are present on the 10BASE-T input stream.

Token Ring Mode. When enabled, the 100BASE-X unlock timer changes to allow long packets.

HSTR FIFO Mode. When enabled, the RMII/SMII receive FIFO will double from 7 nibbles to 14 nibbles.

Block 10BT Echo Mode. When enabled, during 10BASE-T half-duplex transmit operation, the TXEN signal does not echo onto the RXDV pin. The TXEN echoes onto the CRS pin, and the CRS deassertion directly follows the TXEN deassertion.

Traffic Meter LED Mode. When enabled, the Activity LEDs (ACTLED# and FDXLED# if Full-Duplex LED and Interrupt LED modes are not enabled) do not blink based on the internal LED clock (approximately 80 microseconds of time). Instead, they blink based on the rate of receive and transmit activity. Each time a receive or transmit operation occurs, the LED turns on for a minimum of 5 microseconds. During light traffic, the LED blinks at a low rate, while during heavier traffic the LEDs remain on.

Activity LED Force On. When asserted, the Activity LEDs (ACTLED# and FDXLED# if Full-Duplex LED and Interrupt LED modes are not enabled) are turned on. This bit has a higher priority than the Activity LED Force Inactive, bit 4, register 1Dh.

Activity/Link LED Mode. When enabled, the receive output goes active upon acquiring link and pulses during receive or transmit activity.

Qualified Parallel Detect Mode. This bit allows the auto negotiation/parallel detection process to be qualified with information in the Advertisement Register.

If this bit is not set, the local BCM5228 device is enabled to auto-negotiate, and the far-end device is a 10BASE-T or 100BASE-X non auto-negotiating legacy type, the local device auto-negotiates/parallel-detects the far-end device, regardless of the contents of its Advertisement Register (04h).

If this bit is set, the local device compares the link speed detected to the contents of its Advertisement Register. If the particular link speed is enabled in the Advertisement Register, the local device asserts link. If the link speed is disabled in this register, then the local device does not assert link and continues monitoring for a matching capability link speed.

10BASE-T AUXILIARY ERROR & GENERAL STATUS REGISTER

Table 34:   10BASE-T Auxiliary Error & General Status Register (Address 28d, 1Ch)

Bit	Name	R/W	Description	Default
15:14	Reserved	RO	Ignore when read	0
13	MDIX Status	RO	0 = MDI is in use 1 = MDIX is in use	0
12	MDIX Manual Swap	RW	0 = MDI or MDIX if MDIX is not disabled 1 = Force MDIX	0
11	HP Auto-MDIX Disable	R/W	0 = Enable HP Auto-MDIX 1 = Disable HP Auto-MDIX	0
10	Manchester Code Error	RO	1 = Manchester code error (10BASE-T)	0
9	End Of Frame Error	RO	1 = EOF detection error (10BASE-T)	0
8	Reserved	RO	Ignore when read	0
7:5	Reserved	RO	Ignore when read	001
4	Reserved	RO	Ignore when read	0
3	Auto Negotiation Indication	RO	1 = Auto negotiation activated 0 = Speed forced manually	1
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	1
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	0
0	Full-duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Note **All Error bits in the Auxiliary Error and General Status Register are read-only and are latched high. When certain types of errors occur in the BCM5228, one or more corresponding error bits become 1. They remain so until the register is read, or until a chip reset occurs. All such errors necessarily result in data errors, and are indicated by a high value on the RXER output pin at the time the error occurs.**

MDIX Status. This bit, when read as a 1, indicates that the MDI TD± and RD± signals for the BCM5228 have been swapped. The cause for this is one of the following:
• the MDIX Swap bit was manually set to a 1, or
• the HP Auto-MDIX function is enabled and the BCM5228 has detected an MDI cross-over cable.

MDIX Manual Swap. When this bit is set to a 1, the MDI TD± and RD± signals for the BCM5228 are forced into being swapped.

Broadcom Corporation

HP Auto-MDIX Disable. When this bit is set to a 1, the HP Auto-MDIX function is disabled in the BCM5228.

Manchester Code Error. Indicates that a Manchester code violation was received. This bit is only valid during 10BASE-T operation.

End of Frame Error. Indicates that the end of frame (EOF) sequence was improperly received, or not received at all. This error bit is only valid during 10BASE-T operation.

Auto Negotiation Indication. A read-only bit that indicates whether auto negotiation has been enabled or disabled on the BCM5228. A combination of a 1 in bit 12 of the Control Register and a logic 1 on the ANEN input pin is required to enable auto negotiation. When auto negotiation is disabled, bit 15 of the Auxiliary Mode Register returns a 0. At all other times, it returns a 1.

Force 100/10 Indication. A read-only bit that returns a value of 0 when one of following two cases is true:

- The ANEN pin is low *AND* the F100 pin is low, or
- Bit 12 of the Control Register has been written 0 *AND* bit 13 of the Control Register has been written 0.

When bit 2 of the Auxiliary Control Register is 0, the speed of the chip is 10BASE-T. In all other cases, either the speed is not forced (auto negotiation is enabled), or the speed is forced to 100BASE-X.

Speed Indication. A read-only bit that shows the true current operation speed of the BCM5228. A 1 bit indicates 100BASE-X operation, while a 0 indicates 10BASE-T. Note that while the auto negotiation exchange is performed, the BCM5228 is always operating at 10BASE-T speed.

Full-Duplex Indication. A read-only bit that returns a 1 when the BCM5228 is in full-duplex mode. In all other modes, it returns a 0.

AUXILIARY MODE REGISTER

Table 35: Auxiliary Mode Register (Address 29d, 1Dh)

Bit	Name	R/W	Description	Default
15:5	Reserved	RO	Ignore when read	000h
4	Activity LED Disable		1 = Disable XMT/RCV Activity LED outputs 0 = Enable XMT/RCV Activity LED outputs	0
3	Link LED Disable		1 = Disable Link LED output 0 = Enable Link LED output	0
2	Reserved	RO	Ignore when read	0
1	Block TXEN Mode	R/W	1 = Enable Block TXEN mode 0 = Disable Block TXEN mode	0
0	Reserved	RO	Ignore when read	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Activity LED Disable. When set to 1, disables the ACTLED# output pin. When 0, ACTLED# output pin is enabled.

Link LED Disable. When set to 1, disables the Link LED output pin. When 0, Link LED output is enabled.

Block TXEN Mode. When this mode is enabled, short IPGs of 1, 2, 3, or 4 TXC cycles all result in the insertion of two idles before the beginning of the next packet's JK symbols.

Broadcom Corporation

AUXILIARY MULTIPLE PHY REGISTER

Table 36:   Auxiliary Multiple PHY Register (Address 30d, 1Eh)

Bit	Name	R/W	Description	Default
15	HCD_TX_FDX	RO	1 = Auto negotiation result is 100BASE-TX full-duplex	0
14	HCD_T4	RO	1 = Auto negotiation result is 100BASE-T4	0
13	HCD_TX	RO	1 = Auto negotiation result is 100BASE-TX	0
12	HCD_10BASE-T_FDX	RO	1 = Auto negotiation result is 10BASE-T full-duplex	0
11	HCD_10BASE-T	RO	1 = Auto negotiation result is 10BASE-T	0
10:9	Reserved	RO	Ignore when read	00
8	Restart Auto Negotiation	R/W (SC)	1 = Restart auto negotiation process 0 = (No effect)	0
7	Auto Negotiation Complete	RO	1 = Auto negotiation process completed 0 = Auto negotiation process not completed	0
6	Acknowledge Complete	RO	1 = Auto negotiation acknowledge completed	0
5	Acknowledge Detected	RO	1 = Auto negotiation acknowledge detected	0
4	Ability Detect	RO	1 = Auto negotiation waiting for LP ability	0
3	Super Isolate	R/W	1 = Super Isolate mode 0 = Normal operation	0
2	Reserved	RO	Ignore when read	0
1	10BASE-T Serial Mode	R/W	1 = Enable 10BASE-T Serial mode 0 = Disable 10BASE-T Serial mode	0
0	Reserved	R/W	Write as 0, ignore when read	0

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

HCD Bits. Bits 15:11 of the Auxiliary Multiple PHY Register are five read-only bits that report the highest common denominator (HCD) result of the auto negotiation process. Immediately upon entering the Link Pass state after each reset or restart auto negotiation, only one of these five bits will be 1. The Link Pass state is identified by a 1 in bit 6 or 7 of this register. The HCD bits are reset to 0 every time auto negotiation is restarted or the BCM5228 is reset. Note that for their intended application, these bits uniquely identify the HCD only after the first Link Pass after reset or restart of auto negotiation. On later Link Fault and subsequent re-negotiations, if the ability of the Link Partner is different, more than one of the above bits may be active.

Restart Auto Negotiation. A self-clearing bit that allows the auto negotiation process to be restarted, regardless of the current status of the state machine. For this bit to work, auto negotiation must be enabled. Writing a 1 to this bit restarts auto negotiation. Because the bit is self-clearing, it always returns a 0 when read. The operation of this bit is identical to bit 9 of the Control Register.

Auto Negotiation Complete. This read-only bit returns a 1 after the auto negotiation process has been completed. It remains 1 until the auto negotiation process is restarted, a Link Fault occurs, or the chip is reset. If auto negotiation is disabled or the process is still in progress, the bit returns a 0.

Acknowledge Complete. This read-only bit returns a 1 after the acknowledgment exchange portion of the auto negotiation process has been completed and the arbitrator state machine has exited the Complete Acknowledge state. It remains this value until the auto negotiation process is restarted, a Link Fault occurs, auto negotiation is disabled, or the BCM5228 is reset.

Broadcom Corporation

Acknowledge Detected. This read-only bit is set to 1 when the arbitrator state machine exits the Acknowledged Detect state. It remains high until the auto negotiation process is restarted, or the BCM5228 is reset.

Ability Detect. This read-only bit returns a 1 when the auto negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the auto negotiation process begins, and exits after the first FLP burst or link pulses are detected from the Link Partner. This bit returns a 00 any time the auto negotiation state machine is not in the Ability Detect state.

Super Isolate. Writing a 1 to this bit places the BCM5228 into the Super Isolate mode. Similar to the Isolate mode, all RMII inputs are ignored, and all RMII outputs are tri-stated. Additionally, all link pulses are suppressed. This allows the BCM5228 to coexist with another PHY on the same adapter card, with only one being activated at any time.

10BASE-T Serial Mode. Writing a 1 to bit 1 of the Auxiliary Mode Register enables the 10BASE-T Serial mode. In the normal 10BASE-T mode of operation, as defined by the RMII standard, transmit and receive data packets traverse the TXD1, TXD0 and RXD1, RXD0 busses at a rate of 50 MHz. In the special 10BASE-T Serial mode, data packets traverse to the MAC layer across only TXD0 and RXD0 at a rate of 10 MHz. Serial operation is not available in 100BASE-X mode.

BROADCOM TEST REGISTER

Table 37:   Broadcom Test (Address 31d, 1Fh)

BIt	Name	R/W	Description	Default
15:8	Reserved	RO	Ignore when read	00h
7	Shadow Register Enable	R/W	1 = Enable shadow registers 1Ah-1Eh 0 = Disable shadow registers	0
6	Reserved	RO	Ignore when read	0
5	Reserved	R/W	Write as 0, ignore when read	0
4:0	Reserved	R/W	Write as 0Bh, ignore when read	0Bh

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
Use default values of reserved bit(s) when writing to reserved bit(s).

Shadow Register Enable. Writing a 1 to bit 7 of register 1Fh allows R/W access to the Shadow Registers located at addresses 1Ah-1Eh.

AUXILIARY MODE 4 (PHY 1) REGISTER (SHADOW REGISTER)

Table 38:   Auxiliary Mode 4 (PHY 1) Register (Shadow Register 26d, 1Ah)

BIt	Name	R/W	Description	Default
15:9	Reserved	R/O	Write as 0, ignore when read	00h
8	MII LED Select Enable	R/W	1 = Enable LED output selection through MII Register	0
7:6	Parallel LED3 Select[1:0]	R/W	Configuration bits for LED3 output. See Section 5 "LED Modes" on page 25 for details	TXER/ LED1[7:6][a]
5:3	Parallel LED2 Select[2:0]	R/W	Configuration bits for LED2 output. See Section 5 "LED Modes" on page 25 for details	TXER/ LED1[5:3]
2:0	Parallel LED1 Select[2:0]	R/W	Configuration bits for LED1 output. See Section 5 "LED Modes" on page 25 for details	TXER/ LED1[2:0]

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII Shadow register bank 1 is accessed by setting MII Register 1Fh bit 7 to a 1.

a. Status of TXER/LED1[7:0] during power-on reset determines the default values for parallel LED3, LED2 and LED1 selects.

MII LED Select Enable. Configuration of LED functions through MII register writes is enabled when this bit is set to a 1. Otherwise power-on reset configurations are in effect.]

Parallel LED3 Select[1:0]. Bit 7 and 6 select LED output for parallel LED3 pin if MII LED select enable is set to a 1.

Parallel LED2 Select[2:0]. Bit 5 and 3 select LED output for parallel LED2 pin if MII LED select enable is set to a 1.

Parallel LED1 Select[2:0]. Bit 2 and 0 select LED output for parallel LED1 pin if MII LED select enable is set to a 1.

AUXILIARY MODE 4 (PHY 2) REGISTER (SHADOW REGISTER)

Table 39:   Auxiliary Mode 4 (PHY 2) Register (Shadow Register 26d, 1Ah)

BIt	Name	R/W	Description	Default
15:9	Reserved	R/O	Write as 0, ignore when read	00h
8:6	Serial Bank 6 Select[2:0]	R/W	Configuration bits for Bank 6 output in Low-Cost Serial LED mode. See Section 5 "LED Modes" on page 25 for details	000
5:3	Serial Bank 5 Select[2:0]	R/W	Configuration bits for Bank 5 output in Low-Cost Serial LED mode. See Section 5 "LED Modes" on page 25 for details	000
2:0	Serial Bank 4 Select[2:0]	R/W	Configuration bits for Bank 4 output in Low-Cost Serial LED mode. See Section 5 "LED Modes" on page 25 for details	000

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII Shadow register bank 1 is accessed by setting MII Register 1Fh bit 7 to a 1.

Serial Bank 6 Select[2:0]. If Low-Cost Serial LED mode is selected, these bits configure Bank 6 LED output on Serial LED data stream SLED_DO.

Serial Bank 5 Select[2:0]. If Low-Cost Serial LED mode is selected, these bits configure Bank 5 LED output on Serial LED data stream SLED_DO.

Serial Bank 4 Select [2:0]. If Low-Cost Serial LED mode is selected, these bits configure Bank 4 LED output on Serial LED data stream SLED_DO.

AUXILIARY MODE 4 (PHY 3) REGISTER (SHADOW REGISTER)

Table 40:   Auxiliary Mode 4 (PHY 3) Register (Shadow Register 26d, 1Ah)

BIt	Name	R/W	Description	Default
15:9	Reserved	R/O	Write as 0, ignore when read	00h
8:6	Serial Bank 3 Select[2:0]	R/W	Configuration bits for bank 3 output in Low-Cost Serial LED mode. See Section 5 "LED Modes" for details	000
5:3	Serial Bank 2 Select[2:0]	R/W	Configuration bits for bank 2 output in Low-Cost Serial LED mode. See Section 5 "LED Modes" for details	000
2:0	Serial Bank 1 Select[2:0]	R/W	Configuration bits for bank 1 output in Low-Cost Serial LED mode. See Section 5 "LED Modes" for details	000

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII Shadow register bank 1 is accessed by setting MII Register 1Fh bit 7 to a 1.

Serial Bank 3 Select[2:0]. If Low-Cost Serial LED mode is selected, these bits configure Bank 6 LED output on serial LED data stream SLED_DO.

Serial Bank 2 Select[2:0]. If Low-Cost Serial LED mode is selected, these bits configure Bank 5 LED output on serial LED data stream SLED_DO.

Serial Bank 1 Select[2:0]. If Low-Cost Serial LED mode is selected, these bits configure Bank 4 LED output on serial LED data stream SLED_DO.

AUXILIARY STATUS 2 REGISTER (SHADOW REGISTER)

Table 41:   Auxiliary Status 2 Register (Shadow Register 27d, 1Bh)

Blt	Name	R/W	Description	Default
15	MLT3 Detected	R/O	1 = MLT3 Detected	0h
14:12	Cable Length 100X[2:0]	R/O	The BCM5228 shows the cable length in 20-meter increments, as shown in Table 42.	000
11:6	ADC Peak Amplitude[5:0]	R/O	A to D peak amplitude seen	00h
5:0	Reserved	R/W	Write as 000000, ignore when Read	00h

R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation. Use default values of reserved bit(s) when writing to reserved bit(s). MII Shadow register bank 1 is accessed by setting MII Register 1Fh bit 7 to a 1.

MLT3 Detected. The BCM5228 returns a 1 in this bit whenever MLT3 signaling is detected.

ADC Peak Amplitude [5:0]. The BCM5228 returns the A to D converter's 6-bit peak amplitude seen during this link.

Cable Length 100X [2:0]. The BCM5228 provides the cable length for each port when a 100TX link is established.

Table 42:   Cable Length

Cable Length 100x [2:0]	Cable Length in Meters
000	< 20
001	20 to <40
010	40 to <60
011	60 to < 80
100	80 to < 100
101	100 to < 120
110	120 to < 140
111	> 140

AUXILIARY STATUS 3 REGISTER (SHADOW REGISTER)

Table 43:   Auxiliary Status 3 Register (Shadow Register 28d, 1Ch)

Blt	Name	R/W	Description	Default
15:8	Noise [7:0]	R/O	Current Mean Square Error value, valid only if link is established	00h
7:4	Reserved	R/W	Write as 0, ignore when read	000h
3:0	FIFO Consumption [3:0]	R/O	Currently utilized number of nibbles in the receive FIFO	0000

MII Shadow Register bank 1 is accessed by setting MII Register 1Fh bit 7 to a 1.

Broadcom Corporation

Noise[7:0]. The BCM5228 provides the current mean squared error value for noise when a valid link is established.

FIFO Consumption[3:0]. The BCM5228 indicates the number of nibbles of FIFO currently used.

AUXILIARY MODE 3 REGISTER (SHADOW REGISTER)

Table 44:   Auxiliary Mode 3 Register (Shadow Register 29d, 1Dh)

BIt	Name	R/W	Description	Default
15:9	Reserved	R/W	Write as 00h, ignore when Read	0
8	Reserved	R/W	Write as 0, ignore when Read	0
7	Reserved	R/W	Write as 0, ignore when Read	0
6	Reserved	R/W	Write as 0, ignore when Read	0
5:4	Reserved	R/W	Write as 00, ignore when Read	0h
3:0	FIFO Size Select [3:0]	R/W	Currently selected receive FIFO Size	4h

> R/W = Read/Write, RO = Read Only, SC = Self Clear, LL = Latched Low, LH = Latched High, LL & LH Clear after read operation.
> Use default values of reserved bit(s) when writing to reserved bit(s). MII Shadow register bank 1 is accessed by setting MII
> Register 1Fh bit 7 to a 1.

FIFO Size Select[3:0]. The BCM5228 indicates the current selection of receive FIFO size using bit 3 through 0, as shown in Table 45. The size can also be determined by bit "Extended FIFO Enable" (Reg. 10h, bit 2) and bit "HSTR FIFO Enable" (Reg. 1Bh, bit 9) for backward compatibility with the 0.35u products.

Table 45:   Current Receive FIFO Size

FIFO Size Select[3:0]	Receive Fifo size in Use (# of bits)
0000	12
0001	16
0010	20
0011	24
0100	28
0101	32
0110	36
0111	40
1000	44
1001	48
1010	52
1011	56
1100	60
1101	64

Broadcom Corporation

AUXILIARY STATUS 4 REGISTER (SHADOW REGISTER)

Table 46:   Auxiliary Status 4 Register (Shadow Register 30d, 1Eh)

BIt	Name	R/W	Description	Default
15:0	Packet Length Counter[15:0]	R/O	Number of bytes in the last received packet	0000h

Packet Length Counter[15:0]. The BCM5228 shows the number bytes in the last packet received. This is valid only when a valid link is established.

Section 7: Timing and AC Characteristics

All RMII Interface pins comply with IEEE 802.3u timing specifications (see § 22, "Reconciliation Sub-layer and Media Independent Interface"). All digital output timing is specified at $C_L = 30$ pF.

Output rise/fall times are measured between 10% and 90% of the output signal swing. Input rise/fall times are measured between V_{IL} maximum and V_{IH} minimum. Output signal transitions are referenced to the midpoint of the output signal swing. Input signal transitions are referenced to the midpoint between V_{IL} maximum and V_{IH} minimum.

Table 47: Clock Timing

Parameter	Symbol	Min	Typ	Max	Unit
REF_CLK Cycle Time (50-MHz Operation)	CK_CYCLE		20		nanoseconds
REF_CLK Cycle Time (125-MHz Operation)	CK_CYCLE		8		nanoseconds
REF_CLK High/Low Time (50-MHz Operation)	CK_HI CK_LO	7	10	13	nanoseconds
REF_CLK High/Low Time (125-MHz Operation)	CK_HI CK_LO		4		nanoseconds
REF_CLK Rise/Fall Time (50-MHz Operation)	CK_EDGE	–	–	2	nanoseconds
REF_CLK Rise/Fall Time (125-MHz Operation)	CK_EDGE	–	–	1	nanoseconds

Table 48: Reset Timing

Parameter	Symbol	Min	Typ	Max	Unit
Reset Pulse Length with Stable REF_CLK Input	RESET_LEN	2	–	–	microseconds
Activity after End of Reset	RESET_WAIT	100	–	–	microseconds
RESET Rise/Fall Time	RESET_EDGE	–	–	10	nanoseconds

Broadcom Corporation
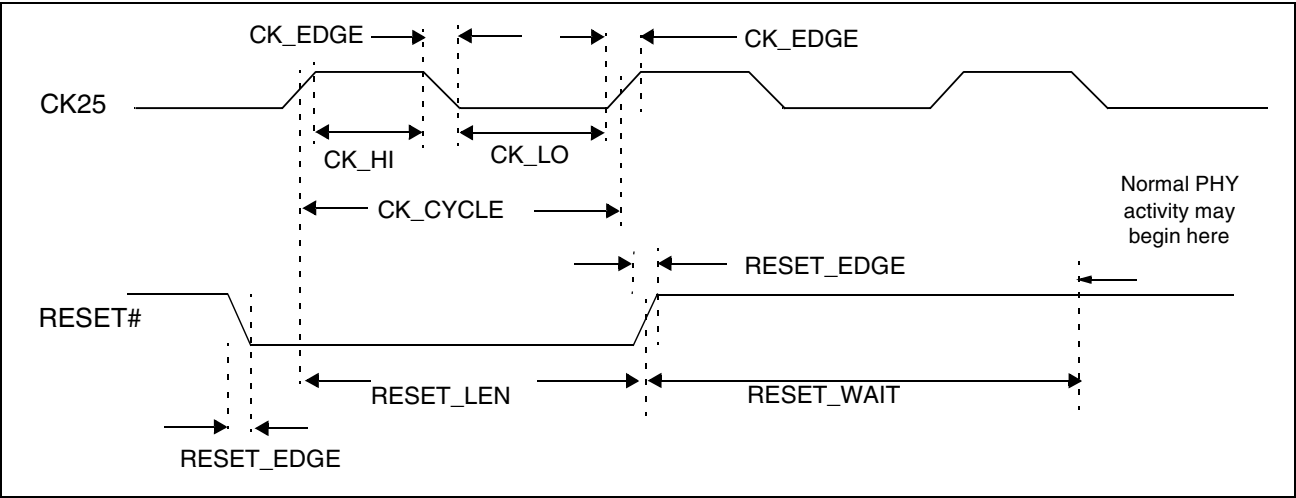
Figure 4: Clock and Reset Timing

Table 49: RMII Transmit Timing

Parameter	Symbol	Min	Typ	Max	Unit
REF_CLK Cycle Time			20		nanoseconds
TXEN, TX_ER, TXD[1:0] Setup Time to REF_CLK Rising	TXEN_SETUP	4			nanoseconds
TXEN, TX_ER, TXD[1:0] Hold Time from REF_CLK Rising	TXEN_HOLD	2			nanoseconds
TD± after TXEN Assert	TXEN_TDATA		89		nanoseconds
TXD to TD± Steady State Delay	TXD_TDATA		95		nanoseconds

TXD[1:0] shall provide valid data for each REF_CLK period while TX_EN is asserted.
As the REF_CLK frequency is 10 times the data rate in 10MB/s mode, the value on TXD[1:0] shall be valid such that TXD[1:0] may be sampled every 10th cycle, regardless of the starting cycle within the group and yield the correct frame data.
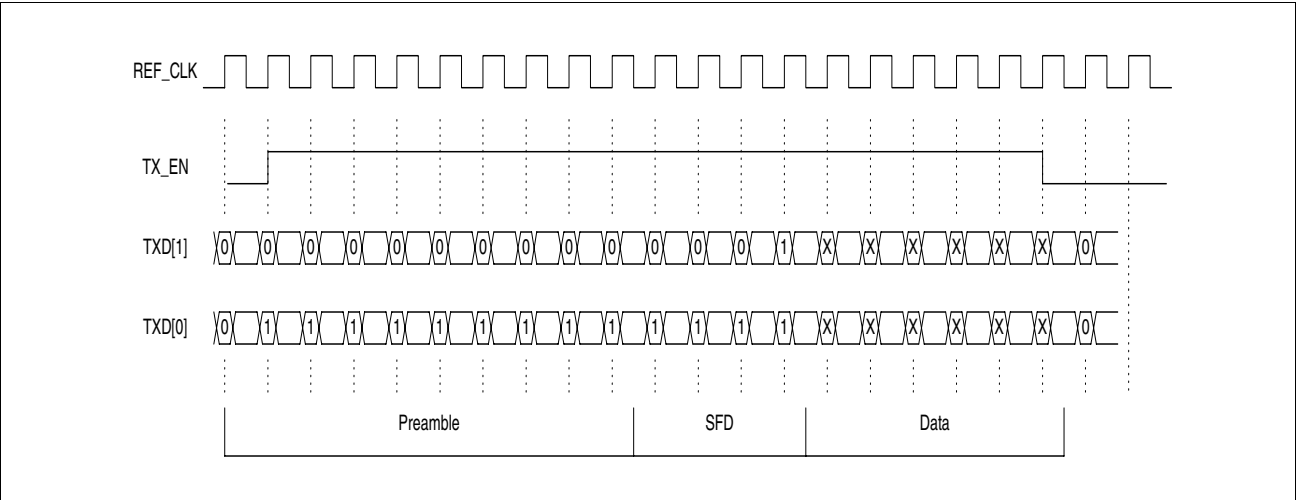

Figure 5: RMII Transmit Packet Timing

Table 50:   RMII Receive Timing

Parameter	Symbol	Min	Typ	Max	Unit
REF_CLK Cycle Time			20		nanoseconds
RXD[1:0], CRS, DV, RX_ER Output Delay from REF_CLK Rising		2		16	nanoseconds
CRS_DV Assert after RD±	RX_CRS_DV		124		nanoseconds
CRS_DV Deassert after RD±	RX_CRS_DV		164		nanoseconds
CRS_DV Deassert after RD±, valid EOP	RX_CRS_DV_EOP		237		nanoseconds

As the REF_CLK frequency is 10 times the data rate in 10Mb/s mode, the value on RXD[1:0] is valid such that RXD[1:0] may be sampled every 10th cycle, regardless of the starting cycle within the group and yield the correct frame data.

The receiver accounts for differences between the local REF_CLK and the recovered clock through use of sufficient elasticity buffering.

The output delay has a load of 25 pf, which accommodates a PCB trace length of over 12 inches.
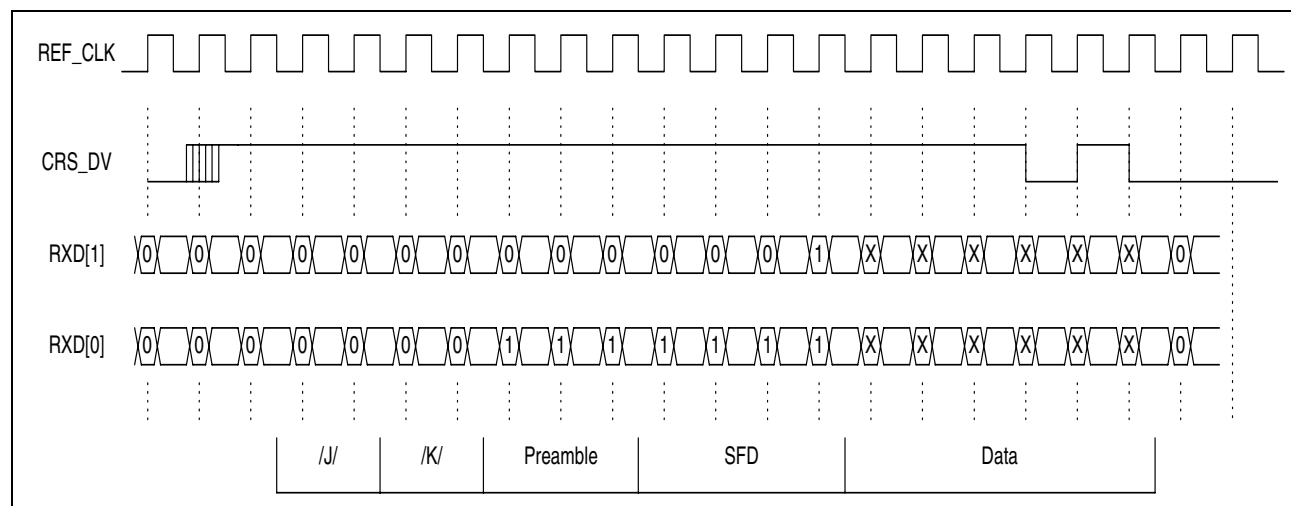
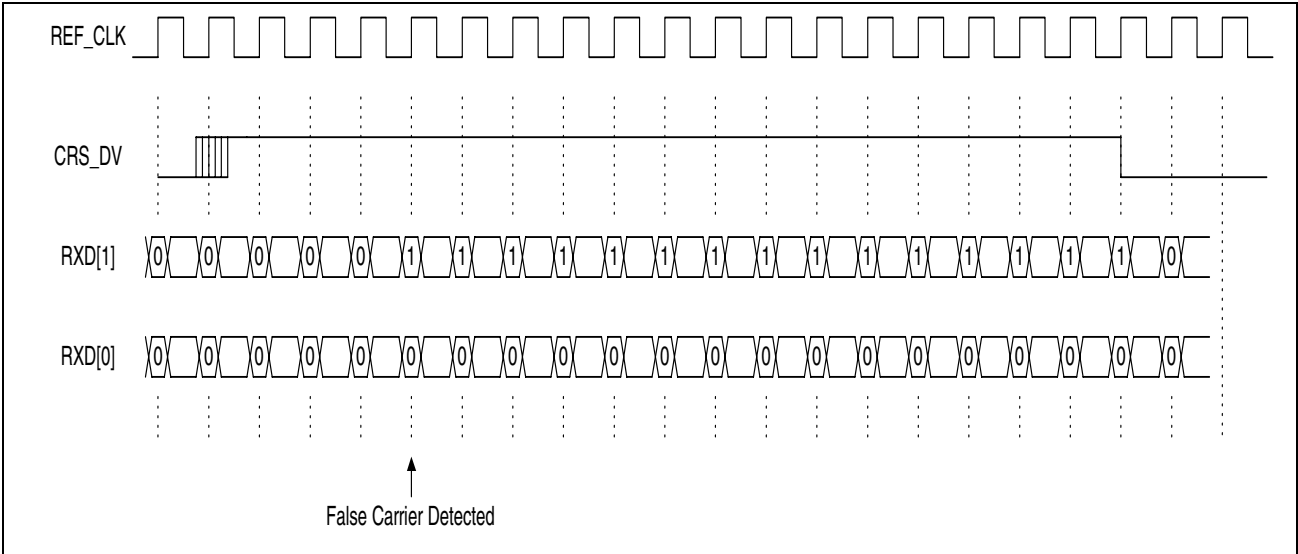**Figure 6:   RMII Receive Packet Timing**

Figure 7: RMII Receive Packet with False Carrier

Table 51: SMII/S3MII Timing

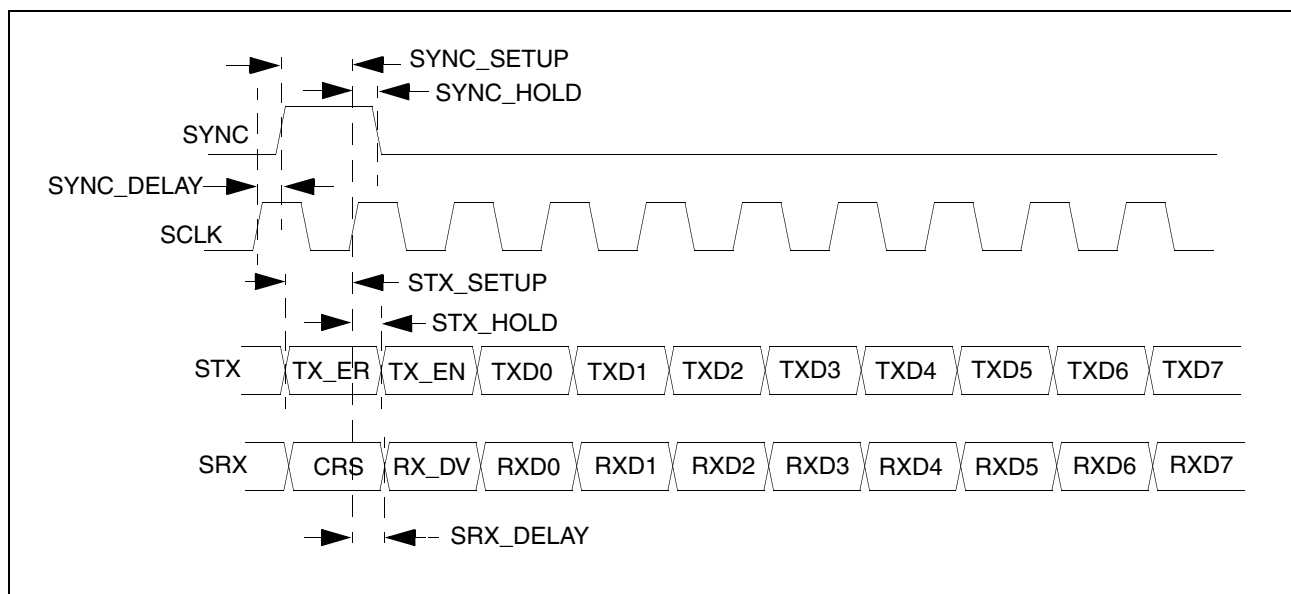| Parameter	Symbol	Min	Typ	Max	Unit
STX (TXD) Setup (SCLK Rising)	STX_SETUP	1.5			nanoseconds
STX (TXD) Hold (SCLK Rising)	STX_HOLD	1.0			nanoseconds
SYNC (SSYNC) Setup (SCLK Rising)	SYNC_SETUP	1.5			nanoseconds
SYNC (SSYNC) Hold (SCLK Rising)	SYNC_HOLD	1.0			nanoseconds
SRX (RXD) Delay (SCLK Rising)	SRX_DELAY	2.0		5.0	nanoseconds
SMII_RSYNC Delay	SYNC_DELAY	2.0		5.0	nanoseconds
SCLK is REF_CLK in SMII mode SCLK is SMII_TXC for S3MII STX SCLK is SMII_RXC for S3MII SRX					

Figure 8:   SMII/S3MII Timing

Table 52:   Auto Negotiation Timing

Parameter	Symbol	Min	Typ	Max	Unit
Link Test Pulse Width			100		nanoseconds
FLP Burst Interval		5.7	16	22.3	milliseconds
Clock Pulse to Clock Pulse		111	123	139	microseconds
Clock Pulse to Data Pulse (Data = 1)		55.5	62.5	69.5	microseconds

Table 53:   LED Timing

Parameter	Symbol	Min	Typ	Max	Unit
LED On Time (ACTLED)			80		milliseconds
LED Off Time (ACTLED)			80		milliseconds

Broadcom Corporation

Table 54:   MII Management Data Interface Timing

Parameter	Symbol	Min	Typ	Max	Unit
MDC Cycle Time		40			nanoseconds
MDC High/Low		20			nanoseconds
MDC Rise/Fall Time				10	nanoseconds
MDIO Input Setup Time to MDC rising		10			nanoseconds
MDIO Input Hold Time from MDC rising		10			nanoseconds
MDIO Output Delay from MDC rising		0		30	nanoseconds
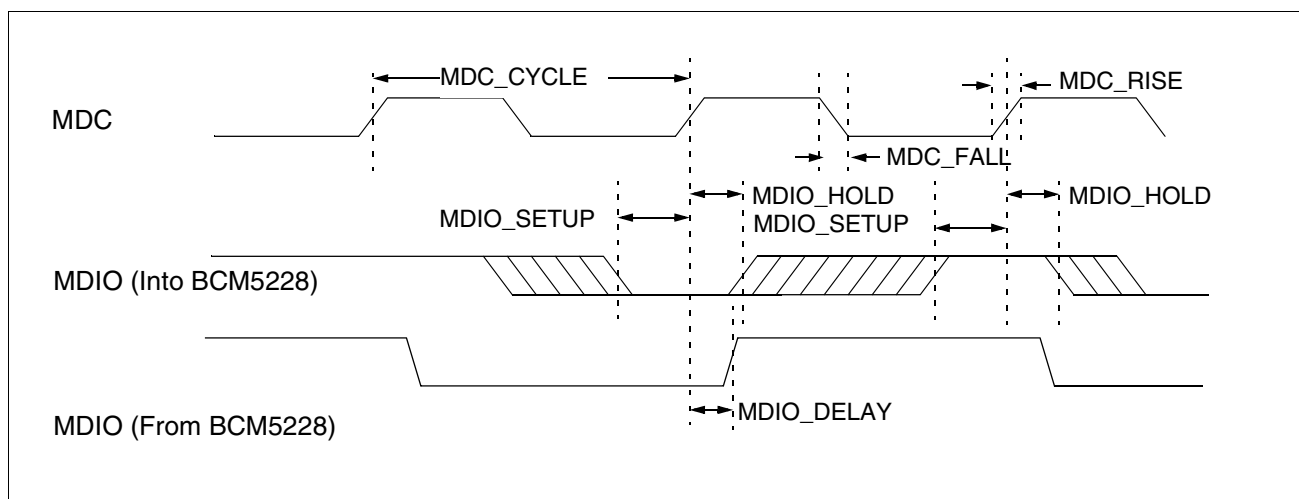
Figure 9:   Management Interface Timing
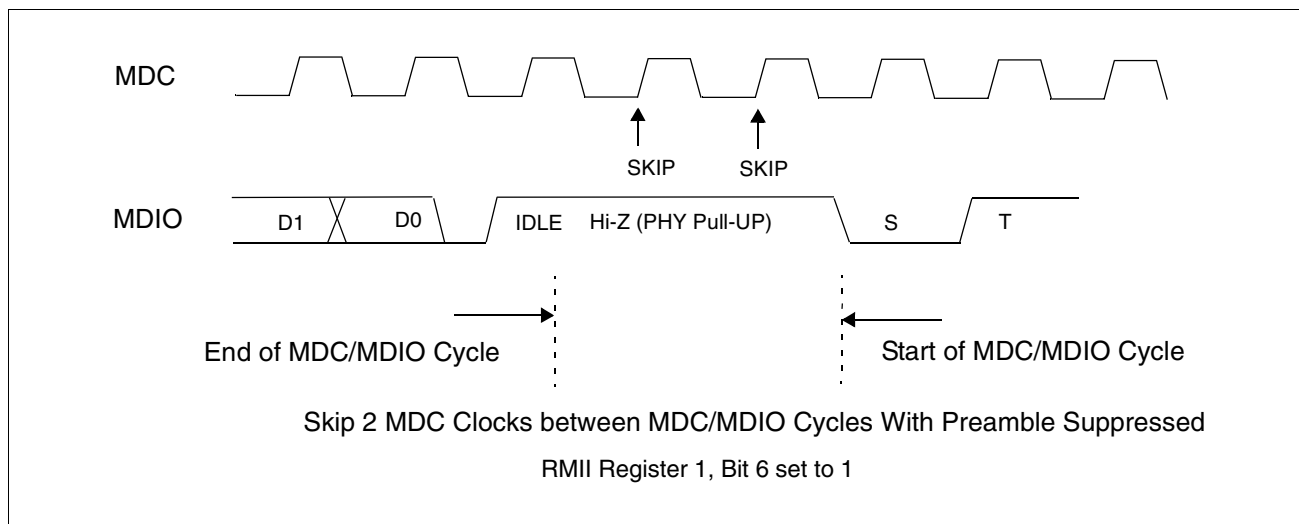
Figure 10:   Management Interface Timing (with Preamble Suppression On)

Section 8: Electrical Characteristics

Table 55: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	Supply Voltage	GND – 0.3	2.75	V
V_I	Input Voltage	GND – 0.3	OVDD + 0.3	V
I_I	Input Current		±10	mA
T_{STG}	Storage Temperature	–40	+125	°C
V_{ESD}	Electrostatic Discharge		1000	V

These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.

Table 56:   Recommended Operating Conditions

Symbol	Parameter	Pins	Operating Mode	Min	Max	Units
V_{DD}	Supply Voltage	OVDD		3.135	3.465	V
V_{DD}	Supply Voltage	AVDD, DVDD, PLLVDDC, BIASVDD		2.375	2.625	V
V_{IH}	High-Level Input Voltage	All digital inputs		2.0		V
V_{IL}	Low-Level Input Voltage	All digital inputs			0.8	V
		SD± {1:8}	100BASE-FX		0.4	V
V_{IDIFF}	Differential Input Voltage	SD± {1:8}	100BASE-FX	150		mV
V_{ICM}	Common Mode Input Voltage	RD± {1:8}	100BASE-TX	1.85	2.05	V
		RD± {1:8}, SD± {1:8}	100BASE-FX	1.60	1.80	V
T_A	Ambient Operating Temperature			0	70	°C

Table 57: Electrical Characteristics

Symbol	Parameter	Pins	Conditions	Min	Typ	Max	Units
I_{DD}	Total Supply Current	AVDD, DVDD	100BASE-TX		839	892	mA
		OVDD	100BASE-TX		59	76	mA
V_{OH}	High-Level Output Voltage	Digital outputs	$I_{OH} = -12$ mA, OVDD = 3.3 V	OVDD − 0.5			V
		Digital outputs	$I_{OH} = -12$ mA, OVDD = 2.5 V	OVDD − 0.4			V
		TD± {1:8}	Driving loaded magnetics module			VDD + 1.5	V
V_{OL}	Low-Level Output Voltage	All digital outputs	$I_{OL} = 8$ mA			0.4	V
		TD± {1:8}	Driving loaded magnetics module	DVDD − 1.5			V
V_{ODIFF}	Differential Output Voltage	TD± {1:8}	100BASE-FX mode	400			mV
I_I	Input Current	Digital inputs w/ pull-up resistors	V_I = OVDD			+100	µA
			V_I = DGND			-200	µA
		Digital inputs w/ pull-down resistors	V_I = OVDD			+200	µA
			V_I = DGND			-100	µA
		All other digital inputs	DGND $\leq V_I \leq$ OVDD			±100	µA
I_{OZ}	High-Impedance Output Current	All three-state outputs	DGND $\leq V_O \leq$ OVDD				µA
		All open-drain outputs	V_O = OVDD				µA
V_{bias}	Bias Voltage	VREF, RDAC		1.18		1.30	V

Section 9: Mechanical Information

Symbol	Millimeter		
	Min	Nom	Max
A	—	—	4.10
A1	0.25	0.37	0.50
A2	3.39	3.49	3.59
D	30.35	30.60	30.85
D1	27.90	28.00	28.10
E	30.35	30.60	30.85
E1	27.90	28.00	28.10
L	0.30	0.60	0.75
b	0.15	0.22	0.30
h	0.13		0.23
e	0.50 BSC		
c	—	0.08	0.102
r_1	—	0.20	—
r_2	—	0.30	—
θ_1	0°	—	7°
θ_2	2°	6°	10°
θ_3	—	10°	—
θ_4	—	10°	—

208-pin detail

Notes:

1. Drawings on this page are not to scale
2. All dimensions are in millimeters except where noted
3. Foot length "L" is measured at gage plane, 0.25mm above the seating plane
4. Seating plane is defined by three lowest lead tips

Figure 11:   208-Pin PQFP

Broadcom Corporation

Figure 12:   256 Fine Pitch BGA (FPBGA) Package

TOP VIEW

SIDE VIEW

BOTTOM VIEW
(256 SOLDER BALLS)

A1 BALL PAD CORNER

Ø0.50 TYP

SEATING PLANE

6   PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY
THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5   DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER,
PARALLEL TO PRIMARY DATUM Z.

4.   THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 256.

3.   THE MAXIMUM SOLDER BALL MATRIX SIZE IS 16 X 16.

2.   THE BASIC SOLDER BALL GRID PITCH IS 1.00.

1.   ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

Broadcom Corporation

Section 10: Packaging Thermal Characteristics

Table 58: Theta—J_A vs. Airflow for the BCM5228B (256 FPBGA) Package

Airflow (feet per minute)	0	100	200	400	600
Theta—J_A(°C/W)	19.02	16.70	15.85	14.84	14.16

Theta—J_C for this package in still air is 5.84 °C/W. The BCM5228B is designed and rated for a maximum junction temperature of 125 °C.

Table 59: Theta—J_A vs. Airflow for the BCM5228F (208 PQFP) Package

Airflow (feet per minute)	0	100	200	400	600
Theta—J_A(°C/W)	16.35	13.96	13.09	12.21	11.70

Theta—J_C for this package in still air is 6.19 °C/W. The BCM5228F is designed and rated for a maximum junction temperature of 125 °C.

Table 60: Theta—J_A vs. Airflow for the BCM5228U (208 PQFP) Package

Airflow (feet per minute)	0	100	200	400	600
Theta—J_A(°C/W)	16.35	13.96	13.09	12.21	11.70

Theta—J_C for this package in still air is 6.19 °C/W. The BCM5228U is designed and rated for a maximum junction temperature of 125 °C.
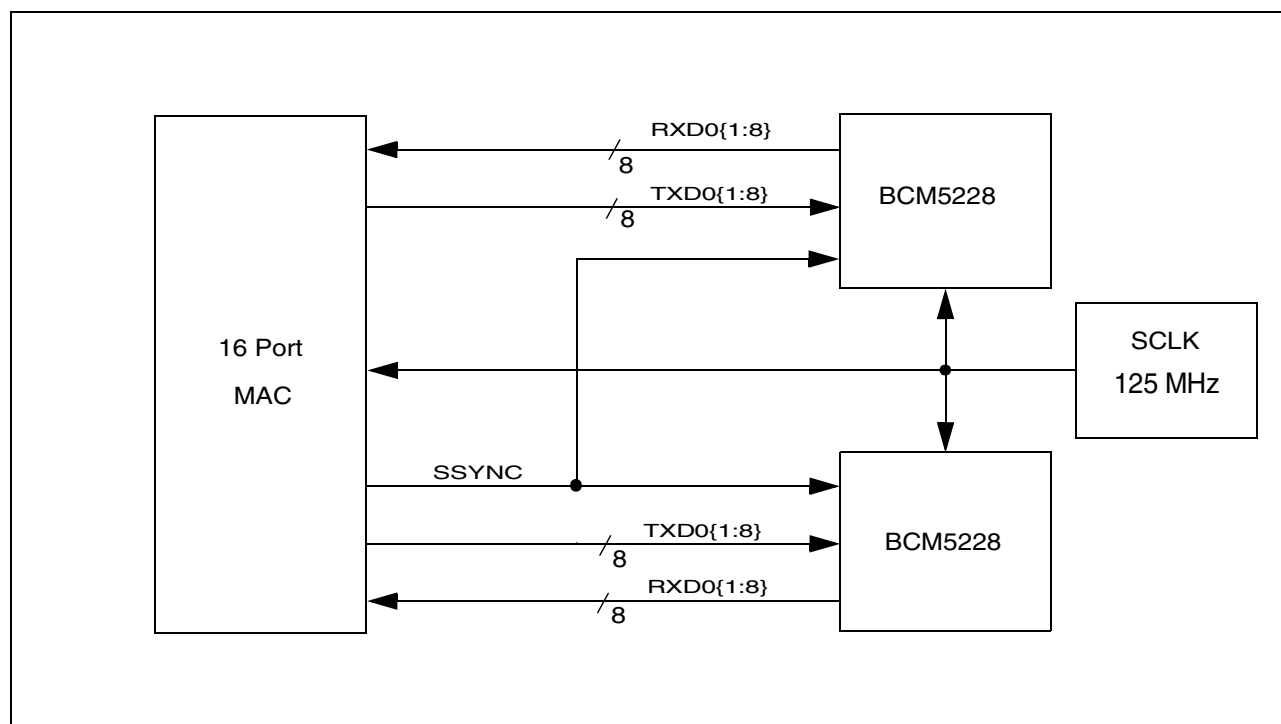
Section 11: Application Examples

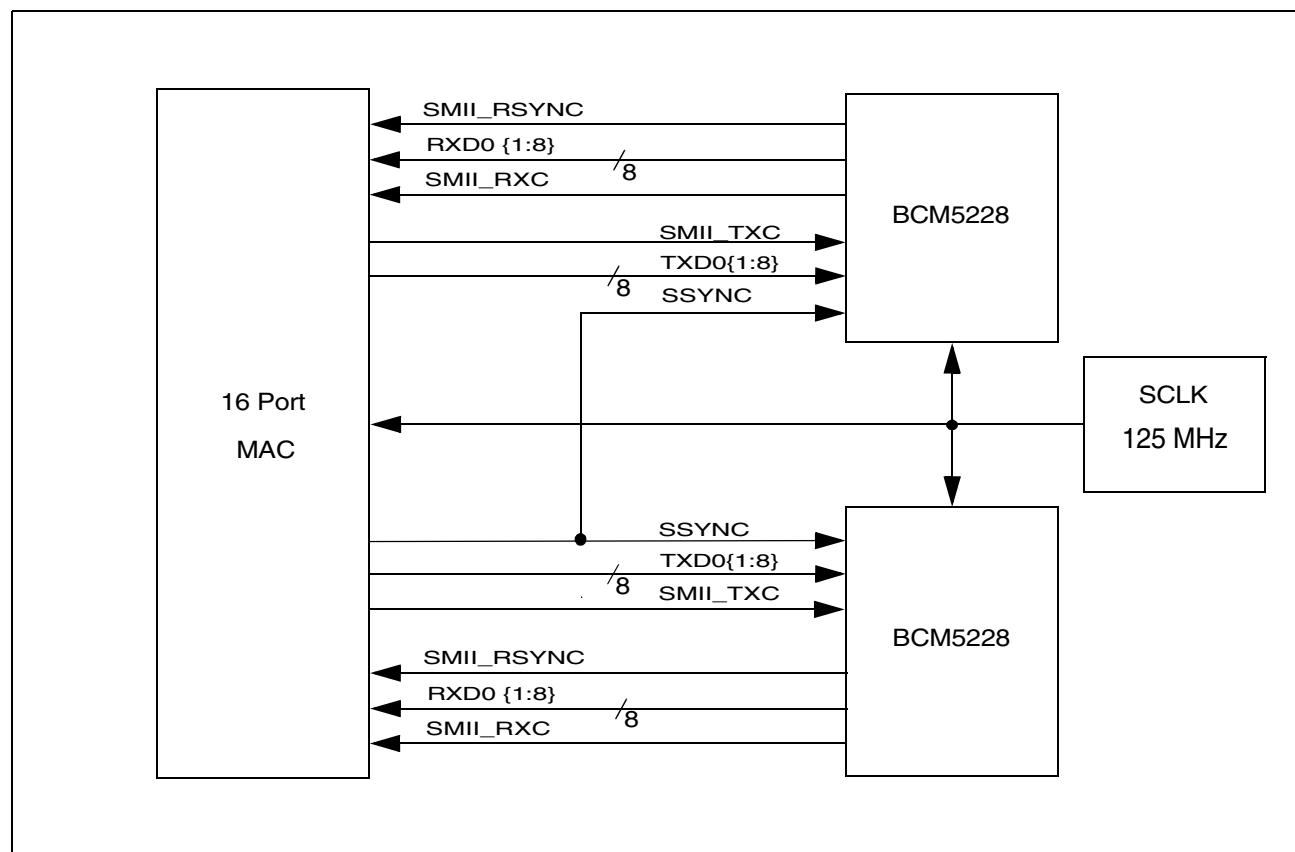
Figure 13:   SMII Application

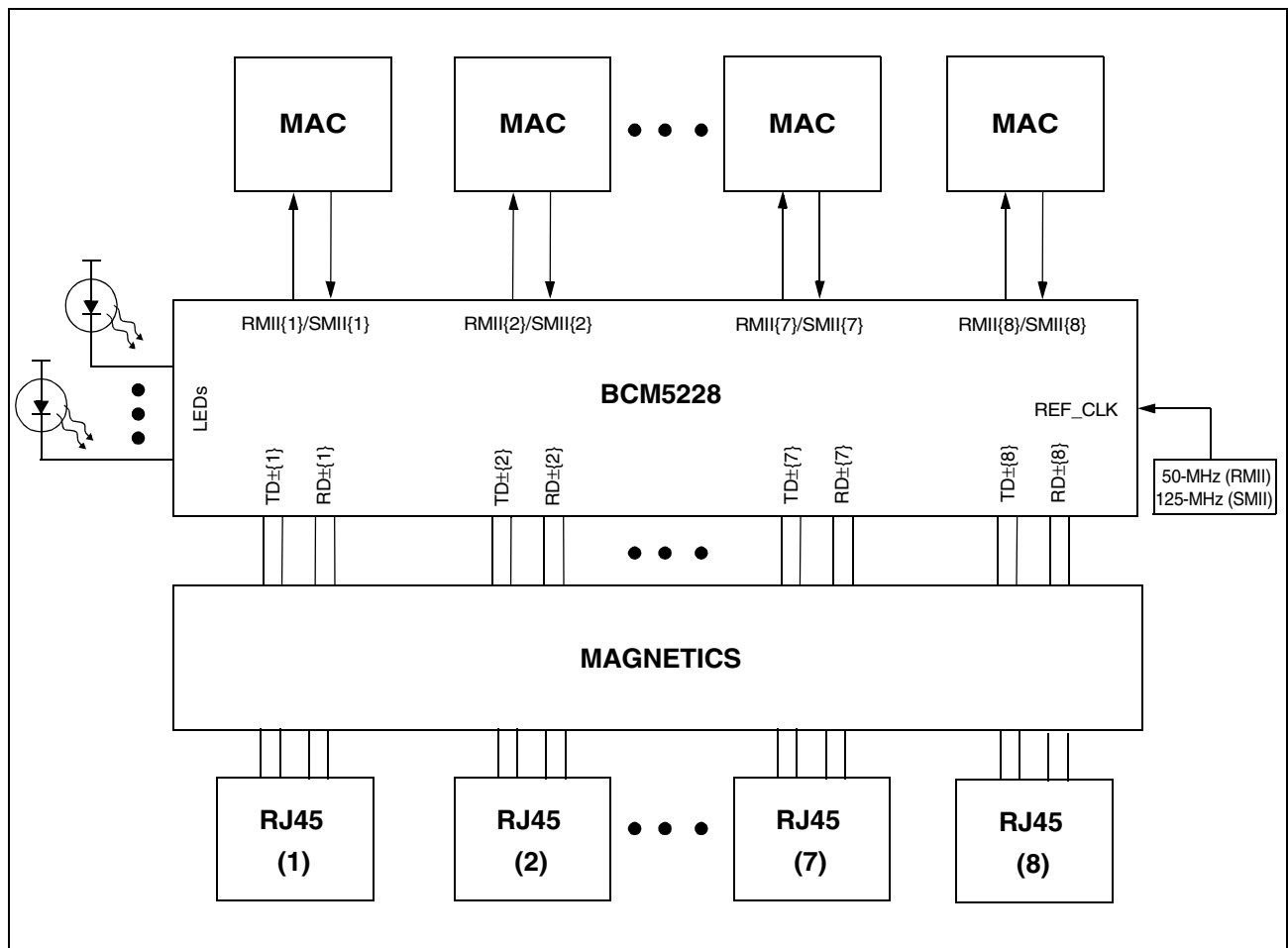**Figure 14:   SMII Application using Source Synchronous Signals**

Figure 15:   Switch Application

Broadcom Corporation

Section 12: Ordering Information

Part Number	Package	Ambient Temperature
BCM5228UA4KPF	208 PQFP	0° C to 70° C (32° F to 158° F)
BCM5228FA4KPF	208 PQFP	0° C to 70° C (32° F to 158° F)
BCM5228BA4KPB	256 FBGA	0° C to 70° C (32° F to 158° F)
BCM5228UA4IPF	208 PQFP	−40° C to 85° C (−40° F to 185° F)
BCM5228FA4IPF	208 PQFP	−40° C to 85° C (−40° F to 185° F)
BCM5228BA4IPB	256 FPBGA	−40° C to 85° C (−40° F to 185° F)
Note: A4 is the current revision number at the time of publication of this data sheet.		

Broadcom Corporation