Frequency Foldback Current Mode PWM Controller

FEATURES

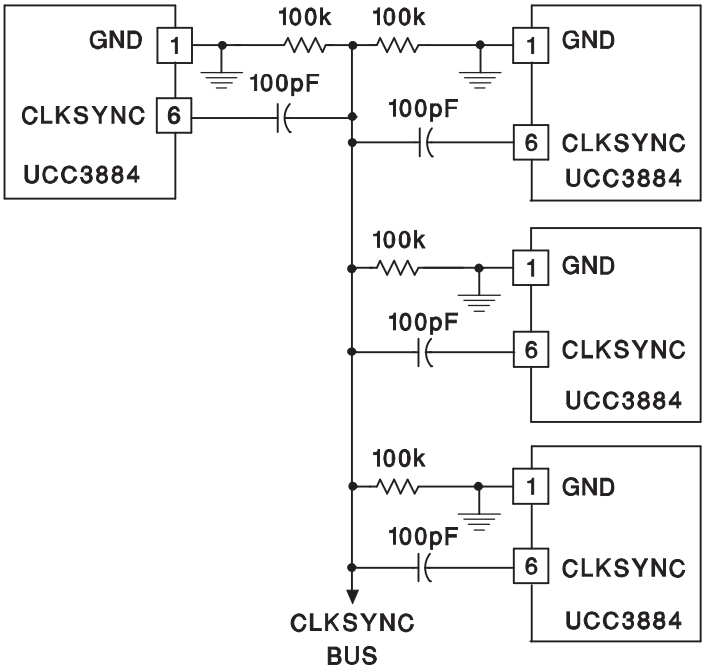
- **Frequency Foldback Reduces Operating Frequency Under Fault Conditions**
- **Accurate Programmable Volt-Second Clamp**
- **Programmable Maximum Duty Cycle Clamp**
- **Oscillator Synchronization**
- **Overcurrent Protection**
- **Shutdown With Full Soft Start**
- **Wide Gain Bandwidth Amplifier (GBW > 2.5 MHz)**
- **Current Mode Operation**
- **Precision 5-V Reference**

DESCRIPTION

The UCC3884 is a high performance current mode PWM controller intended for single ended switch mode power supplies. The chip implements a frequency foldback scheme that decreases the oscillator frequency as the output voltage falls below a programmed value. This technique decreases the average output current sourced into a low impedance load which can occur during an output short circuit or overload condition. Excessive short circuit current is more prevalent in high frequency converters where the propagation delay and switch turn-off time forces a minimum attainable duty cycle. An accurate volt-second clamp limits the duty cycle during line or load transient conditions which could otherwise saturate the transformer. The volt-second clamp may also be used with an external overvoltage protection circuit to handle fault conditions such as current sense disconnect or current transformer saturation.

The frequency foldback, volt-second clamp, cycle-by-cycle current limit, and overcurrent shutdown provide a rich set of protection features for use in peak current-mode pulse width modulators.

OSCILLATOR SYNCHRONIZATION



ABSOLUTE MAXIMUM RATINGS(1)

	VALUE	UNIT
Supply voltage	15	V
Output sink current	1	A
Output source current	0.5	
All other pins	6	V
Storage temperature	–65 TO 150	°C
Junction temperature	–40 TO 150	
Lead temperature (soldering, 10 sec)	300	

(1) Currents are positive into, negative out of the specified terminal.

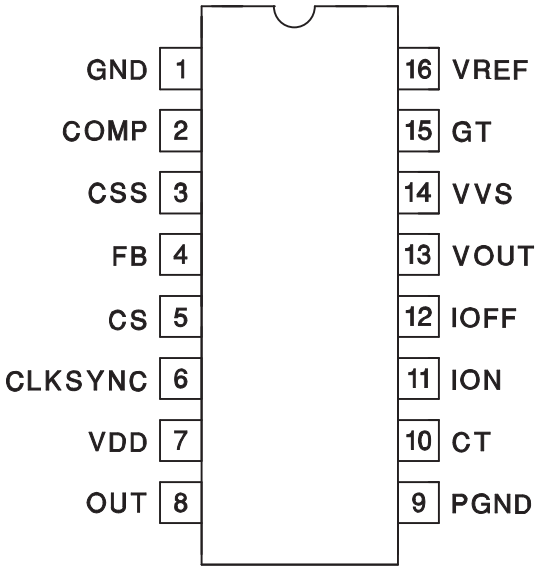
ORDERING INFORMATION

T_J	PACKAGED DEVICES(1)	
	SOP (D)	PDIP(N)
-40°C to 85°C	UCC2884D (16)	UCC2884N (16)
0°C to 70°C	UCC3884D (16)	UCC3884N (16)

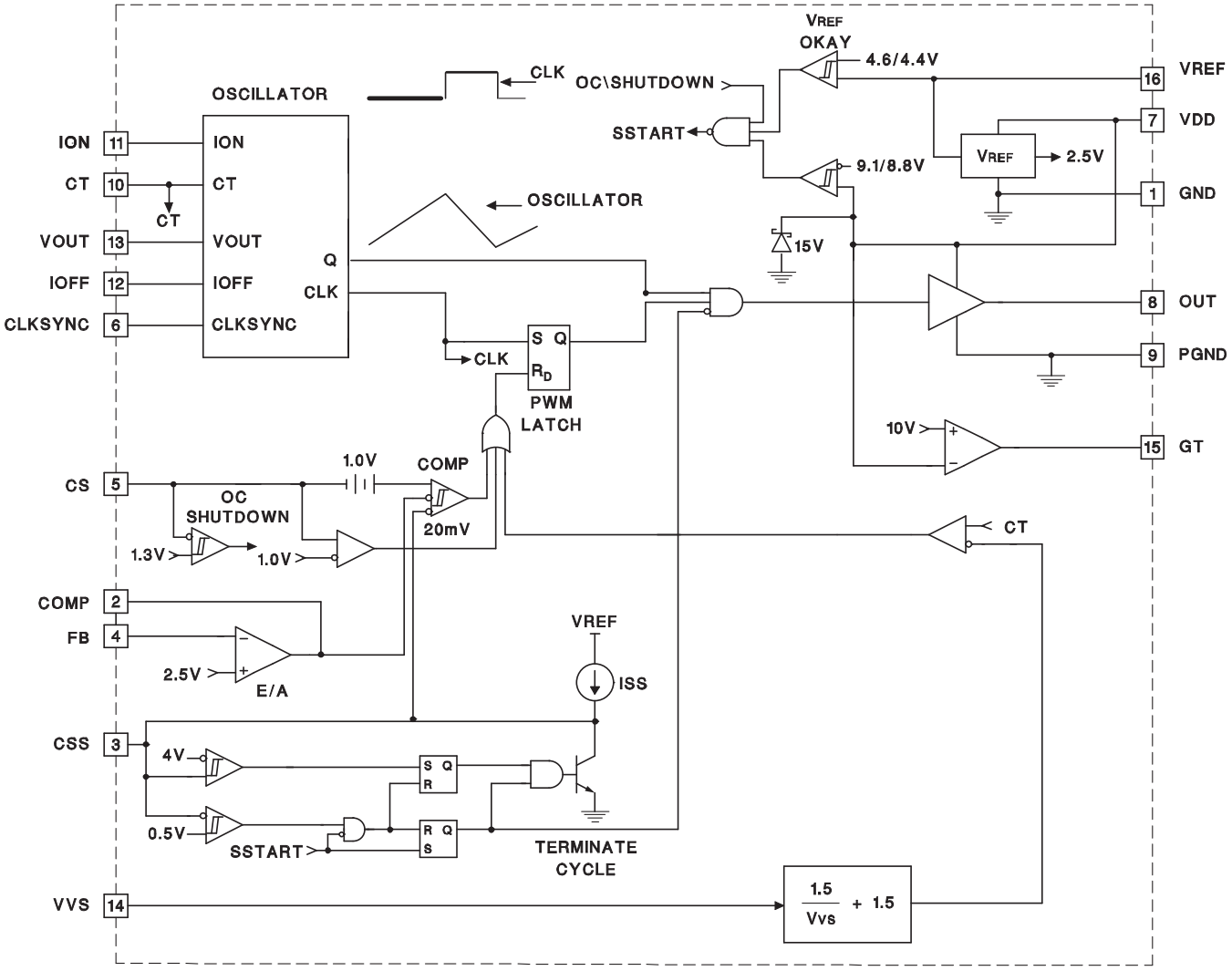
(1) Both the D and N packages are available taped and reeled (indicated by the TR suffix on the device type e.g., UCC2884DTR)

CONNECTION DIAGRAMS

N or D Package (Top View)



Block Diagram



ELECTRICAL CHARACTERISTICS

Unless otherwise specified, these specifications apply for T_A = -40°C to 85°C for the UCC2884, and 0°C to 70°C for the UCC3884, CT = 220 pF, R_{ON} = 53 kΩ, R_{OFF} = 38 kΩ, VOUT = VREF, VVS = 0 V, CSS = 2.5 nF, VDD = 11 V, Output no load, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
5-V Reference					
VREF	I_{REF} = 0 mA	4.86	5	5.14	V
Line regulation	VDD = 10 V to 12 V		1	10	mV
Load regulation	0 < I_{REF} < 5 mA		1	20	
Short circuit	VREF = 0 V		15	45	mA
Oscillator					
Accuracy	$V_{OUT} = V_{REF}$	360	400	440	kHz
Foldback frequency	VOUT = 0.75 V	200	230	260	
CLKSYNC output high		4.8	5	5.2	V
CLKSYNC output low			0.0	0.4	
CLKSYNC sink current	CLKSYNC = 1 V	1.2	2.2		mA
CLKSYNC source current	CLKSYNC = 3 V		–0.2	0.1	
CLKSYNC input threshold	CLKSYNC from 5 V to 0 V (edge detect)	2.5	3.0	3.5	V
Error Amplifier					
I_B	Total bias current; regulating level	–1		1	µA
FB voltage	FB = COMP	2.43	2.5	2.57	V
A_{VO}		50	90		dB
GBW	F = 100 kHz (1)	2.5	5		MHz
Output source current	FB = 2.3 V, COMP = 2.5 V	–0.6	–1.2		mA
Output sink current	FB = 2.7 V, V_{COMP} = 1 V	0.250	1.5		
V_{OL}	I_O = 100 µA		0.3	0.9	V
V_{OL}	I_O = –100 µA	2.7	3.1	3.5	
PWM					
Minimum duty cycle	FB = 3 V, CS = 0 V			0%	
Maximum duty cycle	FB = 0 V, CS = 0 V	75%	78%	81%	
Current Sense					
Input bias current (CS)				3.0	µA
CS shutdown threshold		1.235	1.3	1.365	V
CS shutdown hysteresis			20		mV
CS over current threshold		0.95	1	1.05	V
Current/FAULT					
Soft start charge current		–10	–20	–30	µA
Soft start discharge current		10	20	30	
V_{OL}			0	50	mV
Soft start complete threshold		3.6	4	4.4	V
Soft start restart threshold		0.4	0.5	0.6	

(1) Specified by design. Not 100% tested in production.

ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Volt Second Clamp					
Duty cycle	VVS = 1.4 V, T_A = 40°C to 85°C	50%	60%	70%	
	VVS = 1.4 V, T_A = 0°C to 70°C	52%	57%	67%	
	VVS = 3.6 V, T_A = –40°C to 85°C	20.5%	22.0%	25.5%	
	VVS = 3.6 V, T_A = 0°C to 70°C	20.5%	22.0%	23.5%	
I_B	VVS = 3.7 V	–1		1	µA
Output Stage					
Output low saturation	I_{OUT} = 100 mA		0.5	0.9	V
Output low saturation	I_{OUT} = –50 mA		0.5	0.9	
	I_{OUT} = 200 mA (2)			1.9	
UVLO output low saturation	I_{OUT} = 20 mA, VDD = 0 V		0.7	1.2	
Rise time	C_L = 1 nF		50	70	ns
Fall time	C_L = 1 nF		30	50	
Undervoltage Lockout					
Turn-on threshold voltage		8.4	8.9	9.4	V
Hysteresis		200	600	1000	mV
Startup Regulator					
Regulated VDD voltage		9.5	10	10.5	V
VDD override threshold				10.7	
Overall					
V_{DD} range				14.5	V
I_{DD} (run)	f = 400 kHz	2	5	10	mA
I_{DD} startup current	VDD = 5.4 V	100		250	µA
VDD clamp	IDD = 10 mA	12	13.5	15	V

(2) Specified by design. Not 100% tested in production.

PIN DESCRIPTIONS

CLKSYNC: An edge triggered active low TTL signal to this pin synchronizes the oscillator to an external clock. When VOUT decreases below 3.0 V, the frequency foldback circuit is activated and the controller becomes unsynchronized. When VOUT exceeds 3.0 V, the controller resynchronizes to the external clock.

COMP: The output of the voltage error amplifier used for compensation. The output is clamped to 3.0 V minimum.

CS: Current sense input. This pin accepts a voltage proportional to converter inductor current. The voltage CS is compared to the output of the compensated error amplifier to control the on-time of the switch. Voltage mode control can be realized by driving this pin with fixed sawtooth ramp. Voltage feedforward is achieved by making the peak of this ramp proportional to the input voltage.

CSS: A capacitor, CSS, to ground programs the soft-start time for the power-up sequence. This function is also used when an overcurrent fault occurs. As CSS is charged, the PWM comparator uses the lowest of either the voltage at CSS or the error amplifier output voltage to determine the duty cycle. The duty cycle, therefore, slowly increases during the soft-start cycle. The faults that cause CSS to discharge and shutdown the controller are the logical OR of VREF below 4.4 V or VDD below 8.8 V. If a fault is still present when CSS is discharged below 0.5 V, the supply remains off until the fault is cleared. The soft-start time is determined by:

$$t_{SS} = 3.5 \times \frac{C_{SS}}{I_{SS}}$$

where I_{SS} is 20 μA. A current limit terminates the present cycle. It does not generate a soft start cycle.

CT: A capacitor, C_T to ground, is charged and discharged creating the oscillator waveform. This waveform varies between 1.5 V and 3.5 V. The operating frequency is determined by:

$$f = \frac{4.4}{CT \times \left(\frac{R_{ON}}{1.5} + \frac{R_{OFF}}{3.5} \right)}$$

The ratio of the time duration of the positive sloped portion of the CT voltage waveform to the period gives the maximum duty cycle.

FB: The inverting input of the voltage amplifier used to sense the output voltage. The non-inverting input of the error amplifier is internally connected to 2.5 V.

GND: The ground pin internally used for all the amplifiers and as the return for all resistor and capacitor connections to the UCC3884.

GT: Used to drive an external depletion-mode MOSFET for the housekeeping power supply. The MOSFET is turned off when the bootstrap winding voltage exceeds 10 V. There is 300 mV of hysteresis around the 10-V, turn-off voltage to prevent oscillation. See Typical Application.

IOFF: A resistor, R_{OFF}, to ground, programs the discharge current of the timing capacitor C_T. This is a variable discharge current which determines the negative slope of the oscillator voltage waveform at CT. The discharge time is dependent on the voltage at the VOUT pin. The discharge current is given by:

$$I_{OFF} = \frac{VOUT}{R_{OFF}}$$

The VOUT pin is internally clamped to 3.5 V maximum.

ION: A resistor, R_{ON}, to ground programs the charge current of the timing capacitor, C_T, which generates the positive slope of the oscillator waveform. The charge time is constant and corresponds to the maximum output on-time at OUT. The charge current equation is:

$$I_{ON} = \frac{1.5V}{R_{ON}}$$

When required the linear positive slope of the C_T voltage could be buffered and used to provide slope compensation into the CS pin.

OUT: The output of the controller. The peak source current is 0.5 A and the peak sink current is 1.0 A. The faults listed under the CSS description turn off this output.

PGND: The power ground pin is used as the return for the output transistor drive stage.

VDD: The input voltage of the chip. A low ESR and ESL ceramic capacitor from this pin to GND should be used to bypass internal switching transients.

VOUT: This pin accomplishes frequency foldback by controlling the discharge current for the oscillator CT capacitor. A dc voltage proportional to the output voltage is connected to this pin. To startup with zero output voltage the user should tie a resistor between VREF and VOUT. The value depends on the lowest desired operating frequency. When VOUT decreases below 3.5 V the frequency decreases by reducing the discharge current I_{OFF}. When VOUT increases, the frequency increases by increasing the discharge current. The maximum operating frequency occurs when VOUT = 3.5 V. The C_T charge time is constant to assure a maximum output duty cycle. This pin must be above 3.0 V to allow synchronization to occur.

VREF: This pin is the output of the 5-V regulated reference. Bypass this pin with a low ESR and ESL ceramic capacitor (e.g., 0.47 μF).

VVS: Provides a programmable duty cycle clamp which is dependent upon the input voltage. A resistor divider network reduces the input voltage supplied to VVS. The device determines the reciprocal of the voltage at VVS and scales the result. The voltage is then compared to the oscillator waveform to clamp the duty cycle. The purpose of this clamp is to reduce the likelihood of saturating the isolation transformer during unusual line or load conditions.

APPLICATION INFORMATION

Theory of Operation

The UCC3884 current-mode PWM controller contains a programmable oscillator which includes the ability to synchronize multiple PWMs. The positive and negative sloped portions of the oscillator waveform (measured at CT), have time intervals that are set by external resistors at ION and IOFF. The operating frequency is inversely proportional to the timing capacitor. The negative sloped portion of the oscillator waveform is extended in time as the measured output voltage decreases providing protection during output faults. The power supply output voltage and the voltage from VREF are fed back to VOUT. When the output voltage decreases, the voltage at VOUT also decreases. As VOUT decreases below 3.5 V, the operating frequency decreases. This reduction in frequency allows the duty cycle to decrease below what the CS to OUT delay would otherwise permit. This is referred to as frequency foldback. An output short circuit or overload causes the converter to enter the frequency foldback mode. Synchronization to other controllers can only occur during normal operation, that is, when VOUT is greater than 3.0 V.

GT is provided to turn off an external depletion-mode MOSFET after startup when the bootstrap winding exceeds 10 V. This depletion-mode MOSFET is used in the housekeeping section of the converter to simplify startup biasing circuitry. The amplifier that drives this MOSFET has 300 mV of hysteresis to avoid oscillation during power up.

An accurate programmable volt-second technique clamps the duty cycle. The duty cycle limit is inversely proportional to input voltage and a resistor divider network is used to program the proportionality constant. At a given input voltage and constant load, under closed loop control, the operating duty cycle is a fixed value. The volt-second clamp duty cycle may then be set somewhat higher than this operating duty cycle. For other input voltages, the volt-second clamp still exceeds the steady state operating duty cycle. This allows normal closed loop operation of the converter. It is during a load transient (a fault such as a momentary short circuit) as the error amplifier increases the duty cycle, that when the volt-second clamp accurately limits the maximum volt-seconds. This ensures that the transformer does not saturate during a fault which can fail the power supply. After the fault is removed the converter resumes closed loop control.

CSS is provided which allows the UCC3884 to be disabled with an external transistor. The increasing pulse width at OUT during soft start should be programmed to be less than the pulse width of the duty cycle limit that the frequency foldback circuitry creates. The frequency foldback circuit will be in effect during soft start since the output voltage fed back to VOUT is less than 3.5 V. Designing the circuit in this fashion allows a proper startup sequence.

The current sense feedback pin has an overcurrent protection feature which forces a soft start cycle only if the device is not currently in a soft-start cycle. A 1-V bias at the PWM comparator's non-inverting input and a reset dominant PWM latch permit zero duty cycle operation.

The error amplifier has a wide gain-bandwidth product and its non-inverting input is internally set to 2.5 VDC.

Oscillator

The oscillator has charge and discharge currents programmed with resistors to ground from ION and IOFF respectively, as seen on the Oscillator Block Diagram.(Figure 1). This generates a linear sawtooth waveform on CT. Frequency foldback is accomplished by the level shifted output voltage controlling the VOUT voltage which decreases the discharge current and the frequency.

Synchronization is accomplished by coupling the fastest oscillator CLKSYNC signal as shown on the Oscillator Synchronization Diagram (Figure 2). The fastest (master) CLKSYNC pin couples a negative pulse into the slower (slave) CLKSYNC pins forcing the slaves' CT pins to quickly discharge as shown on the Oscillator Waveform diagram (Figure 3).

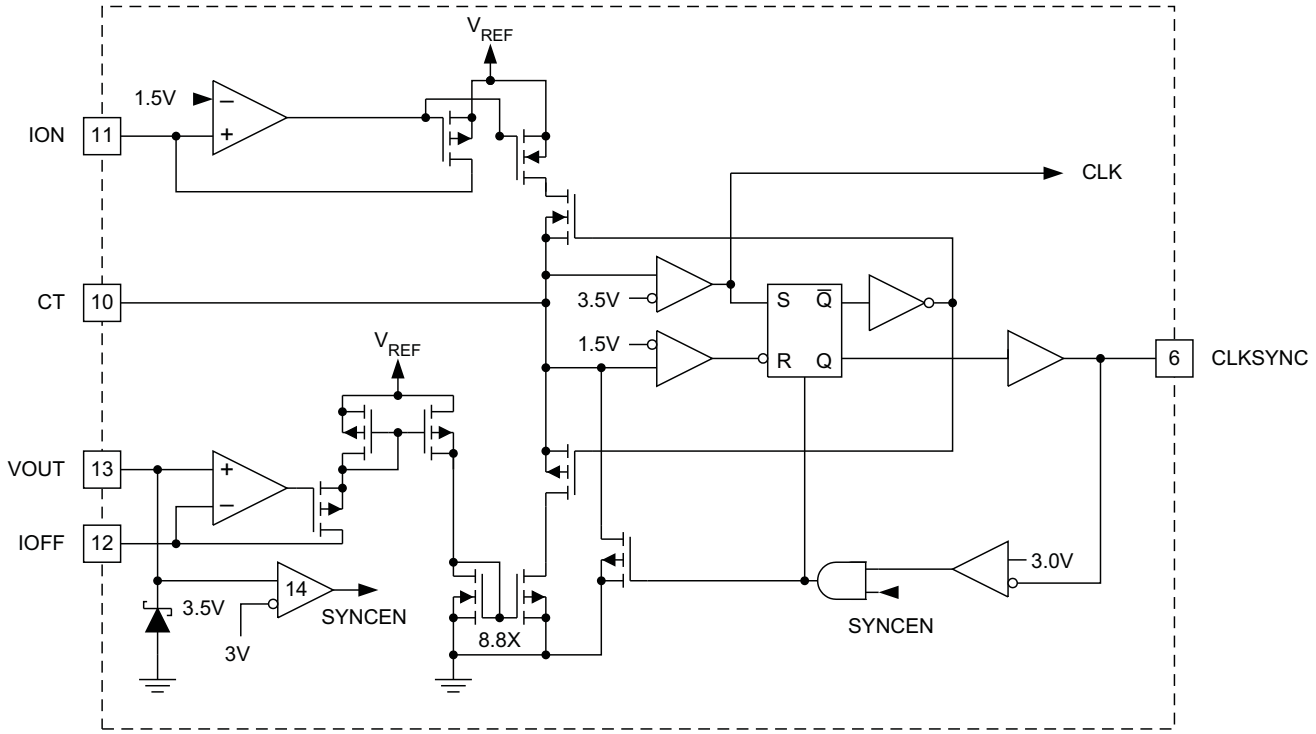

Figure 1. UCC3884 Oscillator

Synchronization Techniques

The following explains two synchronization techniques:

1. **Initially Undefined Master** If the user does not care which unit is the master, then the oscillator frequencies are designed as accurate as necessary and one unit becomes the master and synchronize the remaining units. The user never knows exactly which unit will be the master upon power up.
2. **User-Defined Master** If the user does care which unit is the master, a unit should be identified as the master, and the frequency and maximum duty cycle clamp should be programmed accordingly. The ROFF resistor which programs the slave units oscillator discharge ramp should be between 50% and 100% of the ROFF resistor which programs the master. This ensures that if a slave unit tries to synchronize the master, the master frequency will still be faster than the slave frequency and the master synchronizes all the remaining units.

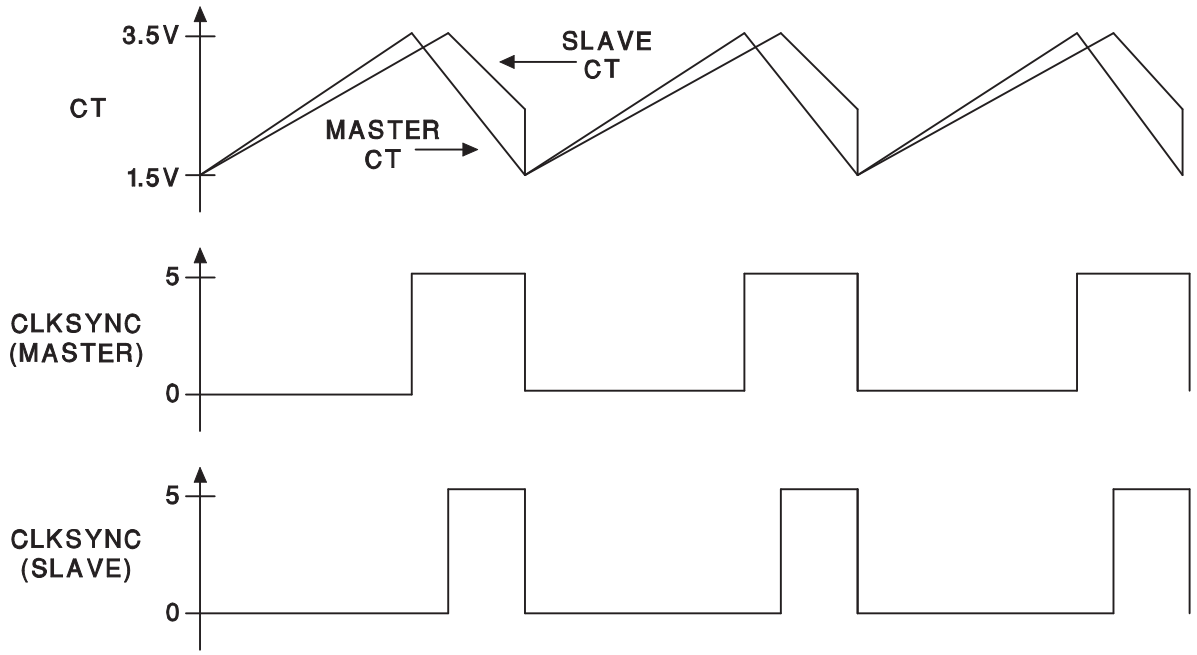

Figure 2. Oscillator Waveforms

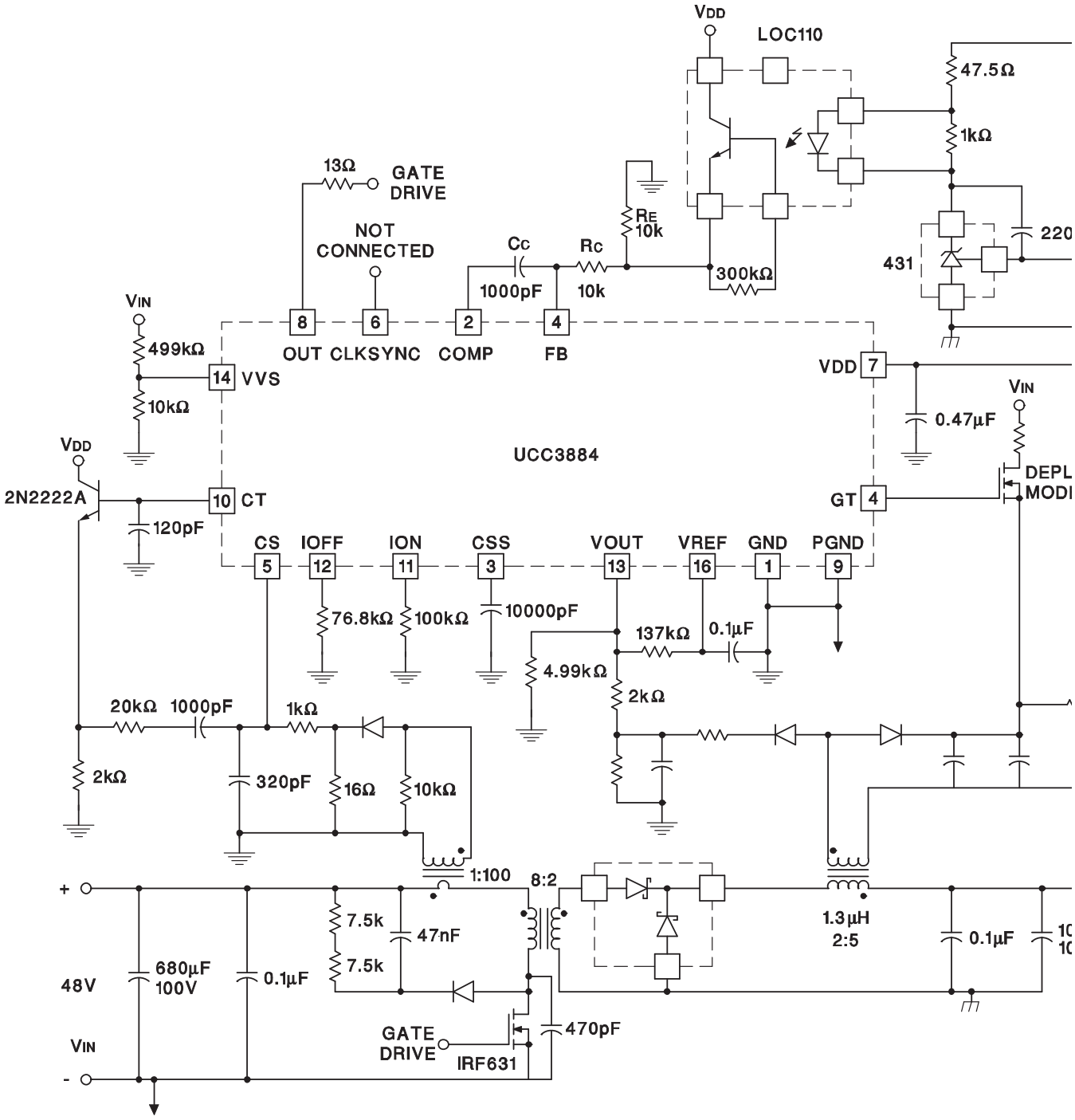

Figure 3. Typical Application

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