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The UniPHY IP is an interface between a memory controller and memory devices and performs read and write operations to the memory. The UniPHY IP creates the datapath between the memory device and the memory controller and user logic in various Altera devices.

The Altera® DDR2, DDR3, and LPDDR2 SDRAM controllers with UniPHY, QDR II and QDR II+ SRAM controllers with UniPHY, RLDRAM II controller with UniPHY, and RLDRAM 3 PHY-only IP provide low latency, high-performance, feature-rich interfaces to industry-standard memory devices. The DDR2, QDR II and QDR II+, and RLDRAM II controllers with UniPHY offer full-rate and half-rate interfaces, while the DDR3 controller with UniPHY and the RLDRAM 3 PHY-only IP offer half-rate and quarter-rate interfaces, and the LPDDR2 controller with UniPHY offers a half-rate interface.

When you generate your external memory interface IP core, the system creates an example top-level project, consisting of an example driver, and your controller custom variation. The controller instantiates an instance of the UniPHY datapath.

The example top-level project is a fully-functional design that you can simulate, synthesize, and use in hardware. The example driver is a self-test module that issues read and write commands to the controller and checks the read data to produce the pass, fail, and test-complete signals.

If the UniPHY datapath does not match your requirements, you can create your own memory interface datapath using the ALTDLL, ALTDQ_DQS, ALTDQ_DQS2, ALTDQ, or ALTDQS IP cores, available in the Quartus® II software, but you are then responsible for all aspects of the design including timing analysis and design constraints.

Release Information

The following table provides information about this release of the DDR2 and DDR3 SDRAM, QDR II and QDR II+ SRAM, and RLDRAM II controllers with UniPHY, and the RLDRAM 3 PHY-only IP.

Table 10-1: Release Information

Item	Protocol			
	DDR2, DDR3, LPDDR2	**QDR II**	**RLDRAM II**	**RLDRAM 3**
Version	13.1	13.1	13.1	13.1
Release Date	November 2013	November 2013	November 2013	November 2013

Item	Protocol			
	DDR2, DDR3, LPDDR2	**QDR II**	**RLDRAM II**	**RLDRAM 3**
Ordering Code	IP-DDR2/UNI IP-DDR3/UNI IP-SDRAM/LPDDR2	IP-QDRII/UNI	IP-RLDII/UNI	—

Altera verifies that the current version of the Quartus II software compiles the previous version of each MegaCore function. The *MegaCore IP Library Release Notes and Errata* report any exceptions to this verification. Altera does not verify compilation with MegaCore function versions older than one release.

Related Information
MegaCore IP Library Release Notes

Device Support Levels

The following terms define the device support levels for Altera IP cores.

Altera IP Core Device Support Levels

- **Preliminary support**—Altera verifies the IP core with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. You can use it in production designs with caution.
- **Final support**—Altera verifies the IP core with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

Device Family and Protocol Support

The following table shows the level of support offered by each of the UniPHY-based external memory interface protocols for Altera device families.

Table 10-2: Device Family Support

Device Family	Support Level					
	DDR2	**DDR3**	**LPDDR2**	**QDR II**	**RLDRAM II**	**RLDRAM 3**
Arria® II GX	No support	No support	No support	Final	No support	No support
Arria II GZ	Final	Final	No support	Final	Final	No support
Arria V	Refer to the *What's New in Altera IP* page of the Altera website.					No support
Arria V GZ	Refer to the *What's New in Altera IP* page of the Altera website.	No support	Refer to the *What's New in Altera IP* page of the Altera website.			

Device Family	Support Level					
	DDR2	DDR3	LPDDR2	QDR II	RLDRAM II	RLDRAM 3
Cyclone V	Refer to the *What's New in Altera IP* page of the Altera website.					No support
Stratix® III	Final	Final (Only Vcc = 1.1V supported)	No support	Final	Final (Only Vcc = 1.1V supported)	No support
Stratix IV	Final	Final	No support	Final	Final	No support
Stratix V	Refer to the *What's New in Altera IP* page of the Altera website.		No support	Refer to the *What's New in Altera IP* page of the Altera website.		
Other device families	No support	No support	No support	No support	No support	No support

For information about features and supported clock rates for external memory interfaces, refer to the *External Memory Specification Estimator*.

Related Information

- **What's New in Altera IP**

- **External Memory Interface Spec Estimator**

UniPHY-Based External Memory Interface Features

The following table summarizes key feature support for Altera's UniPHY-based external memory interfaces.

Table 10-3: Feature Support

Key Feature	Protocol					
	DDR2	DDR3	LPDDR2	QDR II	RLDRAM II	RLDRAM 3
High-performance controller II (HPC II)	Yes	Yes	Yes	—	—	—
Half-rate core logic and user interface	Yes	Yes	Yes	Yes	Yes	Yes
Full-rate core logic and user interface	Yes	—	—	Yes	Yes	—
Quarter-rate core logic and user interface	—	Yes [1]	—	—	—	Yes
Dynamically generated Nios II-based sequencer	Yes	Yes	Yes	Yes	Yes	Yes

Key Feature	Protocol					
	DDR2	DDR3	LPDDR2	QDR II	RLDRAM II	RLDRAM 3
Choice of RTL-based or dynamically generated Nios® II-based sequencer	—	—	—	Yes [2] [3] [12]	Yes [12]	—
Available Efficiency Monitor and Protocol Checker	Yes	Yes	Yes	—	Yes	Yes
DDR3L support	—	Yes [1]	—	—	—	—
UDIMM and RDIMM in any form factor	Yes	Yes [4] [5]	—	—	—	—
Multiple components in a single-rank UDIMM or RDIMM layout	Yes	Yes	—	—	—	—
LRDIMM	—	Yes	—	—	—	—
Burst length (half-rate)	8	—	8 or 16	4	4 or 8	2, 4, or 8
Burst length (full-rate)	4	—	—	2 or 4	2, 4, or 8	—
Burst length (quarter-rate)	—	8	—	—	—	2, 4, or 8
Burst length of 8 and burst chop of 4 (on the fly)	—	Yes	—	—	—	—
With leveling	240 MHz and above [10]	Yes [9] [10]	—	—	—	Yes
Without leveling	Below 240 MHz	—	Yes	—	—	—
Maximum data width	144 bits [6]	144 bits [6]	32 bits	72 bits	72 bits	72 bits
Reduced controller latency	—	—	—	Yes [2] [7]	Yes [2] [7]	—
Read latency	—	—	—	1.5 (QDR II) 2 or 2.5 (QDR II+)	—	—
ODT (in memory device)	—	Yes	—	QDR II+ only	Yes	Yes
x36 emulation mode	—	—	—	Yes [8] [10]	—	—

Key Feature	Protocol					
	DDR2	DDR3	LPDDR2	QDR II	RLDRAM II	RLDRAM 3

Notes:

1. For Arria V GZ and Stratix V devices only.
2. Not available in Arria II GX devices.
3. Nios II-based sequencer not available for full-rate interfaces.
4. For DDR3, the DIMM form is not supported in Arria II GX, Arria II GZ, Arria V, or Cyclone V devices.
5. Arria II GZ uses leveling logic for discrete devices in DDR3 interfaces to achieve high speeds, but that leveling cannot be used to implement the DIMM form in DDR3 interfaces.
6. For any interface with data width above 72 bits, you must use Quartus II software timing analysis of your complete design to determine the maximum clock rate.
7. The maximum achievable clock rate when reduced controller latency is selected must be attained through Quatrus II software timing analysis of your complete design.
8. Emulation mode allows emulation of a larger memory-width interface using multiple smaller memory-width interfaces. For example, an x36 QDR II or QDR II+ interface can be emulated using two x18 interfaces.
9. The leveling delay on the board between first and last DDR3 SDRAM component laid out as a DIMM must be less than 0.69 tCK.
10. Leveling is not available for Arria V or Cyclone V devices.
11. x36 emulation mode is not supported in Arria V, Arria V GZ, Cyclone V, or Stratix V devices.
12. The RTL-based sequencer is not available for QDR II or RLDRAM II interfaces on Arria V devices.

System Requirements

For system requirements and installation instructions, refer to *Altera Software Installation and Licensing*.

The DDR2, DDR3, and LPDDR2 SDRAM controllers with UniPHY, QDR II and QDR II+ SRAM controllers with UniPHY, RLDRAM II controller with UniPHY, and RLDRAM 3 PHY-only IP are part of the MegaCore IP Library, which Altera distributes with the Quartus II software.

Related Information
Altera Software Installation and Licensing Manual

MegaCore Verification

Altera has carried out extensive random, directed tests with functional test coverage using industry-standard models to ensure the functionality of the external memory controllers with UniPHY. Altera's functional verification of the external memory controllers with UniPHY use modified Denali models, with certain assertions disabled.

Resource Utilization

The following topics provide resource utilization data for the external memory controllers with UniPHY for supported device families.

DDR2, DDR3, and LPDDR2 Resource Utilization in Arria V Devices

The following table shows typical resource usage of the DDR2, DDR3, and LPDDR2 SDRAM controllers with UniPHY in the current version of Quartus II software for Arria V devices.

Table 10-4: Resource Utilization in Arria V Devices

Protocol	Memory Width (Bits)	Combina-tional ALUTS	Logic Registers	M10K Blocks	Memory (Bits)	Hard Memory Controler
Controller						
DDR2 (Half rate)	8	2286	1404	4	6560	0
	64	2304	1379	17	51360	0
DDR2 (Fullrate)	32	0	0	0	0	1
DDR3 (Half rate)	8	2355	1412	4	6560	0
	64	2372	1440	17	51360	0
DDR3 (Full rate)	32	0	0	0	0	1
LPDDR2 (Half rate)	8	2230	1617	4	6560	0
	32	2239	1600	10	25760	0
PHY						
DDR2 (Half rate)	8	1652	2015	34	141312	0
	64	1819	2089	34	174080	0
DDR2 (Fullrate)	32	1222	1415	34	157696	1
DDR3 (Half rate)	8	1653	1977	34	141312	0
	64	1822	2090	34	174080	0
DDR3 (Full rate)	32	1220	1428	34	157696	0
LPDDR2 (Half rate)	8	2998	3187	35	150016	0
	32	3289	3306	35	174592	0
Total						
DDR2 (Half rate)	8	4555	3959	39	148384	0
	64	4991	4002	52	225952	0
DDR2 (Fullrate)	32	1776	1890	35	158208	1
DDR3 (Half rate)	8	4640	3934	39	148384	0
	64	5078	4072	52	225952	0

Protocol	Memory Width (Bits)	Combina-tional ALUTS	Logic Registers	M10K Blocks	Memory (Bits)	Hard Memory Controiler
DDR3 (Full rate)	32	1774	1917	35	158208	1
LPDDR2 (Half rate)	8	5228	4804	39	156576	0
	32	5528	4906	45	200352	0

DDR2 and DDR3 Resource Utilization in Arria II GZ Devices

The following table shows typical resource usage of the DDR2 and DDR3 SDRAM controllers with UniPHY in the current version of Quartus II software for Arria II GZ devices.

Table 10-5: Resource Utilization in Arria II GZ Devices

Protocol	Memory Width (Bits)	Combina-tional ALUTS	Logic Registers	Mem ALUTs	M9K Blocks	M144K Blocks	Memory (Bits)
Controller							
DDR2 (Half rate)	8	1,781	1,092	10	2	0	4,352
	16	1,784	1,092	10	4	0	8,704
	64	1,818	1,108	10	15	0	34,560
	72	1,872	1,092	10	17	0	39,168
DDR2 (Full rate)	8	1,851	1,124	10	2	0	2,176
	16	1,847	1,124	10	2	0	4,352
	64	1,848	1,124	10	8	0	17,408
	72	1,852	1,124	10	9	0	19,574
DDR3 (Half rate)	8	1,869	1,115	10	2	0	4,352
	16	1,868	1,115	10	4	0	8,704
	64	1,882	1,131	10	15	0	34,560
	72	1,888	1,115	10	17	0	39,168
PHY							
DDR2 (Half rate)	8	2,560	2,042	183	22	0	157,696
	16	2,730	2,262	183	22	0	157,696
	64	3,606	3,581	183	22	0	157,696
	72	3,743	3,796	183	22	0	157,696

Protocol	Memory Width (Bits)	Combina-tional ALUTS	Logic Registers	Mem ALUTs	M9K Blocks	M144K Blocks	Memory (Bits)
DDR2 (Full rate)	8	2,494	1,934	169	22	0	157,696
	16	2,652	2,149	169	22	0	157,696
	64	3,519	3,428	169	22	0	157,696
	72	3,646	3,642	169	22	0	157,696
DDR3 (Half rate)	8	2,555	2,032	187	22	0	157,696
	16	3,731	2,251	187	22	0	157,696
	64	3,607	3,572	187	22	0	157,696
	72	3,749	3,788	187	22	0	157,696
Total							
DDR2 (Half rate)	8	4,341	3,134	193	24	0	4,374
	16	4,514	3,354	193	26	0	166,400
	64	5,424	4,689	193	37	0	192,256
	72	5,615	4,888	193	39	0	196,864
DDR2 (Full rate)	8	4,345	3,058	179	24	0	159,872
	16	4,499	3,273	179	24	0	162,048
	64	5,367	4,552	179	30	0	175,104
	72	5,498	4,766	179	31	0	177,280
DDR3 (Half rate)	8	4,424	3,147	197	24	0	162,048
	16	5,599	3,366	197	26	0	166,400
	64	5,489	4,703	197	37	0	192,256
	72	5,637	4,903	197	39	0	196,864

DDR2 and DDR3 Resource Utilization in Stratix III Devices

The following table shows typical resource usage of the DDR2 and DDR3 SDRAM controllers with UniPHY in the current version of Quartus II software for Stratix III devices.

Table 10-6: Resource Utilization in Stratix III Devices

Protocol	Memory Width (Bits)	Combina-tional ALUTS	Logic Registers	Mem ALUTs	M9K Blocks	M144K Blocks	Memory (Bits)
Controller							
DDR2 (Half rate)	8	1,807	1,058	0	4	0	4,464
	16	1,809	1,058	0	6	0	8,816
	64	1,810	1,272	10	14	0	32,256
	72	1,842	1,090	10	17	0	39,168
DDR2 (Full rate)	8	1,856	1,093	0	4	0	2,288
	16	1,855	1,092	0	4	0	4,464
	64	1,841	1,092	0	10	0	17,520
	72	1,834	1,092	0	11	0	19,696
DDR3 (Half rate)	8	1,861	1,083	0	4	0	4,464
	16	1,863	1,083	0	6	0	8,816
	64	1,878	1,295	10	14	0	32,256
	72	1,895	1,115	10	17	0	39,168
PHY							
DDR2 (Half rate)	8	2,591	2,100	218	6	1	157,696
	16	2,762	2,320	218	6	1	157,696
	64	3,672	3,658	242	6	1	157,696
	72	3,814	3,877	242	6	1	157,696
DDR2 (Full rate)	8	2,510	1,986	200	6	1	157,696
	16	2,666	2,200	200	6	1	157,696
	64	3,571	3,504	224	6	1	157,696
	72	3,731	3,715	224	6	1	157,696
DDR3 (Half rate)	8	2,591	2,094	224	6	1	157,696
	16	2,765	2,314	224	6	1	157,696
	64	3,680	3,653	248	6	1	157,696
	72	3,819	3,871	248	6	1	157,696

Protocol	Memory Width (Bits)	Combina-tional ALUTS	Logic Registers	Mem ALUTs	M9K Blocks	M144K Blocks	Memory (Bits)
Total							
DDR2 (Half rate)	8	4,398	3,158	218	10	1	162,160
	16	4,571	3,378	218	12	1	166,512
	64	5,482	4,930	252	20	1	189,952
	72	5,656	4,967	252	23	1	196,864
DDR2 (Full rate)	8	4,366	3,079	200	10	1	159,984
	16	4,521	3,292	200	10	1	162,160
	64	5,412	4,596	224	16	1	175,216
	72	5,565	4,807	224	17	1	177,392
DDR3 (Half rate)	8	4,452	3,177	224	10	1	162,160
	16	4,628	3,397	224	12	1	166,512
	64	5,558	4,948	258	20	1	189,952
	72	5,714	4,986	258	23	1	196,864

DDR2 and DDR3 Resource Utilization in Stratix IV Devices

The following table shows typical resource usage of the DDR2 and DDR3 SDRAM controllers with UniPHY in the current version of Quartus II software for Stratix IV devices.

Table 10-7: Resource Utilization in Stratix IV Devices

Protocol	Memory Width (Bits)	Combina-tional ALUTS	Logic Registers	Mem ALUTs	M9K Blocks	M144K Blocks	Memory (Bits)
Controller							
DDR2 (Half rate)	8	1,785	1,090	10	2	0	4,352
	16	1,785	1,090	10	4	0	8,704
	64	1,796	1,106	10	15	0	34,560
	72	1,798	1,090	10	17	0	39,168

Protocol	Memory Width (Bits)	Combina-tional ALUTS	Logic Registers	Mem ALUTs	M9K Blocks	M144K Blocks	Memory (Bits)
DDR2 (Full rate)	8	1,843	1,124	10	2	0	2,176
	16	1,845	1,124	10	2	0	4,352
	64	1,832	1,124	10	8	0	17,408
	72	1,834	1,124	10	9	0	19,584
DDR3 (Half rate)	8	1,862	1,115	10	2	0	4,352
	16	1,874	1,115	10	4	0	8,704
	64	1,880	1,131	10	15	0	34,560
	72	1,886	1,115	10	17	0	39,168
PHY							
DDR2 (Half rate)	8	2,558	2,041	183	6	1	157,696
	16	2,728	2,262	183	6	1	157,696
	64	3,606	3,581	183	6	1	157,696
	72	3,748	3,800	183	6	1	157,696
DDR2 (Full rate)	8	2,492	1,934	169	6	1	157,696
	16	2,652	2,148	169	6	1	157,696
	64	3,522	3,428	169	6	1	157,696
	72	3,646	3,641	169	6	1	157,696
DDR3 (Half rate)	8	2,575	2,031	187	6	1	157,696
	16	2,732	2,251	187	6	1	157,696
	64	3,602	3,568	187	6	1	157,696
	72	3,750	3,791	187	6	1	157,696
Total							
DDR2 (Half rate)	8	4,343	3,131	193	8	1	162,048
	16	4,513	3,352	193	10	1	166,400
	64	5,402	4,687	193	21	1	192,256
	72	5,546	4,890	193	23	1	196,864

Protocol	Memory Width (Bits)	Combinational ALUTS	Logic Registers	Mem ALUTs	M9K Blocks	M144K Blocks	Memory (Bits)
DDR2 (Full rate)	8	4,335	3,058	179	8	1	159,872
	16	4,497	3,272	179	8	1	162,048
	64	5,354	4,552	179	14	1	175,104
	72	5,480	4,765	179	15	1	177,280
DDR3 (Half rate)	8	4,437	3,146	197	8	1	162,048
	16	4,606	3,366	197	10	1	166,400
	64	5,482	4,699	197	21	1	192,256
	72	5,636	4,906	197	23	1	196,864

DDR2 and DDR3 Resource Utilization in Arria V GZ and Stratix V Devices

The following table shows typical resource usage of the DDR2 and DDR3 SDRAM controllers with UniPHY in the current version of Quartus II software for Arria V GZ and Stratix V devices.

Table 10-8: Resource Utilization in Arria V GZ and Stratix V Devices

Protocol	Memory Width (Bits)	Combinational LCs	Logic Registers	M20K Blocks	Memory (Bits)
Controller					
DDR2 (Half rate)	8	1,787	1,064	2	4,352
	16	1,794	1,064	4	8,704
	64	1,830	1,070	14	34,304
	72	1,828	1,076	15	38,400
DDR2 (Full rate)	8	2,099	1,290	2	2,176
	16	2,099	1,290	2	4,352
	64	2,126	1,296	7	16,896
	72	2,117	1,296	8	19,456
DDR3 (Quarter rate)	8	2,101	1,370	4	8,704
	16	2,123	1,440	7	16,896
	64	2,236	1,885	28	69,632
	72	2,102	1,870	30	74,880

Protocol	Memory Width (Bits)	Combinational LCs	Logic Registers	M20K Blocks	Memory (Bits)
DDR3 (Half rate)	8	1,849	1,104	2	4,352
	16	1,851	1,104	4	8,704
	64	1,853	1,112	14	34,304
	72	1,889	1,116	15	38,400
PHY					
DDR2 (Half rate)	8	2,567	1,757	13	157,696
	16	2,688	1,809	13	157,696
	64	3,273	2,115	13	157,696
	72	3,377	2,166	13	157,696
DDR2 (Full rate)	8	2,491	1,695	13	157,696
	16	2,578	1,759	13	157,696
	64	3,062	2,137	13	157,696
	72	3,114	2,200	13	157,696
DDR3 (Quarter rate)	8	2,209	2,918	18	149,504
	16	2,355	3,327	18	157,696
	64	3,358	5,228	18	182,272
	72	4,016	6,318	18	198,656
DDR3 (Half rate)	8	2,573	1,791	13	157,696
	16	2,691	1,843	13	157,696
	64	3,284	2,149	13	157,696
	72	3,378	2,200	13	157,696
Total					
DDR2 (Half rate)	8	4,354	2,821	15	162,048
	16	4,482	2,873	17	166,400
	64	5,103	3,185	27	192,000
	72	5,205	3,242	28	196,096

Protocol	Memory Width (Bits)	Combinational LCs	Logic Registers	M20K Blocks	Memory (Bits)
DDR2 (Full rate)	8	4,590	2,985	15	159,872
	16	4,677	3,049	15	162,048
	64	5,188	3,433	20	174,592
	72	5,231	3,496	21	177,152
DDR3 (Quarter rate)	8	4,897	4,844	23	158,720
	16	5,065	5,318	26	175,104
	64	6,183	7,669	47	252,416
	72	6,705	8,744	49	274,048
DDR3 (Half rate)	8	4,422	2,895	15	162,048
	16	4,542	2,947	17	166,400
	64	5,137	3,261	27	192,000
	72	5,267	3,316	28	196,096

QDR II and QDR II+ Resource Utilization in Arria V Devices

The following table shows typical resource usage of the QDR II and QDR II+ SRAM controllers with UniPHY in the current version of Quartus II software for Arria V devices.

Table 10-9: Resource Utilization in Arria V Devices

PHY Rate	Memory Width (Bits)	Combina-tional ALUTs	Logic Registers	M10K Blocks	Memory (Bits)	Hard Memory Controller
Controller						
Half	9	98	120	0	0	0
	18	96	156	0	0	0
	36	94	224	0	0	0
PHY						
Half	9	234	257	0	0	0
	18	328	370	0	0	0
	36	522	579	0	0	0
Total						

PHY Rate	Memory Width (Bits)	Combina-tional ALUTs	Logic Registers	M10K Blocks	Memory (Bits)	Hard Memory Controiler
Half	9	416	377	0	0	0
	18	542	526	0	0	0
	36	804	803	0	0	0

QDR II and QDR II+ Resource Utilization in Arria II GX Devices

The following table shows typical resource usage of the QDR II and QDR II+ SRAM controllers with UniPHY in the current version of Quartus II software for Arria II GX devices.

Table 10-10: Resource Utilization in Arria II GX Devices

PHY Rate	Memory Width (Bits)	Combinational ALUTS	Logic Registers	Memory (Bits)	M9K Blocks
Half	9	620	701	0	0
	18	921	1122	0	0
	36	1534	1964	0	0
Full	9	584	708	0	0
	18	850	1126	0	0
	36	1387	1962	0	0

QDR II and QDR II+ Resource Utilization in Arria II GZ, Arria V GZ, Stratix III, Stratix IV, and Stratix V Devices

The following table shows typical resource usage of the QDR II and QDR II+ SRAM controllers with UniPHY in the current version of Quartus II software for Arria II GZ, Arria V GZ, Stratix III, Stratix IV, and Stratix V devices.

Table 10-11: Resource Utilization in Arria II GZ, Arria V GZ, Stratix III, Stratix IV, and Stratix V Devices

PHY Rate	Memory Width (Bits)	Combinational ALUTS	Logic Registers	Memory (Bits)	M9K Blocks
Half	9	602	641	0	0
	18	883	1002	0	0
	36	1457	1724	0	0
Full	9	586	708	0	0
	18	851	1126	0	0
	36	1392	1962	0	0

RLDRAM II Resource Utilization in Arria V Devices

The following table shows typical resource usage of the RLDRAM II controller with UniPHY in the current version of Quartus II software for Arria V devices.

Table 10-12: Resource Utilization in Arria V Devices (Part 1 of 2)

PHY Rate	Memory Width (Bits)	Combina-tional ALUTs	Logic Registers	M10K Blocks	Memory (Bits)	Hard Memory Controller
Controller						
Half	9	353	303	1	288	0
	18	350	324	2	576	0
	36	350	402	4	1152	0
PHY						
Half	9	295	474	0	0	0
	18	428	719	0	0	0
	36	681	1229	0	0	0
Total						
Half	9	705	777	1	288	0
	18	871	1043	2	576	0
	36	1198	1631	4	1152	0

RLDRAM II Resource Utilization in Arria II GZ, Arria V GZ, Stratix III, Stratix IV, and Stratix V Devices

The following table shows typical resource usage of the RLDRAM II controller with UniPHY in the current version of Quartus II software for Arria II GZ, Arria V GZ, Stratix III, Stratix IV, and Stratix V devices.

Table 10-13: Resource Utilization in Arria II GZ, Arria V GZ, Stratix III, Stratix IV, and Stratix V Devices [1]

PHY Rate	Memory Width (Bits)	Combinational ALUTS	Logic Registers	Memory (Bits)	M9K Blocks
Half	9	829	763	288	1
	18	1145	1147	576	2
	36	1713	1861	1152	4
Full	9	892	839	288	1
	18	1182	1197	576	1
	36	1678	1874	1152	2

PHY Rate	Memory Width (Bits)	Combinational ALUTS	Logic Registers	Memory (Bits)	M9K Blocks

Note to Table:

1. Half-rate designs use the same amount of memory as full-rate designs, but the data is organized in a different way (half the width, double the depth) and the design may need more M9K resources.

Document Revision History

Date	Version	Changes
August 2014	2014.08.15	Removed occurrences of MegaWizard Plug-In Manager.
December 2013	2013.12.16	• Removed references to ALTMEMPHY. • Removed references to HardCopy.
November 2012	2.1	• Added RLDRAM 3 support. • Added LRDIMM support. • Added Arria V GZ support. • Changed chapter number from 8 to 10.
June 2012	2.0	• Added LPDDR2 support. • Moved *Protocol Support Matrix* to Volume 1. • Added Feedback icon.
November 2011	1.1	• Combined Release Information, Device Family Support, Features list, and Unsupported Features list for DDR2, DDR3, QDR II, and RLDRAM II. • Added Protocol Support Matrix. • Combined Resource Utilization information for DDR2, DDR3, QDR II, and RLDRAM II. • Updated data for 11.1.