HARRIS

HSP43168

November 1991

Dual FIR Filter

Features

- Two Independent 8-Tap FIR Filters Configurable as a Single 16-Tap FIR
- 10 Bit Data & Coefficients
- On-Board Storage for 32 Programmable Coefficient Sets
- Up To: 256 FIR Taps, 16 x 16 2-D Kernels, or 10 x 20 Bit Data and Coefficients
- Programmable Decimation to 16
- Programmable Rounding on Output
- Mixed Mode Arithmetic
- Standard Microprocessor Interface
- 33MHz, 45MHz Versions
- 85-Pin PGA, 84-Pin PLCC Packages

Applications

- Quadrature Filtering
- Correlation
- Image Processing
- Complex Filtering
- PolyPhase Filtering
- Adaptive Filtering

Description

The HSP43168 Dual FIR Filter consists of two independent 8-tap FIR filters. Each filter supports decimation from 1 to 16 and provides on-board storage for 32 sets of coefficients. The Block Diagram shows two FIR cells each fed by a separate coefficient bank and one of two separate inputs. The outputs of the FIR cells are either summed or multiplexed by the MUX/Adder. The compute power in the FIR Cells can be configured to provide quadrature filtering, complex filtering, 2-D convolution, 1-D/2-D correlations, and interpolating/decimating filters.

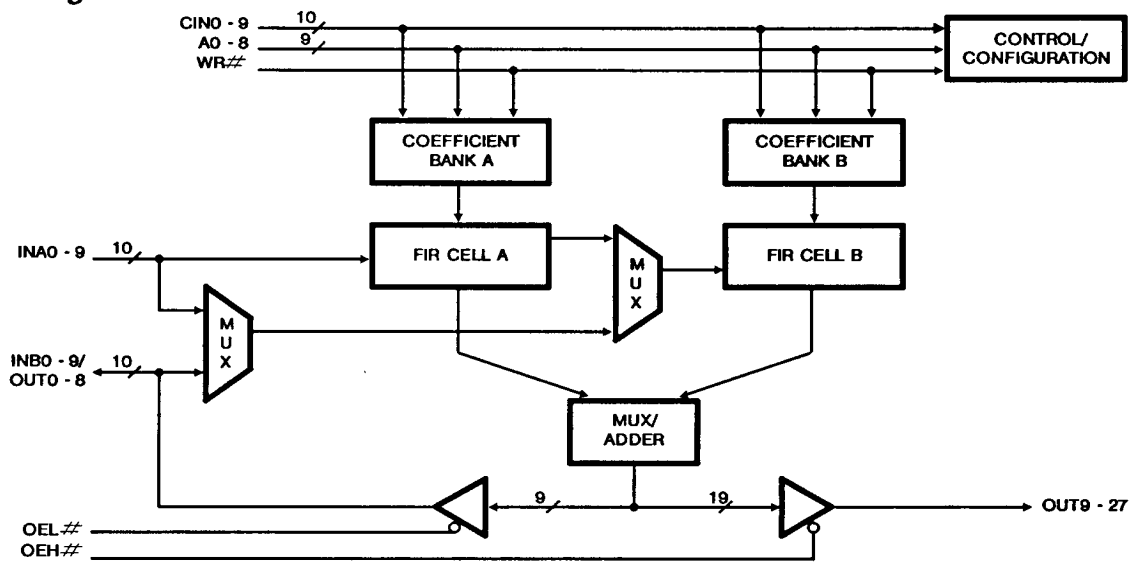
The FIR cells take advantage of symmetry in FIR coefficints by pre-adding data samples prior to multiplication. This allows an 8-tap FIR to be implemented using only 4 multipliers per filter cell. These cells can be configured as either a single 16-tap FIR filter or dual 8-tap FIR filters. Asymmetric filtering is also supported.

Decimation of up to 16 is provided to boost the effective number of filter taps from 2 to 16 times. Further, the decimtion registers provide the delay necessary for fractional data conversion and 2-D filtering with kernels to 16x16.

The flexibility of the Dual is further enhanced by 32 sets of user programmable coefficients. Coefficient selection may be changed asynchronously from clock to clock. The ability to toggle between coefficient sets further simplifies applications such as polyphase or adaptive filtering.

The HSP43168 is a low power fully static design implemented in an advanced CMOS process. The configuration of the device is controlled through a standard microprocessor interface. The Dual FIR Filter is available in 85 pin PGA and 84 pin PLCC packages.

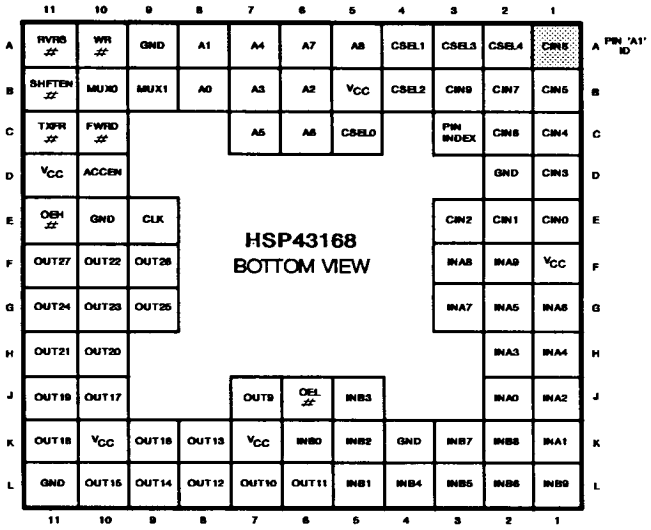
Block Diagram



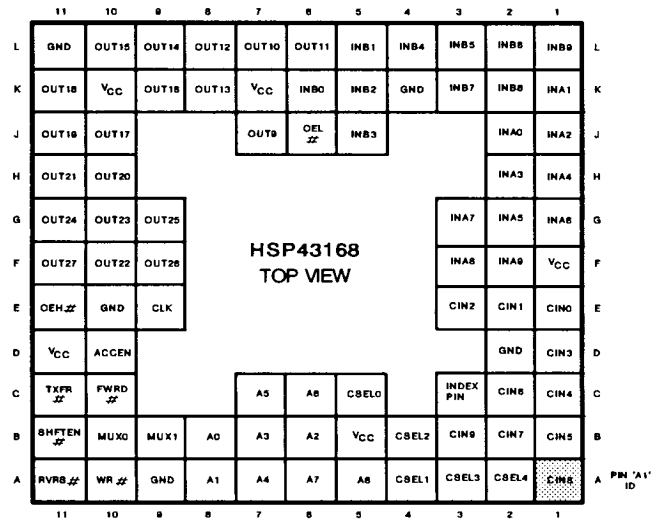
File Number **2808.1**

Pinouts

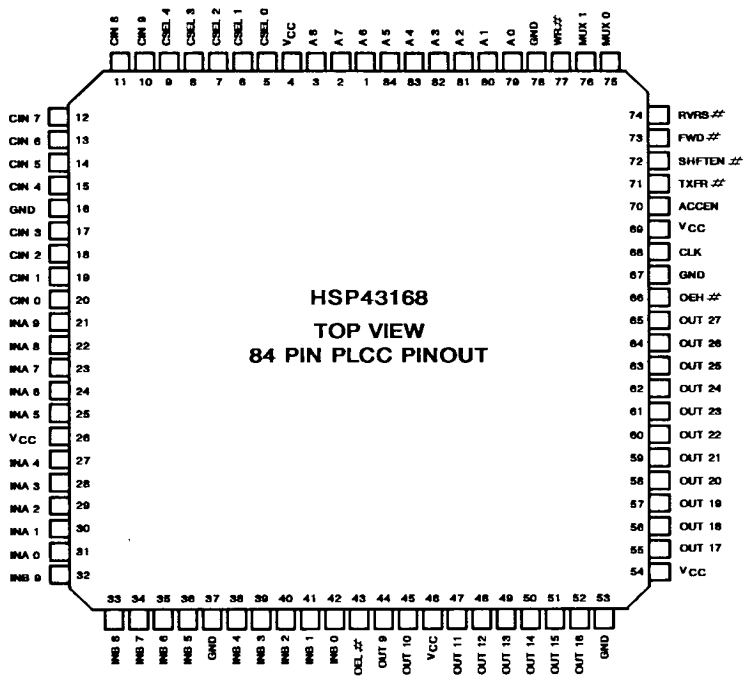
85 PIN PGA
BOTTOM VIEW



85 PIN PGA
TOP VIEW



84 PIN PLCC
TOP VIEW



Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
VCC	B5, D11, K10 K7, F1		VCC: +5V power supply pin.
GND	A9, E10, L11 K4, D2		Ground.
CIN0-9	E1-3, D1, C1-2, B1-3, A1	I	Control/Coefficient Data Bus. Processor interface for loading control data and coefficients. CIN0 is the LSB.
A0-8	A5-8, B6-8, C6-7	I	Control/Coefficient Address Bus. Processor interface for addressing control and coefficient registers. A0 is the LSB.
WR#	A10	I	Control/Coefficient Write Clock. Data is latched into the control and coefficient registers on the rising edge of WR#.
CSEL0-4	A2-4, B4, C5	I	Coefficient Select. This input determines which of the 32 coefficient sets are to be used by FIR A and B. This input is registered and CSEL0 is the LSB.
INA0-9	K1, J1-2, H1-2, G1-3, F2-3	I	Input to FIR A. INA0 is the LSB
INB0-9	L1-5, K2-3 K5-6, J5	I/O	Bidirectional Input for FIR B. INB0 is the LSB and is input only. When used as output, INB1-9 are the LSB's of the output bus.
OUT9-27	F9-11, G9-11, H10-11, J10-11 J7, K11, K8-9, L6-10	O	19 MSB's of Output Bus. Data format is either unsigned or two's complement depending on configuration. OUT27 is the MSB.
SHFTEN#	B11	I	Shift Enable. This active low input enables shifting of data through the decimation registers.
FWRD#	C10	I	Forward ALU Input Enable. When active low, data from the forward decimation path is input to the ALU's through the "a" input. When high, the "a" inputs to the ALUs are zeroed.
RVRS#	A11	I	Reverse ALU Input Enable. When active low, data from the reverse decimation path is input to the ALU's through the "b" input. When high, the "b" inputs to the ALUs are zeroed.
TXFR#	C11	I	Data Transfer Control. This active low input switches the LIFO being read into the reverse decimation path with the LIFO being written from the forward decimation path (see Figure 1).
MUX0-1	B9-10	I	Adder/Mux Control. This input controls data flow through the output Adder/Mux. Table 3.0 lists the various configurations.
CLK	E9	I	Clock. All inputs except those associated with the processor interface (CIN0-9, A0-8, WR#) and the output enables (OEL#, OEH#)are registered by the rising edge of CLK.
OEL#	J6	I	Output Enable Low. This tristate control enables the LSB's of the output bus to INB1-9 when OEL# is low.
OEH#	E11	I	Output Enable High. This tristate control enables OUT9-27 when OEH# is low.
ACCEN	D10	I	Accumulate Enable. This active high input allows accumulation in the FIR Cell Accumulator. A low on this input latches the FIR Accumulator contents into the Output Holding Registers while zeroing the feedback path in the Accumulator.

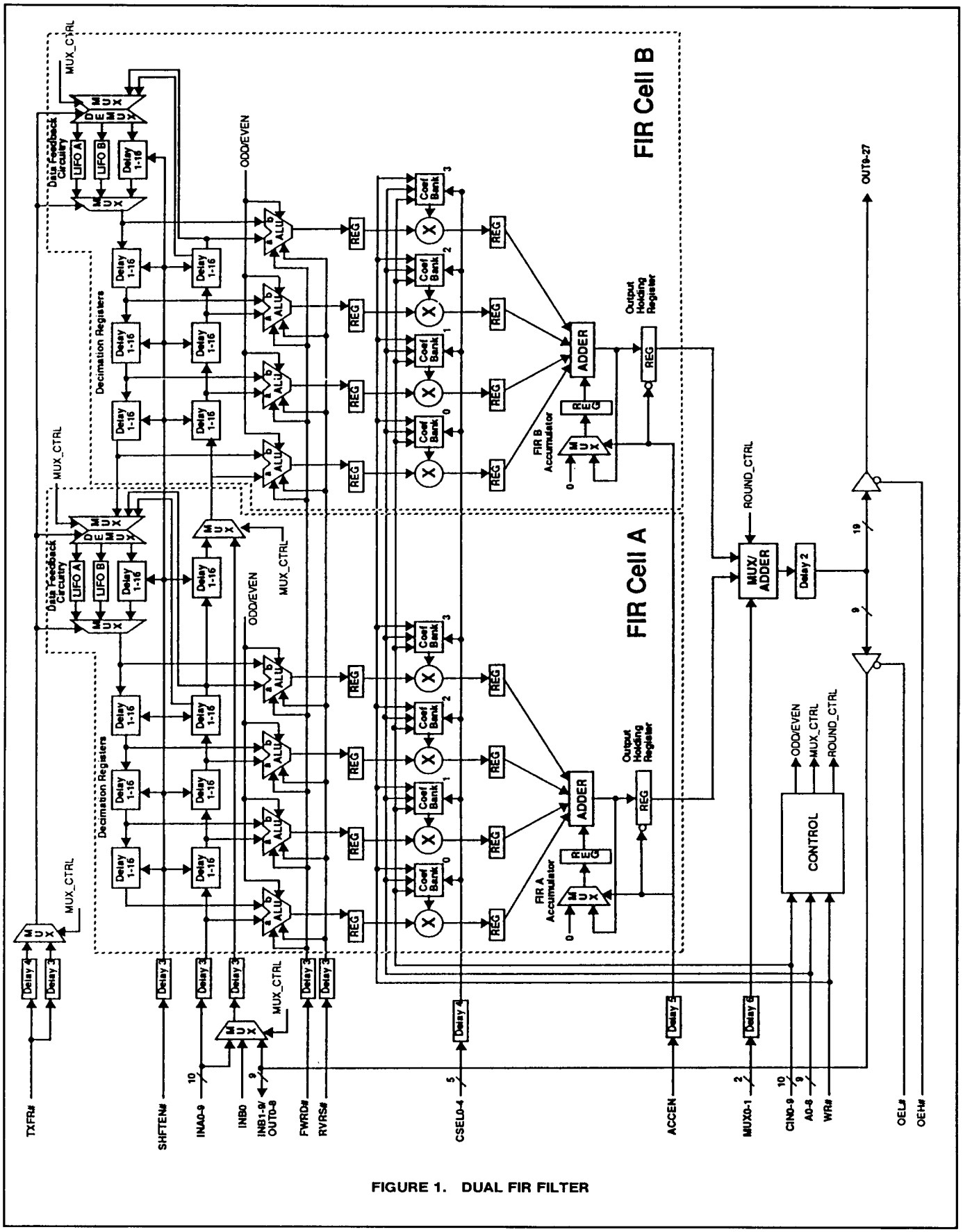


FIGURE 1. DUAL FIR FILTER

Functional Description

As shown in Figure 1.0, the HSP43168 consists of two 4-multiplier FIR filter cells which process 10 bit data and coefficients. The FIR cells can operate as two independent 8-tap FIR filters or two 4-tap asymmetric filters at maximum I/O rates. A single filter mode is provided which allows the FIR cells to operate as one 16-tap FIR filter or one 8-tap asymmetric filter. On board coefficient storage for up to 32 sets of 8 coefficients is provided. The coefficient sets are user selectable and are programmed through a microprocessor interface. Programmable decimation to 16 is also provided. By utilizing decimation registers together with the coefficient sets, polyphase filters are realizable which allow the user to trade data rate for filter taps. The MUX/ Adder can be configured to either add or multiplex the outputs of the filter cells depending upon whether the cells are operating in single or dual filter mode. In addition, a shifter in the MUX/Adder is provided for implementation of filters with 10 bit data and 20 bit coefficients or vice versa.

Microprocessor Interface

The Dual has a 20 pin write only microprocessor interface for loading data into the Control Block and Coefficient Bank. The interface consists of a 10-bit data bus (CIN0-9), a 9 bit address bus (A0-8), and a write input (WR#) to latch the data into the on-board registers. The control and coefficient data can be loaded asynchronously to CLK.

Control Block

The Dual FIR is configured by writing to the registers within the Control Block. These registers are memory mapped to address 000H (H = Hexadecimal) and 001H on A0-8. The format of these registers is shown in Table 1 and Table 2. Writing the Control/Configuration registers causes a reset which lasts for 6 CLK cycles following the assertion of WR#. The reset caused by writing registers in the Control Block will not clear the contents of the Coefficient Bank.

TABLE 1

CONTROL ADDRESS 000H		
BITS	**FUNCTION**	**DESCRIPTION**
3-0	Decimation Factor	0000=No Decimation 1111=Decimation by 16
4	Mode Select	0 = Single FIlter Mode 1 = Dual FIlter Mode
5	Odd/Even Symmetry	0 = Even symmetric coefficients 1 = Odd symmetric coefficients
6	FIR A odd/even taps	0 = Odd number of taps in filter 1 = Even number of taps in filter
7	FIR B odd/even taps	(Defined same as FIR A above)
8	FIR B Input Source	0 = Input from INA0-9 1 = Input from INB0-9
9	Not Used	Set to 0 for proper operation

The 4 LSBs of the control word loaded at address 000H are used to select the decimation factor. For example, if the 4 LSBs are programmed with a value of 0010, the forward and reverse shifting decimation registers are each configured with a delay of 3. Bit 4 is used to select whether the FIR cells operate as two independent filters or one extended length filter. Coefficient symmetry is selected by bit 5. Bits 6 and 7 are programmed to configure the FIR cells for odd or even filter lengths. Bit 8 selects the FIR B input source when the FIR cells are configured for independent operation. Bit 9 must be programmed to 0.

The 4 LSB's of the control word loaded at address 001H are used to configure the format of the FIR cell's data and coefficients. Bit 4 is programmed to enable or disable the reversal of data sample order prior to entering the backward shifting decimation registers. Bits 5-9 are used to support programmable rounding on the output.

TABLE 2

CONTROL ADDRESS 001H		
BITS	**FUNCTION**	**DESCRIPTION**
0	FIR A Input Format	0 = Unsigned 1 = Two's Complement
1	FIR A Coefficient Format	(Defined same as FIR A input)
2	FIR B Input Format	(Defined same as FIR A input)
3	FIR B Coefficient	(Defined same as FIR A input)
4	Data Reversal Enable	0 = Enabled 1 = Disabled
8-5	Round Position	$0000 = 2^{-10}$ $1011 = 2^{1}$
9	Round Enable	0 = Enabled 1 = Disabled

FIR Filter Cells

Each FIR filter cell is based on an array of four 11x10 bit two's complement multipliers. The multipliers get one input from the ALUs which combine data shifting through the forward and backward decimation registers. The second input comes from the user programmable coefficient bank. The multiplier outputs feed an accumulator whose result is passed to the output section where it is multiplexed or added.

Decimation Registers

The forward and backward shifting registers are configurable for decimation by 1 to 16 (see Table 1). The backward shifting registers are used to take advantage of symmetry in linear phase filters by aligning data at the ALU's for pre-addition prior to multiplication by the common coefficient. When the FIR cells are configured in single filter mode, the decimation registers in each cell are cascaded. This lengthened delay path allows computation of a filter which is twice the size of that capable in a single cell. The decimation registers also provide data storage for poly-phase or 2-D filtering applications (See Applications Examples section).

The Data Feedback Circuitry in each FIR cell is responsible for transferring data from the forward to the backward shifting decimation registers. This circuitry feeds blocks of samples into the backward shifting decimation path in either reversed or non-reversed sample order. The MUX/DEMUX structure at the input to the Feedback Circuitry routes data to the LIFO's or the delay stage depending on configuration. The MUX on the Feedback Circuitry Output selects the storage element which feeds the backward shifting decimation registers.

In applications requiring reversal of sample order, such as FIR filtering with decimation, the FIR cells are configured with data reversal enabled (see Table 2). In this mode, data is transferred from the forward to the backward shifting registers through a ping-ponged LIFO structure. While one LIFO is being read into the backward shifting path, the other is written with data samples. The MUX/DEMUX controls which LIFO is being written, and the MUX on the Feedback Circuitry output controls which LIFO is being read. A low on TXFR# and SHIFTEN#, switches the LIFO's being read and written, which causes the block of data read from the structure to be reversed in sample order (See Example 4 in the Application Examples section).

The frequency with which TXFR# is asserted determines size of the data blocks in which sample order is reversed. For example, if TXFR# is asserted once every three CLK's, blocks of 3 data samples with order reversed, would be fed into the backward decimation registers. Note: altering the frequency or phase of TXFR# assertion once a filtering operation has been started will cause unknown results.

In applications which do not require sample order reversal, the FIR cells must be configured with data reversal disabled (see Table 2). In addition, TXFR# must be asserted to ensure proper data flow. In this configuration, data to the backward shifting decimation path is routed though a delay stage instead of the ping-pong LIFO's. The number of registers in the delay stage is based on the programmed decimation factor. Note: data reversal must be disabled and TXFR# must be asserted for filtering applications which do not use decimation.

The shifting of data through the forward and reverse decimation registers is enabled by asserting the SHFTEN# input. When SHFTEN# transitions high, data shifting is disabled, and the data sample latched into the part on the previous clock is the last input to the forward decimation path. When SHFTEN# is asserted, shifting of data through the decimation paths is enabled. The data sample at the part input when SHFTEN# is asserted will be the next data sample into the forward decimation path.

When operating the FIR cells as two independent filters, FIR A receives input data via INA0-9 and FIR B receives data from either INA0-9 or INB0-9 depending on the configuration (Table 1). When the FIR cells are configured as a single extended length filter, the forward and backward decimation paths are cascaded. In this mode, data is transferred from the forward decimation path to the backward decimation path by the Data Feedback Circuitry in FIR B. Thus, the manner in which data is read into the backward shifting decimation path is determined by FIR B's configuration.

When the decimation paths are cascaded, data is routed through the delay stage in FIR A's Data Feedback Circuitry.

The configuration of the FIR cells as even or odd length filters determines the point in the forward decimation path from which data is multiplexed to the Data Feedback Circuitry. For example, if the FIR cell is configured as an odd length filter, data prior to the last register in the third forward decimation stage is routed to the Feedback Circuitry. If the FIR cell is configured as an even length filter, data output from the third forward decimation stage is multiplexed to the Feedback Circuitry. This is required to insure proper data alignment with symmetric filter coefficients (See Application Examples).

ALUs

Data shifting through the forward and reverse decimation path feeds the "a" and "b" inputs of the ALUs respectively. The ALU's perform an "b+a" operation if the FIR cell is configured for even symmetric coefficients or an "b-a" operation if configured for odd symmetric coefficients.

For applications in which a pre-add or subtract is not required, the "a" or "b" input can be zeroed by disabling FWRD# or RVRS# respectively. This has the effect of producing an ALU output which is either "a","-a", or "b" depending on the filter symmetry chosen. For example, if the FIR cell is configured for an even symmetric filter with FWRD# low and RVRS# high, the data shifting through the forward decimation registers would appear on the ALU output.

Coefficient Bank

The output of the ALU is multiplied by a coefficient from one of 32 user programmable coefficient sets. Each set consists of 8 coefficients (4 coefficients for FIR A and 4 for FIR B). The active coefficient set is selected using CSEL0-4. The coefficient set may be switched every clock to support polyphase filtering operations.

The coefficients are loaded into on-board registers using the microprocessor interface, CIN0-9, A0-8, and WR#. Each multiplier within the FIR Cells is driven by a coefficient bank with one of 32 coefficients. These coefficients are addressed as shown in Table 3. The inputs A0-1 specify the Coefficient Bank for one of the four multipliers in each FIR Cell; A2 specifies FIR Cell A or B; Bits A7-3 specify one of 32 sets in which the coefficient is to be stored. For example, an address of 10dH would access the coefficient for the second multiplier in FIR B in the second coefficient set.

TABLE 3

A8	A7-3	A2	A0-1	FIR	BANK
1	xxxxx	0	00	A	0
1	xxxxx	0	01	A	1
1	xxxxx	0	10	A	2
1	xxxxx	0	11	A	3
1	xxxxx	1	00	B	0
1	xxxxx	1	01	B	1
1	xxxxx	1	10	B	2
1	xxxxx	1	11	B	3

FIR Cell Accumulator

The registered outputs from the multipliers in each FIR cell feed the FIR cell's accumulator. The ACCEN input controls each accumulator's running sum and the latching of data from the accumulator into the Output Holding Registers. When ACCEN is low, feedback from the accumulator adder is zeroed which disables accumulation. Also, output from the accumulator is latched into the Output Holding Registers. When ACCEN is asserted, accumulation is enabled and the contents of the Output Holding Registers remain unchanged.

Output MUX/Adder

The contents of each FIR Cell's Output Holding Register is summed or multiplexed in the Mux/Adder. The operation of the Mux/Adder is controlled by the MUX0-1 inputs as shown in Table 4. Applications requiring 10 bit data and 20 bit coefficients or 20 bit data and 10 bit coefficients are made possible by configuring the MUX/Adder to scale FIR B's output by 2^{-10} prior to summing with FIR A. When the Dual FIR is configured as two independent filters, the MUX0-1 inputs would be used to multiplex the filter outputs of each cell. For applications in which FIR A and B are configured as a single filter, the MUX/Adder is configured to sum the output of each FIR cell.

TABLE 4

MUX0-1 DECODING	
MUX0-1	**OUT0-27**
00	FIRA + FIRB (FIR B Scaled by 2^{-10})
01	FIRA + FIRB
10	FIRA
11	FIRB

Input/Output Formats

The Dual FIR supports mixed mode arithmetic with both unsigned and two's complement data and coefficients. The input and output formats for both data types is shown below. If the Dual FIR is configured as an even symmetric filter with unsigned data and coefficients, the output will be unsigned. Otherwise, the output will be two's complement.

INPUT DATA FORMAT INA0-9, INB0-9
FRACTIONAL TWO'S COMPLEMENT

9	8	7	6	5	4	3	2	1	0
-2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT9-27
FRACTIONAL TWO'S COMPLEMENT

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
-2^9	2^8	2^7	2^6	2^4	2^5	2^3	2^2	2^1	2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT0-8
FRACTIONAL TWO'S COMPLEMENT

8	7	6	5	4	3	2	1	0
2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}

INPUT DATA FORMAT INA0-9, INB0-9
FRACTIONAL UNSIGNED

9	8	7	6	5	4	3	2	1	0
2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT9-27
FRACTIONAL UNSIGNED

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
2^9	2^8	2^7	2^6	2^4	2^5	2^3	2^2	2^1	2^0	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT0-8
FRACTIONAL UNSIGNED

8	7	6	5	4	3	2	1	0
2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}

The MUX/Adder can be configured to implement programmable rounding at bit locations 2^{-10} through 2^1. The round is implemented by adding a 1 to the specified location (see Table 2.0). For example, to configure the part such that the output is rounded to the 10 MSBs, OUT18-27, the round position would be chosen to be 2^{-1}.

Application Examples

In this section a number of examples which show even, odd, symmetric, asymmetric and decimating filters are presented. These examples are intended to show different operational modes of the HSP43168. The examples are all based on a dual filter configuration. However, the same principles apply when the part is configured with both FIR cells operating as a single filter.

Example 1. Even-Tap Symmetric Filter Example

The HSP43168 may be configured as two independent 8-tap symmetric filters as shown by the block diagram in Figure 2. Each of the FIR cells takes advantage of symmetric filter coefficients by pre-adding data samples common to a given coefficient. As a result, each FIR cell can implement an 8-tap symmetric filter using only four multipliers. Similarly, when the HSP43168 is configured in single filter mode a 16-tap symmetric filter is possible by using the multipliers in both cells.

The operation of the FIR cell is better understood by comparing the data and coefficient alignment for a given filter output, Figure 3, with the data flow through the FIR cell, as shown in Figure 4. The block diagrams in Figure 4 are a simplification of the FIR cell shown in Figure 1. For simplicity, the ALU's and FIR Cell Accumulators were replaced by adders, and the pipeline delay registers were omitted.

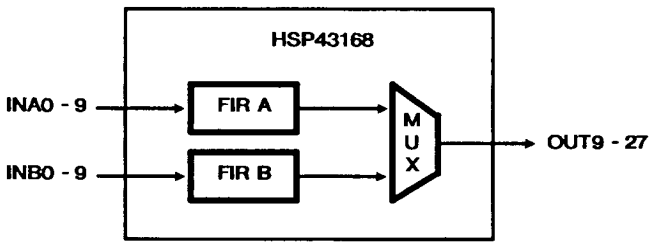


FIGURE 2. USING HSP43168 AS TWO INDEPENDENT FILTERS

In Figure 4, the order of the data samples within the filter cell is shown by the numbers in the forward and backward shifting decimation paths. The output of the filter cell is given by the equation at the bottom of each block diagram. Figure 4a shows the data sample alignment at the pre-adders for the data/coefficient alignment shown in Figure 3.

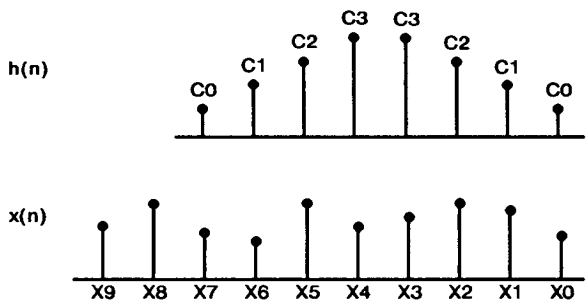
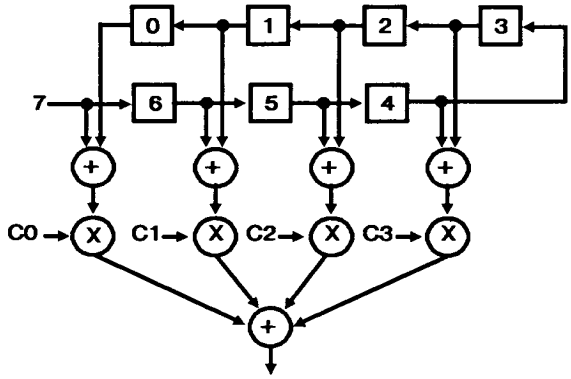


FIGURE 3. DATA/COEFFICIENT ALIGNMENT FOR 8-TAP EVEN SYMMETRIC FILTER

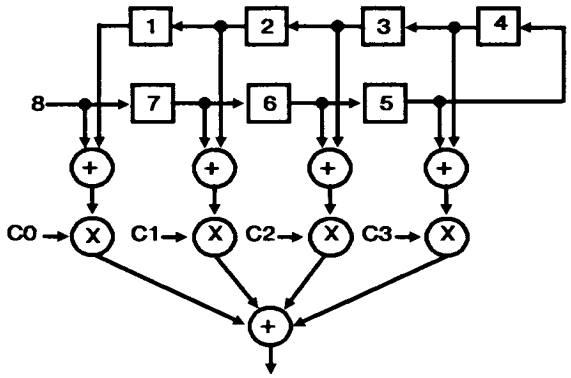
The dual filter application is configured by writing 1d0H to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Since this application does not use decimation, the 4th bit of the control register at address 001H must be set to disable data reversal (see Table 2). Failure to disable data reversal will produce erroneous results.

A. DATA FLOW AS DATA SAMPLE 7 IS CLOCKED INTO THE FEED FORWARD STAGE.



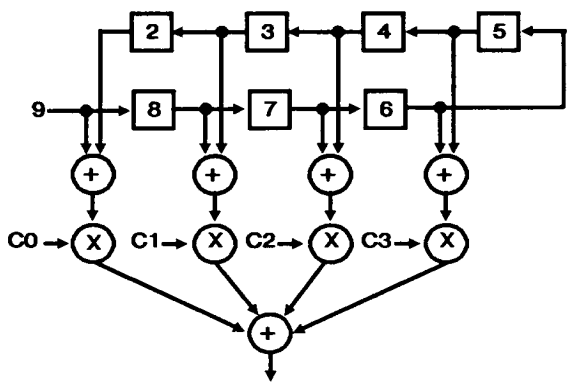
(X7+ X0)C0+ (X6+ X1)C1+ (X5+ X2)C2+ (X4+ X3)C3

B. DATA FLOW AS DATA SAMPLE 8 IS CLOCKED INTO THE FEED FORWARD STAGE.



(X8+ X1)C0+ (X7+ X2)C1+ (X6+ X3)C2+ (X5+ X4)C3

C. DATA FLOW AS DATA SAMPLE 9 IS CLOCKED INTO THE FEED FORWARD STAGE.



(X9+ X2)C0+ (X8+ X3)C1+ (X7+ X4)C2+ (X6+ X5)C3

FIGURE 4. DATA FLOW DIAGRAMS FOR 8-TAP SYMMETRIC FILTER

Using this architecture, only the unique coefficients need to be stored in the Coefficient Bank. For example, the above filter would be stored in the first coefficient set for FIR A by writing C0, C1, C2, and C3 to address 100H, 101H, 102H, and 103H respectively. To write the same filter to the first coefficient set for FIR B, the address sequence would change to 104H, 105H, 106H, and 107H.

To operate the HSP43168 in this mode, TXFR# is tied low to ensure proper data flow; both FWRD# and RVRS# are tied low to enable data samples from the forward and reverse data paths to the ALU's for pre-adding; ACCEN is tied low to prevent accumulation over multiple CLK's; SHFTEN# is tied low to allow shifting of data through the decimation registers; MUX0-1 is programmed to multiplex the output the of either FIR A or FIR B; CSEL0-4 is programmable to access the stored coefficient set, in this example CSEL = 0000.

Example 2. Odd-Tap Symmetric Filter Example

The HSP43168 may be configured as two independent 7-tap symmetric filters with a functional block diagram resembling Figure 2. As in the 8-tap filter example, the HSP43168 implements the filtering operation by summing data samples sharing a common coefficient prior to multiplication by that coefficient. However, for odd length filters the pre-addition requires that the center coefficient be scaled by 1/2.

The operation of the FIR cell for odd length filters is better understood by comparing the data/coefficient alignment in Figure 5 with the data flow diagrams in Figure 6. The block diagrams in Figure 6 are a simplification of the FIR cell shown in Figure 1.

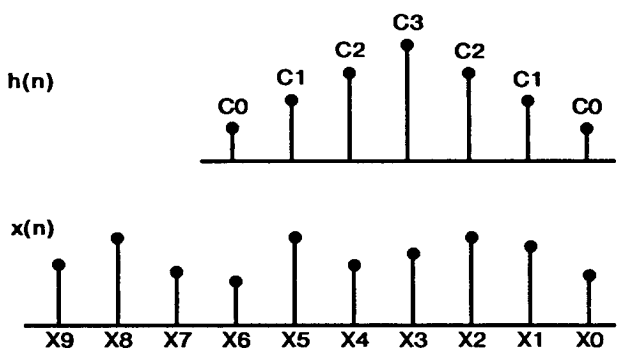
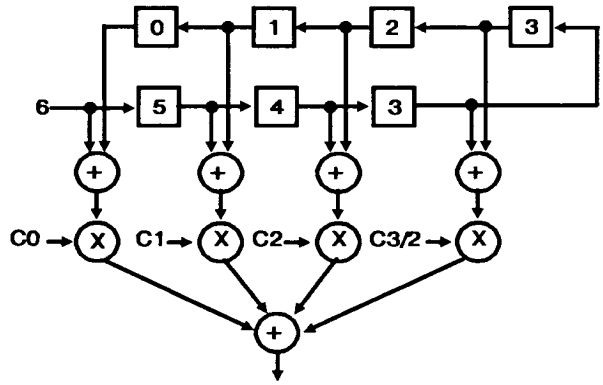


FIGURE 5. DATA/COEFFICIENT ALIGNMENT FOR 7-TAP SYMMETRIC FILTER

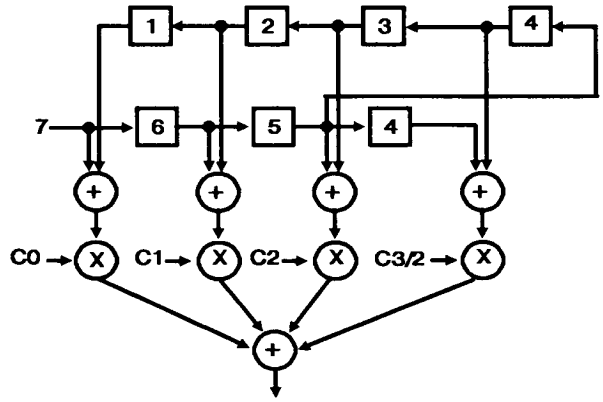
For odd length filters, proper data/coefficient alignment is ensured by routing data entering the last register in the third forward decimation stage to the backward shifting registers. In this configuration, the center coefficient must be scaled by 1/2 to compensate for the summation of the same data sample from both the forward and backward shifting registers.

A. DATA FLOW AS DATA SAMPLE 6 IS CLOCKED INTO THE FEED FORWARD STAGE.



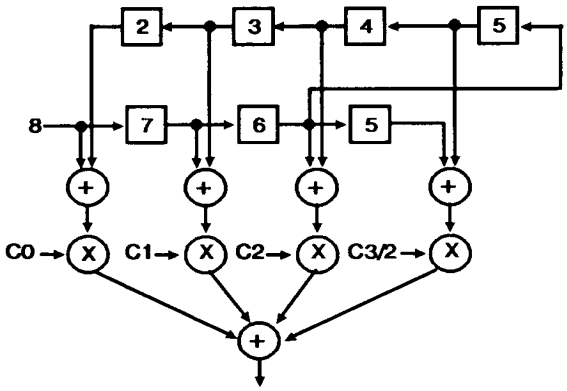
(X6+ X0)C0+ (X5+ X1)C1+ (X4+ X2)C2+ (X3+ X3)C3/2

B. DATA FLOW AS DATA SAMPLE 7 IS CLOCKED INTO THE FEED FORWARD STAGE.



(X7+ X1)C0+ (X6+ X2)C1+ (X5+ X3)C2+ (X4+ X4)C3/2

C. DATA FLOW AS DATA SAMPLE 8 IS CLOCKED INTO THE FEED FORWARD STAGE.



(X8+ X2)C0+ (X7+ X3)C1+ (X6+ X4)C2+ (X5+ X5)C3/2

FIGURE 6. DATA FLOW DIAGRAMS FOR 7-TAP SYMMETRIC FILTER.

In the data flow diagrams of Figure 6, the order of the data samples input in to the filter cell is shown by the numbers in the forward and backward shifting decimation paths. The output of the filter cell is given by the equation at the bottom of the block. The diagram in Figure 6a shows data sample alignment at the pre-adders for the data/coefficient alignment shown in Figure 5.

This dual filter application is configured by writing 110H to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Also, data reversal must be disabled by setting bit 4 of the control register at address 0001H. As in the 8-tap example, only the unique coefficients need to be stored in the Coefficient Bank. These coefficients are stored in the first coefficient set for FIR A by writing C0, C1, C2, and C3 to address 100H, 101H, 102H, and 103H respectively. To write the same filter to the first coefficient set for FIR B, the address sequence would change to 104H, 105H, 106H, and 107H. The control signals TXFR#, FWRD#, RVRS#, ACCEN, SHFTEN#, and CSEL0-4 are controlled as described in Example 1.

Example 3. Asymmetric Filter Example

The FIR cells within the HSP43168 can each calculate 4 asymmetric taps on each clock. Thus, a single FIR cell can implement an 8-tap asymmetric filter if the HSP43168 is clocked at twice the input data rate. Similarly, if the Dual is configured as a single filter, a 16- tap asymmetric filter is realizable.

For this example, the FIR cells are configured as two 8- tap asymmetric filters which are clocked at twice the input data rate. New data is shifted into the forward and backward decimation paths every other CLK by the assertion of SHFTEN#. The filter output is computed by passing data from each decimation path to the multipliers on alternating clocks. Two sets of coefficients are required, one for data on the forward decimation path, and one for data on the reverse path. The filter output is generated by accumulating the multiplier outputs for two CLKs.

The operation of this configuration is better understood by comparing the data/coefficient alignment in Figure 7 with the data flow diagrams in Figure 8. The ALU's have been omitted from the FIR cell diagrams because data is fed to the multipliers directly from the forward and reverse decimation paths. The data samples within the FIR cell are shown by the numbers in the decimation paths.

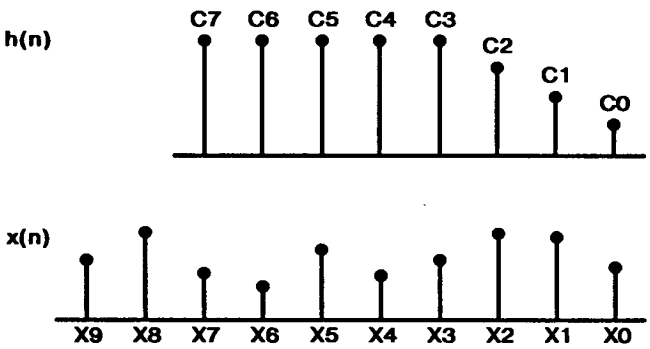
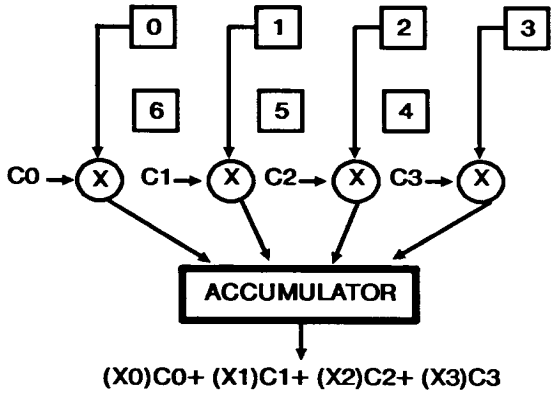
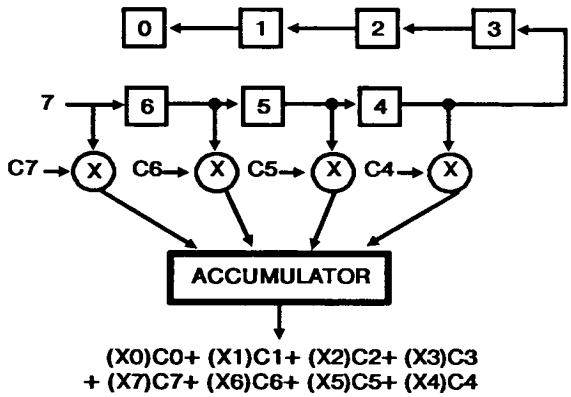


FIGURE 7. DATA/COEFFICIENT ALIGNMENT FOR 8-TAP ASYMMETRIC FILTER

A. DATA SHIFTING DISABLED, BACKWARD SHIFTING DECIMATION REGISTERS FEEDING MULTIPLIERS.



B. SHIFTING OF DATA SAMPLE 7 INTO FIR CELL ENABLED, FORWARD SHIFTING REGISTERS FEEDING MULTIPLIERS.



C. DATA SHIFTING DISABLED, BACKWARD SHIFTING DECIMATION REGISTERS FEEDING MULTIPLIERS.

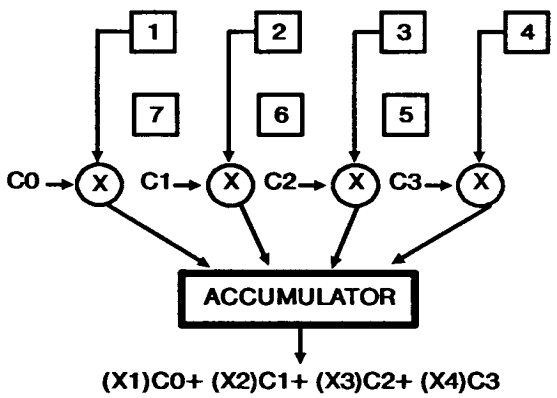


FIGURE 8. DATA FLOW DIAGRAMS FOR 8-TAP ASYMMETRIC FILTER

D. SHIFTING OF DATA SAMPLE 8 INTO FIR CELL ENABLED, FORWARD SHIFTING REGISTERS FEEDING MULTIPLIERS

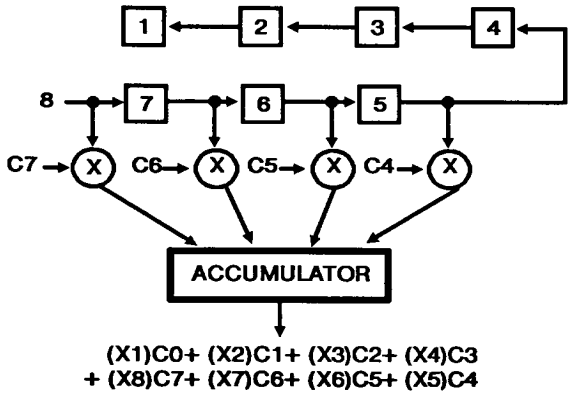


FIGURE 8. DATA FLOW DIAGRAMS FOR 8-TAP ASYMMETRIC FILTER CONTINUED

For this application, each filter cell is configured as an odd length filter by writing 110H to the control register at address 000H. Even though an even tap filter is being implemented, the filter cells must be configured as odd length to ensure proper data flow. Also, the 4th bit at control address 001H must be set to disable data reversal, and TXFR# must be tied low. Since an 8-tap asymmetric filter is being implemented, two sets of coefficients must be stored. These eight coefficients could be loaded into the first two coefficient sets for FIR A by writing C0, C1, C2, C3, C7, C6, C5, and C4 to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, and 10bH respectively.

The sum of products required for this 8-tap filter require dynamic control over FWRD#, RVRS#, ACCEN, and CSEL0-4. The relative timing of these signals is shown in Figure 9.

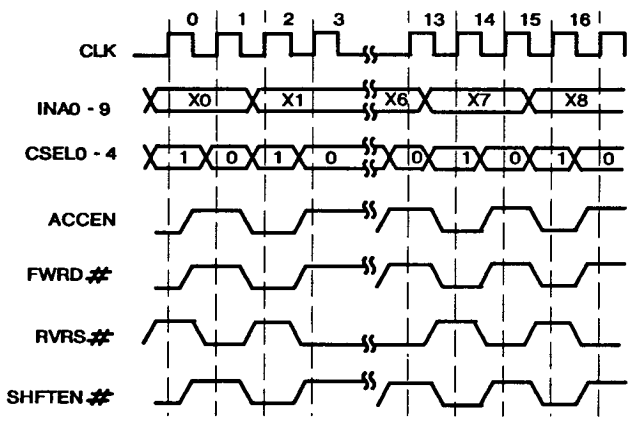


FIGURE 9. CONTROL TIMING FOR 8-TAP ASYMMETRIC FILTER

Example 4. Even-Tap Decimating Filter Example

The HSP43168 supports filtering applications requiring decimation to 16. In these applications the output data rate is reduced by a factor of N. As a result, N clock cycles can be used for the computation of the filter output. For example, each FIR cell can calculate 8 symmetric or 4 asymmetric taps in one clock. If the application requires decimation by two, the filter output can be calculated over two clocks thus boosting the number of taps per FIR cell to 16 symmetric or 8 asymmetric. For this example, each FIR cell is configured as an independent 24-tap decimate x3 filter.

The alignment of data relative to the 24 filter coefficients for a particular output is depicted graphically in Figure 10. As in previous examples, the HSP43168 implements the filtering operation by summing data samples prior to multiplication by the common coefficient. In this example an output is required every third CLK which allows 3 CLK's for computation. On each CLK, one of three sets of coefficients are used to calculate 8 of the filter taps. The block diagrams in Figure 12 show the data flow and accumulator output for the data/coefficient alignment in Figure 10.

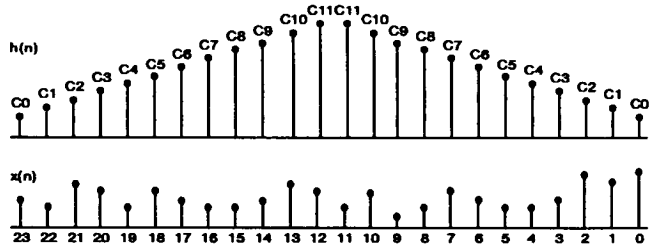
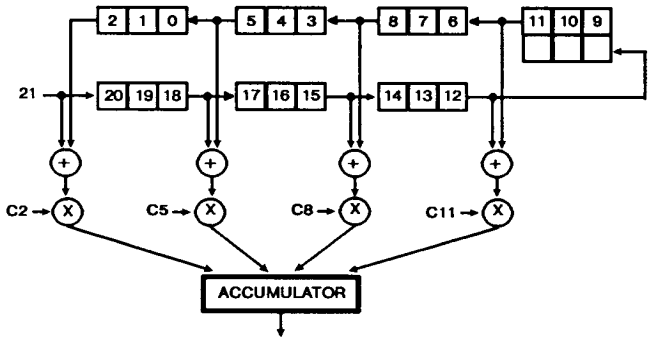


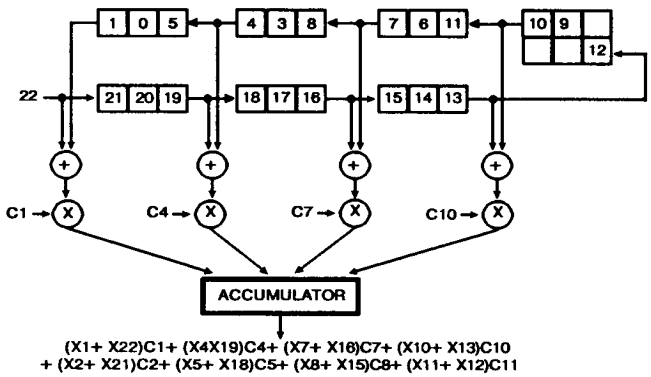
FIGURE 10. DATA/COEFFICIENT ALIGNMENT FOR 24-TAP DECIMATE BY 3 FIR FILTER

Proper data and coefficient alignment is achieved by asserting TXFR# once every three CLK's to switch the LIFO's which are being read and written. This has the effect of feeding blocks of three samples into the backward shifting decimation path which are reversed in sample order. In addition, ACCEN is de-asserted once every three clocks to allow accumulation over three CLK's. The three sets of coefficients required in the calculation of a 24-tap symmetric filter are cycled through using CSEL0-4. The timing relationship between the CSEL0-4, ACCEN, and TXFR# are shown in Figure 12.

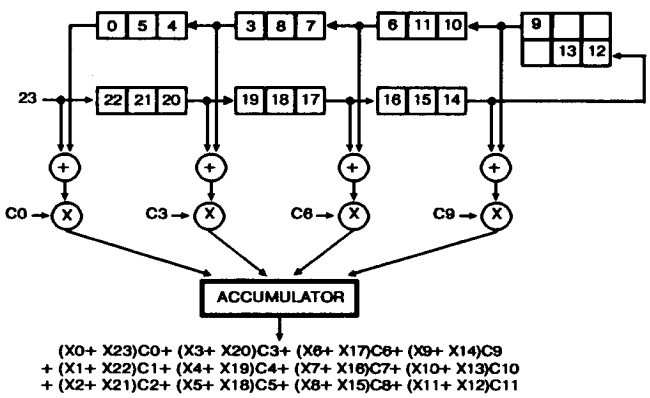
A. COMPUTATIONAL FLOW AS DATA SAMPLE 21 IS CLOCKED INTO THE FEED FORWARD STAGE



B. COMPUTATIONAL FLOW AS DATA SAMPLE 22 IS CLOCKED INTO THE FEED FORWARD STAGE



C. COMPUTATIONAL FLOW AS DATA SAMPLE 23 IS CLOCKED INTO THE FEED FORWARD STAGE



To operate in this mode the Dual is configured by writing 1d2 to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Data reversal must be enabled see (Table 2.0). The 12 unique coefficients for this example are stored as three sets of coefficients for either FIR cell. For FIR A, the coefficients are loaded into the Coefficient Bank by writing C2, C5, C8, C11, C1, C4, C7, C10, C0, C3, C6, and C9 to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, 10bH, 110H, 111H, 112H, and 113H respectively.

D. COMPUTATIONAL FLOW AS DATA SAMPLE 24 IS CLOCKED INTO THE FEED FORWARD STAGE

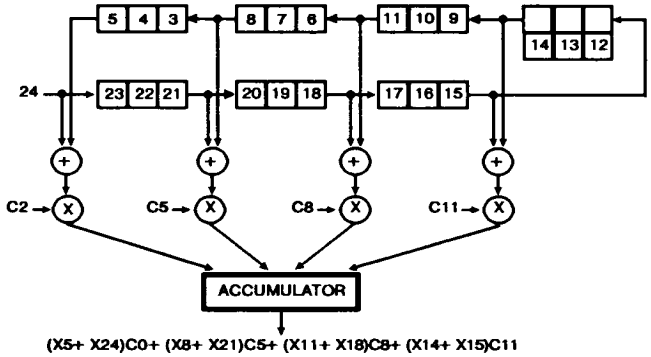


FIGURE 11. DATA FLOW DIAGRAMS FOR 24-TAP DECIMATE BY 3 FIR FILTER

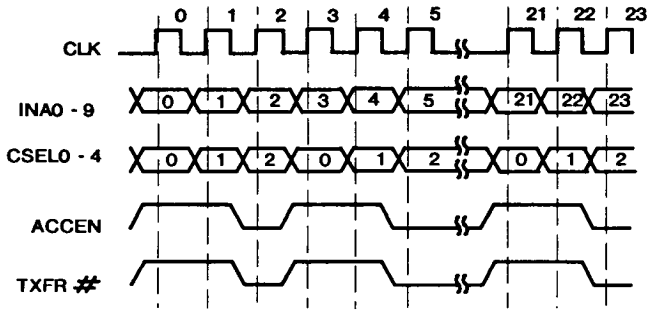


FIGURE 12. CONTROL SIGNAL TIMING FOR 24-TAP DECIMATE X3 FILTER

Example 5. Odd-Tap Decimating Symmetric Filter

This example highlights the use of the HSP43168 as two independent, 23-tap, symmetric, decimate by 3 filters. In this example, the operational differences in the control signals and data reversal structure may be compared to the previously discussed even-tap decimating filter.

As in the 24-tap example, an output is required every third CLK which allows 3 CLK's for computation. On each CLK, one of three sets of coefficients are used to calculate the filter taps. Since this is an odd length filter, the center coefficient must be scaled by 1/2 to compensate for the summation of the same data sample from the forward and backward shifting decimation paths.The block diagrams in Figure 14 show the data flow and accumulator output for the data coefficient alignment in Figure 13.

Proper data and coefficient alignment is achieved by asserting TXFR# once every three CLK's to switch the LIFO's which are being read and written. For odd length filters, data prior to the last register in the forward decimation path is routed to the Feedback Circuitry. As a result, TXFR# should be asserted one cycle prior to the input data samples which align with the center tap. The timing relationship between the CSEL0-5, ACCEN, and TXFR# are shown in Figure 15.

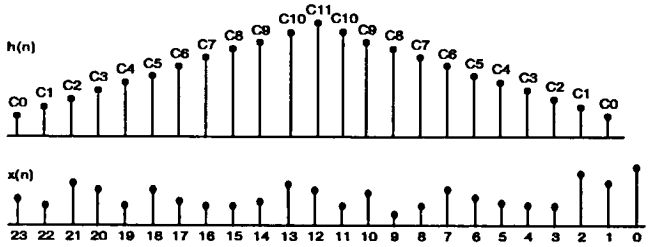
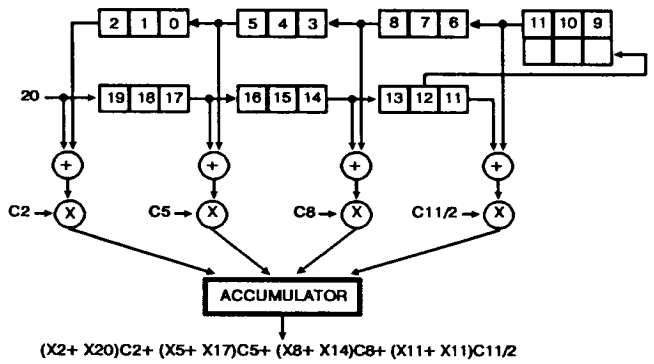
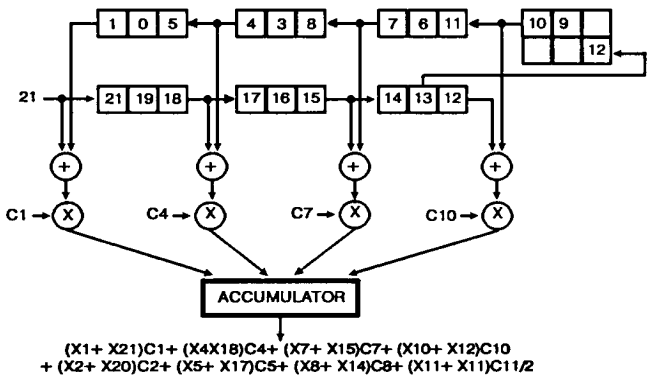


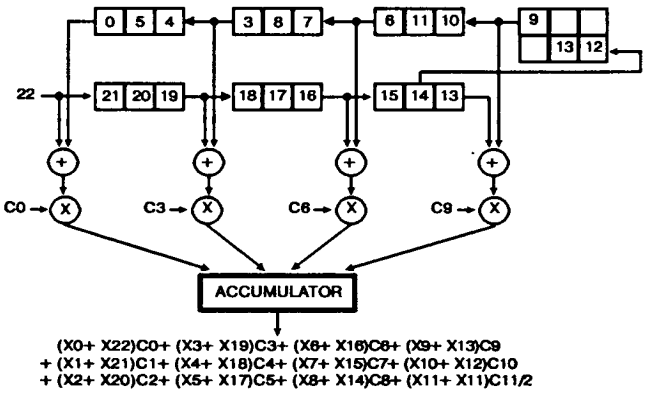
FIGURE 13. DATA/COEFFICIENT ALIGNMENT FOR 23-TAP DECIMATE BY 3 SYMMETRIC FILTER



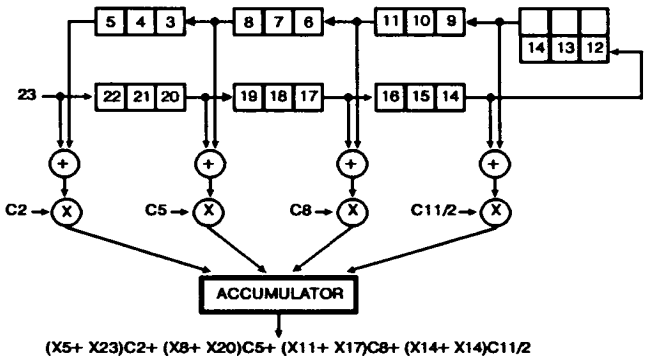
A. COMPUTATIONAL FLOW AS DATA SAMPLE 20 IS CLOCKED INTO THE FEED FORWARD STAGE



B. COMPUTATIONAL FLOW AS DATA SAMPLE 21 IS CLOCKED INTO THE FEED FORWARD STAGE



C. COMPUTATIONAL FLOW AS DATA SAMPLE 22 IS CLOCKED INTO THE FEED FORWARD STAGE



D. COMPUTATIONAL FLOW AS DATA SAMPLE 23 IS CLOCKED INTO THE FEED FORWARD STAGE

FIGURE 14. DATA FLOW DIAGRAMS FOR 23-TAP DECIMATE BY 3 SYMMETRIC FILTER

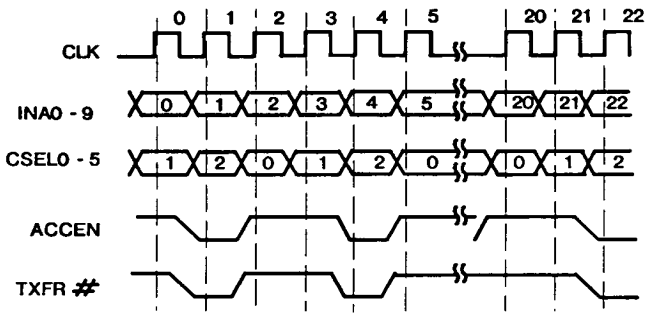


FIGURE 15. CONTROL SIGNAL TIMING FOR 23-TAP SYMMETRIC FILTER

To operate in this mode, the Dual is configured by writing 132H to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Data reversal must be enabled (see Table 2.0). The 12 unique coefficients for this example are stored as three sets of coefficients for either FIR cell. For FIR A, the coefficients are loaded into the Coefficient Bank by writing C2, C5, C8, (C11)/ 2, C1, C4, C7, C10, C0, C3, C6, and C9 to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, 10bH, 110H, 111H, 112H, and 113H respectively.

Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Input, Output Voltage ..... GND -0.5V to V_{CC} +0.5V
Storage Temperature ..... -65°C to +150°C
ESD ..... Class 1
Maximum Package Power Dissipation at +70°C ..... 2.4W (PLCC), 3.1W (PGA)
θ_{jc} ..... 11.0°C/W (PLCC), 7.5°C/W (PGA)
θ_{ja} ..... 33.6°C/W (PLCC), 33.5°C/W (PGA)
Gate Count 32529
Junction Temperature ..... +175°C (PGA), +150°C (PLCC)
Lead Temperature (Soldering 10s) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range, Commercial ..... 5V ± 5%
Operating Temperature Range
Commercial ..... 0°C to +70°C

D.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
I_{CCOP}	Power Supply Current	-	363	mA	V_{CC} = Max CLK Frequency 33MHz Note 2, Note 3
I_{CCSB}	Standby Power Supply Current	-	500	µA	V_{CC} = Max, Outputs Not Loaded
I_I	Input Leakage Current	-10	10	µA	V_{CC} = Max, Input = 0V or V_{CC}
I_O	Output Leakage Current	-10	10	µA	V_{CC} = Max, Input = 0V or V_{CC}
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = Max
V_{IL}	Logical Zero Input Voltage	-	0.8	V	V_{CC} = Min
V_{OH}	Logical One Output Voltage	2.6	-	V	I_{OH} = -400θA, V_{CC} = Min
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = 2mA, V_{CC} = Min
V_{IHC}	Clock Input High	3.0	-	V	V_{CC} = Max
V_{ILC}	Clock input Low	-	0.8	V	V_{CC} = Min
C_{IN}	Input Capacitance	-	12	pF	CLK Frequency 1MHz All measurements referenced
C_{OUT}	Output Capacitance	-	12	pF	to GND. T_A = +25°C, Note 1

NOTES:

1. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.
2. Power Supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 11mA/MHz.
3. Output load per test load circuit and C_L = 40pF.

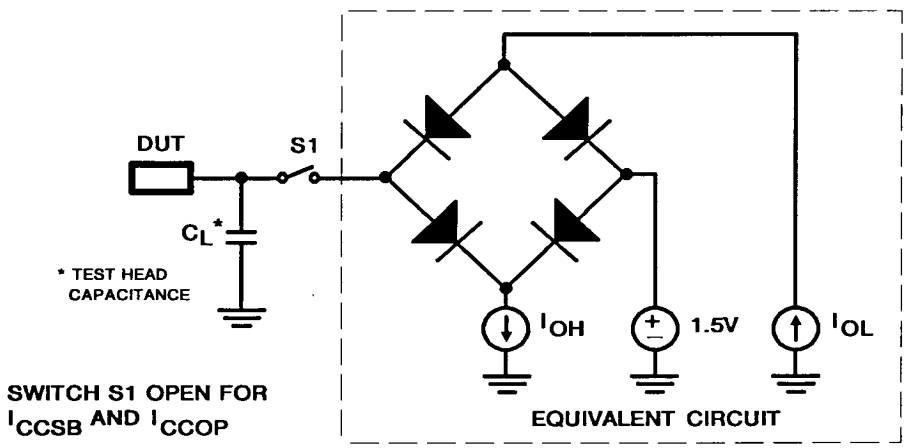
A.C. Electrical Specifications (Note 1)

SYMBOL	PARAMETER	33MHz		45MHz		COMMENTS
		MIN	MAX	MIN	MAX	
T_{CP}	CLK Period	30	-	22	-	ns
T_{CH}	CLK High	12	-	8	-	ns
T_{CL}	CLK Low	12	-	8	-	ns
T_{WP}	WR# Period	30	-	22	-	ns
T_{WH}	WR# High	12	-	10	-	ns
T_{WL}	WR# Low	12	-	10	-	ns
T_{AWS}	Set-up Time A0-8 to WR# Going Low	10	-	8	-	ns
TAWH	Hold Time A0-8 from WR# Going High	0	-	0	-	ns
TCWS	Set-up Time CIN0-9 to WR# Going High	12	-	10	-	ns
TCWH	Hold Time CIN0-9 from WR# Going High	1	-	1	-	ns
TWLCL	Set-up Time WR# Low to CLK Low	5	-	3	-	ns, Note 2
TCVCL	Set-up Time CIN0-9 to CLK Low	7	-	7	-	ns, Note 2
TECS	Set-up Time CSEL0-5, SHFTEN#, FWRD#, RVRS#, TXFR#, MUX0-1 to CLK Going High	15	-	12	-	ns
TECH	Hold Time CSEL0-5, SHFTEN#, FWRD#, RVRS#, TXFR#, MUX0-1 to CLK Going High	0	-	0	-	ns
TDO	CLK to Output Delay OUT0-27	-	14	-	12	ns
TOE	Output Enable Time	-	12	-	12	ns
TOD	Output Disable Time	-	12	-	12	ns, Note 3
TRF	Output Rise, Fall Time	-	6	-	6	ns, Note 3

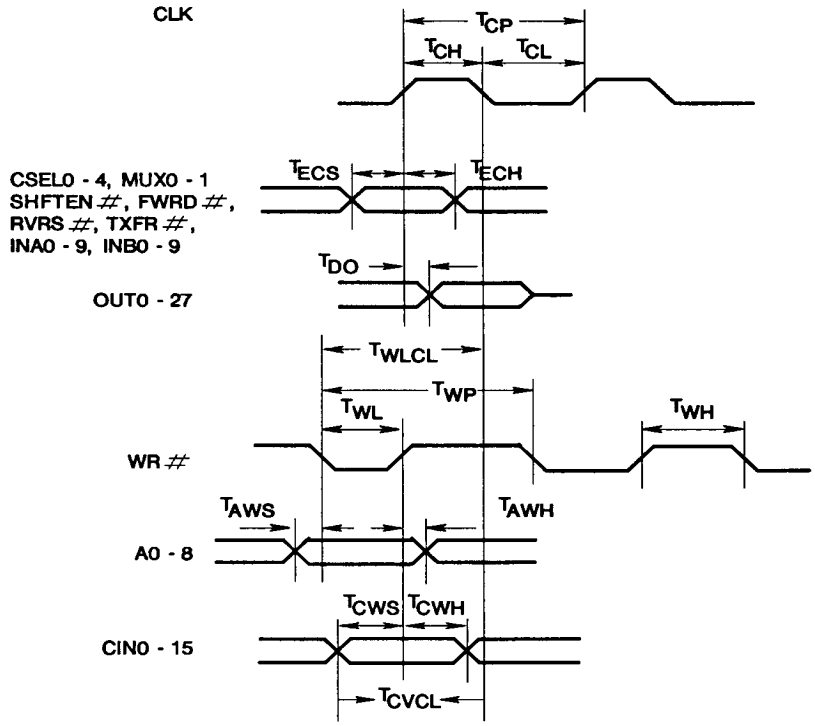
NOTES:

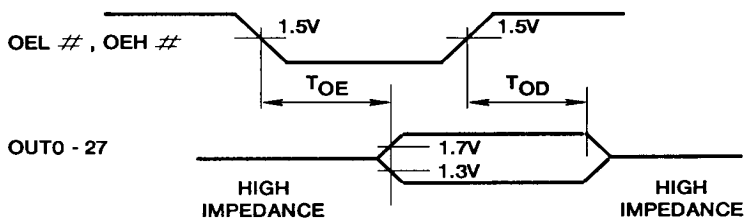
1. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -400µA. Input reference level CLK = 2.0V. Input reference level for all other inputs is 1.5V. Input rise and fall times 5ns max. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V, V_{ILC} = 0V.
2. Set-up time requirement for loading of data on CIN0-9 to guaranteed recognition on the following clock.
3. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

A.C. Test Load Circuit

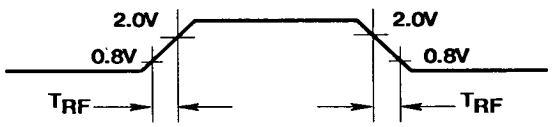


Waveforms



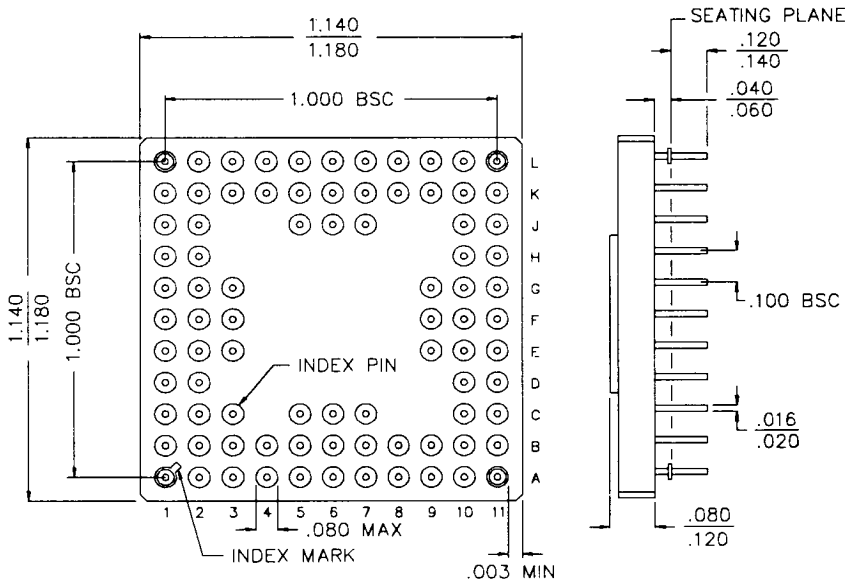


OUTPUT ENABLE, DISABLE TIMING

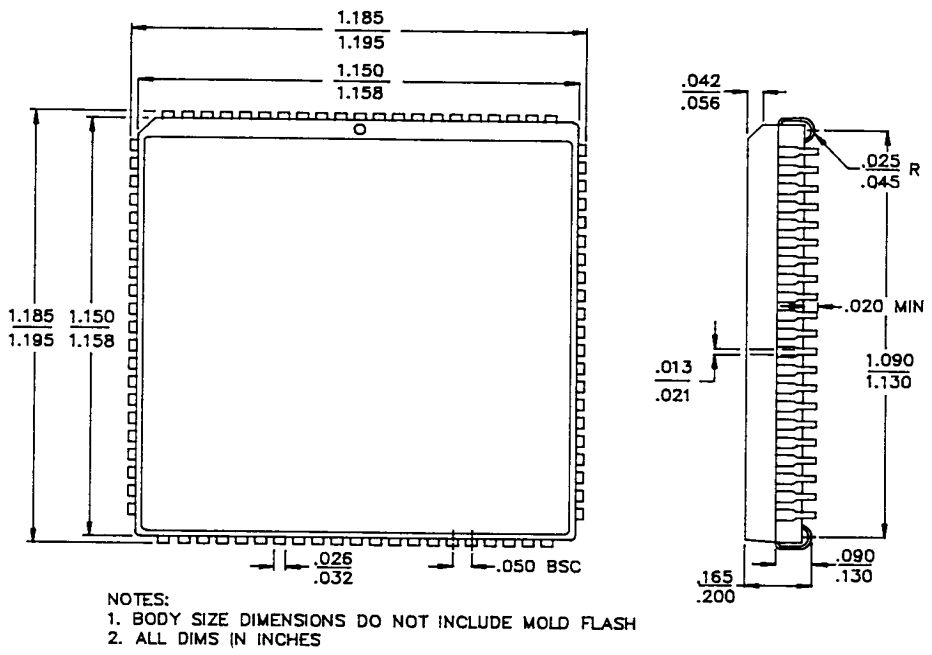


OUTPUT RISE AND FALL TIMES

Packaging



85 PIN GRID ARRAY (PGA)



NOTES:
1. BODY SIZE DIMENSIONS DO NOT INCLUDE MOLD FLASH
2. ALL DIMS IN INCHES

84 PIN PLASTIC LEADED CHIP CARRIER (PLCC)

Ordering Information

HSP43168	J	C	-33
DEVICE	PACKAGE	TEMPERATURE RANGE	PERFORMANCE GRADE
	J: PLCC G: PGA	C: Commercial 0°C to +70°C	33: Commercial 33MHz 45: Commercial 45MHz

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