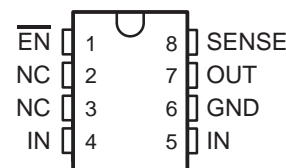


TPS7415, TPS7418, TPS7425, TPS7430, TPS7433 FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR 200-mA LOW-DROPOUT VOLTAGE REGULATORS

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- Fast Transient Response Using Small Output Capacitor (10 μ F)
- 200-mA Low-Dropout Voltage Regulator
- Available in 1.5-V, 1.8-V, 2.5-V, 3-V and 3.3-V
- Dropout Voltage Down to 170 mV at 200 mA (TPS7433)
- 3% Tolerance Over Specified Conditions
- 8-Pin SOIC Package
- Thermal Shutdown Protection

D PACKAGE
(TOP VIEW)

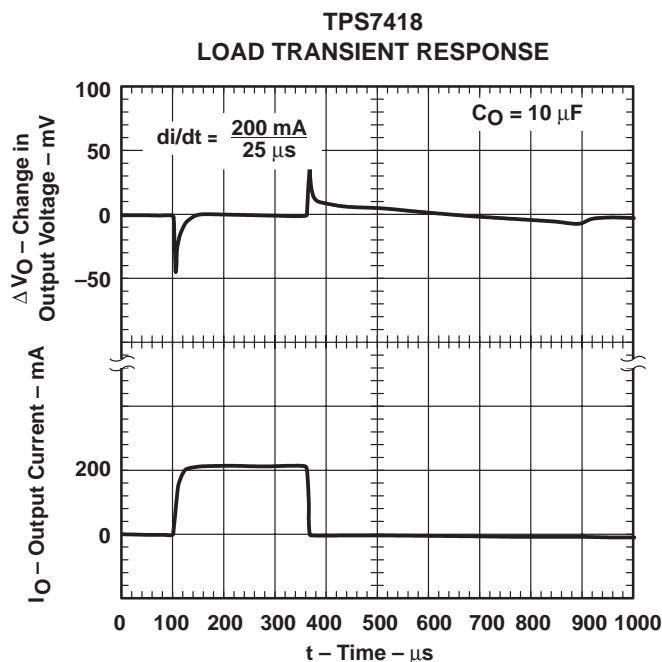
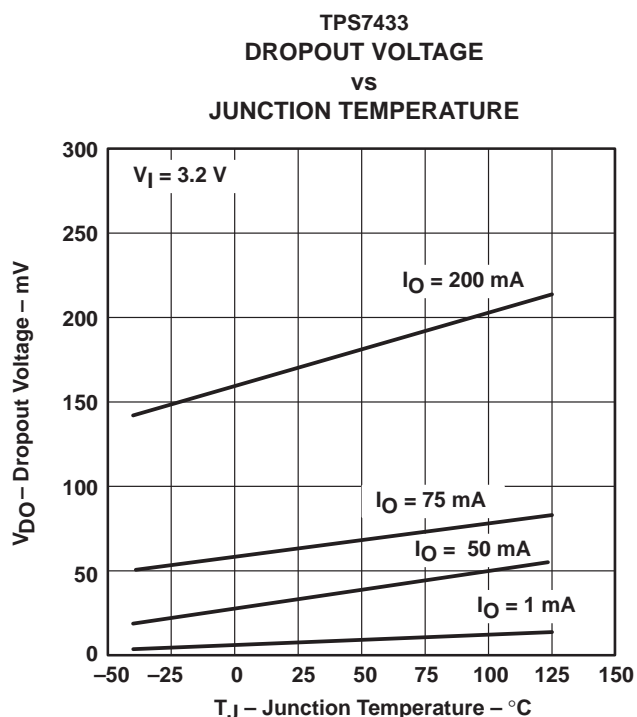
NC – No internal connection

description

This device is designed to have a fast transient response and be stable with 1- μ F capacitors. This combination provides high performance at a reasonable cost.

Because the PMOS device behaves as a low-value resistor, the dropout voltage is very low (typically 170 mV at an output current of 200-mA for the TPS7433). This LDO family also features a sleep mode; applying a TTL high signal to $\overline{\text{EN}}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1 μ A at $T_J = 25^\circ\text{C}$.

The TPS74xx is offered in 1.5-V, 1.8-V, 2.5-V, 3-V, and 3.3-V. Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TPS74xx family is available in 8 pin SOIC package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TPS7415, TPS7418, TPS7425, TPS7430, TPS7433

FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR

200-mA LOW-DROPOUT VOLTAGE REGULATORS

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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
$\overline{\text{EN}}$	1	I	Enable input
GND	6		Regulator ground
IN	4, 5	I	Input voltage
NC	2, 3		Not connected
OUT	7	O	Regulated output voltage
SENSE	8	I	Sense

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Input voltage range [‡] , V_I	–0.3 V to 8 V
Voltage range at $\overline{\text{EN}}$	–0.3 V to $V_I + 0.3$ V
Peak output current	Internally limited
Continuous total power dissipation	See dissipation rating tables
Operating virtual junction temperature range, T_J	–40°C to 125°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All voltage values are with respect to network terminal ground.

DISSIPATION RATING TABLE 1 – FREE-AIR TEMPERATURES

PACKAGE	AIR FLOW (CFM)	$T_A < 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
D	0	568 mW	5.68 mW/°C	312 mW	227 mW
	250	904 mW	9.04 mW/°C	497 mW	361 mW

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I [§]	2.5	7	V
Output current, I_O (see Note 1)	0	200	mA
Operating virtual junction temperature, T_J (see Note 1)	–40	125	°C

[§] To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(\text{min})} = V_{O(\text{max})} + V_{\text{DO}(\text{max load})}$.

NOTE 1: Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

TPS7415, TPS7418, TPS7425, TPS7430, TPS7433

FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR

200-mA LOW-DROPOUT VOLTAGE REGULATORS

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electrical characteristics over recommended operating free-air temperature range,
 $V_i = V_{O(\text{typ})} + 1 \text{ V}$, $I_O = 1 \text{ mA}$, $\overline{\text{EN}} = 0 \text{ V}$, $C_O = 1 \mu\text{F}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage (10 μA to 200 mA load) (see Note 2)	TPS7415	2.5 V < V _I < 7 V		T _J = 25°C		1.5		V
				T _J = −40°C to 125°C	1.455	1.545		
	TPS7418	2.8 V < V _I < 7 V		T _J = 25°C		1.8		
				T _J = −40°C to 125°C	1.746	1.854		
	TPS7425	3.5 V < V _I < 7 V		T _J = 25°C		2.5		
				T _J = −40°C to 125°C	2.425	2.575		
	TPS7430	4.0 V < V _I < 7 V		T _J = 25°C		3.0		
				T _J = −40°C to 125°C	2.910	3.090		
TPS7433	4.3 V < V _I < 7 V		T _J = 25°C		3.3			
			T _J = −40°C to 125°C	3.201	3.399			
Quiescent current (GND current) (See Note 2)		I _O = 1 mA, EN = 0 V		T _J = 25°C		80		μA
				T _J = −40°C to 125°C		115		
		I _O = 100 mA, EN = 0 V		T _J = 25°C		550		μA
				T _J = −40°C to 125°C		850		
		I _O = 200 mA, EN = 0 V		T _J = 25°C		1300		μA
				T _J = −40°C to 125°C		1500		
Output voltage line regulation (ΔV _O /V _O) (see Notes 2 and 3)		V _O + 1 V < V _I ≤ 7 V, T _J = 25°C			0.06		%/V	
Load regulation					5		mV	
Output noise voltage		BW = 300 Hz to 50 kHz, C _O = 1 μF, T _J = 25°C			190		μVrms	
Output current Limit		V _O = 0 V			500	750	mA	
Thermal shutdown junction temperature					150		°C	
Standby current		2.5 V < V _I < 7 V, T _J = 25°C	EN = V _I ,			1	μA	
		2.5 V < V _I < 7 V, T _J = −40°C to 125°C	EN = V _I ,			3	μA	
High level enable input voltage					2		V	
Low level enable input voltage						0.7	V	
Input current (EN)		EN = 0 V			−1	1	μA	
		EN = V _I			−1	1		
Power supply ripple rejection (see Note 2)		f = 100 Hz, T _J = 25°C	C _O = 1 μF,		55		dB	
Dropout voltage (see Note 4)	TPS7430	I _O = 200 mA,	T _J = 25°C		180		mV	
		I _O = 200 mA,	T _J = −40°C to 125°C		350			
	TPS7433	I _O = 200 mA,	T _J = 25°C		170			
		I _O = 200 mA,	T _J = −40°C to 125°C		315			

NOTES: 2. Minimum I_N operating voltage is 2.5 V or $V_{O(\text{typ})} + 1 \text{ V}$, whichever is greater. Maximum I_N voltage 7 V.

3. If $V_O = 1.5 \text{ V}$ then $V_{\text{imax}} = 7 \text{ V}$, $V_{\text{imin}} = 2.5 \text{ V}$:

4. I_N voltage equals $V_O(\text{Typ}) - 100 \text{ mV}$; TPS7430 and TPS7433 dropout limited by input voltage range limitations (i.e., TPS7430 input voltage needs to drop to 2.9 V for purpose of this test).

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - 2.5 \text{ V})}{100} \times 1000$$

If $V_O \geq 2.5 \text{ V}$ then $V_{\text{imax}} = 7 \text{ V}$, $V_{\text{imin}} = V_O + 1 \text{ V}$:

$$\text{Line Reg. (mV)} = (\%/V) \times \frac{V_O(V_{\text{imax}} - (V_O + 1 \text{ V}))}{100} \times 1000$$



TPS7415, TPS7418, TPS7425, TPS7430, TPS7433

FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR

200-mA LOW-DROPOUT VOLTAGE REGULATORS

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Table of Graphs

			FIGURE
V_O	Output voltage	vs Output current	2, 3, 4
		vs Junction temperature	5, 6
	Ground current	vs Junction temperature	7, 8
	Power supply ripple rejection	vs Frequency	12
	Output noise	vs Frequency	9
Z_O	Output impedance	vs Frequency	10
V_{DO}	Dropout voltage	vs Junction temperature	11
	Line transient response		13, 15
	Load transient response		14, 16
	Output voltage	vs Time	17
	(Stability) Equivalent series resistance (ESR)	vs Output current	19

TYPICAL CHARACTERISTICS

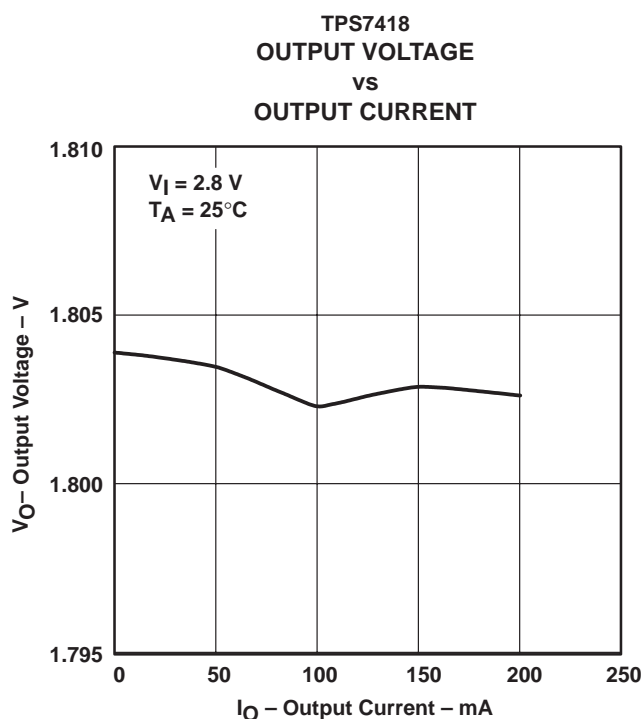


Figure 2

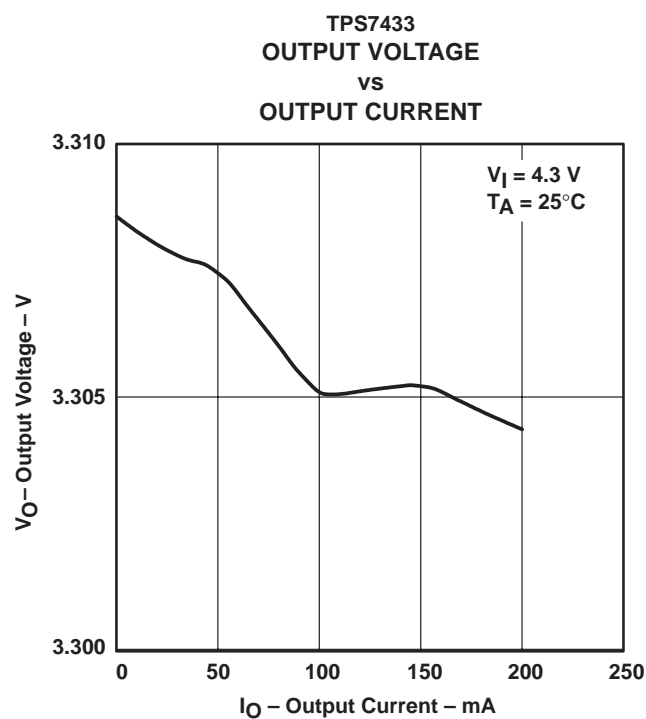


Figure 3

TPS7415, TPS7418, TPS7425, TPS7430, TPS7433

FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR

200-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

TPS7425
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

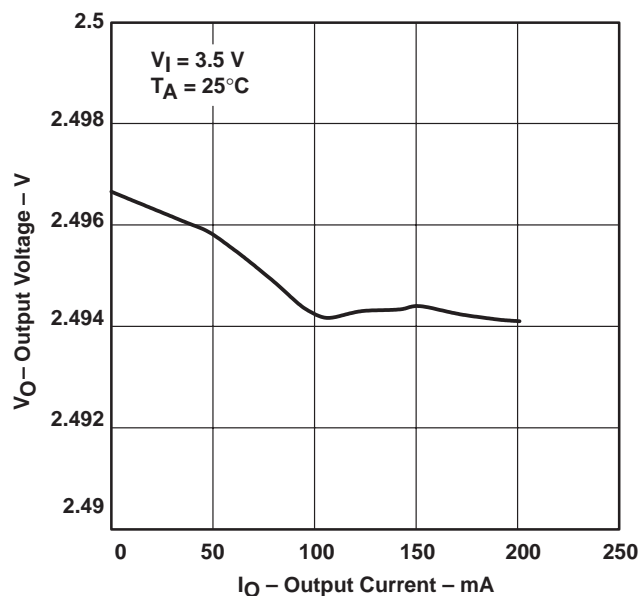


Figure 4

TPS7418
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

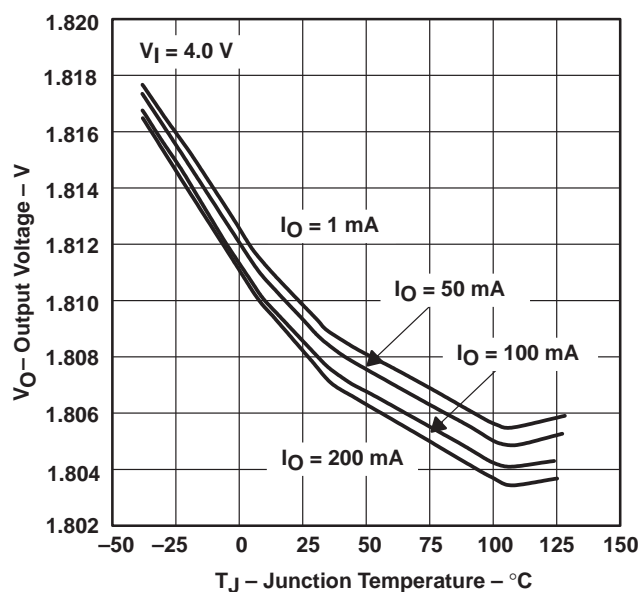


Figure 5

TPS7433
OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

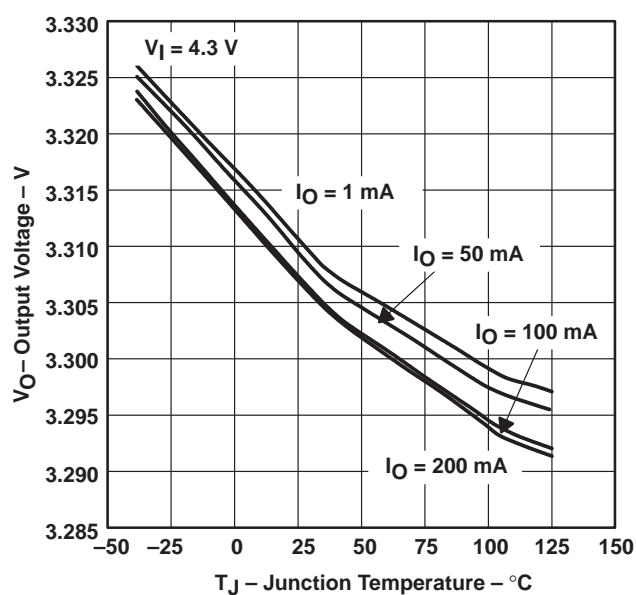


Figure 6

TPS7418
GROUND CURRENT
vs
JUNCTION TEMPERATURE

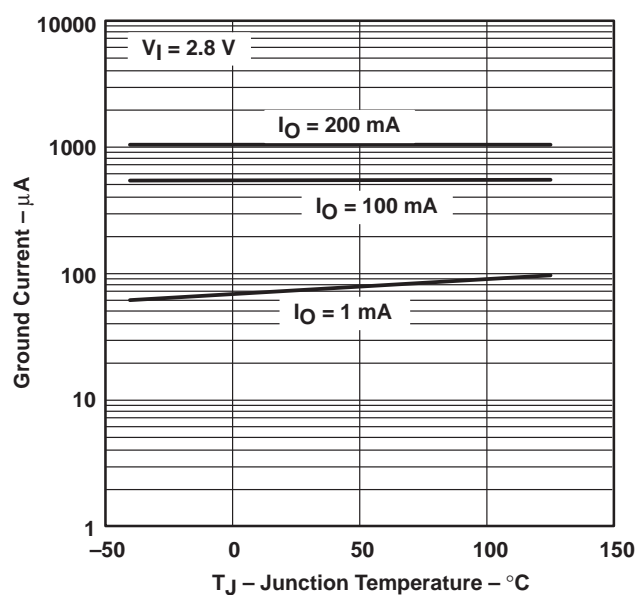


Figure 7

TPS7415, TPS7418, TPS7425, TPS7430, TPS7433 FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR 200-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

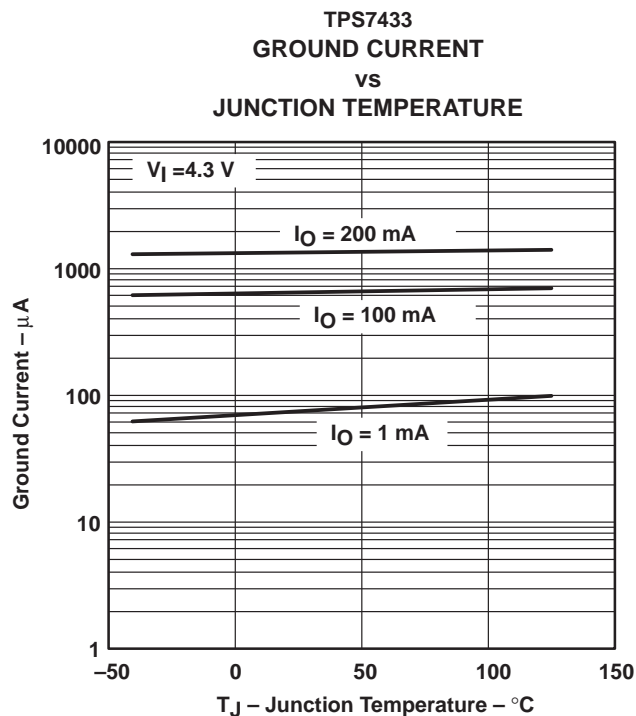


Figure 8

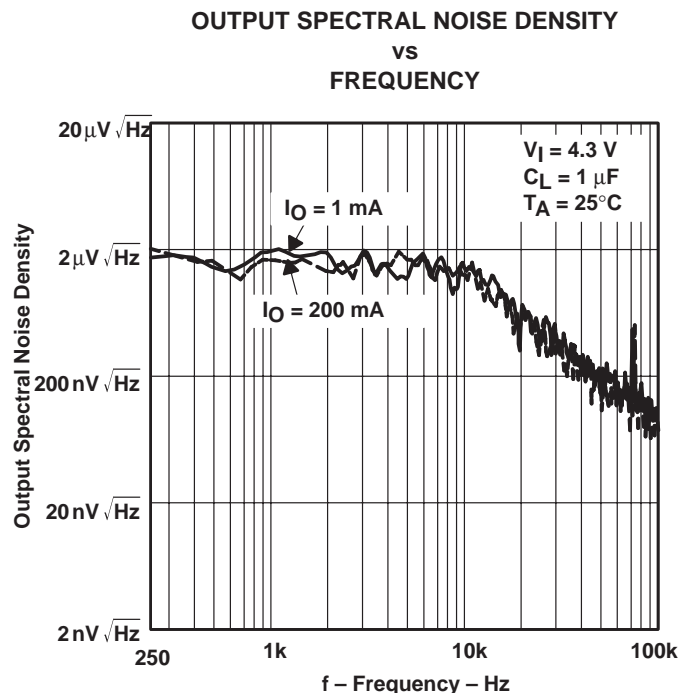


Figure 9

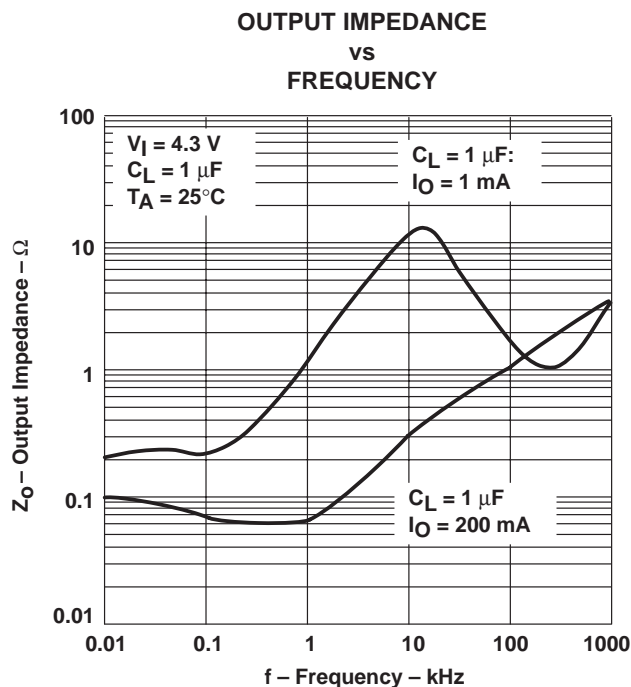


Figure 10

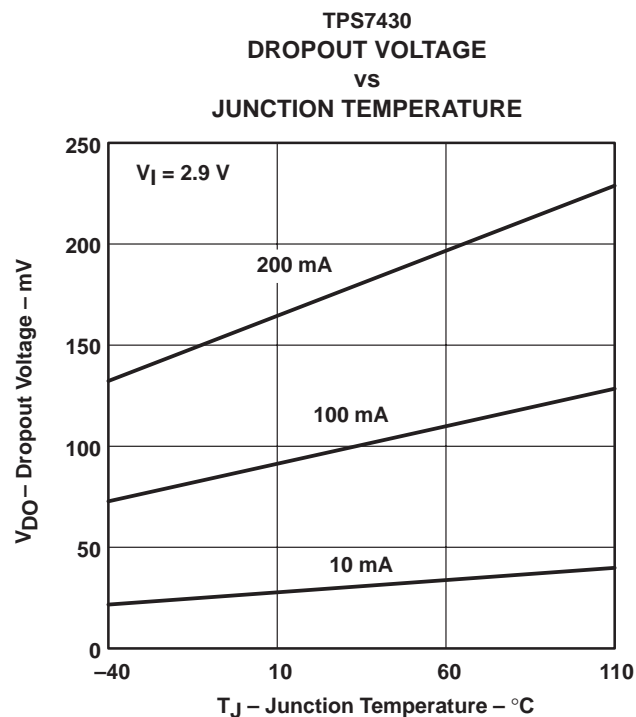


Figure 11

TPS7415, TPS7418, TPS7425, TPS7430, TPS7433

FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR

200-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

RIPPLE REJECTION vs FREQUENCY

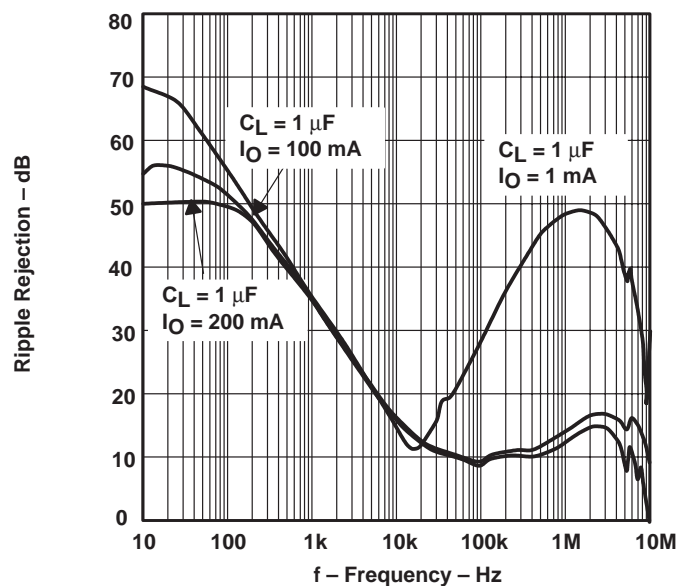


Figure 12

TPS7418 LINE TRANSIENT RESPONSE

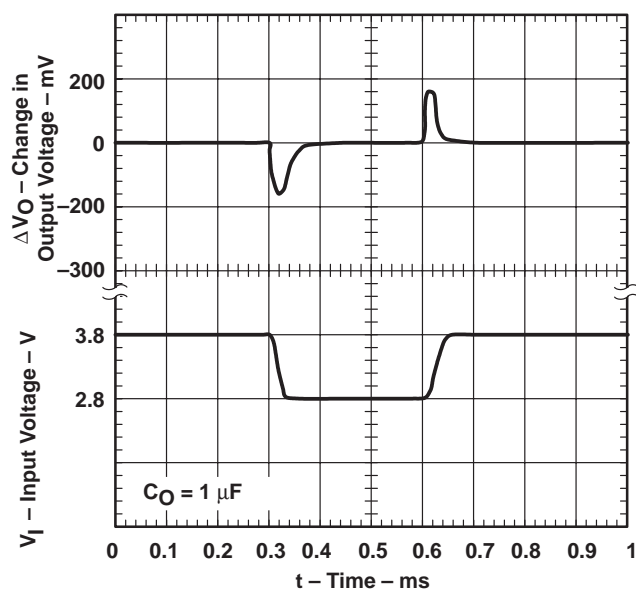


Figure 13

TPS7418 LOAD TRANSIENT RESPONSE

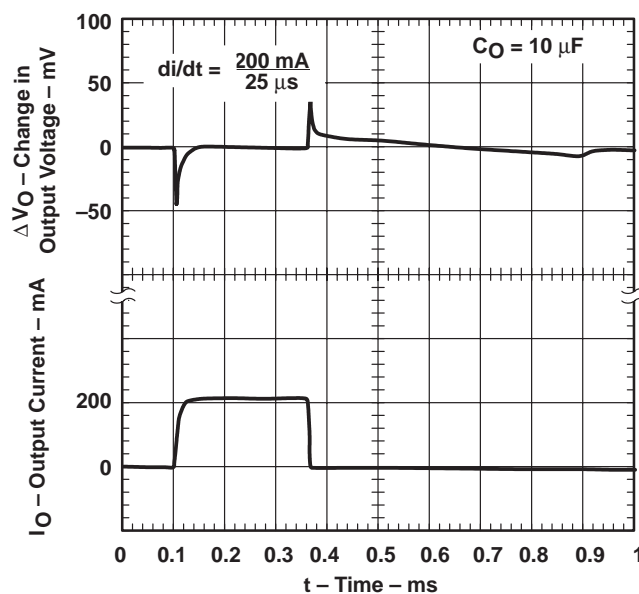


Figure 14

TPS7415, TPS7418, TPS7425, TPS7430, TPS7433 FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR 200-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

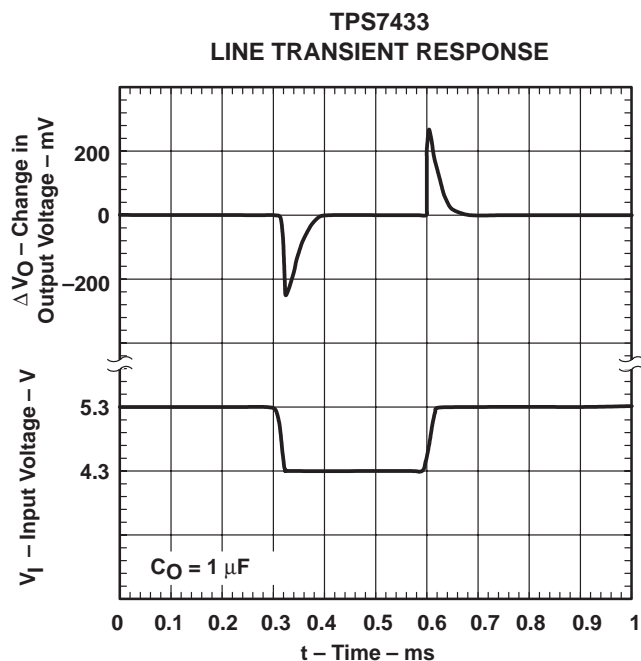


Figure 15

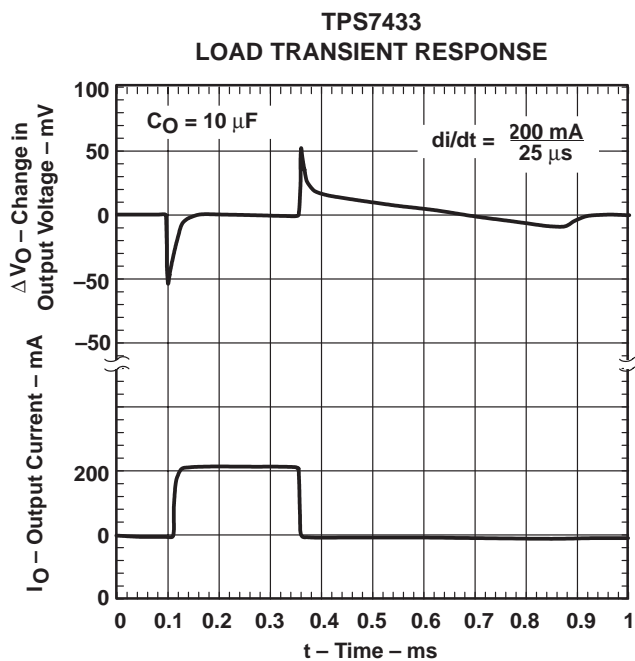


Figure 16

TPS7433 OUTPUT VOLTAGE vs TIME (AT STARTUP)

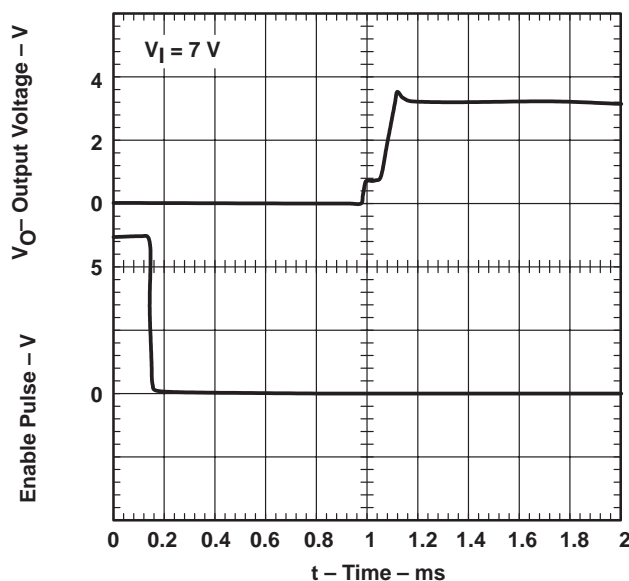


Figure 17

TPS7415, TPS7418, TPS7425, TPS7430, TPS7433

FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR

200-mA LOW-DROPOUT VOLTAGE REGULATORS

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TYPICAL CHARACTERISTICS

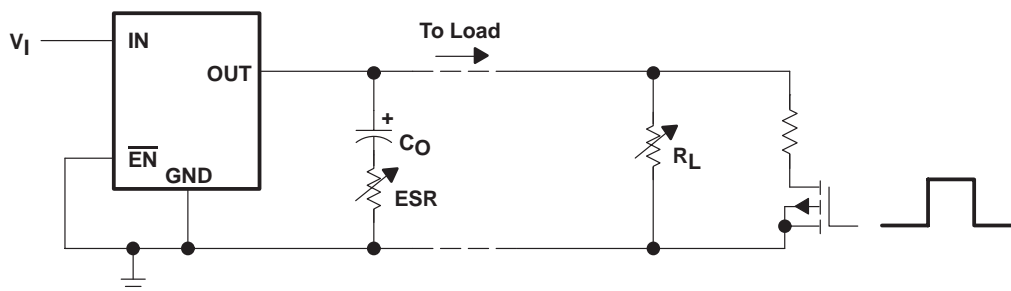


Figure 18. Test Circuit for Typical Regions of Stability (Figure 19)

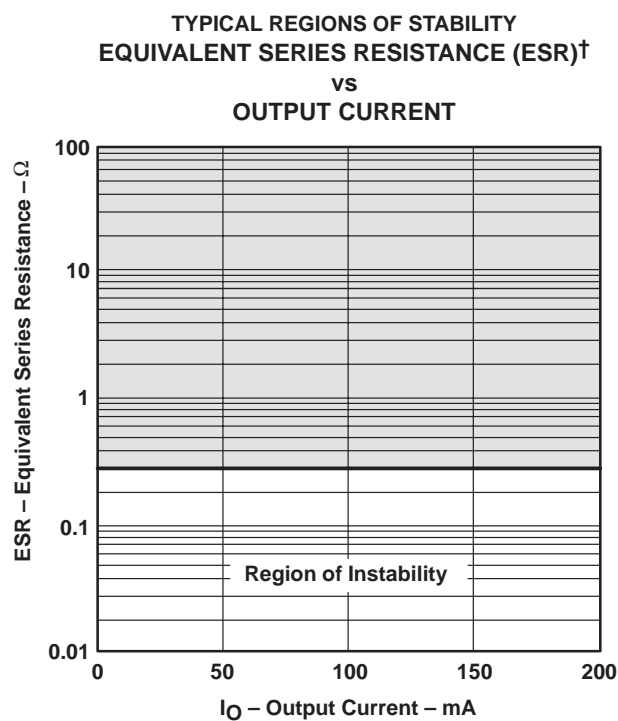


Figure 19

[†] ESR refers to the total series resistance, including the ESR of the capacitor, any series resistance added externally, and PWB trace resistance to C_O .

TPS7415, TPS7418, TPS7425, TPS7430, TPS7433 FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR 200-mA LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

The TPS74xx family includes five voltage regulators (1.5 V, 1.8 V, 2.5 V, 3 V, and 3.3 V).

minimum load requirements

The TPS74xx family is stable even at zero load; no minimum load is required for operation.

SENSE terminal connection

The SENSE terminal must be connected to the regulator output for proper functioning of the regulator. Normally, this connection should be as short as possible; however, the connection can be made near a critical circuit (remote sense) to improve performance at that point. Internally, SENSE connects to a high-impedance wide-bandwidth amplifier through a resistor-divider network and noise pickup feeds through to the regulator output. Routing the SENSE connection to minimize/avoid noise pickup is essential. Adding an RC network between SENSE and OUT to filter noise is not recommended because it can cause the regulator to oscillate.

external capacitor requirements

An input capacitor is not usually required; however, a ceramic bypass capacitor (1 μF or larger) improves load transient response and noise rejection if the TPS74xx is located more than a few inches from the power supply. A higher-capacitance electrolytic capacitor may be necessary if large (hundreds of milliamps) load transients with fast rise times are anticipated.

Like all low dropout regulators, the TPS74xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance value is 1 μF and the ESR (equivalent series resistance) must be at least 300 m Ω . Solid tantalum electrolytic and aluminum electrolytic are all suitable, provided they meet the requirements described previously.

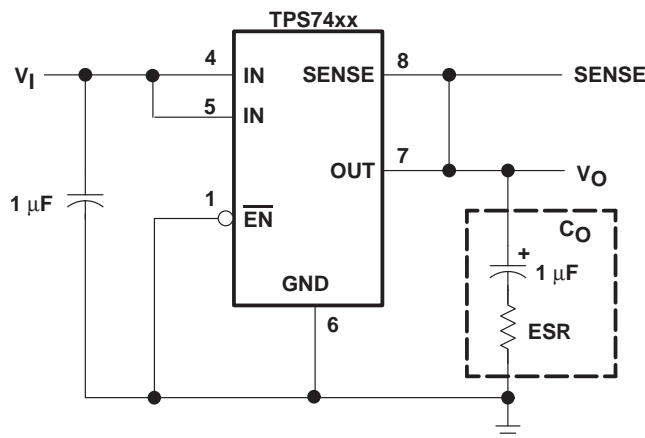


Figure 20. Typical Application Circuit

regulator protection

The TPS74xx PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

TPS7415, TPS7418, TPS7425, TPS7430, TPS7433

FAST-TRANSIENT-RESPONSE USING SMALL OUTPUT CAPACITOR

200-mA LOW-DROPOUT VOLTAGE REGULATORS

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APPLICATION INFORMATION

regulator protection (continued)

The TPS74xx also features internal current limiting and thermal protection. During normal operation, the TPS74xx limits output current to approximately 500 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 150°C(typ), thermal-protection circuitry shuts it down. Once the device has cooled below 130°C (typ), regulator operation resumes.

power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where

T_{Jmax} is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 172°C/W for the 8-terminal SOIC.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7415D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7415	Samples
TPS7415DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7415	Samples
TPS7415DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7415	Samples
TPS7418D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7418	Samples
TPS7418DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7418	Samples
TPS7425D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7425	Samples
TPS7425DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7425	Samples
TPS7430D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7430	
TPS7433D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7433	Samples
TPS7433DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7433	Samples
TPS7433DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7433	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7415DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7433DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7415DR	SOIC	D	8	2500	367.0	367.0	38.0
TPS7433DR	SOIC	D	8	2500	367.0	367.0	38.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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