OVERVOLTAGE AND OVERCURRENT PROTECTION IC AND Li+ CHARGER FRONT-END PROTECTION IC

FEATURES

- **Provides Protection for Three Variables:**
  - **Input Overvoltage**
  - **Input Overcurrent (User-Programmable)**
  - **Battery Overvoltage**
- **30V Maximum Input Voltage**
- **Supports up to 1.5A Input Current**
- **High Immunity Against False Triggering Due to Voltage Spikes**
- **Robust Against False Triggering Due to Current Transients**
- **Thermal Shutdown**
- **Status Indication – Fault Condition**
- **Available in Space-Saving Small 8 Lead 2×2 SON and 12 Lead 4x3 SON Packages**

APPLICATIONS

- **Smart Phones**
- **PDAs**
- **MP3 Players**
- **Low-Power Handheld Devices**
- **Bluetooth Headsets**

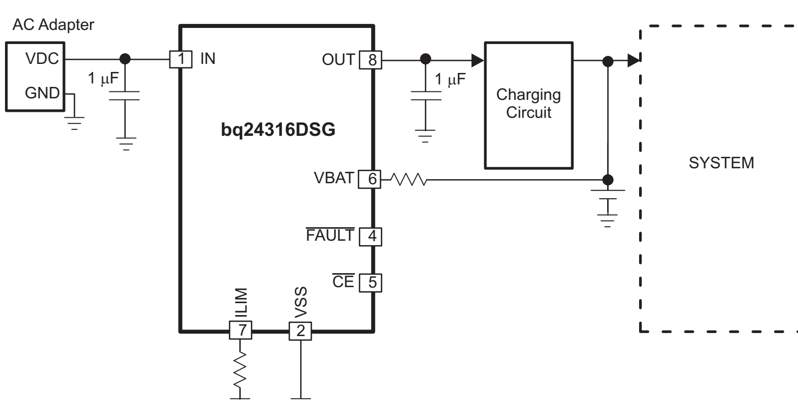
PRODUCT PREVIEW

DESCRIPTION

The bq24314 and bq24316 are highly integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the IC also monitors its own die temperature and switches off if it becomes too hot. The input overcurrent threshold is user-programmable.

The IC can be controlled by a processor and also provides status information about fault conditions to the host.

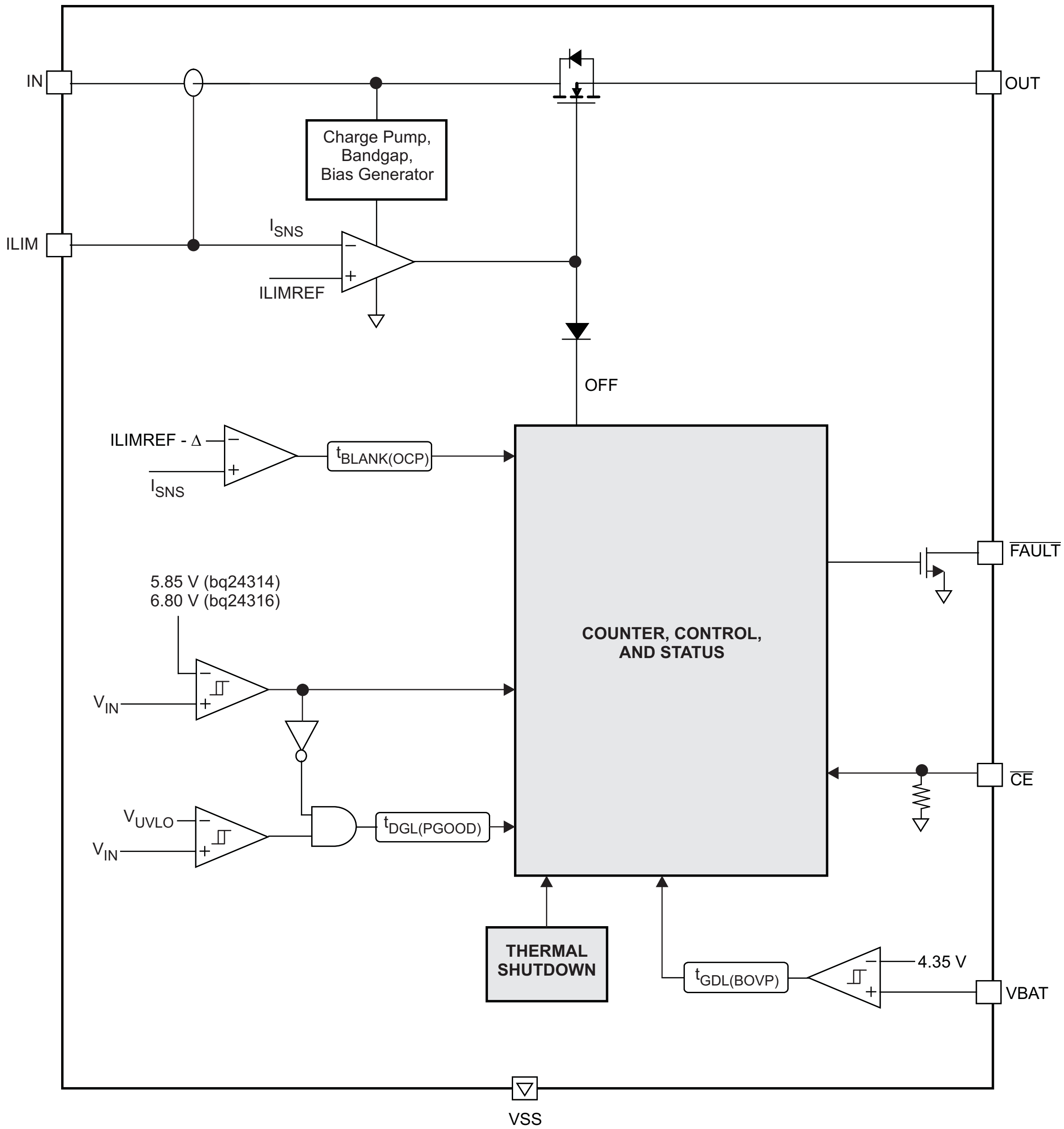
APPLICATION SCHEMATIC



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SIMPLIFIED BLOCK DIAGRAM

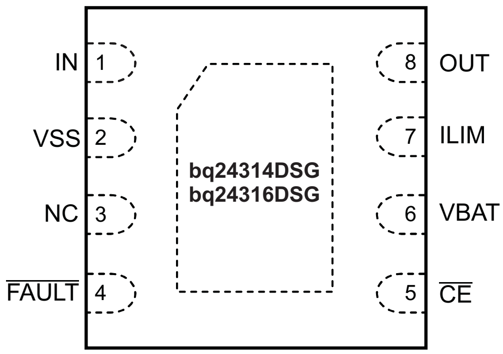


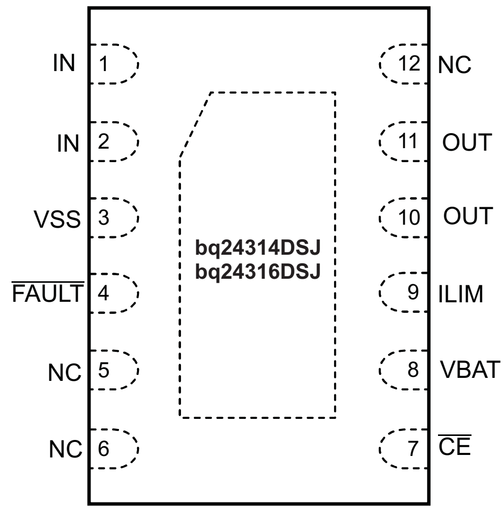
TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	DSJ	DSG		
IN	1, 2	1	I	Input power, connect to external DC supply. Connect external 1μF capacitor (minimum) to VSS. For the 12 pin (DSJ-suffix) device, ensure that pins 1 and 2 are connected together on the PCB at the device.
OUT	10, 11	8	O	Output terminal to the charging system. Connect external 1μF capacitor (minimum) to VSS.
VBAT	8	6	I	Battery voltage sense input. Connect to pack positive terminal through a resistor.

PRODUCT PREVIEW

TERMINAL			I/O	DESCRIPTION
NAME	DSJ	DSG		
ILIM	9	7	I/O	Input overcurrent threshold programming. Connect a resistor to VSS to set the overcurrent threshold.
$\overline{\text{CE}}$	7	5	I	Chip enable input. Active low. When $\overline{\text{CE}}$ = High, the input FET is off. Internally pulled down.
$\overline{\text{FAULT}}$	4	4	O	Open-drain output, device status. $\overline{\text{FAULT}}$ = Low indicates that the input FET has been turned off due to input overvoltage or input overcurrent conditions, or because the battery voltage is outside safe limits.
VSS	3	2	–	Ground terminal
NC	5, 6, 12	3		These pins may have internal circuits used for test purposes. Do not make any external connections at these pins for normal operation.
Thermal PAD			–	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. The VSS pin must be connected to ground at all times.





ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	PIN	VALUE	UNIT
Input voltage	IN (with respect to VSS)	–0.3 to 30	V
	OUT (with respect to VSS)	–0.3 to 12	
	ILIM, $\overline{\text{FAULT}}$, $\overline{\text{CE}}$, VBAT (with respect to VSS)	–0.3 to 7	
Input current	IN	2.0	A
Output current	OUT	2.0	A
Output sink current	$\overline{\text{FAULT}}$	15	mA
Junction temperature, T_J		–40 to 150	°C
Storage temperature, T_{STG}		–65 to 150	°C
Lead temperature (soldering, 10 seconds)		300	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

PRODUCT PREVIEW

PRODUCT PREVIEW

PACKAGE DISSIPATION RATINGS

PART NO.	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR $T_A > 25°C$
BQ24314DSG BQ24316DSG	2×2 SON				
BQ24314DSJ BQ24316DSJ	4×3 SON				

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		3.3	26	V
I_{IN}	Input current, IN pin			1.5	A
I_{OUT}	Output current, OUT pin			1.5	A
R_{ILIM}	OCP Programming resistor		16.67	83.33	kΩ
T_J	Junction temperature		0	125	°C

ELECTRICAL CHARACTERISTICS

over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IN						
V_{UVLO}	Under-voltage lock-out, input power detected threshold	$\overline{CE}$ = Low or High, V_{IN}: 2V → 3V	2.5		2.8	V
$V_{HYS\text{-}UVLO}$	Hysteresis on UVLO	$\overline{CE}$ = Low or High, V_{IN}: 3V → 2V	200		300	mV
$T_{DGL(PGOOD)}$	Deglitch time, input power detected status	$\overline{CE}$ = Low or High. Time measured from V_{IN} 0V → 5V 1μs rise-time, to output turning ON		8		ms
I_{DD}	Operating current	$\overline{CE}$ = Low, No load on OUT pin, V_{IN} < 6V		600		μA
I_{STDBY}	Standby current	$\overline{CE}$ = High, V_{IN} < 6V		55		μA
INPUT TO OUTPUT CHARACTERISTICS						
VDO	Drop-out voltage IN to OUT	$\overline{CE}$ = Low, V_{IN} = 5V, I_{OUT} = 1A			300	mV
INPUT OVERVOLTAGE PROTECTION						
V_{OVP}	Input overvoltage protection threshold (bq24314)		5.67	5.85	6.00	V
	Input overvoltage protection threshold (bq24316)		6.60	6.80	7.00	V
$t_{PD(OVP)}$	Input OV propagation delay	$\overline{CE}$ = Low			1	μs
$V_{HYS\text{-}OVP}$	Hysteresis on OVP	$\overline{CE}$ = Low or High, V_{IN}: 7.5V → 5V		60		mV
$t_{ON(OVP)}$	Recovery time from input overvoltage condition	$\overline{CE}$ = Low, Time measured from V_{IN} 7.5V → 5V, 1μs fall-time		8		ms
INPUT OVERCURRENT PROTECTION						
I_{OCP}	Input overcurrent protection threshold range	$\overline{CE}$ = Low, R_{ILIM} = 16.67kΩ to 83.33kΩ	300		1500	mA
ΔI_{OCP}	OCP threshold accuracy	$\overline{CE}$ = Low, R_{ILIM} = 16.67kΩ to 83.33kΩ		±10 %		
I_{OCP}	Input overcurrent protection threshold	$\overline{CE}$ = Low, R_{ILIM} = 25kΩ	930	1000	1070	mA
K_{ILIM}	Current limit programming: $I_{OCP} = K_{ILIM} \div R_{ILIM}$			25000		AΩ
$t_{BLANK(OCP)}$	Blanking time, input overcurrent detected	$\overline{CE}$ = Low		176		μs
$t_{ON(OCP)}$	Recovery time from input overcurrent condition	$\overline{CE}$ = Low		64		ms
BATTERY OVERVOLTAGE PROTECTION						

ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{OVP}	Battery overvoltage protection threshold	$\overline{CE}$ = Low, V_{IN} > 4.3V	4.30	4.35	4.4	V
$V_{HYS-BOVP}$	Hysteresis on BV_{OVP}	$\overline{CE}$ = Low, V_{IN} > 4.3V		270		mV
I_{VBAT}	Input bias current on VBAT pin				20	nA
$T_{DGL(BOVP)}$	Deglitch time, battery overvoltage detected	$\overline{CE}$ = Low, V_{IN} > 4.3V		176		µs
THERMAL PROTECTION						
$T_{J(OFF)}$	Thermal shutdown temperature			140	150	°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC LEVELS ON $\overline{CE}$						
V_{IL}	Low-level input voltage		0		0.4	V
V_{IH}	High-level input voltage		1.4			V
I_{IL}	Low-level input current	V_{CE} = 0V			1	µA
I_{IH}	High-level input current	V_{CE} = 1.8V			10	µA
LOGIC LEVELS ON $\overline{FAULT}$						
V_{OL}	Output low voltage	I_{SINK} = 5mA			0.4	V

TYPICAL OPERATING PERFORMANCE

For Figure 1 through Figure 4, V_{IN} = 5 V to 12 V, C_{OUT} = 0.47 µF, R_{OUT} = 33 Ω, R_{ILIM} = 25 kΩ, Channel 1 = V_{IN}, Channel 2 = V_{OUT}, Channel 4 = $\overline{FAULT}$

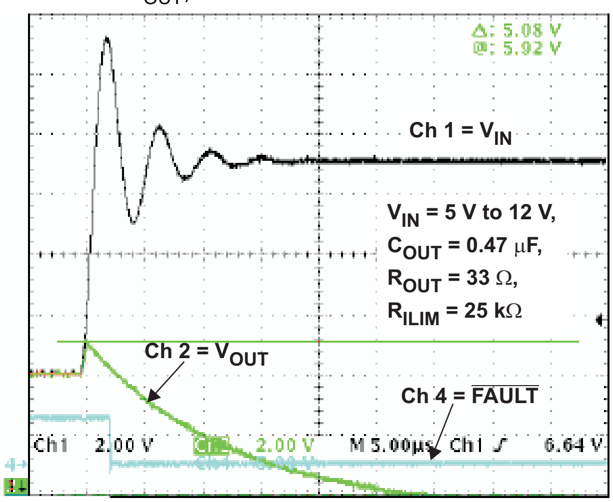


Figure 1. bq24314 OVP Response for Input Step, t_R = 1 µs

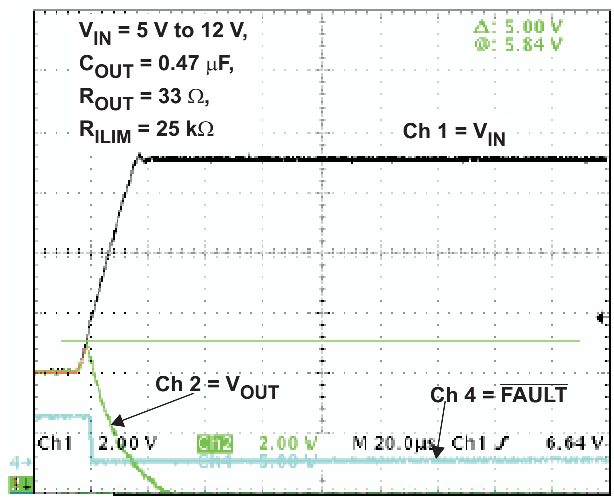


Figure 2. bq24314 OVP Response for Input Step, t_R = 20 µs

PRODUCT PREVIEW

TYPICAL OPERATING PERFORMANCE (continued)

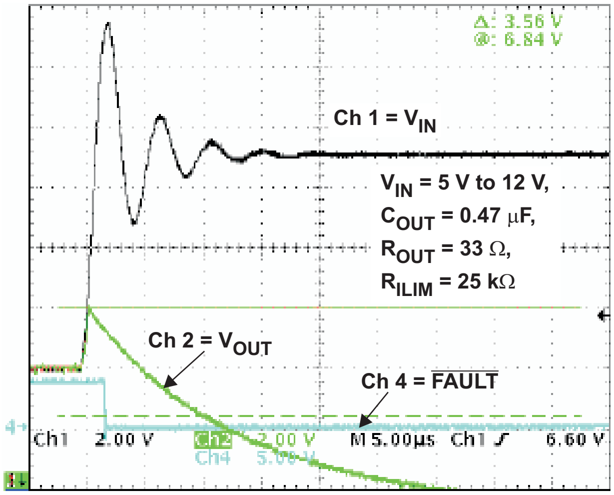


Figure 3. bq24316 OVP Response for Input Step, t_R = 1 µs

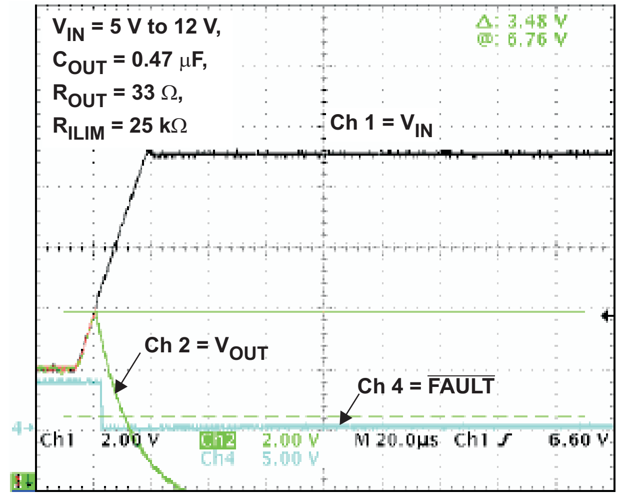


Figure 4. bq24316 OVP Response for Input Step, t_R = 20 µs

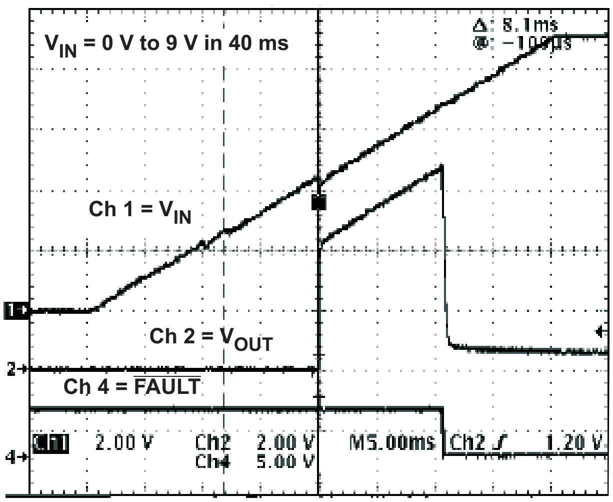


Figure 5. bq24316 Response for Slow Input Ramp
Channel 1 = V_{IN}, Channel 2 = V_{OUT}, Channel 4 = $\overline{FAULT}$,
V_{IN} = 0V to 9V in 40ms

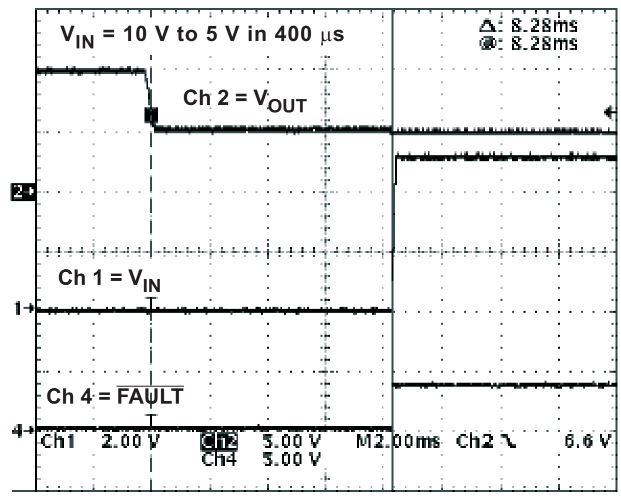


Figure 6. bq24316 Recovery From OVP
Channel 2 = V_{IN},
Channel 1 = V_{OUT}, Channel 4 = $\overline{FAULT}$, V_{IN} = 10V to 5V in 400µs

PRODUCT PREVIEW

TYPICAL OPERATING PERFORMANCE (continued)

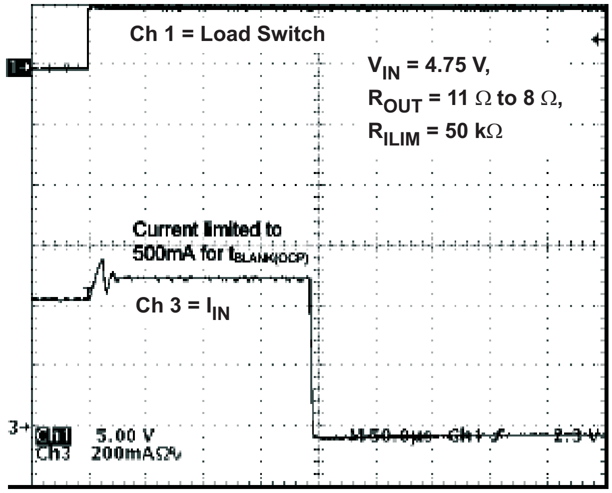


Figure 7. bq24316 OCP Response
Channel 1 = Load Switch, Channel 3 = I_{IN}, V_{IN} = 4.75V, R_{ILIM} = 50kΩ, R_{OUT} = 11Ω to 8Ω

TYPICAL APPLICATION CIRCUIT

(Terminal numbers shown are for the 2×2 DSG package)

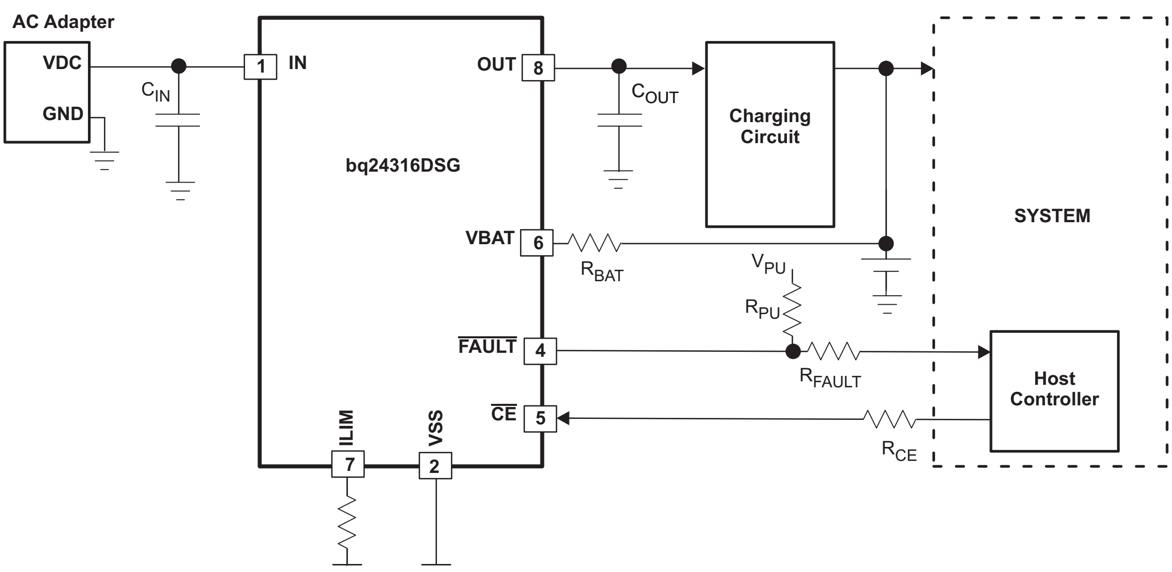


Figure 8. Simple Protection

DETAILED FUNCTIONAL DESCRIPTION

POWER DOWN

The device remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold V_{UVLO}. The FET Q1 connected between IN and OUT pins is off, and the status output, $\overline{\text{FAULT}}$, is set to Hi-Z.

PRODUCT PREVIEW

POWER-ON RESET

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. All internal counters and other circuit blocks are reset.

OPERATION

The device continuously monitors the input voltage, the input current, and the battery voltage.

Input Overvoltage Protection

If the input voltage rises above V_{OVP}, the internal FET is turned off, removing power from the circuit. The $\overline{\text{FAULT}}$ pin is driven low. When the input voltage returns below V_{OVP} – $V_{HYS\text{-}OVP}$ (but is still above V_{UVLO}), the FET is turned on again after a deglitch time of $t_{ON(OVP)}$ to ensure that the input supply has stabilized.

Input Overcurrent Protection

The overcurrent threshold is programmed by a resistor R_{ILIM} connected from the ILIM pin to VSS. The overcurrent threshold is given by $I_{OCP} = K_{ILIM} \div R_{ILIM}$.

If the load current tries to exceed the I_{OCP} threshold, the device limits the current for a blanking duration of $t_{BLANK(OCP)}$. If the load current returns to less than I_{OCP} before $t_{BLANK(OCP)}$ times out, the device continues to operate. However, if the overcurrent situation persists for $t_{BLANK(OCP)}$, the FET is turned off for a duration of $t_{ON(OCP)}$, and the $\overline{\text{FAULT}}$ pin is driven low. The FET is then turned on again after $t_{ON(OCP)}$ and the current is monitored all over again. Each time an OCP fault occurs, an internal counter is incremented. If 15 OCP faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the $\overline{\text{CE}}$ pin.

Battery Overvoltage Protection

The battery overvoltage threshold BV_{OVP} is internally set to 4.35V. If the battery voltage exceeds the BV_{OVP} threshold, the FET is turned off, and the $\overline{\text{FAULT}}$ pin is driven low. The FET is turned back on once the battery voltage drops to BV_{OVP} – $V_{HYS\text{-}BOVP}$. Each time a battery overvoltage fault occurs, an internal counter is incremented. If 15 such faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the $\overline{\text{CE}}$ pin.

THERMAL PROTECTION

If the junction temperature of the device exceeds $T_{J(OFF)}$, the FET is turned off, and the $\overline{\text{FAULT}}$ pin is driven low. The FET is turned back on when the junction temperature falls below $T_{J(OFF)}$ – $T_{J(OFF\text{-}HYS)}$.

PRODUCT PREVIEW

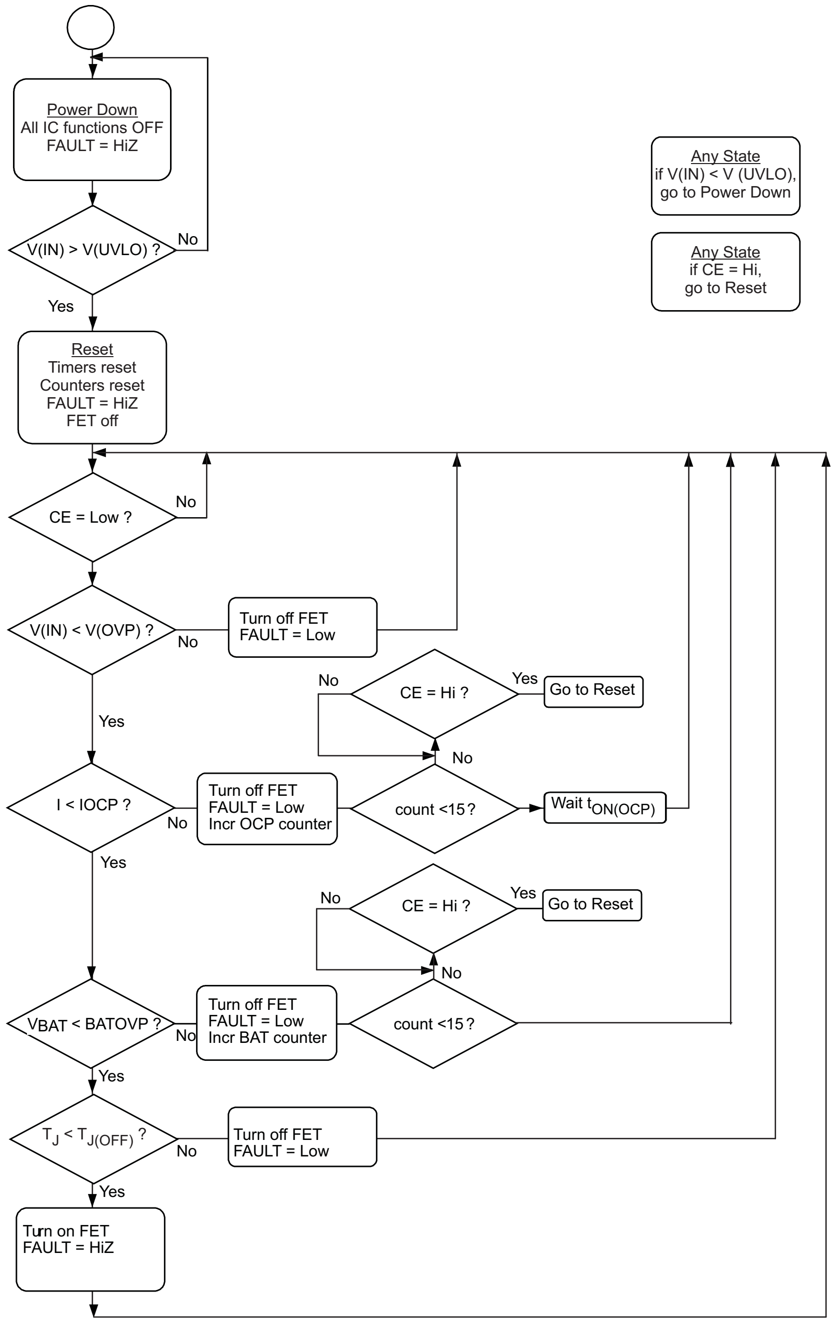


Figure 9. Flow Diagram

$\overline{\text{CE}}$ Pin

The IC has an enable pin which can be used to enable or disable the device. When the $\overline{\text{CE}}$ pin is driven high, the internal FET is turned off. When the $\overline{\text{CE}}$ pin is low, the FET is turned on if other conditions are safe. The $\overline{\text{CE}}$ pin has an internal pulldown resistor and can be left floating. Note that the $\overline{\text{FAULT}}$ pin functionality is also disabled when the $\overline{\text{CE}}$ pin is high.

PRODUCT PREVIEW

APPLICATION INFORMATION (WITH REFERENCE TO FIGURE 8)

Selection of R_{BAT}

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30V, and applying 30V to the battery in case of the failure of the bq2431x can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in case of a failure of the IC. In the interests of safety, R_{BAT} should have a very high value. The problem with a large R_{BAT} is that the voltage drop across this resistor because of the VBAT bias current I_{VBAT} causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35V BV_{OVP} threshold.

Choosing R_{BAT} equal to 220kΩ is a good compromise. In the case of an IC failure, the maximum current flowing into the battery would be (30V – 3V) ÷ 220kΩ = 123µA, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 220kΩ would result in a worst-case voltage drop of $R_{BAT} \times I_{VBAT}$ = 4.4mV. This added to the internal tolerance of 50mV results in a total BV_{OVP} threshold error of less than 55mV, which should be acceptable in most applications.

Selection of R_{CE}

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As in the case of the VBAT pin (see above), the $\overline{CE}$ pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor should be greater than V_{IH} of the bq2431× $\overline{CE}$ pin. The drop across the resistor is given by $R_{CE} \times I_{IH}$.

$\overline{\text{FAULT}}$ Pin

The $\overline{\text{FAULT}}$ pin is an open-drain output that goes low during OV, OC, and battery-OV events. If the application does not require monitoring of the $\overline{\text{FAULT}}$ pin, it can be left unconnected. But if the $\overline{\text{FAULT}}$ pin has to be monitored, it should be pulled high externally through R_{PU}, and connected to the host through R_{FAULT}. R_{FAULT} prevents damage to the host controller if the bq2431x fails (see above). The resistors should be of high value, in practice values between 22kΩ and 100kΩ should be sufficient.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24314DSGR	PREVIEW	SON	DSG	8	3000	TBD	Call TI	Call TI
BQ24316DSGR	PREVIEW	SON	DSG	8	3000	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

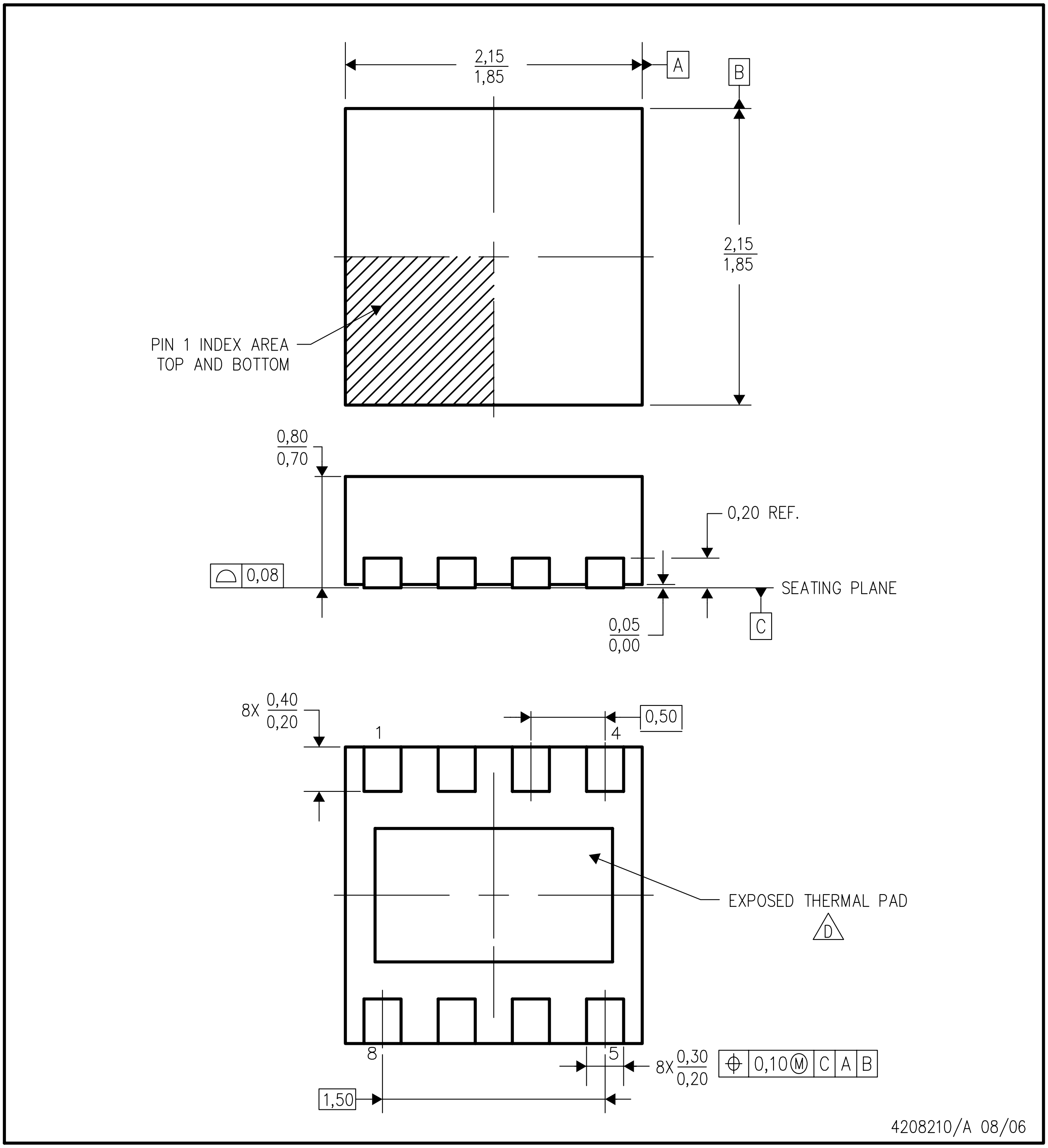
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DSG (S–PDSO–N8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.