

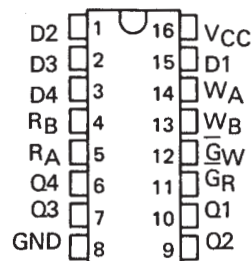
SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

SDLS193 – MARCH 1974 – REVISED MARCH 1988

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- For Use as:
 - Scratch-Pad Memory
 - Buffer Storage between Processors
 - Bit Storage in Fast Multiplication Designs
- 3-State Outputs
- SN54LS170 and SN74LS170 Are Similar But Have Open-Collector Outputs

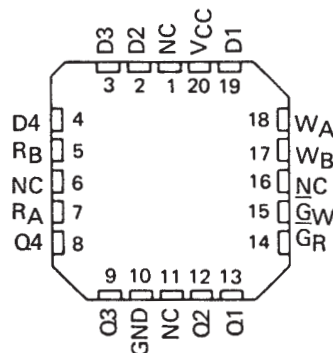
SN54LS670 . . . J OR W PACKAGE
SN74LS670 . . . D OR N PACKAGE

(TOP VIEW)



SN54LS670 . . . FK PACKAGE

(TOP VIEW)



NC — No internal connection.

description

The SN54LS670 and SN74LS670 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, $\overline{GW}$, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, $\overline{GR}$, is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical) and the read time (24 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 128 of these outputs may be bus connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

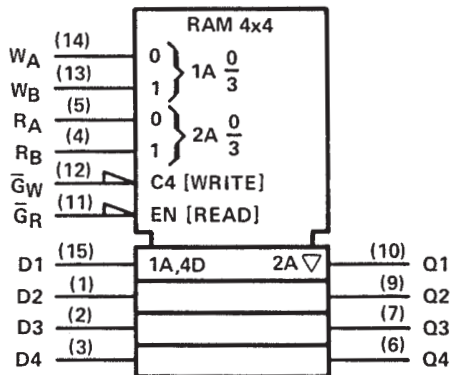
The SN54LS670 is characterized for operation over the full military temperature range of -55°C to 125°C ; the SN74LS670 is characterized for operation from 0°C to 70°C .

SN54LS670, SN74LS670

4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

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logic symbol[†]



† This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

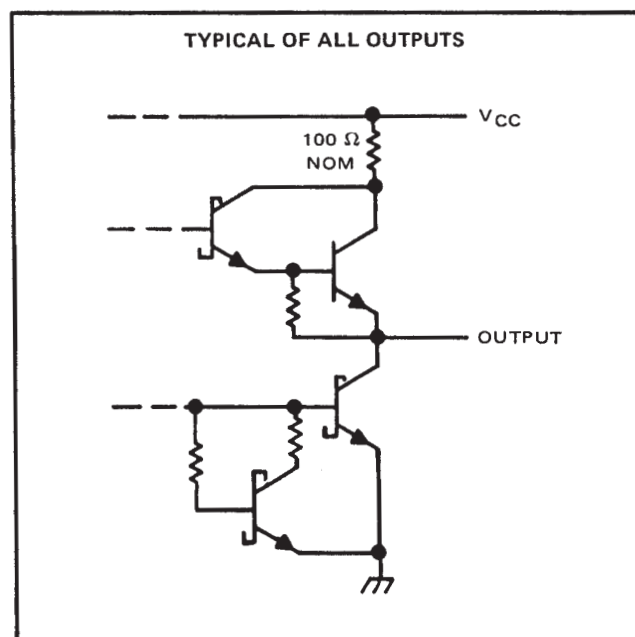
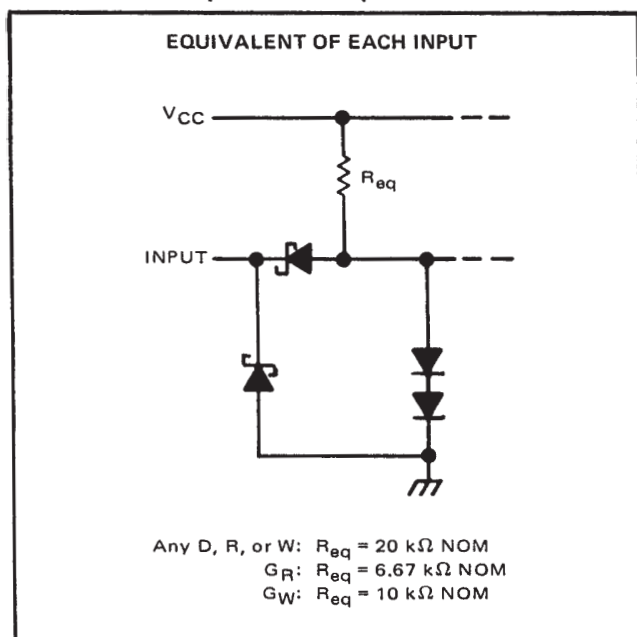
WRITE INPUTS			WORD			
W_B	W_A	$\bar{W}_W$	0	1	2	3
L	L	L	$Q = D$	Q_0	Q_0	Q_0
L	H	L	Q_0	$Q = D$	Q_0	Q_0
H	L	L	Q_0	Q_0	$Q = D$	Q_0
H	H	L	Q_0	Q_0	Q_0	$Q = D$
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R _B	R _A	$\bar{R}$	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

NOTES: A. H = high level, L = low level, X = irrelevant, Z = high impedance (off)
 B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
 C. Q₀ = the level of Q before the indicated input conditions were established.
 D. W0B1 = The first bit of word 0, etc.

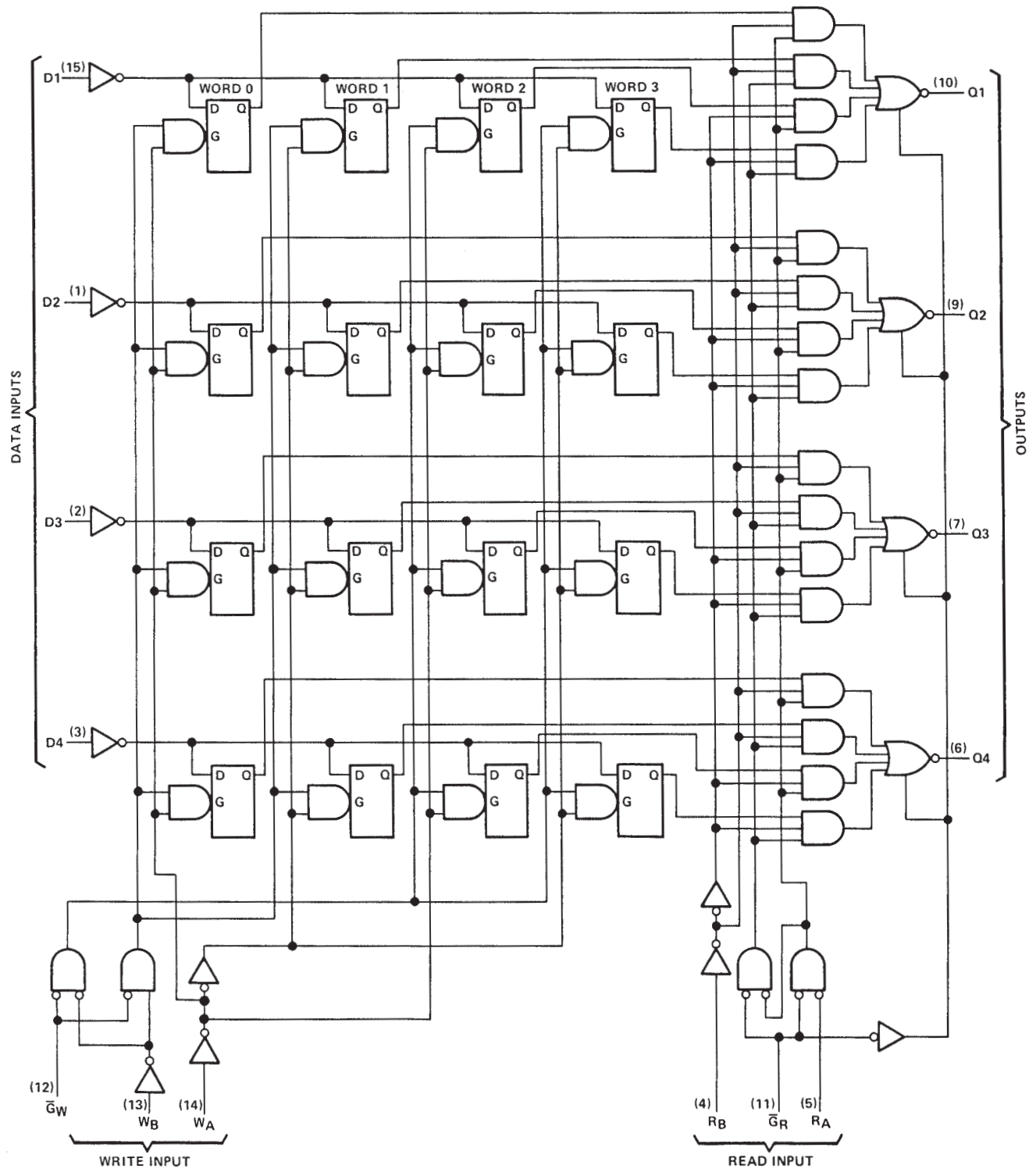
schematics of inputs and outputs



SN54LS670, SN74LS670 4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

SN54LS670, SN74LS670

4-BY-4 REGISTER FILES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS670	–55°C to 125°C
SN74LS670	0°C to 70°C
Storage temperature range	–65°C to 150°C

recommended operating conditions

		SN54LS670			SN74LS670			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				–1			–2.6	mA
Low-level output current, I_{OL}				4			8	mA
Width of write-enable or read-enable pulse, t_W		25			25			ns
Setup times, high- or low-level data (see Figure 2)	Data input with respect to write enable, $t_{SU}(D)$	10			10			ns
	Write select with respect to write enable, $t_{SU}(W)$	15			15			ns
Hold times, high- or low-level data (see Note 2 and Figure 2)	Data input with respect to write enable, $t_H(D)$	15			15			ns
	Write select with respect to write enable, $t_H(W)$	5			5			ns
Latch time for new data, t_{latch} (see Note 3)		25			25			ns
Operating free-air temperature range, T_A		–55		125	0		70	°C

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{SU}(W)$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_H(W)$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS670			SN74LS670			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	2.4	3.4	$I_{OH} = -1 \text{ mA}$				V
				$I_{OH} = -2.6 \text{ mA}$	2.4	3.1		
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	0.25	0.4	$I_{OL} = 4 \text{ mA}$			0.25	V
				$I_{OL} = 8 \text{ mA}$			0.35	
I_{OZH} Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 2.7 \text{ V}$			20			20	μA
I_{OZL} Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}, V_{IH} = 2 \text{ V}, V_O = 0.4 \text{ V}$			-20			-20	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$	Any D, R, or W		0.1			0.1	mA
		$\bar{G}_W$		0.2			0.2	
		$\bar{G}_R$		0.3			0.3	
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	Any D, R, or W		20			20	μA
		$\bar{G}_W$		40			40	
		$\bar{G}_R$		60			60	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	Any D, R, or W		-0.4			-0.4	mA
		$\bar{G}_W$		-0.8			-0.8	
		$\bar{G}_R$		-1.2			-1.2	
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	-30		-130	-30		-130	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 4		30	50		30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 4: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

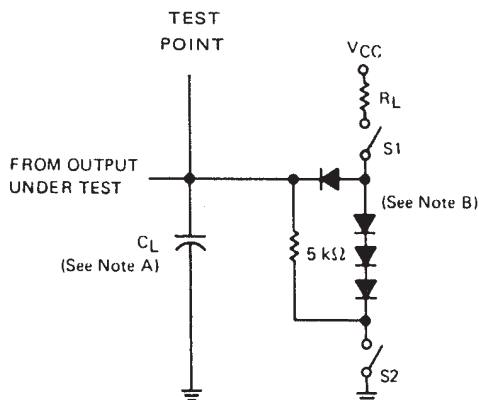
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tPLH	Read select	Any Q	CL = 15 pF, RL = 2 kΩ, See Figures 1 and 2	23	40	ns	
tPHL				25	45		
tPLH	Write enable	Any Q	CL = 15 pF, RL = 2 kΩ, See Figures 1 and 3	26	45	ns	
tPHL				28	50		
tPLH	Data	Any Q		25	45	ns	
tPHL				23	40		
tPZH	Read enable	Any Q	CL = 15 pF, RL = 2 kΩ, See Figures 1 and 4	15	35	ns	
tPZL				22	40		
tPHZ			CL = 5 pF, RL = 2 kΩ, See Figures 1 and 4	30	50	ns	
tPLZ				16	35		

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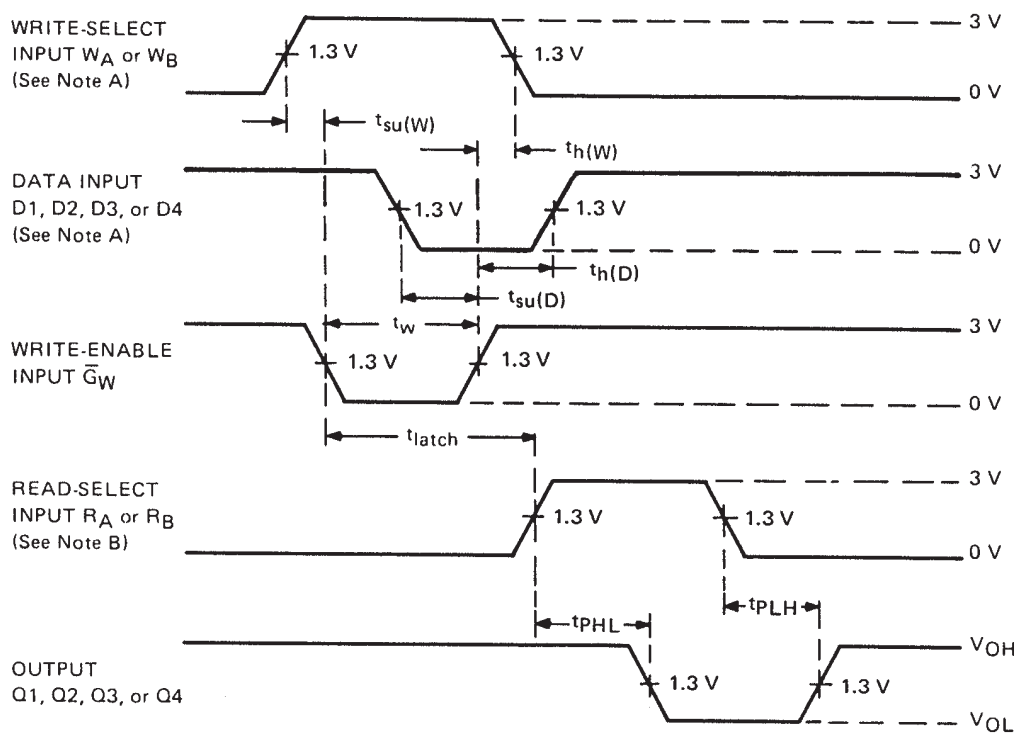
PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.

LOAD CIRCUIT

FIGURE 1



VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

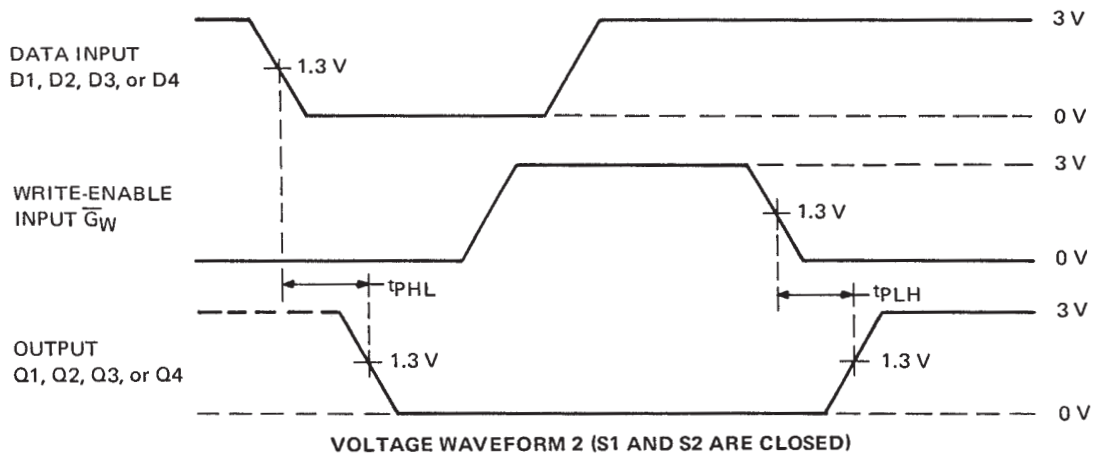
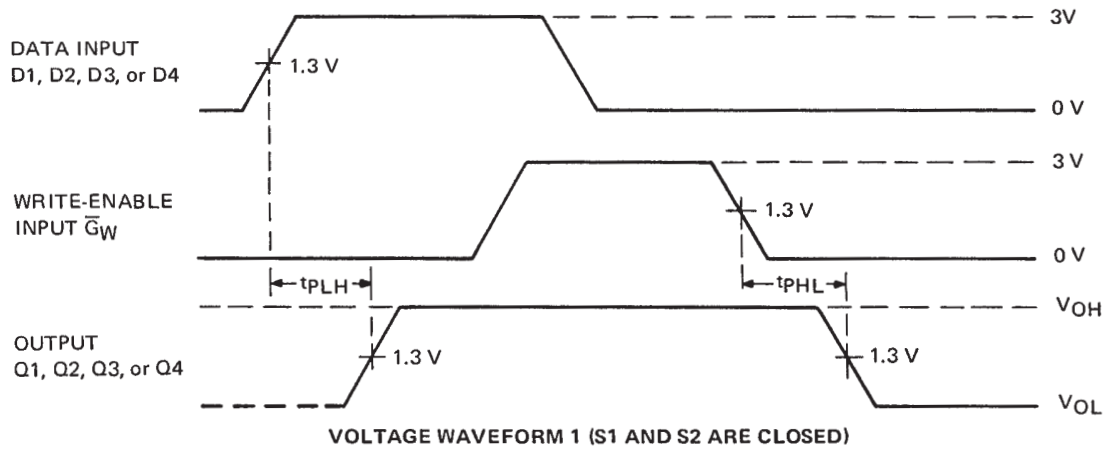
NOTES: A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
B. When measuring delay times from a read-select input, the read-enable input is low.
C. Input waveforms are supplied by generators having the following characteristics: $PRR \leq 2 \text{ MHz}$, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

FIGURE 2



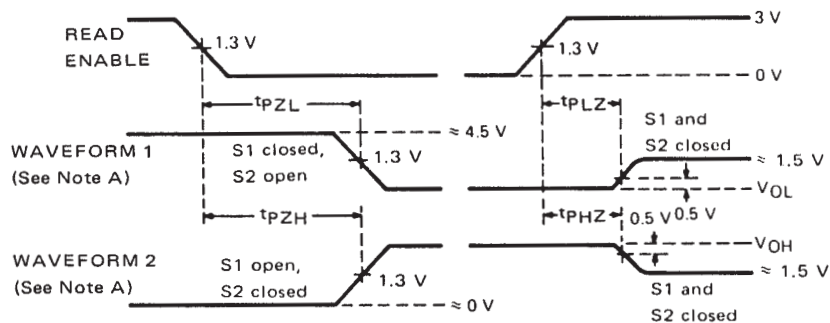
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low.
B. Input waveforms are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

FIGURE 3



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

- NOTES: A. Waveforms 1 is for an output with internal conditions such that the output is low except when disabled by the read-enable input. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the read-enable input.
B. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
C. Input waveforms are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

FIGURE 4

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