

- State-of-the-Art **EPIC-IITM** BiCMOS Design Significantly Reduces Power Dissipation
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs (-32-mA I_{OH} , 64-mA I_{OL})
- Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, Ceramic Chip Carriers (FK), Ceramic Flat (W) Package, and Plastic (NT) and Ceramic (JT) DIPs

description

These 10-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the devices provide true data at the Q outputs.

A buffered output-enable (\overline{OE}) input can be used to place the ten outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect the internal operations of the latch. Previously stored data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT821 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT821A is characterized for operation from -40°C to 85°C .

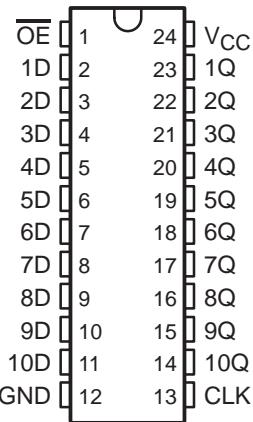


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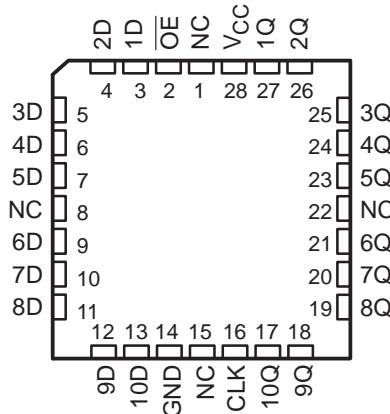
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

SN54ABT821 . . . JT OR W PACKAGE
SN74ABT821A . . . DB, DW, OR NT PACKAGE
(TOP VIEW)



SN54ABT821 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

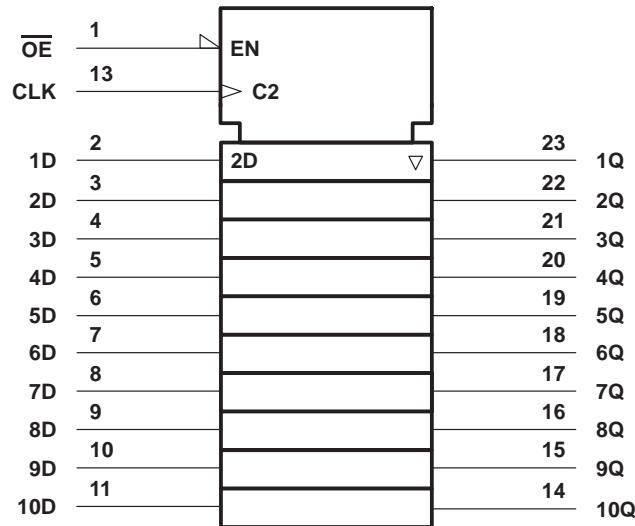
**SN54ABT821, SN74ABT821A
10-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS**

SCBS193E – FEBRUARY 1991 – REVISED MAY 1997

FUNCTION TABLE
(each flip-flop)

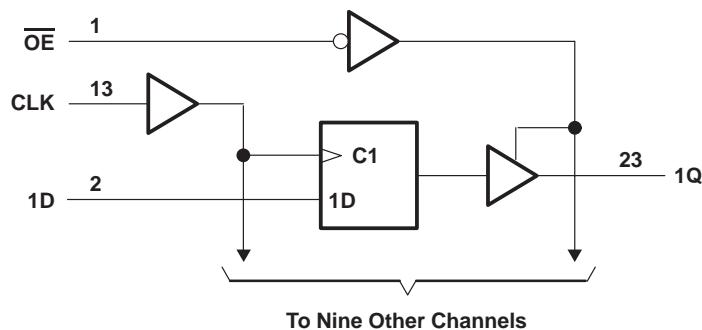
INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the DB, DW, JT, NT, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I (see Note 1)	-0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	-0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT821	96 mA
	SN74ABT821A
	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	-18 mA
Output clamp current, I_{OK} ($V_O < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package	104°C/W
	DW package
	81°C/W
	NT package
	67°C/W
Storage temperature range, T_{Stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with EIA/JEDEC Std JESD51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions (see Note 3)

		SN54ABT821		SN74ABT821A		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage		2		2	V
V _{IL}	Low-level input voltage			0.8	0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current			-24	-32	mA
I _{OL}	Low-level output current			48	64	mA
Δt/Δv	Input transition rise or fall rate			10	10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

**SN54ABT821, SN74ABT821A
10-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TA = 25°C			SN54ABT821		SN74ABT821A		UNIT
		MIN	TYPT†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5		2.5		V
	V _{CC} = 5 V, I _{OH} = -3 mA	3			3		3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2		2				
		I _{OH} = -32 mA	2*				2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.55		0.55			V
		I _{OL} = 64 mA		0.55*				0.55	
V _{hys}		100							mV
I _I	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND		±1		±1		±1		µA
I _{OZPU} ‡	V _{CC} = 0 to 2.1 V, V _O = 0.5 to 2.7 V, OE = X		±50*				±50		µA
I _{OZPD} ‡	V _{CC} = 2.1 V to 0, V _O = 0.5 to 2.7 V, OE = X		±50*				±50		µA
I _{OZH}	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, OE ≥ 2 V		10		10		10		µA
I _{OZL}	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, OE ≥ 2 V		-10		-10		-10		µA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V		±100				±100		µA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V	Outputs high		50		50		50	µA
I _O §	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-100	-180	-50	-180	-50	-180	mA
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	1	250		250		250	µA
		Outputs low	24	38		38		38	mA
		Outputs disabled	0.5	250		250		250	µA
ΔI _{CC} ¶	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5		1.5	mA
C _i	V _I = 2.5 V or 0.5 V		3.5						pF
C _o	V _O = 2.5 V or 0.5 V		7.5						pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ This parameter is characterized, but not production tested.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

			V _{CC} = 5 V, TA = 25°C		SN54ABT821		SN74ABT821A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		0	125	0	125	0	125	MHz
t _w	Pulse duration, CLK high or low	High	2.9		2.9		2.9		ns
		Low	3.8		3.8		3.8		
t _{su}	Setup time, data before CLK↑		2.1		2.1		2.1		ns
t _h	Hold time, data after CLK↑		1.3		1.3		1.3		ns

SN54ABT821, SN74ABT821A
10-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT821			UNIT	
			$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$				
			MIN	TYP	MAX		
f_{max}			125		125	MHz	
t_{PLH}	CLK	Q	1.6†	4.1	5.6	ns	
			2.1†	4.6	6.2	ns	
t_{PHL}	\overline{OE}	Q	1	3	4.5	ns	
			2.2	4.1	5.6	ns	
t_{PZH}	\overline{OE}	Q	2.7	4.7	6.2	ns	
			1.7†	4.6	6.1	ns	
t_{PZL}							
t_{PHZ}	\overline{OE}	Q	2.7	4.7	6.2	ns	
			1.7†	4.6	6.1	ns	
t_{PLZ}							

† This data sheet limit may vary among suppliers.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50 \text{ pF}$ (unless otherwise noted) (see Figure 1)

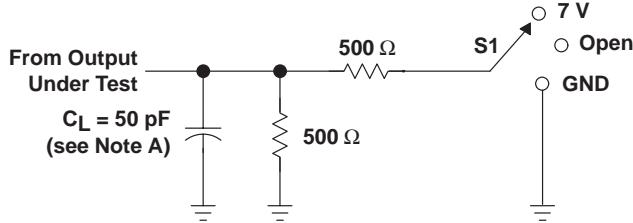
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT821A			UNIT	
			$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$				
			MIN	TYP	MAX		
f_{max}			125		125	MHz	
t_{PLH}	CLK	Q	1.6†	4.1	5.6	ns	
			2.3†	4.6	6.2	ns	
t_{PHL}	\overline{OE}	Q	1	3	4.5	ns	
			2.2	4.1	5.6	ns	
t_{PZH}	\overline{OE}	Q	2.7	4.7	6.2	ns	
			1.7†	4.6	6.1	ns	
t_{PZL}							
t_{PHZ}	\overline{OE}	Q	2.7	4.7	6.2	ns	
			1.7†	4.6	6.1	ns	
t_{PLZ}							

† This data sheet limit may vary among suppliers.

**SN54ABT821, SN74ABT821A
10-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS**

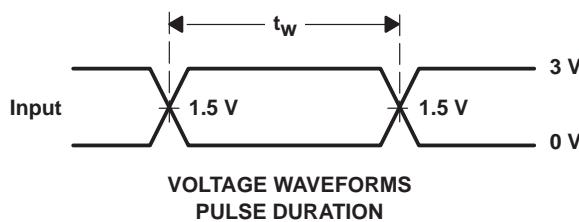
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PARAMETER MEASUREMENT INFORMATION

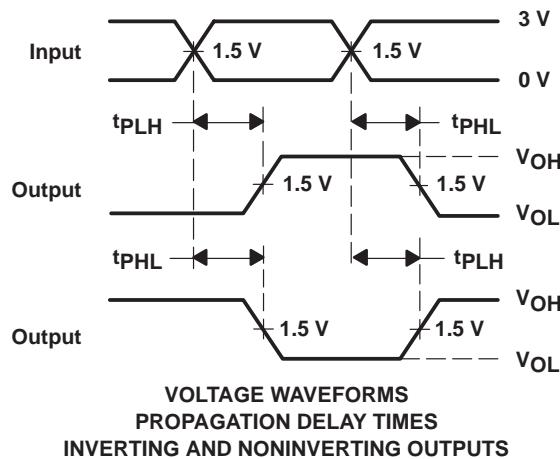
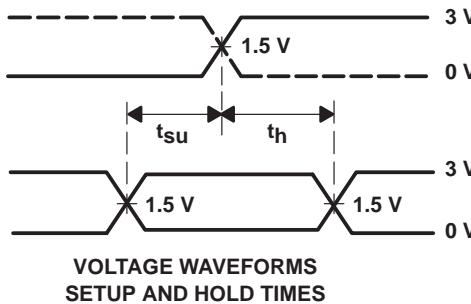


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

LOAD CIRCUIT



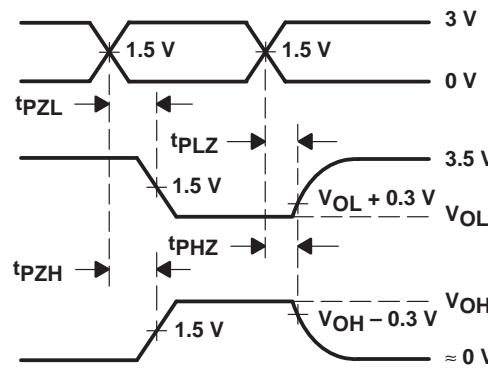
Timing Input



Output Control

Output Waveform 1
S1 at 7 V
(see Note B)

Output Waveform 2
S1 at Open
(see Note B)



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.

D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9469101Q3A	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9469101Q3A SNJ54ABT821FK	Samples
5962-9469101QKA	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9469101QKA SNJ54ABT821W	Samples
5962-9469101QLA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9469101QLA SNJ54ABT821JT	Samples
SN74ABT821ADBLE	OBsolete	SSOP	DB	24		TBD	Call TI	Call TI	-40 to 85		
SN74ABT821ADBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB821A	Samples
SN74ABT821ADBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB821A	Samples
SN74ABT821ADBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB821A	Samples
SN74ABT821ADW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT821A	Samples
SN74ABT821ADWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT821A	Samples
SN74ABT821ADWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT821A	Samples
SN74ABT821ADWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT821A	Samples
SN74ABT821ADWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT821A	Samples
SN74ABT821ADWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT821A	Samples
SN74ABT821ANT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT821ANT	Samples
SN74ABT821ANTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT821ANT	Samples
SNJ54ABT821FK	ACTIVE	LCCC	FK	28	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9469101Q3A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54 ABT821FK	
SNJ54ABT821JT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9469101QL A SNJ54ABT821JT	Samples
SNJ54ABT821W	ACTIVE	CFP	W	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9469101QK A SNJ54ABT821W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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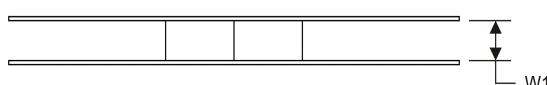
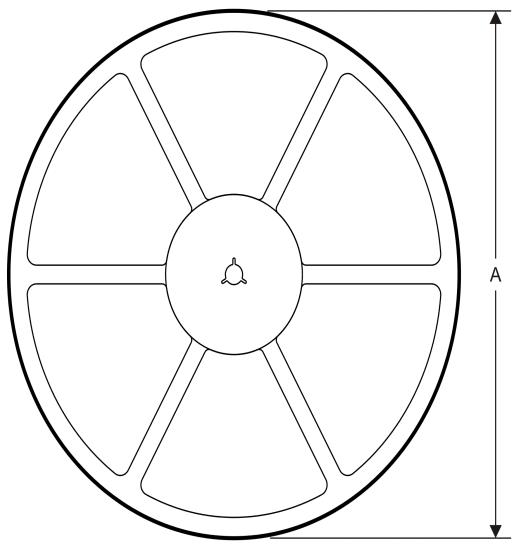
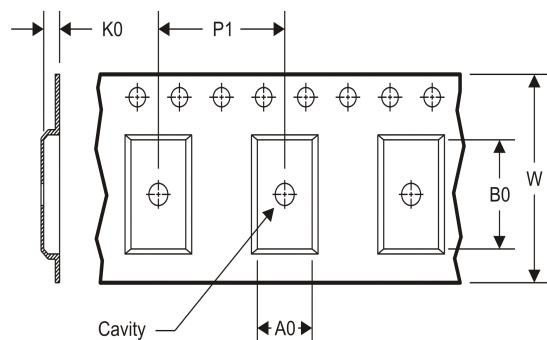
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OTHER QUALIFIED VERSIONS OF SN54ABT821 :

- Catalog: [SN74ABT821](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT821ABDR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74ABT821ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

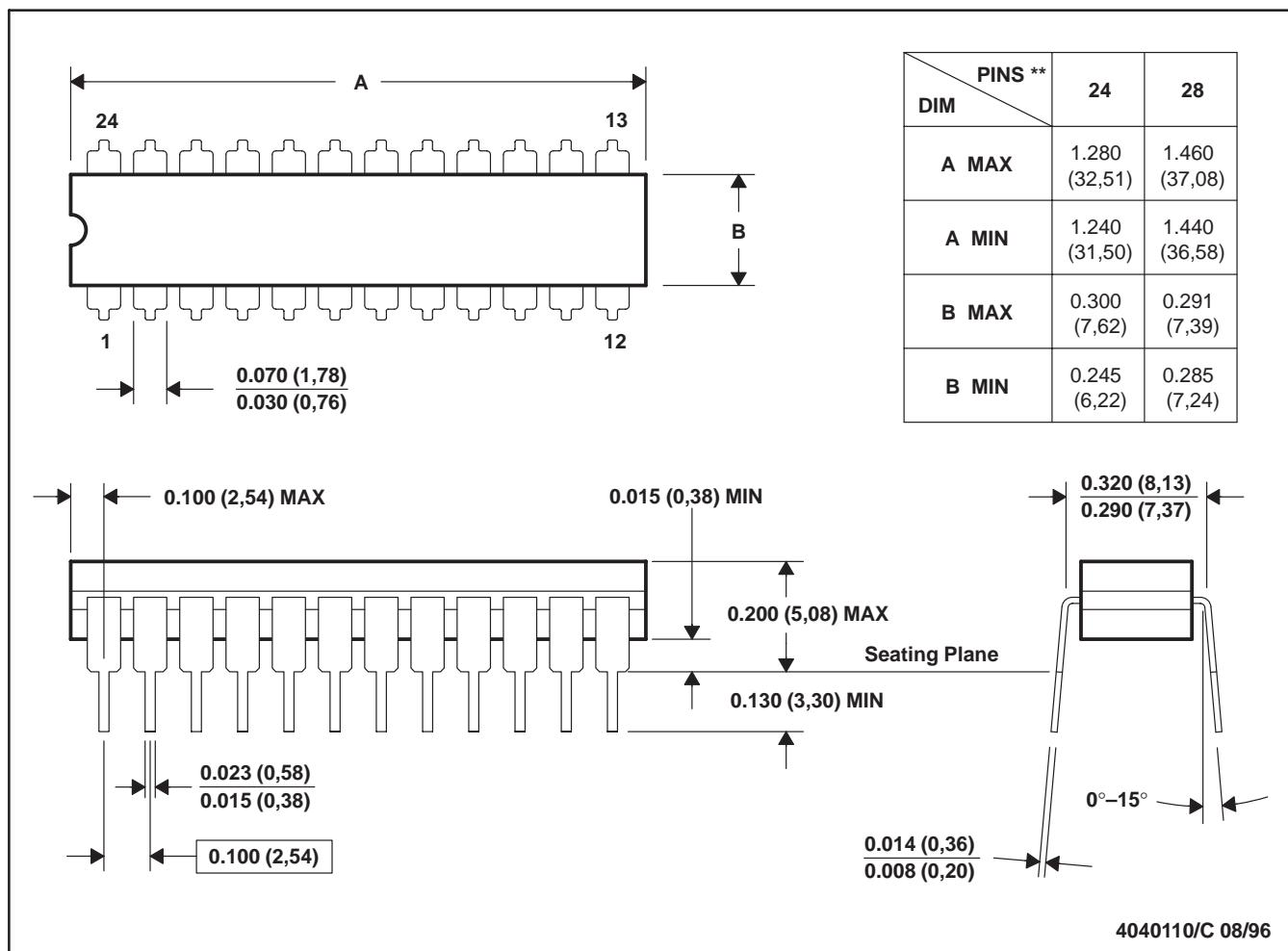

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT821ABR	SSOP	DB	24	2000	367.0	367.0	38.0
SN74ABT821ADWR	SOIC	DW	24	2000	367.0	367.0	45.0

JT (R-GDIP-T**)

24 LEADS SHOWN

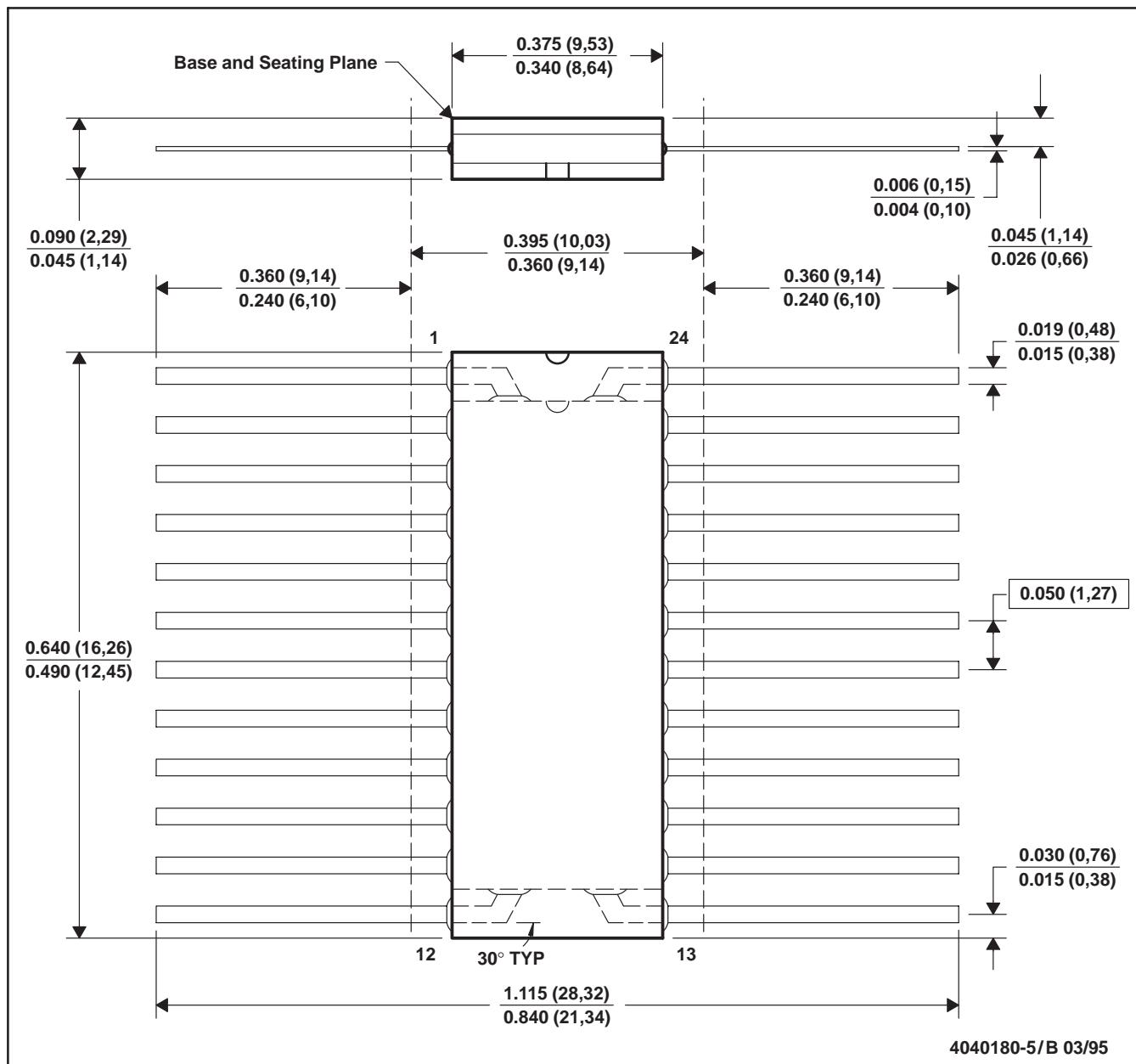
CERAMIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 E. Index point is provided on cap for terminal identification only.

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a metal lid.
- Falls within JEDEC MS-004

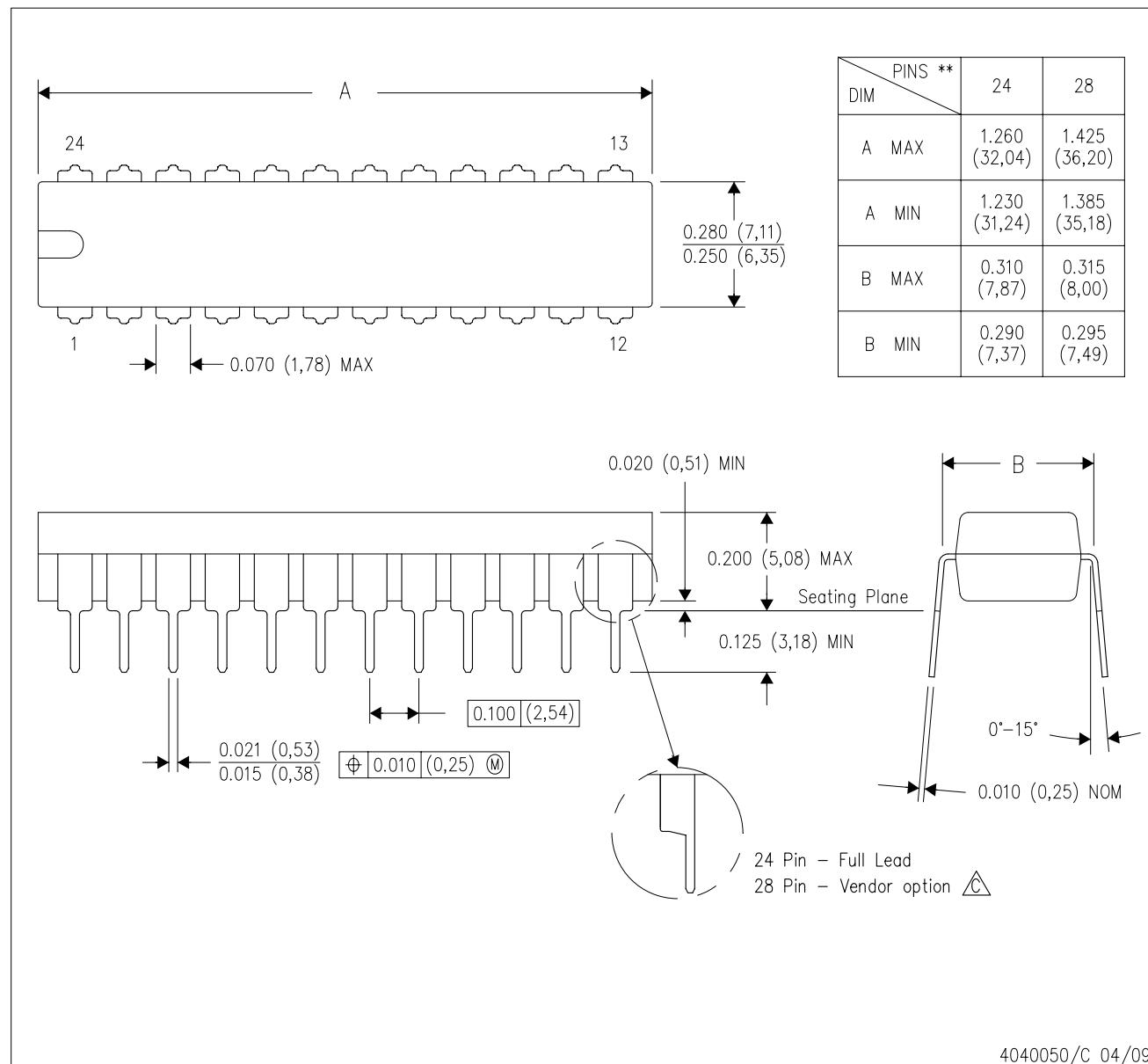
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MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

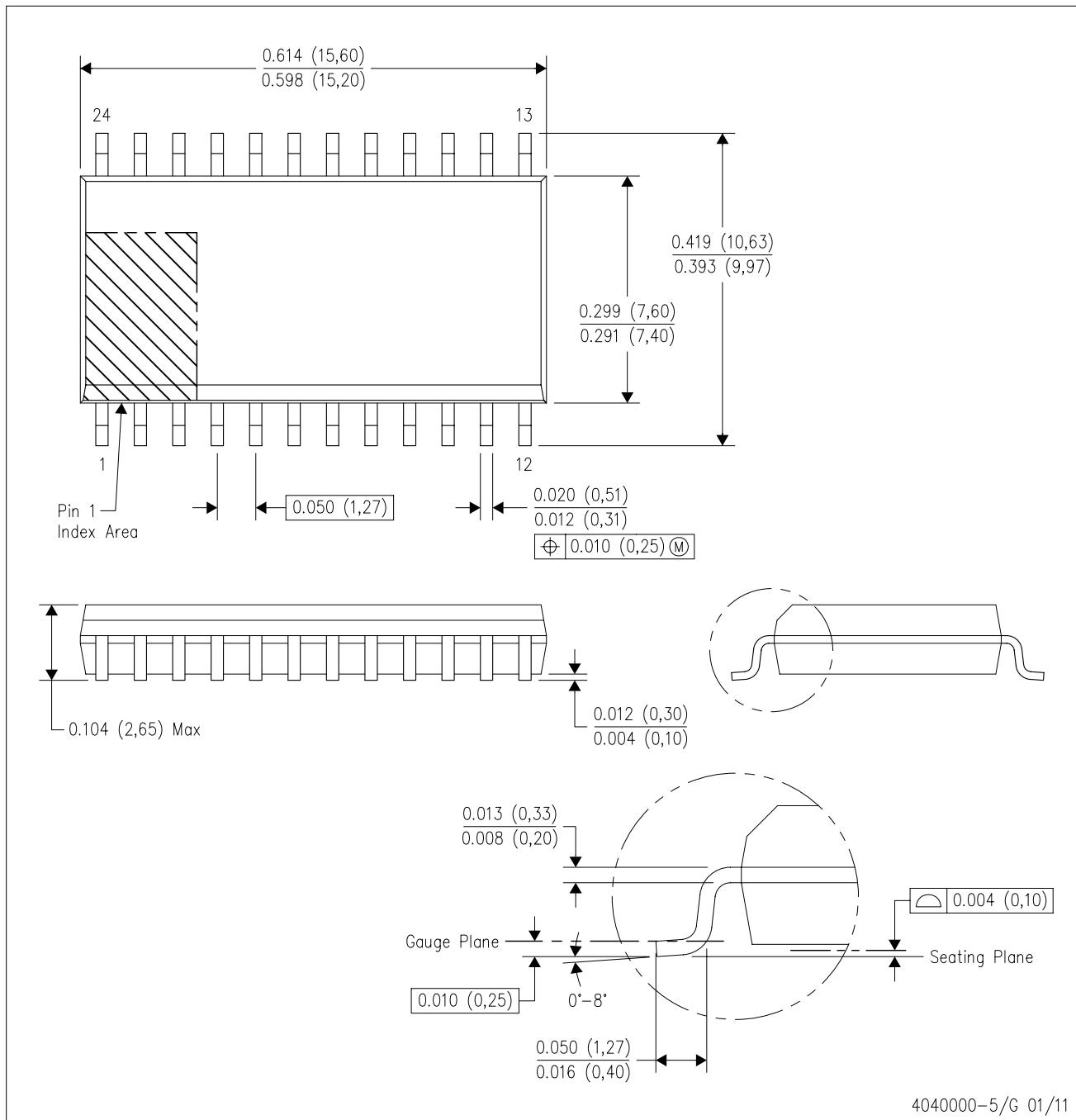
B. This drawing is subject to change without notice.

 The 28 pin end lead shoulder width is a vendor option, either half or full width.

4040050/C 04/09

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

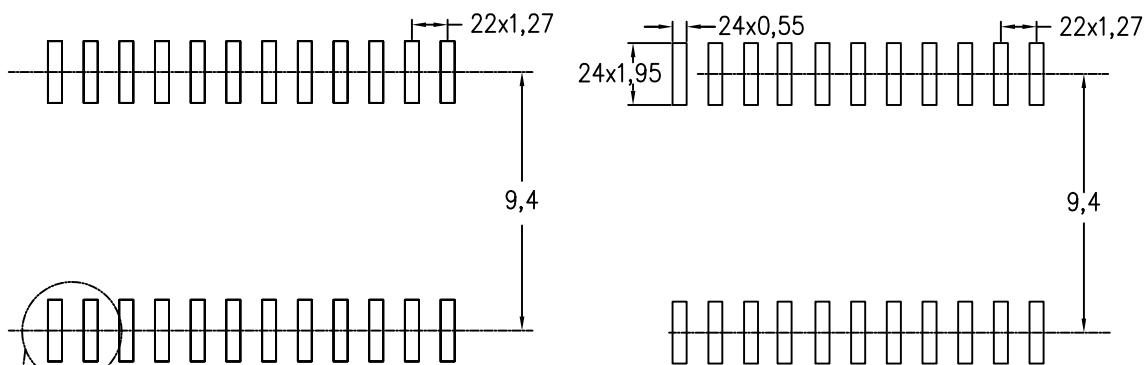


NOTES:

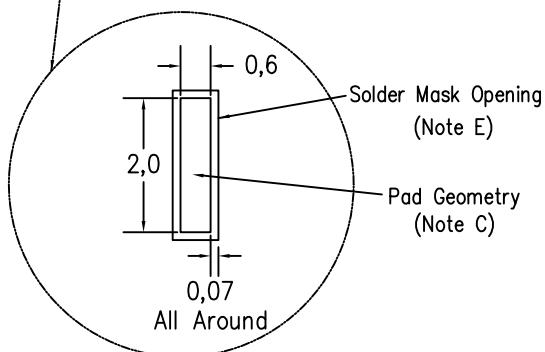
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)

Non Solder Mask Define Pad



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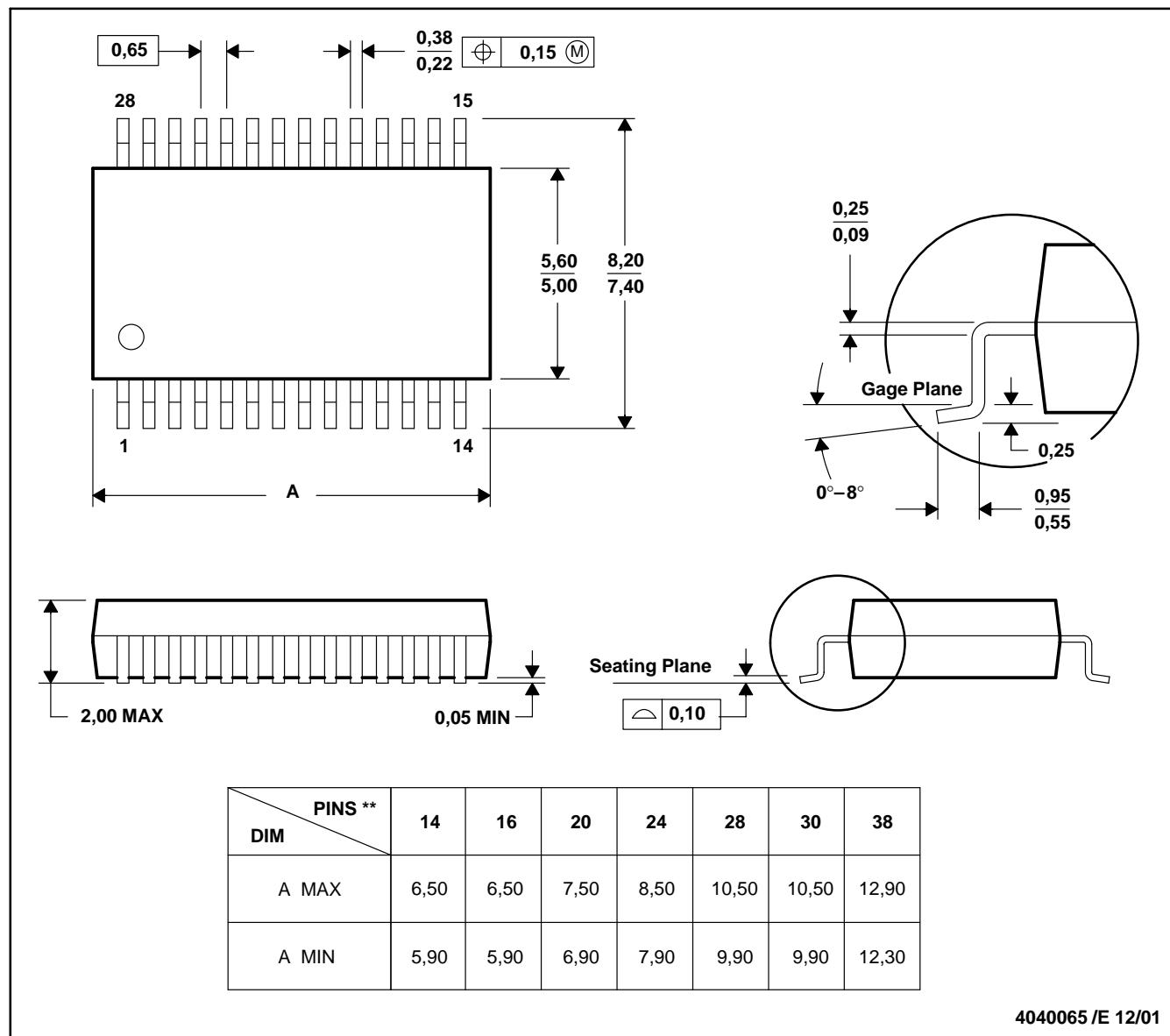
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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