FAIRCHILD SEMICONDUCTOR TM

September 1997

74VHC161284
IEEE 161284 Transceiver

General Description

The VHC161284 contains eight bidirectional data buffers and eleven control/status buffers to implement a full IEEE P1284 compliant interface. The device supports the IEEE 1284 standard and is intended to be used in Extended Capabilities Port mode (ECP). The pinout allows for easy connection from the Peripheral (A-side) to the Host (cable side).

Outputs on the cable side can be configured to be either open drain or high drive (± 14 mA). The pull-up and pull-down series termination resistance of these outputs on the cable side is optimized to drive an external cable. In addition, all inputs (except HLH) and outputs on the cable side contain internal pull-up resistors connected to the V_{CC} supply to provide proper termination and pull-ups for open drain mode.

Outputs on the Peripheral side are standard low-drive CMOS outputs. The DIR input controls data flow on the A_1–A_8/B_1–B_8 transceiver pins.

Features

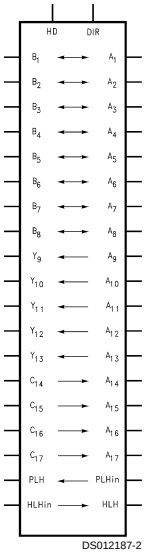
- Supports IEEE P1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals
- Replaces the function of two (2) 74ACT1284 devices
- All inputs have hysteresis to provide noise margin
- B and Y output resistance optimized to drive external cable
- B and Y outputs in high impedance mode during power down
- Inputs and outputs on cable side have internal pull-up resistors
- Flow-through pin configuration allows easy interface between the Peripheral and Host

Ordering Code:

Ordering Number	Package Number	Package Description
74VHC161284MEA	MS48A	48-Lead Molded JEDEC, SSOP
74VHC161284MTD	MTD48	48-Lead Molded JEDEC, TSSOP

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter"X" to the ordering code.

Logic Symbol



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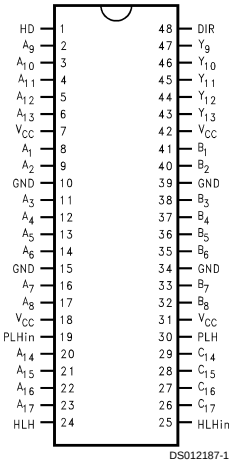
Connection Diagram

Pin Assignment for SSOP/TSSOP



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Connection Diagram (Continued)

Pin Descriptions

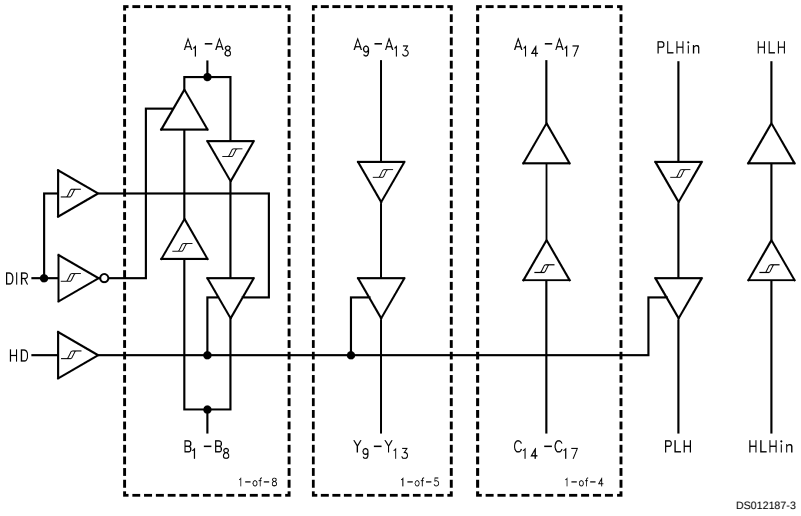
Pin Names	Description
HD	High Drive Enable Input (Active High)
DIR	Direction Control Input
A_1–A_8	Inputs or Outputs
B_1–B_8	Inputs or Outputs
A_9–A_{13}	Inputs
Y_9–Y_{13}	Outputs
A_{14}–A_{17}	Outputs
C_{14}–C_{17}	Inputs
PLH_{IN}	Peripheral Logic High Input
PLH	Peripheral Logic High Output
HLH_{IN}	Host Logic High Input
HLH	Host Logic High Output

Truth Table

Inputs		Outputs
DIR	HD	
L	L	B_1–B_8 Data to A_1–A_8, and A_9–A_{13} Data to Y_9–Y_{13}* C_{14}–C_{17} Data to A_{14}–A_{17} PLH Open Drain Mode
L	H	B_1–B_8 Data to A_1–A_8, and A_9–A_{13} Data to Y_9–Y_{13} C_{14}–C_{17} Data to A_{14}–A_{17}
H	L	A_1–A_8 Data to B_1–B_8** A_9–A_{13} Data to Y_9–Y_{13}* C_{14}–C_{17} Data to A_{14}–A_{17} PLH Open Drain Mode
H	H	A_1–A_8 Data to B_1–B_8 A_9–A_{13} Data to Y_9–Y_{13} C_{14}–C_{17} Data to A_{14}–A_{17}

*Y_9–Y_{13} Open Drain Outputs
**B_1–B_8 Open Drain Outputs

Logic Diagram



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Absolute Maximum Ratings (Note 1)

Supply Voltage	
V_{CC}	−0.5V to + 7.0V
Input Voltage (V_I) — (Note 2)	
A_1–A_{13}, PLH_{IN}, DIR, HD	−0.5V to V_{CC} + 0.5V
B_1–B_8, C_{14}–C_{17}, HLH_{IN}	−0.5V to + 5.5V (DC)
B_1–B_8, C_{14}–C_{17}, HLH_{IN}	−2.0V to + 7.0V *
	*40 ns Transient
Output Voltage (V_O)	
A_1–A_8, A_{14}–A_{17}, HLH	−0.5V to V_{CC} + 0.5V
B_1–B_8, Y_9–Y_{13}, PLH	−0.5V to + 5.5V (DC)
B_1–B_8, Y_9–Y_{13}, PLH	−2.0V to + 7.0V*
	*40 ns Transient
DC Output Current (I_O)	
A_1–A_8, HLH	±25 mA
B_1–B_8, Y_9–Y_{13}	±50 mA
PLH (Output LOW)	84 mA
PLH (Output HIGH)	−50 mA
Input Diode Current (I_{IK}) — (Note 2)	
DIR, HD, A_9–A_{13}, PLH, HLH, C_{14}–C_{17}	−20 mA
Output Diode Current (I_{OK})	
A_1–A_8, A_{14}–A_{17}, HLH	±50 mA
B_1–B_8, Y_9–Y_{13}, PLH	−50 mA
DC Continuous V_{CC} or Ground Current	±200 mA
Storage Temperature	−65˚C to +150˚C
ESD (HBM) Last Passing Voltage	2000V

Recommended Operating Conditions

Supply Voltage	
V_{CC}	4.5V to 5.5V
DC Input Voltage (V_I)	0V to V_{CC}
Open Drain Voltage (V_O)	0V to 5.5V
Operating Temperature (T_A)	−40˚C to +85˚C

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Fairchild does not recommend operation outside the databook specifications.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	T_A = −40˚C to +85˚C Guaranteed Limits	Units	Conditions
V_{IK}	Input Clamp Diode Voltage		3.0	−1.2	V	I_I = −18 mA
V_{IH}	Minimum High Level Input Voltage	A_n, PLH_{IN}, DIR, HD	4.5–5.5	0.7 V_{CC}	V	
		B_n	4.5–5.5	2.0		
		C_n	4.5–5.5	2.3		
		HLH_{IN}	4.5–5.5	2.6		
V_{IL}	Maximum High Level Input Voltage	A_n, PLH_{IN}, DIR, HD	4.5–5.5	0.3 V_{CC}	V	
		B_n	4.5–5.5	0.8		
		C_n	4.5–5.5	0.8		
		HLH_{IN}	4.5–5.5	1.6		
ΔVT	Minimum Input Hysteresis	A_n, PLH_{IN}, HLH_{IN}, DIR, HD	4.5–5.5	0.4	V	V_T^+–V_T^-
		B_n	4.5–5.5	0.4		V_T^+–V_T^-
		C_n	4.5–5.5	0.8		V_T^+–V_T^-
V_{OH}	Minimum High Level Output Voltage	A_n, HLH	4.5	4.4	V	I_{OH} = −50 µA
			4.5	3.8		I_{OH} = −8 mA
		B_n, Y_n	4.5	3.73		I_{OH} = −14 mA
		PLH	4.5	4.45		I_{OH} = −500 µA
V_{OL}	Maximum Low Level Output Voltage	A_n, HLH	4.5	0.1	V	I_{OL} = 50 µA
			4.5	0.44		I_{OH} = 8 mA
		B_n, Y_n	4.5	0.77		I_{OH} = 14 mA
		PLH	4.5	0.7		I_{OL} = 84 mA
RD	Maximum Output Impedance	B_1–B_8, Y_9–Y_{13}	5.0	55	Ω	(Notes 3, 4, 6)
	Minimum Output Impedance	B_1–B_8, Y_9–Y_{13}	5.0	35	Ω	(Notes 3, 4, 6)
RP	Maximum Pull-Up Resistance	B_1–B_8, Y_9–Y_{13}, C_{14}–C_{17}	5.0	1650	Ω	(Note 4)
	Minimum Pull-Up Resistance	B_1–B_8, Y_9–Y_{13}, C_{14}–C_{17}	5.0	1150	Ω	(Note 4)

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	$T_A = -40^\circ C$ to $+85^\circ C$ Guaranteed Limits	Units	Conditions
I_{IH}	Maximum Input Current in High State	A_9–A_{13}, PLH_{IN}, HD, DIR, HLH_{IN}	5.5	1.0	µA	V_I = 5.5V
		C_{14}–C_{17}	5.5	100		V_I = 5.5V
I_{IL}	Maximum Input Current in Low State	A_9–A_{13}, PLH_{IN}, HD, DIR, HLH_{IN}	5.5	−1.0	µA	V_I = 0.0V
		C_{14}–C_{17}	5.5	−5.0	mA	V_I = 0.0V
I_{OZH}	Maximum Output Disable Current (High)	A_1 — A_8	5.5	20	µA	V_O = 5.5V
		B_1–B_8	5.5	100		V_O = 5.5V
I_{OZL}	Maximum Output Disable Current (Low)	A_1 — A_8	5.5	−20	µA	V_O = 0.0V
		B_1–B_8	5.5	−5.0	mA	
I_{OFF}	Power Down Output Leakage	B_1–B_8, Y_9–Y_{13}, PLH	0.0	100	µA	V_O = 5.5V
I_{OFF}	Power Down Input Leakage	C_{14}–C_{17}, HLH_{IN}	0.0	100	µA	V_I = 5.5V
I_{OFF} — I_{CC}	Power Down Leakage to V_{CC}		0.0	250	µA	(Note 5)
I_{CC}	Maximum Supply Current		5.5	70	mA	V_I = V_{CC} or GND

Note 3: Output impedance is measured with the output active low and active high (HD = high).

Note 4: Resistance is calculated using the following formula:

$$\text{Resistance} = \frac{1V}{(\text{Current at 2V on pin}) - (\text{Current at 1V on pin})}$$

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Note 5: Power-down leakage to V_{CC} is tested by simultaneously forcing all pins on the cable-side (B_1–B_8, Y_9–Y_{13}, PLH, C_{14}–C_{17} and HLH_{IN} to 5.5V and measuring the resulting I_{CC}.

Note 6: This parameter is guaranteed but not tested, characterized only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40^\circ C$ to $+85^\circ C$, $V_{CC} = 4.5V-5.5V$		Units	Fig. No.
		Min	Max		
t_{PHL}	A_1-A_8 to B_1-B_8	2.0	30.0	ns	*Figure 1*
t_{PLH}	A_1-A_8 to B_1-B_8	2.0	30.0	ns	*Figure 2*
t_{PHL}	B_1-B_8 to A_1-A_8	2.0	30.0	ns	*Figure 3*
t_{PLH}	B_1-B_8 to A_1-A_8	2.0	30.0	ns	*Figure 3*
t_{PHL}	A_9-A_{13} to Y_9-Y_{13}	2.0	30.0	ns	*Figure 1*
t_{PLH}	A_9-A_{13} to Y_9-Y_{13}	2.0	30.0	ns	*Figure 2*
t_{PHL}	$C_{14}-C_{17}$ to $A_{14}-A_{17}$	2.0	30.0	ns	*Figure 3*
t_{PLH}	$C_{14}-C_{17}$ to $A_{14}-A_{17}$	2.0	30.0	ns	*Figure 3*
t_{SKEW}	LH-LH or HL-HL		6.0	ns	(Note 8)
t_{PHL}	PLH_{IN} to PLH	2.0	30.0	ns	*Figure 1*
t_{PLH}	PLH_{IN} to PLH	2.0	30.0	ns	*Figure 2*
t_{PHL}	HLH_{IN} to HLH	2.0	30.0	ns	*Figure 3*
t_{PLH}	HLH_{IN} to HLH	2.0	30.0	ns	*Figure 3*
t_{PHZ}	Output Disable Time	2.0	18.0	ns	*Figure 7*
t_{PLZ}	DIR to A_1-A_8	2.0	18.0		
t_{PZH}	Output Enable Time	2.0	25.0	ns	*Figure 8*
t_{PZL}	DIR to A_1-A_8	2.0	25.0		
t_{PHZ}	Output Disable Time	2.0	25.0	ns	*Figure 9*
t_{PLZ}	DIR to B_1-B_8	2.0	25.0		
t_{pEN}	Output Enable Time	2.0	28.0	ns	*Figure 2*
	HD to B_1-B_8, Y_9-Y_{13}				
t_{pDis}	Output Disable Time	2.0	28.0	ns	*Figure 2*
	HD to B_1-B_8, Y_9-Y_{13}				
$t_{pEn}-t_{pDis}$	Output Enable-Output Disable		20.0	ns	
t_{SLEW}	Output Slew Rate				
t_{PLH}	B_1-B_8, Y_9-Y_{13}	0.05	0.40	V/ns	*Figure 5*
t_{PHL}		0.05	0.40		*Figure 4*
t_r, t_f	t_{RISE} and t_{FALL}		120	ns	*Figure 6*
	B_1-B_8, Y_9-Y_{13} (Note 7)		120		(Note 9)

Note 7: Open Drain

Note 8: t_{SKEW} is measured for common edge output transitions and compares the measured propagation delay for a given path type.

(i) A_1-A_8 to B_1-B_8, A_9-Y_{13} to Y_9-Y_{13}

(ii) B_1-B_8 to A_1-A_8

(iii) $C_{14}-C_{17}$ to $A_{14}-A_{17}$

Note 9: This parameter is guaranteed but not tested, characterized only.

Note 10: Pulse Generator for all pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5	pF	V_{CC} = 0.0V (HD, DIR, A_9 — A_{13}, C_{14} — C_{17}, PLH_{IN} and HLH_{IN})
$C_{I/O}$ (Note 11)	I/O Pin Capacitance	12	pF	V_{CC} = 3.3V

Note 11: $C_{I/O}$ is measured at frequency = 1 MHz per MIL-STD-883B. Method 3012

AC Loading and Waveforms

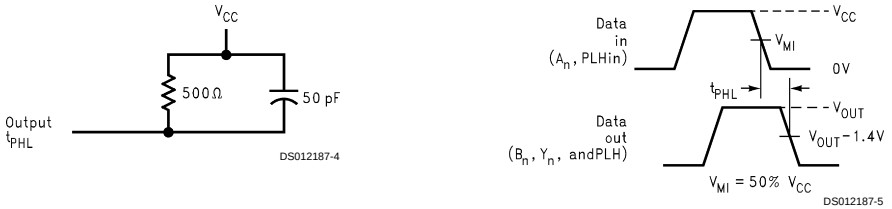

FIGURE 1. t_{PHL} Test Load and Waveforms
A_1–A_8 to B_1–B_8
A_9–A_{13} to Y_9–Y_{13}
PLH_{IN} to PLH

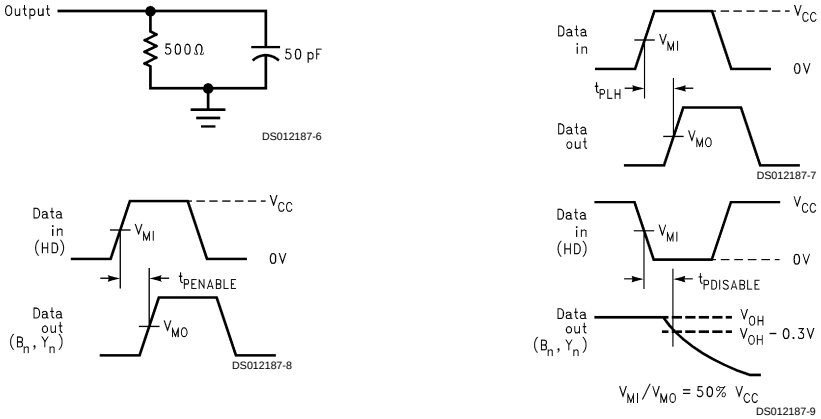

FIGURE 2. t_{PLH}, t_{pEn}, t_{pDis}Test Load and Waveforms
A_1–A_8 to B_1–B_8, A_9–A_{13} to Y_9–Y_{13}
PLH_{IN} to PLH, HD to B_1–B_8, Y_9–Y_{13}, PLH

FIGURE 3. t_{PHL}, t_{PLH} Test Load and Waveforms
B_1–B_8 to A_1–A_8, C_{14}–C_{17} to A_{14}–A_{17}, HLH_{IN} to HLH

AC Loading and Waveforms (Continued)

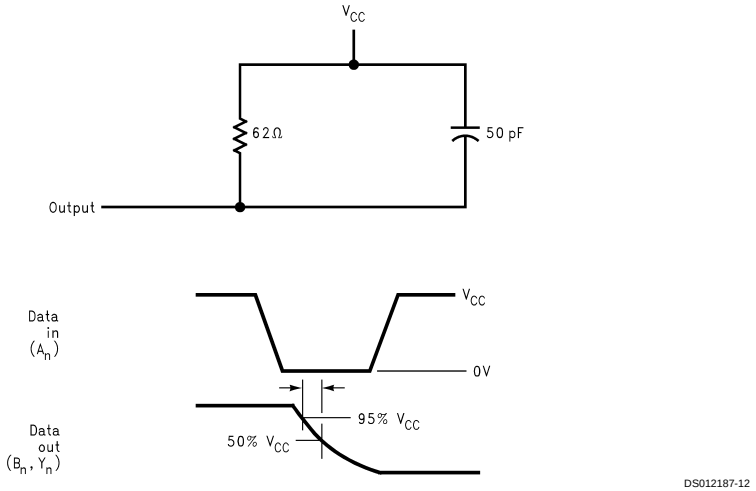

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FIGURE 4. t_{SLEW} HL Test Load and Waveforms
A_1–A_8 to B_1–B_8
A_9–A_{13} to Y_9–Y_{13}

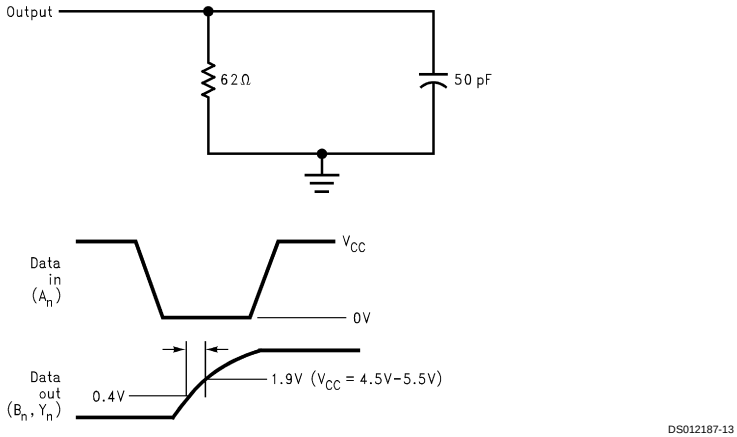

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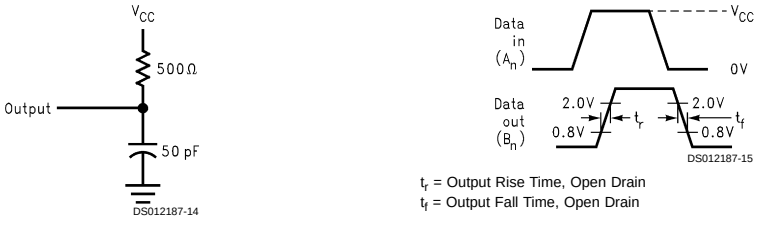
FIGURE 5. t_{SLEW} LH Test Load and Waveforms
A_1–A_8 to B_1–B_8
A_9–A_{13} to Y_9–Y_{13}



t_r = Output Rise Time, Open Drain
t_f = Output Fall Time, Open Drain

FIGURE 6. t_{RISE} and t_{FALL} Test Load and Waveforms for Open Drain Outputs
A_1–A_8 to B_1–B_8, A_9–A_{13} to Y_9–Y_{13}

AC Loading and Waveforms (Continued)

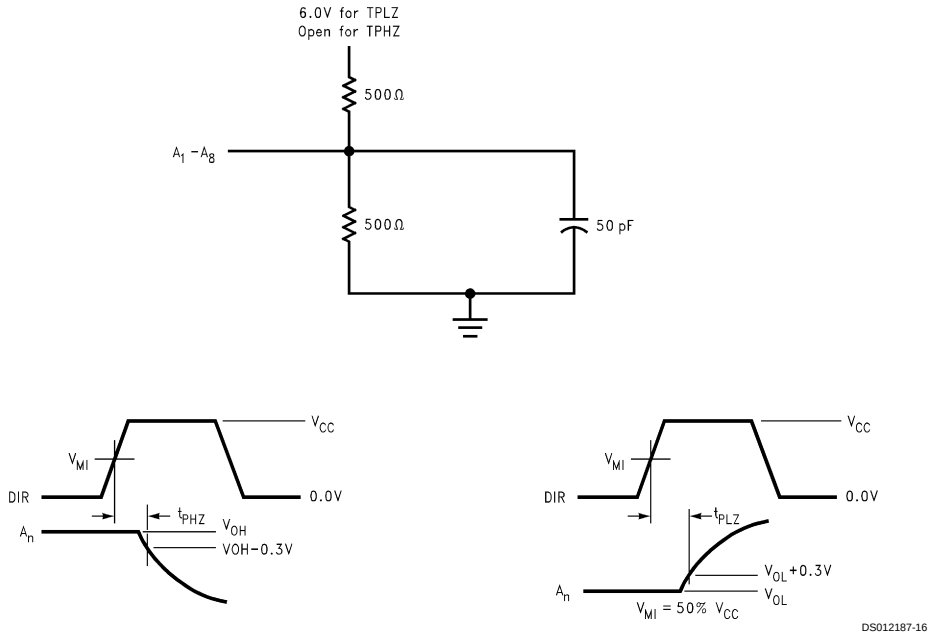


FIGURE 7. t_{PHZ} and t_{PLZ} Test Load and Waveforms, DIR to A_1–A_8

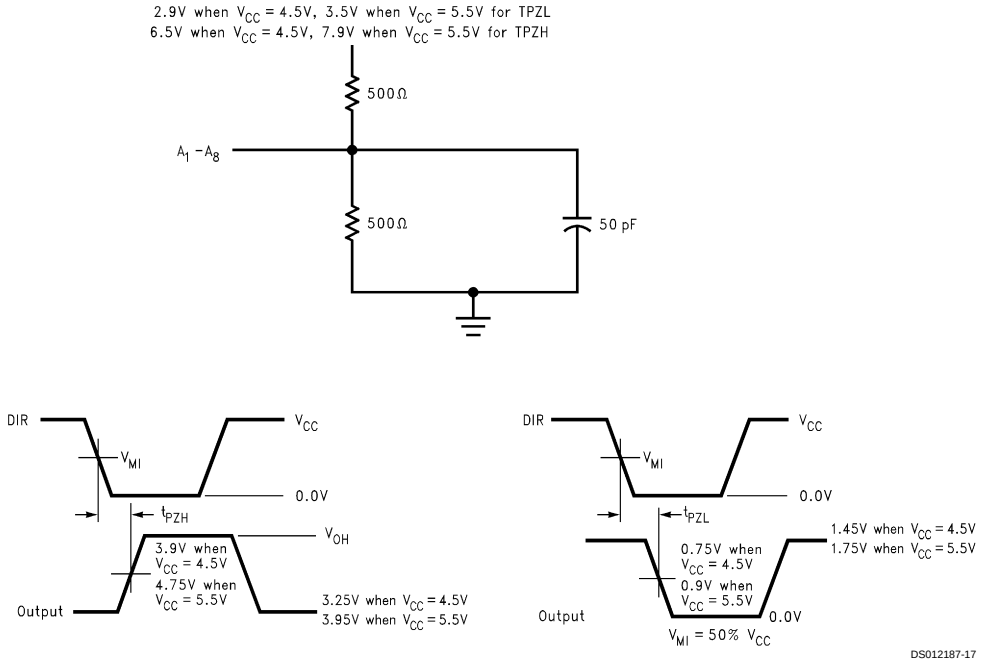


FIGURE 8. t_{PZH} and t_{PZL} Test Load and Waveforms, DIR to A_1–A_8

AC Loading and Waveforms (Continued)

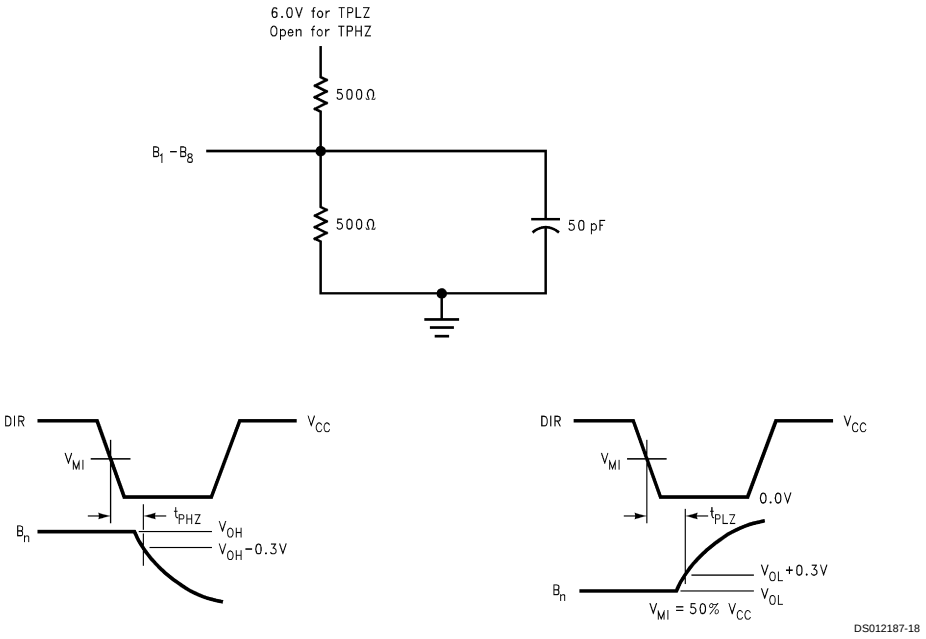
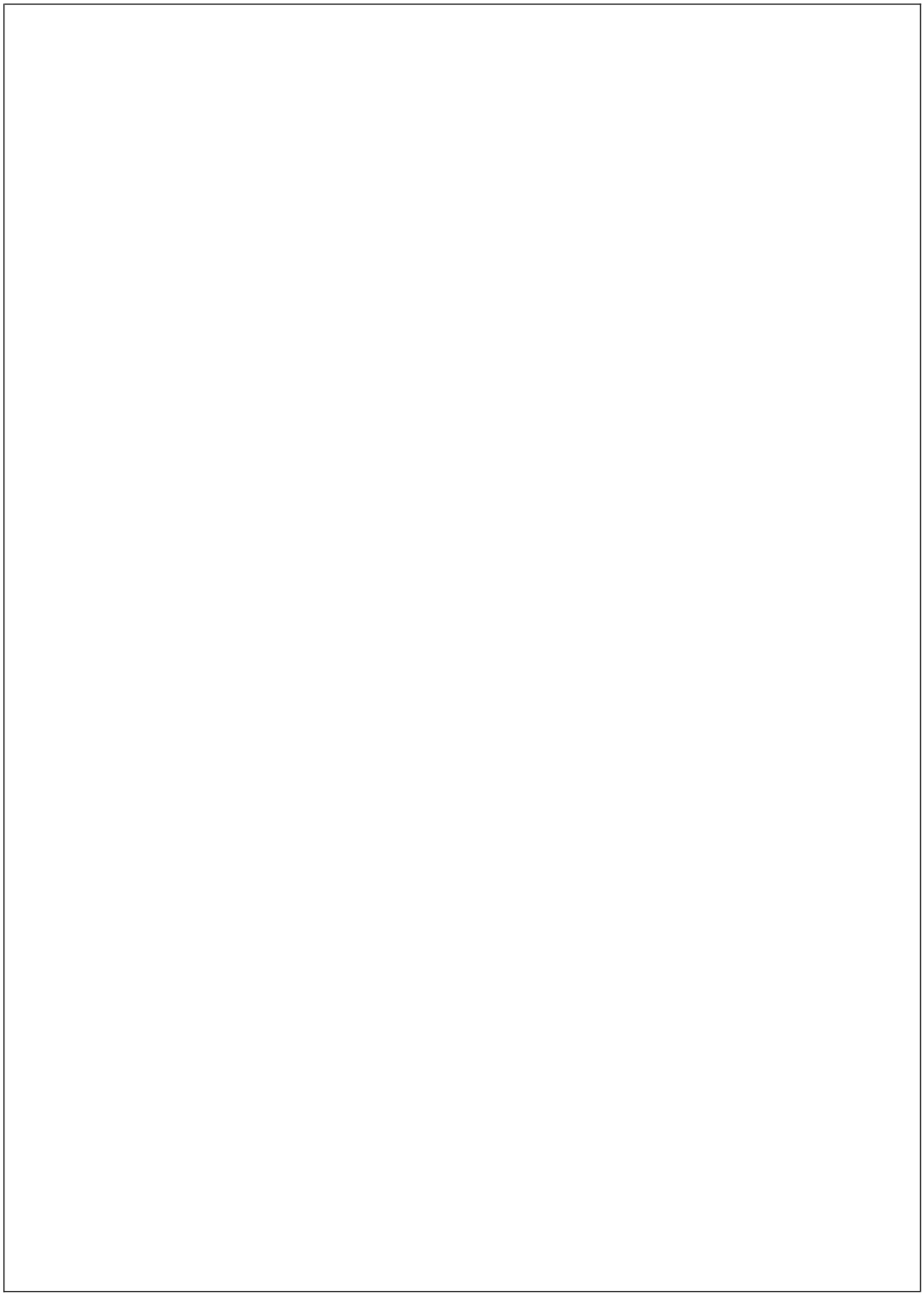
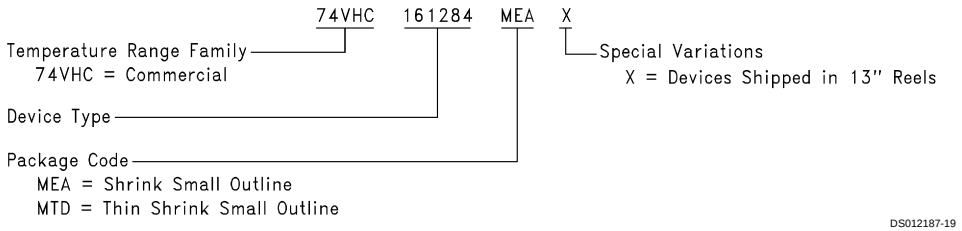


FIGURE 9. t_{PHZ} and t_{PLZ} Test Load and Waveforms, DIR to B_1–B_8



Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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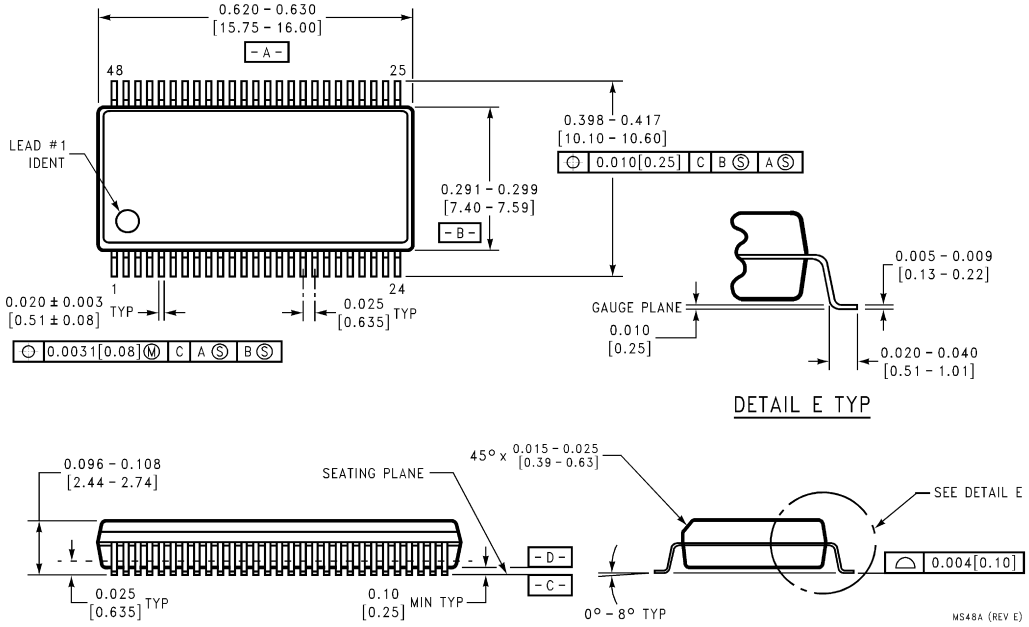
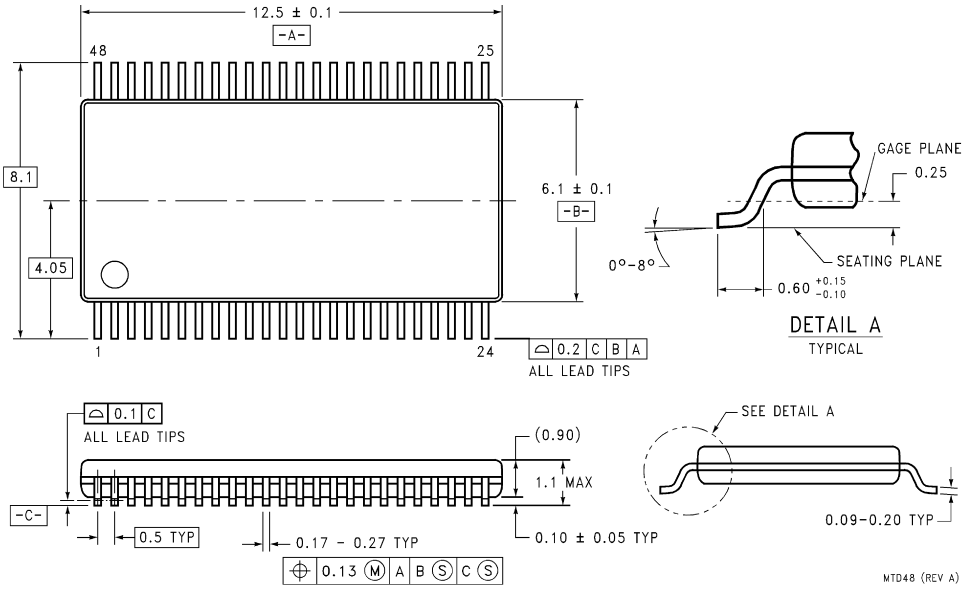
Physical Dimensions inches (millimeters) unless otherwise noted



48-Lead (0.300" Wide) Molded Shrink Small Outline Package, JEDEC
Order Number 74VHC161284MEA or 74VHC161284MEAX
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Molded Thin Shrink Small Outline Package, JEDEC, 6.1mm Body Width
Order Number 74VHC161284MTD or 74VHC161284MTDX
Package Number MTD48

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