CY7C1385D

18-Mbit (512 K × 32) Flow-Through SRAM

Features

- Supports 133 MHz bus operations
- 512 K × 32 common I/O
- 3.3 V core power supply (V_{DD})
- 2.5 V or 3.3 V I/O supply (V_{DDQ})
- Fast clock-to-output time
  - 6.5 ns (133 MHz version)
- Provides high performance 2-1-1-1 access rate
- User selectable burst counter supporting Intel Pentium interleaved or linear burst sequences
- Separate processor and controller address strobes
- Synchronous self-timed write
- Asynchronous output enable
- CY7C1385D is available in JEDEC-standard Pb-free 100-pin TQFP package
- ZZ sleep mode option

Functional Description

The CY7C1385D is a 3.3 V, 512 K × 32 synchronous flow through SRAMs, designed to interface with high speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 6.5 ns (133 MHz version). A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access. All synchronous inputs are gated by registers controlled by a positive edge triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, address pipelining chip enable ($\overline{CE}_1$), depth-expansion chip enables (CE_2 and $\overline{CE}_3$), burst control inputs (ADSC, ADSP, and ADV), write enables (BW_x, and BWE), and global write ($\overline{GW}$). Asynchronous inputs include the output enable ($\overline{OE}$) and the ZZ pin.

The CY7C1385D allows interleaved or linear burst sequences, selected by the MODE input pin. A HIGH selects an interleaved burst sequence, while a LOW selects a linear burst sequence. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

Addresses and chip enables are registered at rising edge of clock when address strobe processor ($\overline{ADSP}$) or address strobe controller ($\overline{ADSC}$) are active. Subsequent burst addresses can be internally generated as controlled by the advance pin ($\overline{ADV}$).

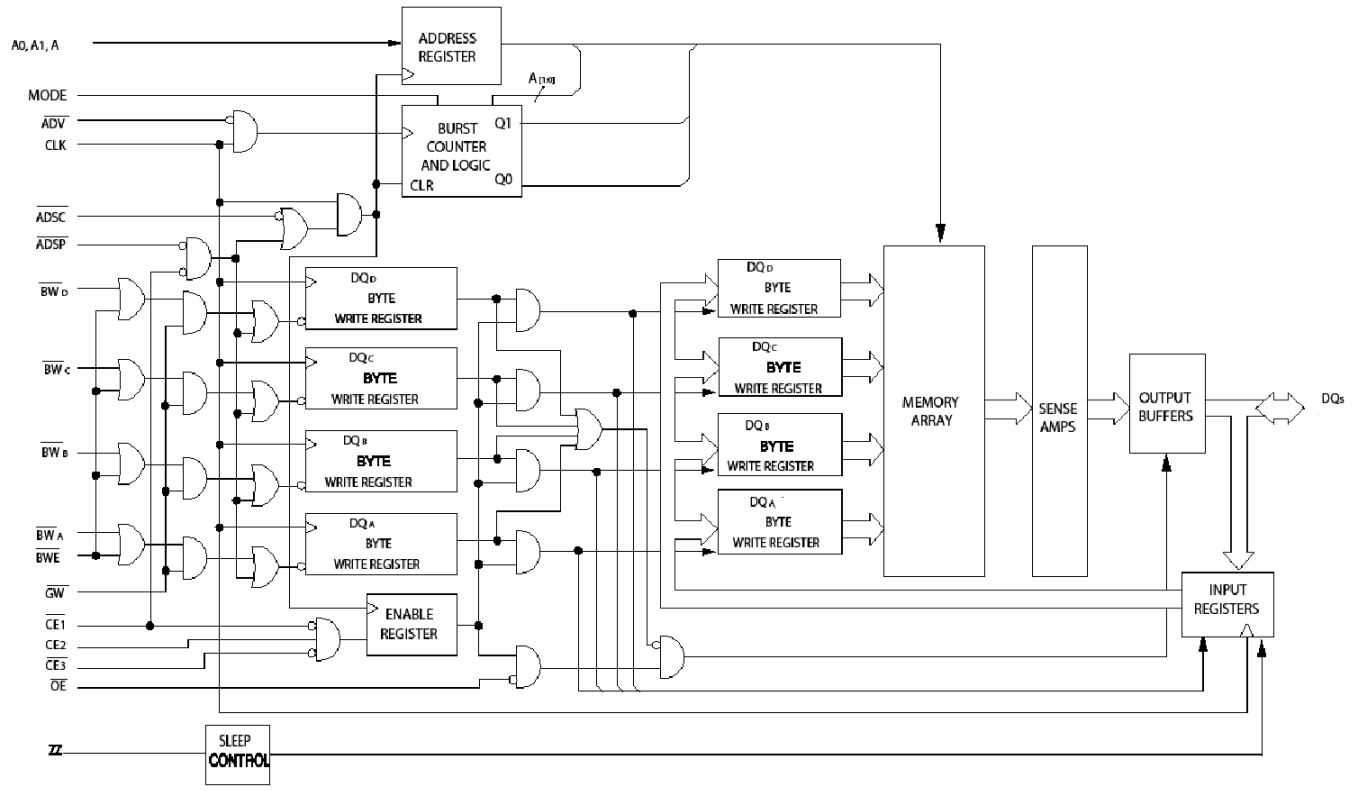
CY7C1385D operates from a +3.3 V core power supply while all outputs operate with a +2.5 V or +3.3 V supply. All inputs and outputs are JEDEC-standard and JESD8-5-compatible.

For a complete list of related resources, click here.

Selection Guide

Description	133 MHz	Unit
Maximum Access Time	6.5	ns
Maximum Operating Current	210	mA
Maximum CMOS Standby Current	70	mA

Logic Block Diagram – CY7C1385D



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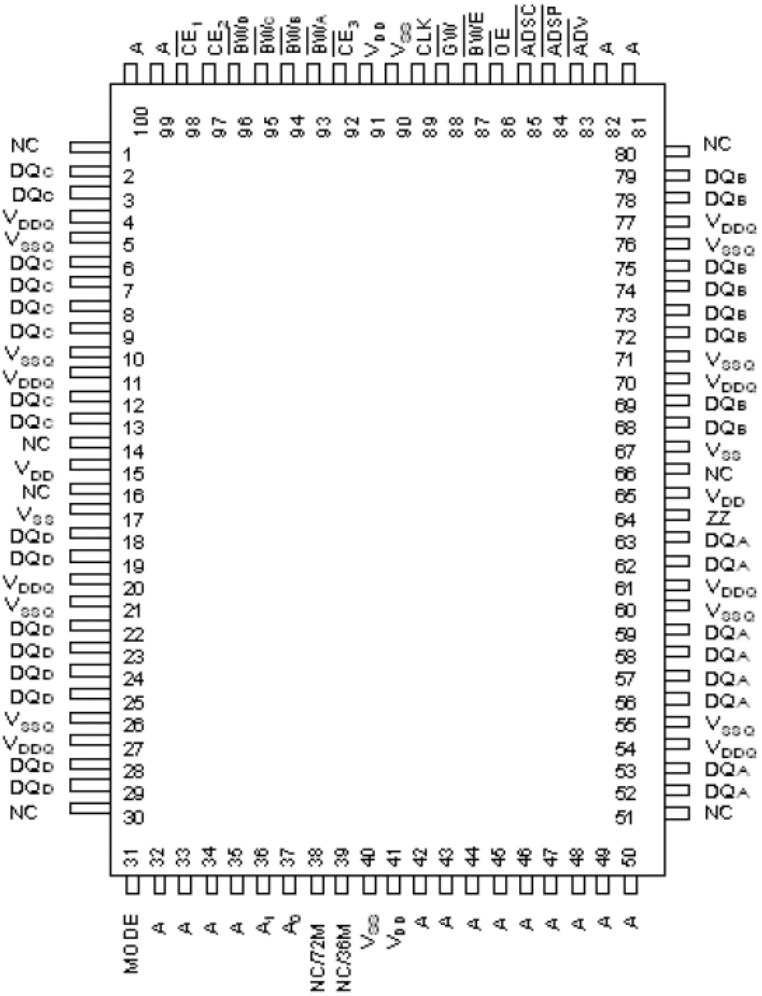
Pin Configurations

Figure 1. 100-pin TQFP (14 × 20 × 1.4 mm) pinout (3 Chip Enable)

CY7C1385D (512 K × 32)



Pin Definitions

Name	I/O	Description
A_0, A_1, A	Input Synchronous	**Address inputs used to select one of the address location**s. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW}_A$, $\overline{BW}_B$, $\overline{BW}_C$, $\overline{BW}_D$	Input Synchronous	**Byte write select inputs, active LOW**. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input Synchronous	**Global write enable input, active LOW**. When asserted LOW on the rising edge of CLK, a global write is conducted (all bytes are written, regardless of the values on $\overline{BW}_{[A:D]}$ and $\overline{BWE}$).
CLK	Input Clock	**Clock input**. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE}_1$	Input Synchronous	**Chip enable 1 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select or deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. $\overline{CE}_1$ is sampled only when a new external address is loaded.
CE_2	Input Synchronous	**Chip enable 2 input, active HIGH**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select or deselect the device. CE_2 is sampled only when a new external address is loaded.
$\overline{CE}_3$	Input Synchronous	**Chip enable 3 input, active LOW**. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select or deselect the device. $\overline{CE}_3$ is sampled only when a new external address is loaded.
$\overline{OE}$	Input Asynchronous	**Output enable, asynchronous input, active LOW**. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input Synchronous	**Advance input signal.** Sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input Synchronous	**Address strobe from processor, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
$\overline{ADSC}$	Input Synchronous	**Address strobe from controller, sampled on the rising edge of CLK, active LOW**. When asserted LOW, addresses presented to the device are captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized·
$\overline{BWE}$	Input Synchronous	**Byte write enable input, active LOW**. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
ZZ	Input Asynchronous	**ZZ sleep input**. This active HIGH input places the device in a non time critical sleep condition with data integrity preserved. For normal operation, this pin has to be LOW or left floating. ZZ pin has an internal pull down.
DQ_s	I/O Synchronous	**Bidirectional data I/O lines**. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by the addresses presented during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, DQ_s are placed in a tristate condition.The outputs are automatically tristated during the data portion of a write sequence, during the first clock when emerging from a deselected state, and when the device is deselected, regardless of the state of $\overline{OE}$.
MODE	Input Static	**Selects burst order**. When tied to GND selects linear burst sequence. When tied to V_{DD} or left floating selects interleaved burst sequence. This is a strap pin and must remain static during device operation. Mode pin has an internal pull-up.
V_{DD}	Power Supply	**Power supply inputs to the core of the device**.

Pin Definitions *(continued)*

Name	I/O	Description
V_{DDQ}	I/O Power Supply	**Power supply for the I/O circuitry**.
V_{SS}	Ground	**Ground for the core of the device**.
V_{SSQ}	I/O Ground	**Ground for the I/O circuitry**.
NC	–	**No connects**. Not internally connected to the die. 36M, 72M, 144M, 288M, 576M, and 1G are address expansion pins and are not internally connected to the die.
V_{SS}/DNU	Ground/DNU	This pin can be connected to ground or can be left floating.

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CDV}) is 6.5 ns (133 MHz device).

CY7C1385D supports secondary cache in systems using a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that use a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the ADV input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the byte write enable ($\overline{BW_E}$) and byte write select ($\overline{BW_X}$) inputs. A global write enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ($\overline{CE_1}$, CE_2, $\overline{CE_3}$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output tristate control. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, and (2) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW (if the access is initiated by $\overline{ADSC}$, the write inputs must be deasserted during this first cycle). The address presented to the address inputs is latched into the address register and the burst counter and/or control logic, and later presented to the memory core. If the OE input is asserted LOW, the requested data is available at the data outputs with a maximum to t_{CDV} after clock rise. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, $\overline{CE_3}$ are all asserted active, and (2) $\overline{ADSP}$ is asserted LOW. The addresses presented are loaded into the address register and the burst inputs ($\overline{GW}$, $\overline{BW_E}$, and $\overline{BW_X}$) are ignored during this first clock cycle. If the write inputs are asserted active (see Truth Table for Read/Write on page 9 for appropriate states that indicate a write) on the next clock rise, the appropriate data is latched and written into the device. Byte writes are allowed. All I/O are tristated during a byte write. As this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/O must be tristated prior to the presentation of data to DQs. As a safety precaution, the data lines are tristated when a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are all asserted active, (2) $\overline{ADSC}$ is asserted LOW, (3) $\overline{ADSP}$ is deasserted HIGH, and (4) the write input signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_X}$) indicate a write access. $\overline{ADSC}$ is ignored if $\overline{ADSP}$ is active LOW.

The addresses presented are loaded into the address register and the burst counter, the control logic, or both, and delivered to the memory core The information presented to $DQ_{[A:D]}$ is written into the specified address location. Byte writes are allowed. All I/O are tristated when a write is detected, even a byte write. Because this is a common I/O device, the asynchronous $\overline{OE}$ input signal must be deasserted and the I/O must be tristated prior to the presentation of data to DQ_s. As a safety precaution, the data lines are tristated when a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

CY7C1385D provides an on-chip two-bit wraparound burst counter inside the SRAM. The burst counter is fed by $A_{[1:0]}$, and can follow either a linear or interleaved burst order. The burst order is determined by the state of the MODE input. A LOW on MODE selects a linear burst sequence. A HIGH on MODE selects an interleaved burst order. Leaving MODE unconnected causes the device to default to a interleaved burst sequence.

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation sleep mode. Two clock cycles are required to enter into or exit from this sleep mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the sleep mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the sleep mode. $\overline{CE_1}$, CE_2, $\overline{CE_3}$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

Interleaved Burst Address Table

(MODE = Floating or V_{DD})

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Address Table

(MODE = GND)

First Address A1:A0	Second Address A1:A0	Third Address A1:A0	Fourth Address A1:A0
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{DDZZ}	Sleep mode standby current	ZZ $\geq$ V_{DD} – 0.2 V	–	80	mA
t_{ZZS}	Device operation to ZZ	ZZ $\geq$ V_{DD} – 0.2 V	–	$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	ZZ $\leq$ 0.2 V	$2t_{CYC}$	–	ns
t_{ZZI}	ZZ active to sleep current	This parameter is sampled	–	$2t_{CYC}$	ns
t_{RZZI}	ZZ inactive to exit sleep current	This parameter is sampled	0	–	ns

Truth Table

The truth table for CY7C1385D follows. [1, 2, 3, 4, 5]

Cycle Description	Address Used	$\overline{CE_1}$	CE_2	$\overline{CE_3}$	ZZ	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power Down	None	H	X	X	L	X	L	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	L	L	X	L	L	X	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	L	X	H	L	L	X	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	L	L	X	L	H	L	X	X	X	L–H	Tri-State
Deselected Cycle, Power Down	None	X	X	X	L	H	L	X	X	X	L–H	Tri-State
Sleep Mode, Power Down	None	X	X	X	H	X	X	X	X	X	X	Tri-State
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	L	L–H	Q
Read Cycle, Begin Burst	External	L	H	L	L	L	X	X	X	H	L–H	Tri-State
Write Cycle, Begin Burst	External	L	H	L	L	H	L	X	L	X	L–H	D
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	L	L–H	Q
Read Cycle, Begin Burst	External	L	H	L	L	H	L	X	H	H	L–H	Tri-State
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L–H	Tri-State
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L–H	Q
Read Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L–H	Tri-State
Write Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L–H	D
Write Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L–H	D
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L–H	Tri-State
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L–H	Q
Read Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L–H	Tri-State
Write Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L–H	D
Write Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L–H	D

Notes
1. X = Don't Care, H = Logic HIGH, L = Logic LOW.
2. $\overline{WRITE}$ = L when any one or more byte write enable signals, and $\overline{BWE}$ = L or $\overline{GW}$ = L. $\overline{WRITE}$ = H when all byte write enable signals, $\overline{BWE}$, $\overline{GW}$ = H.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.
4. The SRAM always initiates a read cycle when $\overline{ADSP}$ is asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW_X}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to tristate. $\overline{OE}$ is a don't care for the remainder of the write cycle.
5. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle all data bits are tristate when $\overline{OE}$ is inactive or when the device is deselected, and all data bits behave as output when $\overline{OE}$ is active (LOW).

Truth Table for Read/Write

The truth table for CY7C1385D read/write follows.

Function (CY7C1385D)	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_D}$	$\overline{BW_C}$	$\overline{BW_B}$	$\overline{BW_A}$
Read	H	H	X	X	X	X
Read	H	L	H	H	H	H
Write Byte A (DQ_A)	H	L	H	H	H	L
Write Byte B(DQ_B)	H	L	H	H	L	H
Write Bytes A, B (DQ_A, DQ_B)	H	L	H	H	L	L
Write Byte C (DQ_C)	H	L	H	L	H	H
Write Bytes C, A (DQ_C, DQ_A)	H	L	H	L	H	L
Write Bytes C, B (DQ_C, $DQ_{B,}$)	H	L	H	L	L	H
Write Bytes C, B, A (DQ_C, DQ_B, DQ_A)	H	L	H	L	L	L
Write Byte D (DQ_D)	H	L	L	H	H	H
Write Bytes D, A (DQ_D, DQ_A)	H	L	L	H	H	L
Write Bytes D, B (DQ_D, DQ_A)	H	L	L	H	L	H
Write Bytes D, B, A (DQ_D, DQ_B, DQ_A)	H	L	L	H	L	L
Write Bytes D, B (DQ_D, DQ_B)	H	L	L	L	H	H
Write Bytes D, B, A (DQ_D, DQ_C, DQ_A)	H	L	L	L	H	L

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. For user guidelines, not tested.

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage on V_{DD} Relative to GND .....–0.3 V to +4.6 V

Supply Voltage on V_{DDQ} Relative to GND .... –0.3 V to +V_{DD}

DC Voltage Applied to Outputs in Tri-State .....–0.5 V to V_{DDQ} + 0.5 V

DC Input Voltage .....–0.5 V to V_{DD} + 0.5 V

Current into Outputs (LOW) .....20 mA

Static Discharge Voltage (per MIL-STD-883, Method 3015) .....> 2001 V

Latch-up Current .....> 200 mA

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Industrial	–40 °C to +85 °C	3.3 V – 5% / + 10%	2.5 V – 5% to V_{DD}

Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max [6]	Unit
LSBU	Logical Single-Bit Upsets	25 °C	361	394	FIT/ Mb
LMBU	Logical Multi-Bit Upsets	25 °C	0	0.01	FIT/ Mb
SEL	Single Event Latch Up	85 °C	0	0.1	FIT/ Dev

Electrical Characteristics

Over the Operating Range

Parameter [7, 8]	Description	Test Conditions		Min	Max	Unit
V_{DD}	Power Supply Voltage			3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	for 3.3 V I/O		3.135	V_{DD}	V
		for 2.5 V I/O		2.375	2.625	V
V_{OH}	Output HIGH Voltage	for 3.3 V I/O, I_{OH} = –4.0 mA		2.4	–	V
		for 2.5 V I/O, I_{OH} = –1.0 mA		2.0	–	V
V_{OL}	Output LOW Voltage	for 3.3 V I/O, I_{OL} = 8.0 mA		–	0.4	V
		for 2.5 V I/O, I_{OL} = 1.0 mA		–	0.4	V
V_{IH}	Input HIGH Voltage [7]	for 3.3 V I/O		2.0	V_{DD} + 0.3 V	V
		for 2.5 V I/O		1.7	V_{DD} + 0.3 V	V
V_{IL}	Input LOW Voltage [7]	for 3.3 V I/O		–0.3	0.8	V
		for 2.5 V I/O		–0.3	0.7	V
I_X	Input Leakage Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30	–	µA
		Input = V_{DD}		–	5	µA
	Input Current of ZZ	Input = V_{SS}		–5	–	µA
		Input = V_{DD}		–	30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DD}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = 1/t_{CYC}	7.5 ns cycle, 133 MHz	–	210	mA

Notes

6. No LMBU or SEL events occurred during testing; this column represents a statistical c2, 95% confidence limit calculation. For more details refer to Application Note AN54908 – Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates.
7. Overshoot: $V_{IH(AC)}$ < V_{DD} + 1.5 V (pulse width less than t_{CYC}/2), undershoot: $V_{IL(AC)}$ > –2 V (pulse width less than t_{CYC}/2).
8. $T_{power\ up}$: Assumes a linear ramp from 0 V to $V_{DD(min)}$ within 200 ms. During this time V_{IH} < V_{DD} and V_{DDQ} ≤ V_{DD}.

Electrical Characteristics *(continued)*

Over the Operating Range

Parameter [7, 8]	Description	Test Conditions		Min	Max	Unit
I_{SB1}	Automatic CE Power Down Current – TTL Inputs	Max V_{DD}, Device Deselected, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz	–	140	mA
I_{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max V_{DD}, Device Deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = 0, inputs static	All speeds	–	70	mA
I_{SB3}	Automatic CE Power Down Current – CMOS Inputs	Max V_{DD}, Device Deselected, $V_{IN} \geq V_{DDQ} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = f_{MAX}, inputs switching	7.5 ns cycle, 133 MHz	–	130	mA
I_{SB4}	Automatic CE Power Down Current – TTL Inputs	Max V_{DD}, Device Deselected, $V_{IN} \geq V_{DD} - 0.3$ V or $V_{IN} \leq 0.3$ V, f = 0, inputs static	All Speeds	–	80	mA

Capacitance

Parameter [9]	Description	Test Conditions	100-pin TQFP Package	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{DD} = 3.3 V, V_{DDQ} = 2.5 V	5	pF
C_{CLK}	Clock input capacitance		5	pF
C_{IO}	Input/Output capacitance		5	pF

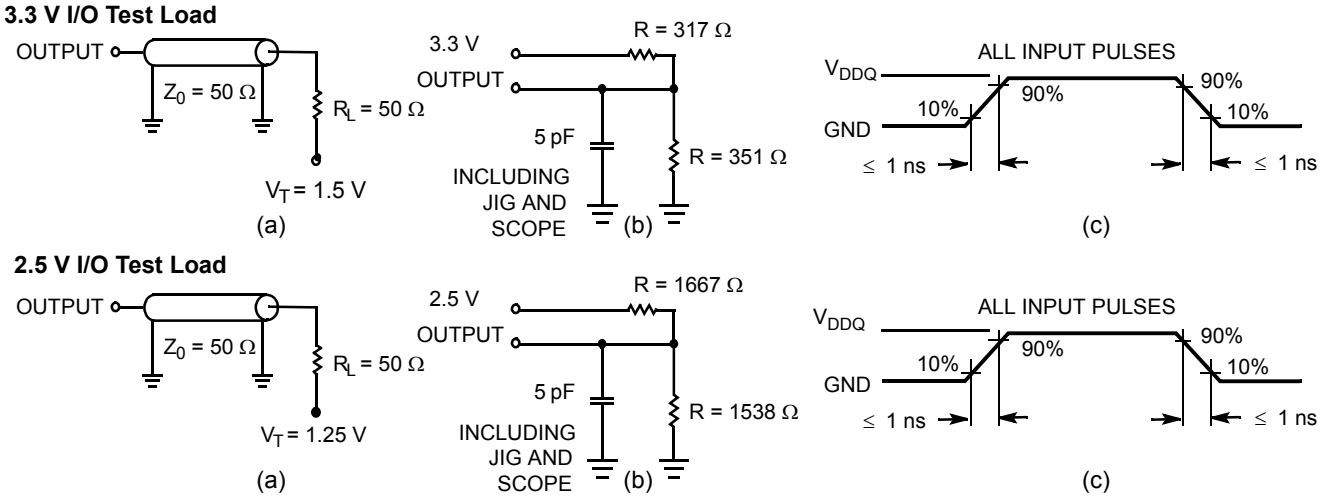
Thermal Resistance

Parameter [9]	Description	Test Conditions	100-pin TQFP Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	28.66	°C/W
Θ_{JC}	Thermal resistance (junction to case)		4.08	°C/W

Note
9. Tested initially and after any design or process change that may affect these parameters.

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Switching Characteristics

Over the Operating Range

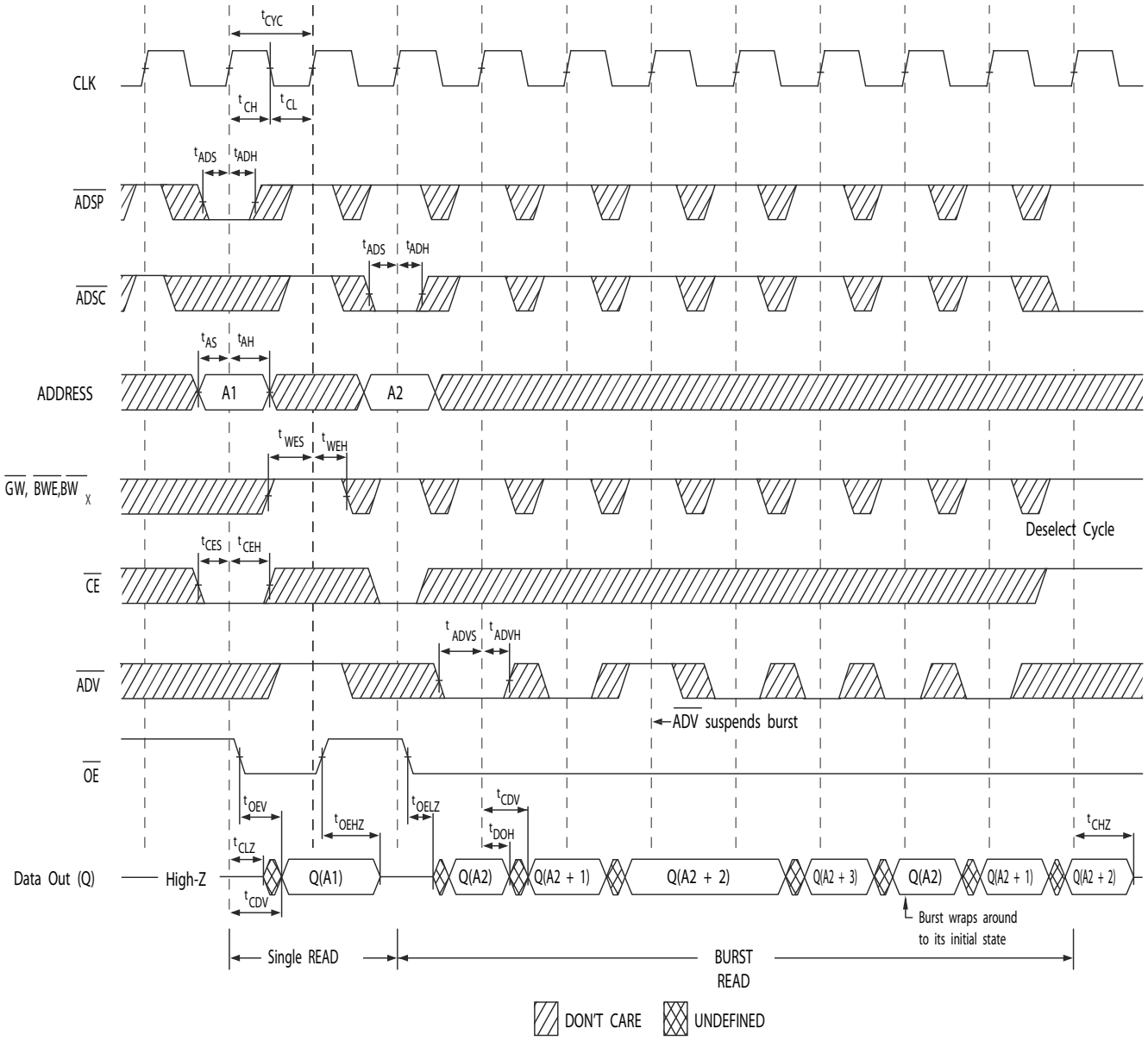
Parameter [10, 11]	Description	133 MHz		Unit
		Min	Max	
t_{POWER}	V_{DD}(typical) to the first access [12]	1	–	ms
Clock				
t_{CYC}	Clock cycle time	7.5	–	ns
t_{CH}	Clock HIGH	2.1	–	ns
t_{CL}	Clock LOW	2.1	–	ns
Output Times				
t_{CDV}	Data output valid after CLK rise	–	6.5	ns
t_{DOH}	Data output hold after CLK rise	2.0	–	ns
t_{CLZ}	Clock to low Z [13, 14, 15]	2.0	–	ns
t_{CHZ}	Clock to high Z [13, 14, 15]	0	4.0	ns
t_{OEV}	$\overline{OE}$ LOW to output valid	–	3.2	ns
t_{OELZ}	$\overline{OE}$ LOW to output low Z [13, 14, 15]	0	–	ns
t_{OEHZ}	$\overline{OE}$ HIGH to output high Z [13, 14, 15]	–	4.0	ns
Setup Times				
t_{AS}	Address setup before CLK rise	1.5	–	ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ setup before CLK rise	1.5	–	ns
t_{ADVS}	$\overline{ADV}$ setup before CLK rise	1.5	–	ns
t_{WES}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ setup before CLK rise	1.5	–	ns
t_{DS}	Data input setup before CLK rise	1.5	–	ns
t_{CES}	Chip enable setup	1.5	–	ns
Hold Times				
t_{AH}	Address hold after CLK rise	0.5	–	ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ hold after CLK rise	0.5	–	ns
t_{WEH}	$\overline{GW}$, $\overline{BWE}$, $\overline{BW}_{[A:D]}$ hold after CLK rise	0.5	–	ns
t_{ADVH}	$\overline{ADV}$ hold after CLK rise	0.5	–	ns
t_{DH}	Data input hold after CLK rise	0.5	–	ns
t_{CEH}	Chip enable hold after CLK rise	0.5	–	ns

Notes

10. Timing reference level is 1.5 V when V_{DDQ} = 3.3 V and is 1.25 V when V_{DDQ} = 2.5 V.
11. Test conditions shown in (a) of Figure 2 on page 12 unless otherwise noted.
12. This part has a voltage regulator internally; t_{POWER} is the time that the power needs to be supplied above $V_{DD(minimum)}$ initially, before a read or write operation can be initiated.
13. t_{CHZ}, t_{CLZ}, t_{OELZ}, and t_{OEHZ} are specified with AC test conditions shown in part (b) of Figure 2 on page 12. Transition is measured ±200 mV from steady-state voltage.
14. At any given voltage and temperature, t_{OEHZ} is less than t_{OELZ} and t_{CHZ} is less than t_{CLZ} to eliminate bus contention between SRAMs when sharing the same data bus. These specifications do not imply a bus contention condition, but reflect parameters guaranteed over worst case user conditions. Device is designed to achieve high Z prior to low Z under the same system condition.
15. This parameter is sampled and not 100% tested.

Timing Diagrams

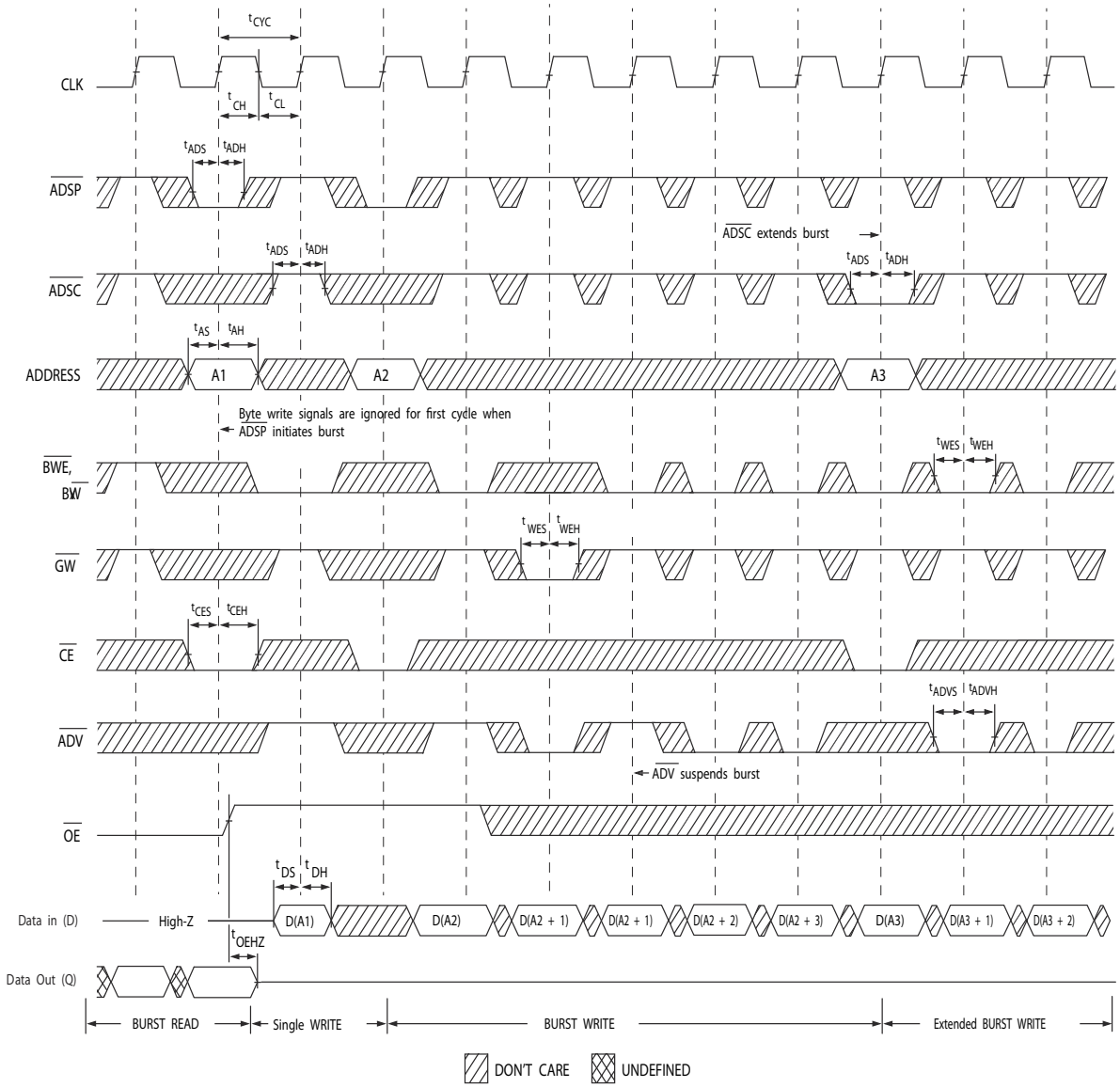
Figure 3. Read Cycle Timing [16]



Note
16. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.

Timing Diagrams *(continued)*

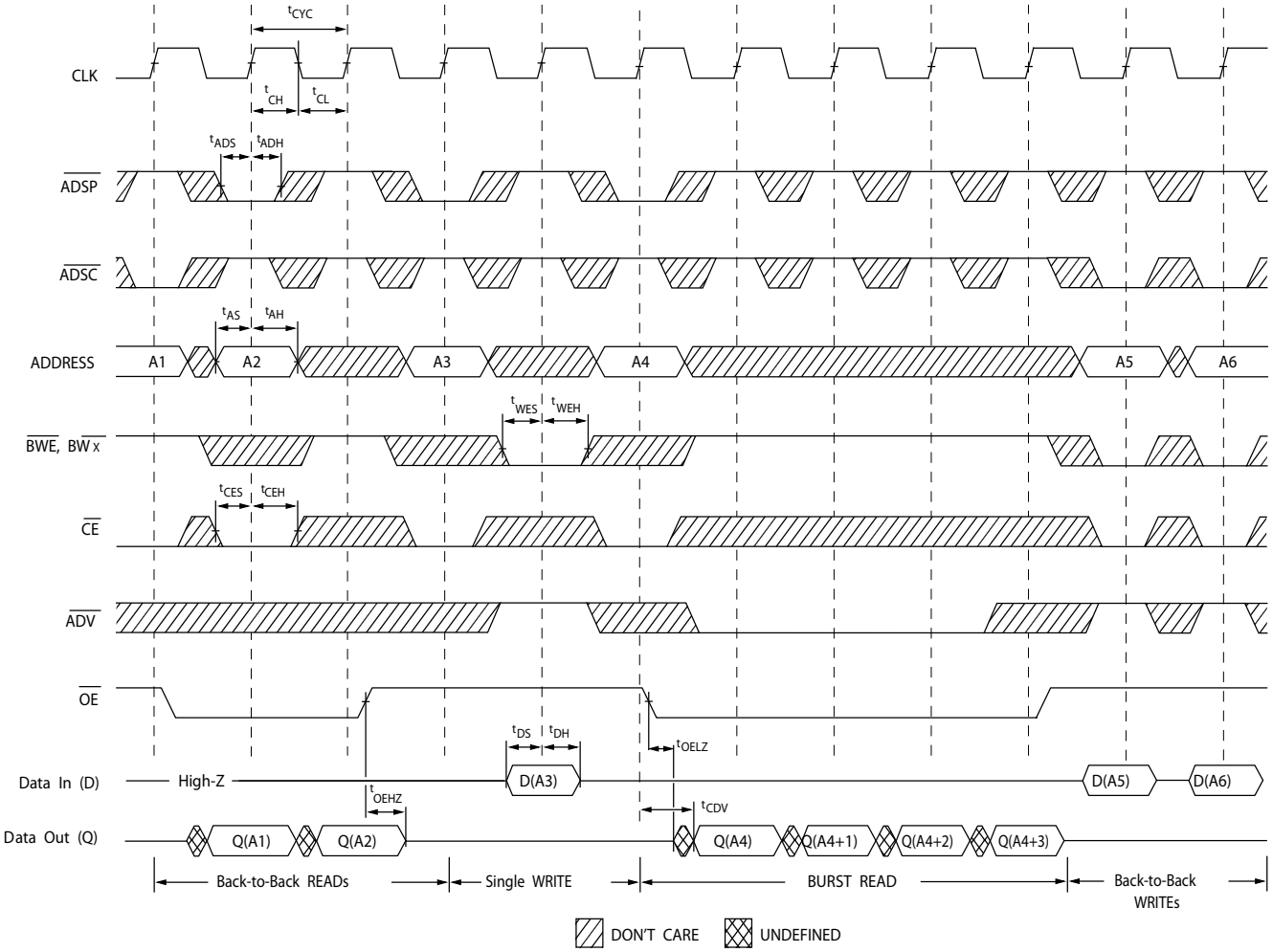
Figure 4. Write Cycle Timing [17, 18]



Notes
17. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
18. Full width write can be initiated by either $\overline{GW}$ LOW; or by $\overline{GW}$ HIGH, $\overline{BWE}$ LOW and $\overline{BW}_X$ LOW.

Timing Diagrams *(continued)*

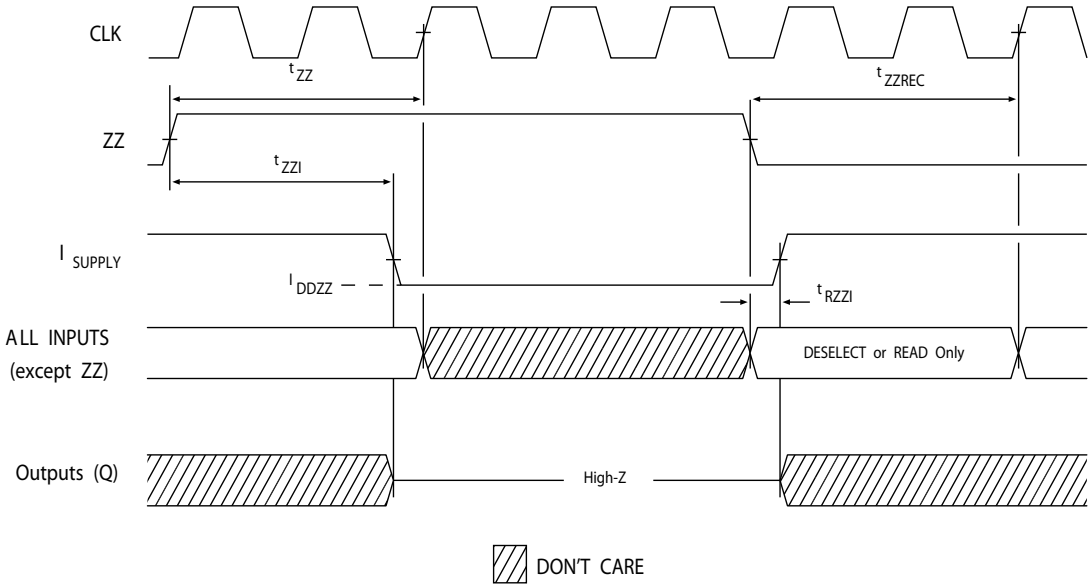
Figure 5. Read/Write Cycle Timing [19, 20, 21]



Notes
19. On this diagram, when $\overline{CE}$ is LOW: $\overline{CE}_1$ is LOW, CE_2 is HIGH and $\overline{CE}_3$ is LOW. When $\overline{CE}$ is HIGH: $\overline{CE}_1$ is HIGH or CE_2 is LOW or $\overline{CE}_3$ is HIGH.
20. The data bus (Q) remains in high Z following a WRITE cycle, unless a new read access is initiated by $\overline{ADSP}$ or $\overline{ADSC}$.
21. $\overline{GW}$ is HIGH.

Timing Diagrams *(continued)*

Figure 6. ZZ Mode Timing [22, 23]



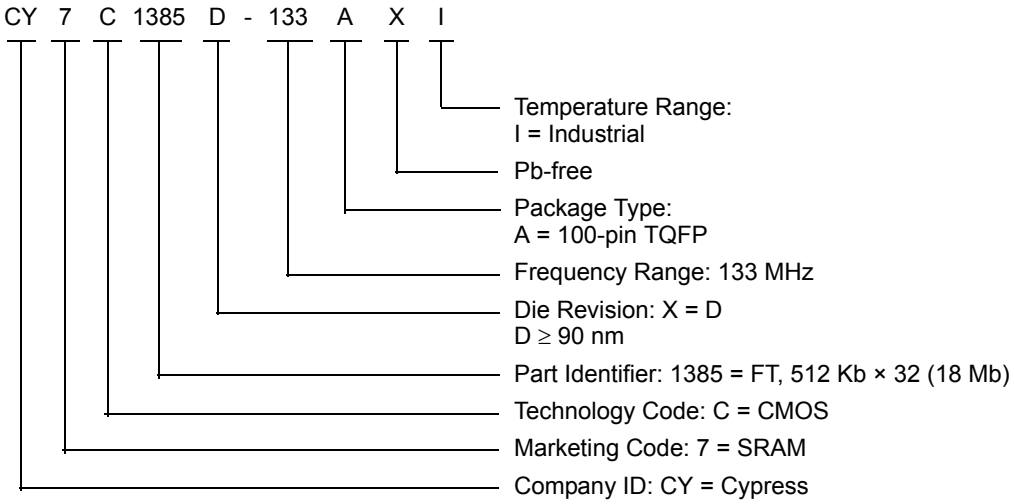
Notes
22. Device must be deselected when entering ZZ mode. See Truth Table on page 8 for all possible signal conditions to deselect the device.
23. DQs are in high Z when exiting ZZ sleep mode.

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The below table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative. Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at t http://www.cypress.com/go/datasheet/offices.

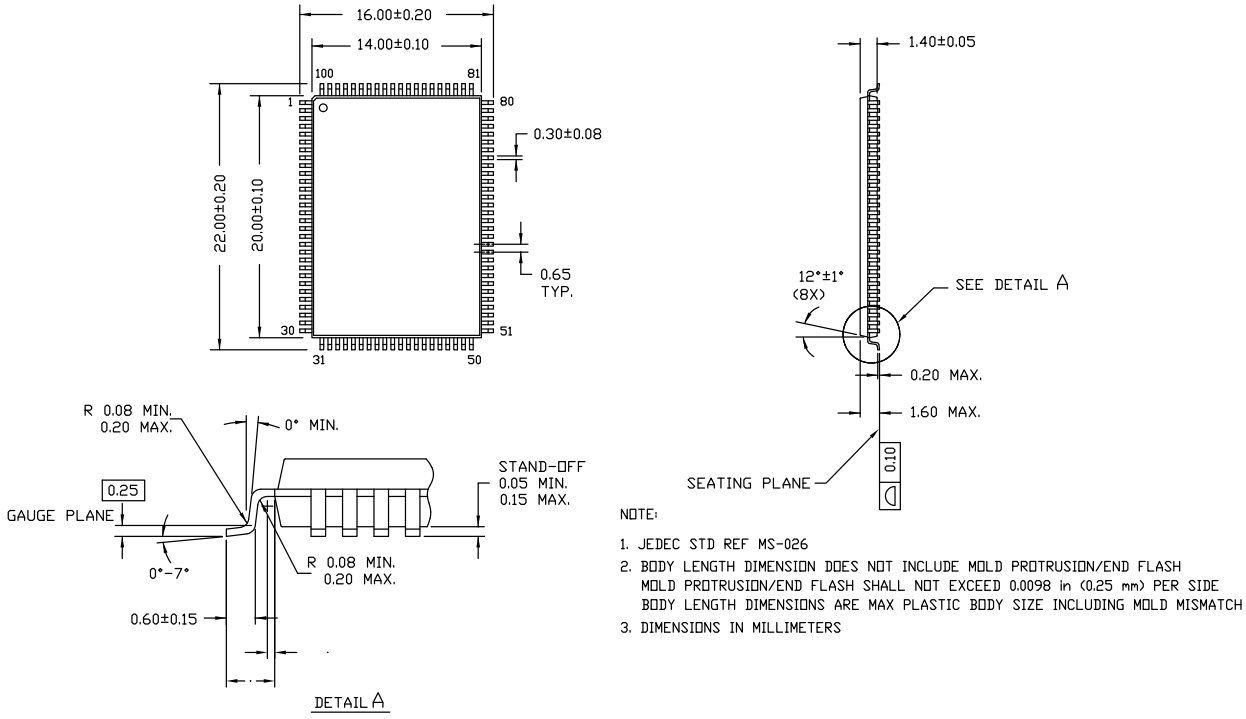
Speed (MHz)	Ordering Code	Package Diagram	Part and Package Type	Operating Range
133	CY7C1385D-133AXI	51-85050	100-pin TQFP (14 × 20 × 1.4 mm) Pb-free	Industrial

Ordering Code Definitions



Package Diagrams

Figure 7. 100-pin TQFP (14 × 20 × 1.4 mm) A100RA Package Outline, 51-85050



51-85050 *E

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LMBU	Logical Multi-Bit Upsets
LSBU	Logical Single-Bit Upsets
$\overline{OE}$	Output Enable
SEL	Single Event Latch-up
SRAM	Static Random Access Memory
TQFP	Thin Quad Flat Pack
TTL	Transistor-Transistor Logic

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1385D, 18-Mbit (512 K × 32) Flow-Through SRAM Document Number: 001-74016				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3454705	NJY	12/04/2011	New data sheet.
*A	3617718	PRIT / NJY	05/15/2012	Changed status from Preliminary to Final.
*B	4585009	PRIT	12/02/2014	Updated Functional Description: Added “For a complete list of related resources, click here.” at the end. Updated Timing Diagrams: Updated Figure 3, Figure 4, Figure 5, Figure 6. Updated Package Diagrams: spec 51-85050 – Changed revision from *D to *E. Updated to new template. Completing Sunset Review.
*C	5067238	PRIT	12/29/2015	Updated to new template. Completing Sunset Review.

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