

## LM5109 100V/1A Peak Half Bridge Gate Driver

Check for Samples: [LM5109](#)

### FEATURES

- Drives Both a High Side and Low Side N-Channel MOSFET
- 1A Peak Output Current (1.0A Sink / 1.0A Source)
- Independent TTL Compatible Inputs
- Bootstrap Supply Voltage to 118V DC
- Fast Propagation Times (27 ns Typical)
- Drives 1000 pF Load with 15ns Rise and Fall Times
- Excellent Propagation Delay Matching (2 ns Typical)
- Supply Rail Under-voltage Lockout
- Low Power Consumption
- Pin Compatible with ISL6700

### PACKAGE

- SOIC-8
- WSON-8 (4 mm x 4 mm)

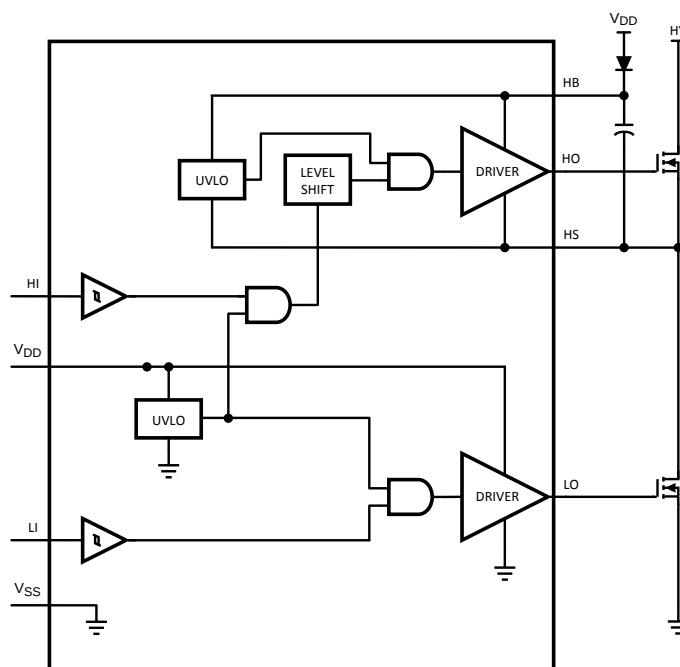
### DESCRIPTION

The LM5109 is a low cost high voltage gate driver, designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 100V. The outputs are independently controlled with TTL compatible input thresholds. A robust level shifter technology operates at high speed while consuming low power and providing clean level transitions from the control input logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails. The device is available in the SOIC-8 and the thermally enhanced WSON-8 packages.

### TYPICAL APPLICATIONS

- Current Fed Push-pull Converters
- Half and Full Bridge Power Converters
- Solid State Motor Drives
- Two Switch Forward Power Converters

### SIMPLIFIED BLOCK DIAGRAM



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## CONNECTION DIAGRAMS



**Figure 1.**

**Table 1. PIN DESCRIPTION**

| Pin No. |                       | Name            | Description                                | Application Information                                                                                                                                                                         |
|---------|-----------------------|-----------------|--------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SO-8    | WSON-8 <sup>(1)</sup> |                 |                                            |                                                                                                                                                                                                 |
| 1       | 1                     | V <sub>DD</sub> | Positive gate drive supply                 | Locally decouple to V <sub>SS</sub> using low ESR/ESL capacitor located as close to IC as possible.                                                                                             |
| 2       | 2                     | HI              | High side control input                    | The LM5109 HI input is compatible with TTL input thresholds. Unused HI input should be tied to ground and not left open                                                                         |
| 3       | 3                     | LI              | Low side control input                     | The LM5109 LI input is compatible with TTL input thresholds. Unused LI input should be tied to ground and not left open.                                                                        |
| 4       | 4                     | V <sub>SS</sub> | Ground reference                           | All signals are referenced to this ground.                                                                                                                                                      |
| 5       | 5                     | LO              | Low side gate driver output                | Connect to the gate of the low side N-MOS device.                                                                                                                                               |
| 6       | 6                     | HS              | High side source connection                | Connect to the negative terminal of the bootstrap capacitor and to the source of the high side N-MOS device.                                                                                    |
| 7       | 7                     | HO              | High side gate driver output               | Connect to the gate of the low side N-MOS device.                                                                                                                                               |
| 8       | 8                     | HB              | High side gate driver positive supply rail | Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal of the bootstrap capacitor to HS. The bootstrap capacitor should be placed as close to IC as possible. |

- (1) For WSON-8 package it is recommended that the exposed pad on the bottom of the LM5109 be soldered to ground plane on the PCB board and the ground plane should extend out from underneath the package to improve heat dissipation.

## ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.

|                               |                                    |
|-------------------------------|------------------------------------|
| $V_{DD}$ to $V_{SS}$          | -0.3V to 18V                       |
| HB to HS                      | -0.3V to 18V                       |
| LI or HI to $V_{SS}$          | -0.3V to $V_{DD} + 0.3V$           |
| LO to $V_{SS}$                | -0.3V to $V_{DD} + 0.3V$           |
| HO to $V_{SS}$                | $V_{HS} - 0.3V$ to $V_{HB} + 0.3V$ |
| HS to $V_{SS}$ <sup>(2)</sup> | -5V to 100V                        |
| HB to $V_{SS}$                | 118V                               |
| Junction Temperature          | -40°C to +150°C                    |
| Storage Temperature Range     | -55°C to +150°C                    |
| ESD Rating HBM <sup>(3)</sup> | 2 kV                               |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings **do not** imply specified performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics tables.
- (2) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than  $V_{DD} - 15V$ . For example, if  $V_{DD} = 10V$ , the negative transients at HS must not exceed -5V.
- (3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. Pin 6, Pin 7 and Pin 8 are rated at 500V.

## RECOMMENDED OPERATING CONDITIONS

|                      |                                 |
|----------------------|---------------------------------|
| $V_{DD}$             | 8V to 14V                       |
| HS <sup>(1)</sup>    | -1V to 100V                     |
| HB                   | $V_{HS} + 8V$ to $V_{HS} + 14V$ |
| HS Slew Rate         | < 50 V/ns                       |
| Junction Temperature | -40°C to +125°C                 |

- (1) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than  $V_{DD} - 15V$ . For example, if  $V_{DD} = 10V$ , the negative transients at HS must not exceed -5V.

## ELECTRICAL CHARACTERISTICS

Specifications in standard typeface are for  $T_J = +25^\circ\text{C}$ , and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified,  $V_{DD} = V_{HB} = 12V$ ,  $V_{SS} = V_{HS} = 0V$ , No Load on LO or HO.

| Symbol                          | Parameter                          | Conditions                  | Min <sup>(1)</sup> | Typ  | Max <sup>(1)</sup> | Units |
|---------------------------------|------------------------------------|-----------------------------|--------------------|------|--------------------|-------|
| <b>SUPPLY CURRENTS</b>          |                                    |                             |                    |      |                    |       |
| $I_{DD}$                        | $V_{DD}$ Quiescent Current         | LI = HI = 0V                |                    | 0.3  | <b>0.6</b>         | mA    |
| $I_{DDO}$                       | $V_{DD}$ Operating Current         | f = 500 kHz                 |                    | 2.1  | <b>3.4</b>         | mA    |
| $I_{HB}$                        | Total HB Quiescent Current         | LI = HI = 0V                |                    | 0.06 | <b>0.2</b>         | mA    |
| $I_{HBO}$                       | Total HB Operating Current         | f = 500 kHz                 |                    | 1.6  | <b>3.0</b>         | mA    |
| $I_{HBS}$                       | HB to $V_{SS}$ Current, Quiescent  | $V_{HS} = V_{HB} = 100V$    |                    | 0.1  | <b>10</b>          | μA    |
| $I_{HBSO}$                      | HB to $V_{SS}$ Current, Operating  | f = 500 kHz                 |                    | 0.5  |                    | mA    |
| <b>INPUT PINS LI and HI</b>     |                                    |                             |                    |      |                    |       |
| $V_{IL}$                        | Low Level Input Voltage Threshold  |                             | <b>0.8</b>         | 1.8  |                    | V     |
| $V_{IH}$                        | High Level Input Voltage Threshold |                             |                    | 1.8  | <b>2.2</b>         | V     |
| $R_I$                           | Input Pulldown Resistance          |                             | <b>100</b>         | 180  | <b>500</b>         | kΩ    |
| <b>UNDER VOLTAGE PROTECTION</b> |                                    |                             |                    |      |                    |       |
| $V_{DDR}$                       | $V_{DD}$ Rising Threshold          | $V_{DDR} = V_{DD} - V_{SS}$ | <b>6.0</b>         | 6.9  | <b>7.4</b>         | V     |

- (1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Texas Instrument's Average Outgoing Quality Level (AOQL).

## ELECTRICAL CHARACTERISTICS (continued)

Specifications in standard typeface are for  $T_J = +25^{\circ}\text{C}$ , and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified,  $V_{DD} = V_{HB} = 12\text{V}$ ,  $V_{SS} = V_{HS} = 0\text{V}$ , No Load on LO or HO.

| Symbol                    | Parameter                     | Conditions                                              | Min <sup>(1)</sup> | Typ  | Max <sup>(1)</sup> | Units                |
|---------------------------|-------------------------------|---------------------------------------------------------|--------------------|------|--------------------|----------------------|
| $V_{DDH}$                 | $V_{DD}$ Threshold Hysteresis |                                                         |                    | 0.5  |                    | V                    |
| $V_{HBR}$                 | HB Rising Threshold           | $V_{HBR} = V_{HB} - V_{HS}$                             | <b>5.7</b>         | 6.6  | <b>7.1</b>         | V                    |
| $V_{HBH}$                 | HB Threshold Hysteresis       |                                                         |                    | 0.4  |                    | V                    |
| <b>LO GATE DRIVER</b>     |                               |                                                         |                    |      |                    |                      |
| $V_{OLL}$                 | Low-Level Output Voltage      | $I_{LO} = 100\text{ mA}$ , $V_{OHL} = V_{LO} - V_{SS}$  |                    | 0.28 | <b>0.45</b>        | V                    |
| $V_{OHL}$                 | High-Level Output Voltage     | $I_{LO} = -100\text{ mA}$ , $V_{OHL} = V_{DD} - V_{LO}$ |                    | 0.45 | <b>0.75</b>        | V                    |
| $I_{OHL}$                 | Peak Pullup Current           | $V_{LO} = 0\text{V}$                                    |                    | 1.0  |                    | A                    |
| $I_{OLL}$                 | Peak Pulldown Current         | $V_{LO} = 12\text{V}$                                   |                    | 1.0  |                    | A                    |
| <b>HO GATE DRIVER</b>     |                               |                                                         |                    |      |                    |                      |
| $V_{OLH}$                 | Low-Level Output Voltage      | $I_{HO} = 100\text{ mA}$ , $V_{OLH} = V_{HO} - V_{HS}$  |                    | 0.28 | <b>0.45</b>        | V                    |
| $V_{OHH}$                 | High-Level Output Voltage     | $I_{HO} = -100\text{ mA}$ , $V_{OHH} = V_{HB} - V_{HO}$ |                    | 0.45 | <b>0.75</b>        | V                    |
| $I_{OHH}$                 | Peak Pullup Current           | $V_{HO} = 0\text{V}$                                    |                    | 1.0  |                    | A                    |
| $I_{OLH}$                 | Peak Pulldown Current         | $V_{HO} = 12\text{V}$                                   |                    | 1.0  |                    | A                    |
| <b>THERMAL RESISTANCE</b> |                               |                                                         |                    |      |                    |                      |
| $\theta_{JA}^{(2)}$       | Junction to Ambient           | SOIC-8                                                  |                    | 160  |                    | $^{\circ}\text{C/W}$ |
|                           |                               | WSO8-8 <sup>(3)</sup>                                   |                    | 40   |                    |                      |

(2) The  $\theta_{JA}$  is not a constant for the package and depends on the printed circuit board design and the operating conditions.

(3) 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187 ([SNOA401](#)).

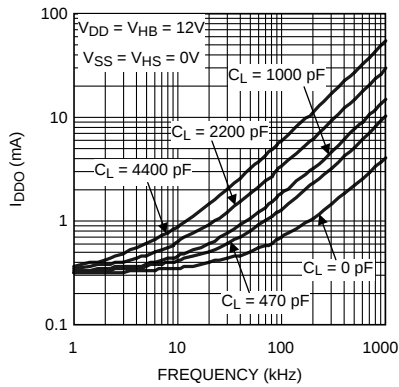
## SWITCHING CHARACTERISTICS

Specifications in standard typeface are for  $T_J = +25^{\circ}\text{C}$ , and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified,  $V_{DD} = V_{HB} = 12\text{V}$ ,  $V_{SS} = V_{HS} = 0\text{V}$ , No Load on LO or HO.

| Symbol              | Parameter                                                   | Conditions             | Min | Typ | Max       | Units |
|---------------------|-------------------------------------------------------------|------------------------|-----|-----|-----------|-------|
| <b>LM5109</b>       |                                                             |                        |     |     |           |       |
| $t_{LPHL}$          | Lower Turn-Off Propagation Delay (LI Falling to LO Falling) |                        |     | 27  | <b>56</b> | ns    |
| $t_{HPHL}$          | Upper Turn-Off Propagation Delay (HI Falling to HO Falling) |                        |     | 27  | <b>56</b> | ns    |
| $t_{LPLH}$          | Lower Turn-On Propagation Delay (LI Rising to LO Rising)    |                        |     | 29  | <b>56</b> | ns    |
| $t_{HPLH}$          | Upper Turn-On Propagation Delay (HI Rising to HO Rising)    |                        |     | 29  | <b>56</b> | ns    |
| $t_{MON}$           | Delay Matching: Lower Turn-On and Upper Turn-Off            |                        |     | 2   | <b>15</b> | ns    |
| $t_{MOFF}$          | Delay Matching: Lower Turn-Off and Upper Turn-On            |                        |     | 2   | <b>15</b> | ns    |
| $t_{RC}$ , $t_{FC}$ | Either Output Rise/Fall Time                                | $C_L = 1000\text{ pF}$ |     | 15  | -         | ns    |
| $t_{PW}$            | Minimum Input Pulse Width that Changes the Output           |                        |     | 50  |           | ns    |

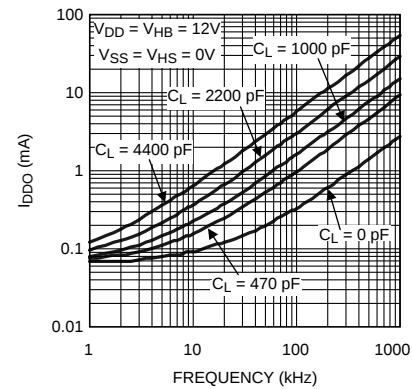
## TYPICAL PERFORMANCE CHARACTERISTICS

**V<sub>DD</sub> Operating Current vs Frequency**



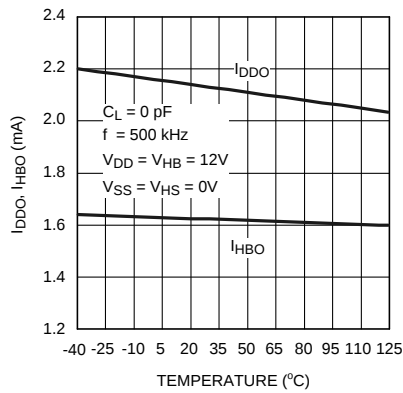
**Figure 2.**

**HB Operating Current vs Frequency**



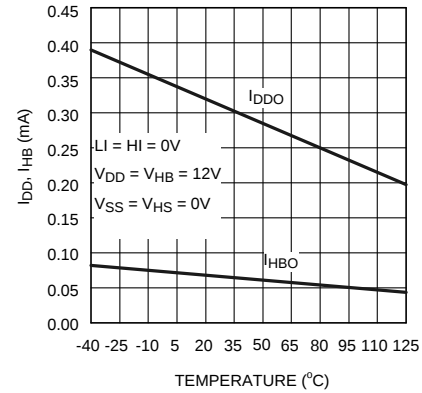
**Figure 3.**

**Operating Current vs Temperature**



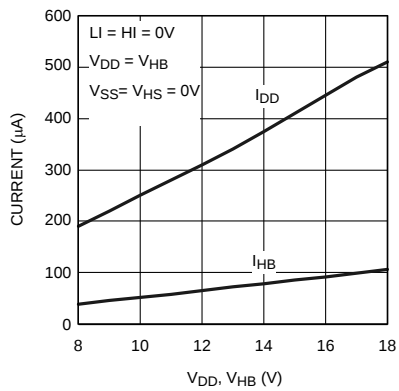
**Figure 4.**

**Quiescent Current vs Temperature**



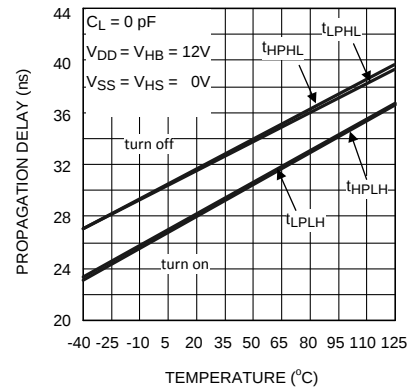
**Figure 5.**

**Quiescent Current vs Voltage**



**Figure 6.**

**Propagation Delay vs Temperature**



**Figure 7.**

## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

### LO and HO High Level Output Voltage vs Temperature

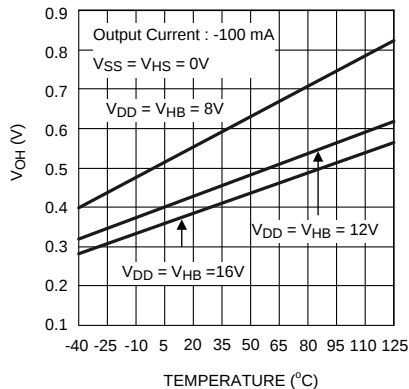


Figure 8.

### LO and HO Low Level Output Voltage vs Temperature

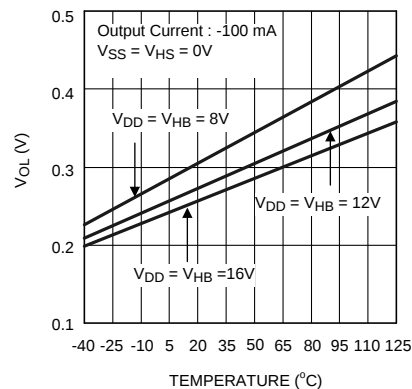


Figure 9.

### Undervoltage Rising Thresholds vs Temperature

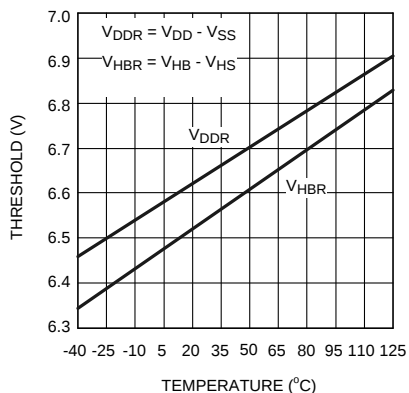


Figure 10.

### Undervoltage Hysteresis vs Temperature

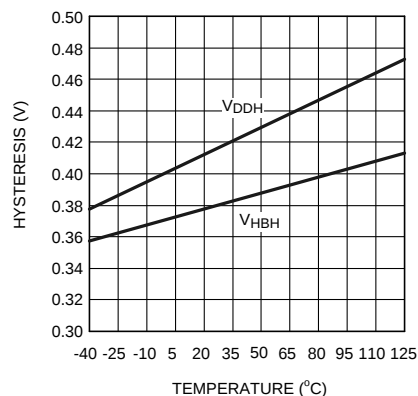


Figure 11.

### Input Thresholds vs Temperature

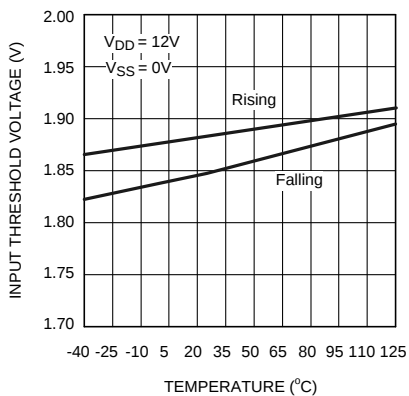


Figure 12.

### Input Thresholds vs Supply Voltage

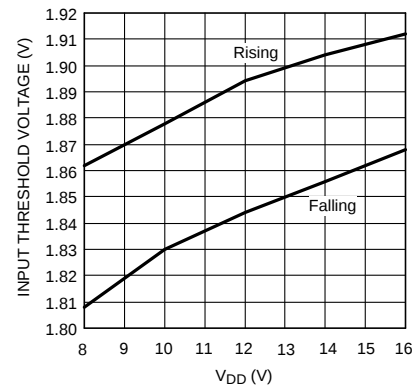
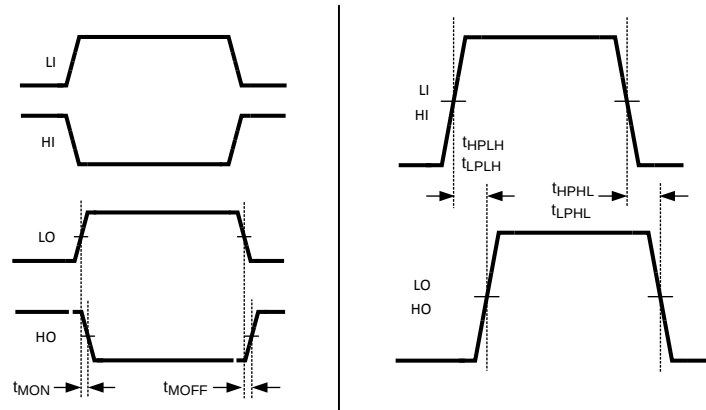


Figure 13.

## TIMING DIAGRAM



## LAYOUT CONSIDERATIONS

The optimum performance of high and low side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR / ESL capacitor must be connected close to the IC, and between  $V_{DD}$  and  $V_{SS}$  pins and between HB and HS pins to support high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground ( $V_{SS}$ ).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
  - (a) The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
  - (b) The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced  $V_{DD}$  bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

## HS TRANSIENT VOLTAGES BELOW GROUND

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than -0.3V below HS can activate parasitic transistors resulting in excessive current to flow from the HB supply possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 15V or less. Hence, if the HS pin transient voltage is -5V, VDD should be ideally limited to 10V to keep HB to HS below 15V.
3. A low ESR bypass capacitor between HB to HS as well as VDD to VSS is essential for proper operation. The capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

## PACKAGING INFORMATION

| Orderable part number | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C)           | Part marking<br>(6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|------------------------|---------------------|
| LM5109MA/NOPB         | Active        | Production           | SOIC (D)   8   | 95   TUBE             | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -                      | L5109<br>MA         |
| LM5109MA/NOPB.A       | Active        | Production           | SOIC (D)   8   | 95   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | See LM5109MA/NOPB      | L5109<br>MA         |
| LM5109MA/NOPB.B       | Active        | Production           | SOIC (D)   8   | 95   TUBE             | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | See LM5109MA/NOPB      | L5109<br>MA         |
| LM5109MAX/NOPB        | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU   SN                          | Level-1-260C-UNLIM                | -                      | L5109<br>MA         |
| LM5109MAX/NOPB.A      | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | See LM5109MAX/<br>NOPB | L5109<br>MA         |
| LM5109MAX/NOPB.B      | Active        | Production           | SOIC (D)   8   | 2500   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | See LM5109MAX/<br>NOPB | L5109<br>MA         |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM5109MAX/NOPB | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.5     | 5.4     | 2.0     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device         | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM5109MAX/NOPB | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |

## TUBE



\*All dimensions are nominal

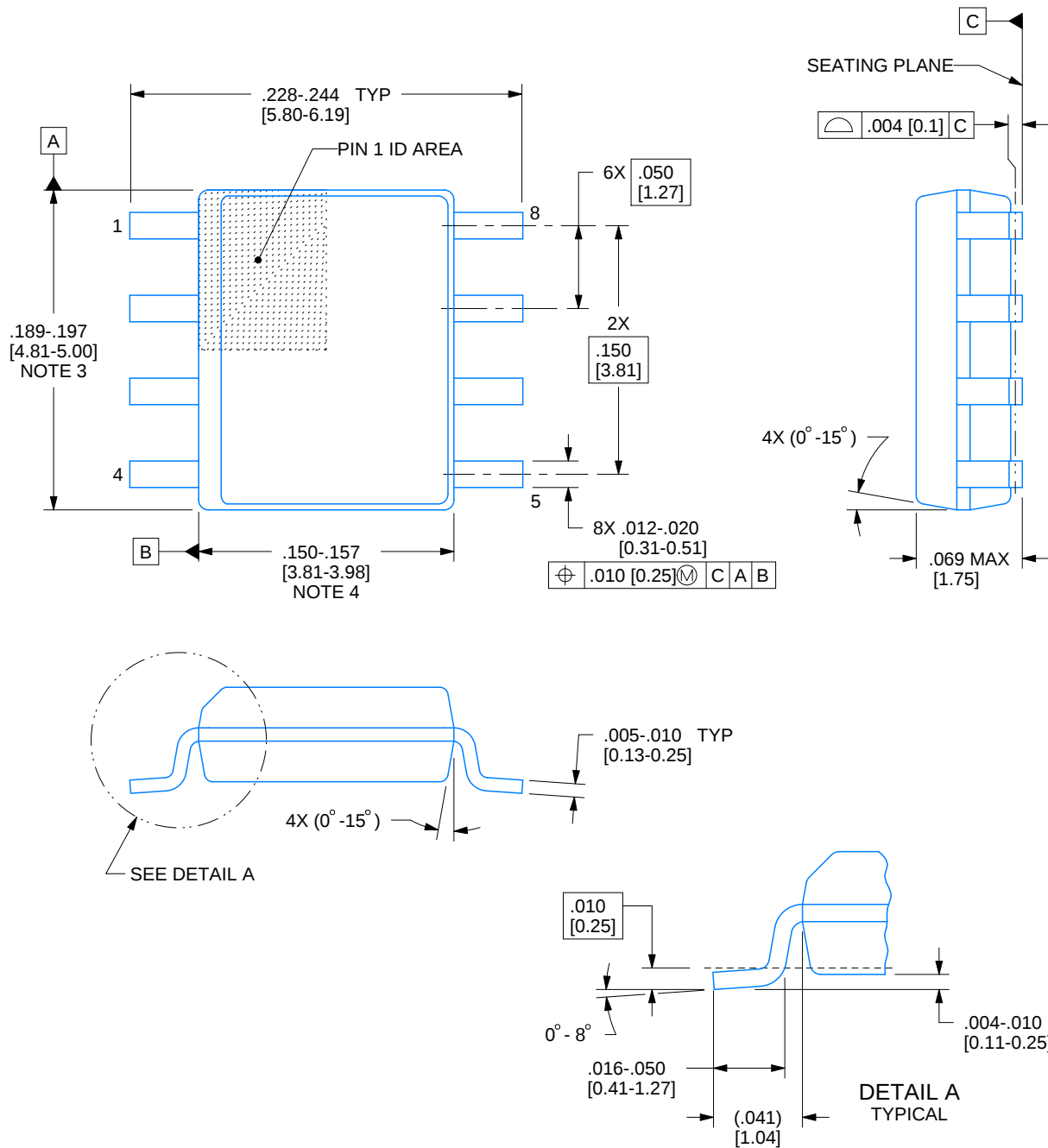
| Device          | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| LM5109MA/NOPB   | D            | SOIC         | 8    | 95  | 495    | 8      | 4064   | 3.05   |
| LM5109MA/NOPB.A | D            | SOIC         | 8    | 95  | 495    | 8      | 4064   | 3.05   |
| LM5109MA/NOPB.B | D            | SOIC         | 8    | 95  | 495    | 8      | 4064   | 3.05   |

**D0008A**

## PACKAGE OUTLINE

**SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

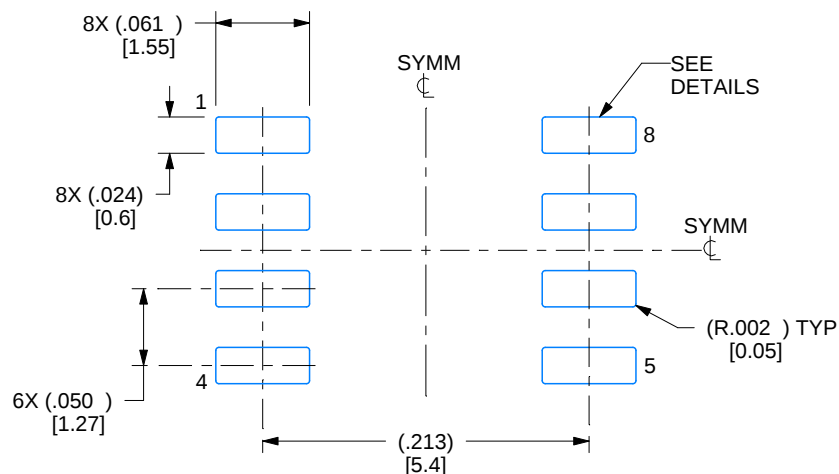
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

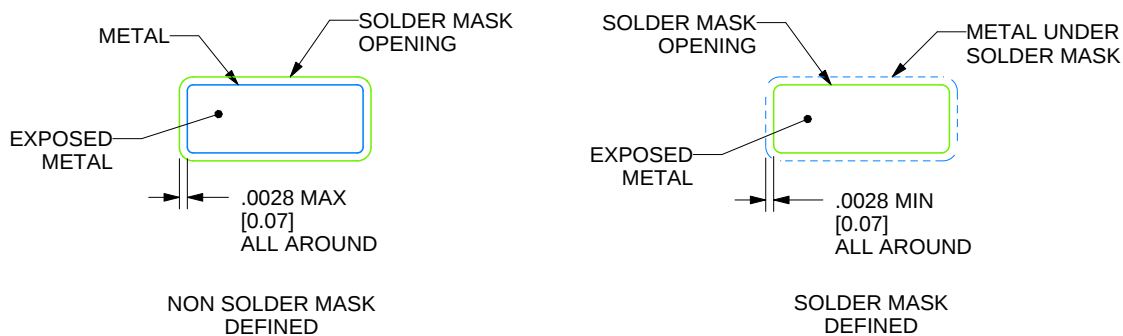
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

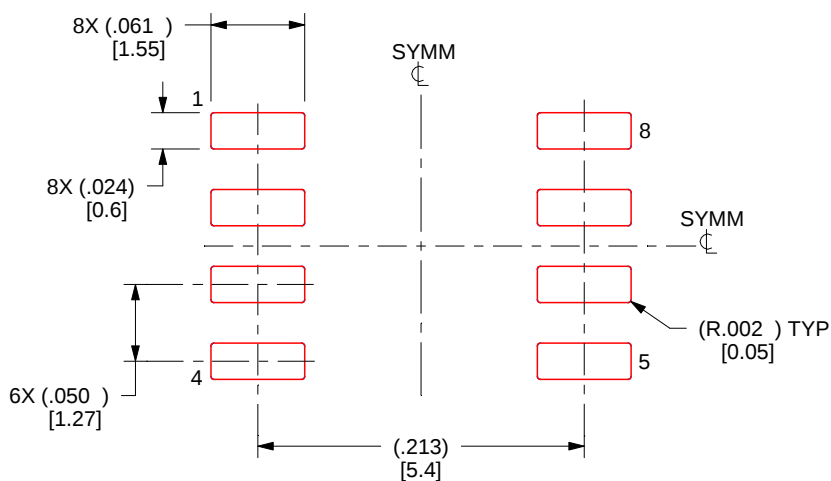
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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