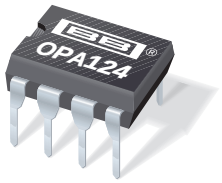
BURR - BROWN®



OPA124

Low Noise Precision *Difet*® OPERATIONAL AMPLIFIER

FEATURES

- LOW NOISE: 6nV/√Hz (10kHz)
- LOW BIAS CURRENT: 1pA max
- LOW OFFSET: 250μV max
- LOW DRIFT: 2μV/°C max
- HIGH OPEN-LOOP GAIN: 120dB min
- HIGH COMMON-MODE REJECTION: 100dB min
- AVAILABLE IN 8-PIN PLASTIC DIP AND 8-PIN SOIC PACKAGES

APPLICATIONS

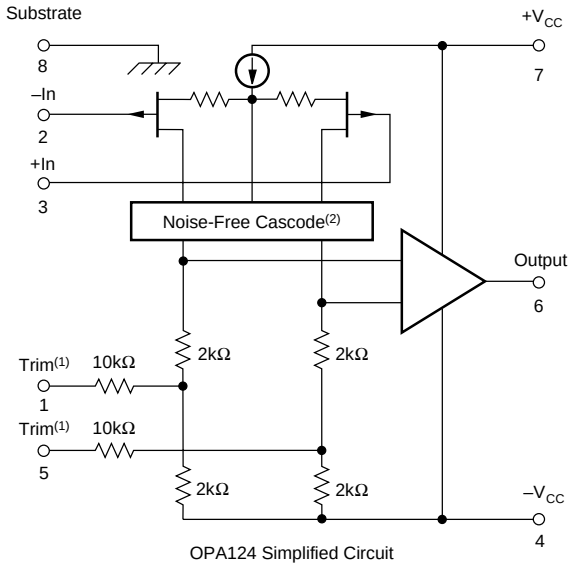
- PRECISION PHOTODIODE PREAMP
- MEDICAL EQUIPMENT
- OPTOELECTRONICS
- DATA ACQUISITION
- TEST EQUIPMENT

DESCRIPTION

The OPA124 is a precision monolithic FET operational amplifier using a ***Difet*** (dielectrical isolation) manufacturing process. Outstanding DC and AC performance characteristics allow its use in the most critical instrumentation applications.

Bias current, noise, voltage offset, drift, open-loop gain, common-mode rejection and power supply rejection are superior to BIFET and CMOS amplifiers. ***Difet*** fabrication achieves extremely low input bias currents without compromising input voltage noise performance. Low input bias current is maintained over a wide input common-mode voltage range with unique cascode circuitry. This cascode design also allows high precision input specifications and reduced susceptibility to flicker noise. Laser trimming of thin-film resistors gives very low offset and drift.

Compared to the popular OPA111, the OPA124 gives comparable performance and is available in an 8-pin PDIP and 8-pin SOIC package.



OPA124 Simplified Circuit

NOTES: (1) Omitted on SOIC. (2) Patented.

BIFET® National Semiconductor Corp.,
Difet® Burr-Brown Corp.

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PDS-1203C
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SBOS028

SPECIFICATIONS

ELECTRICAL

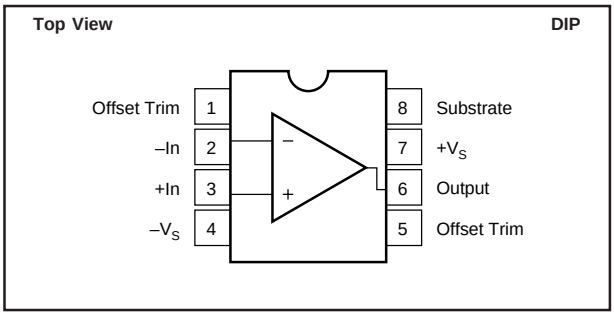
At V_{CC} = ±15VDC and T_A = +25°C, unless otherwise noted.

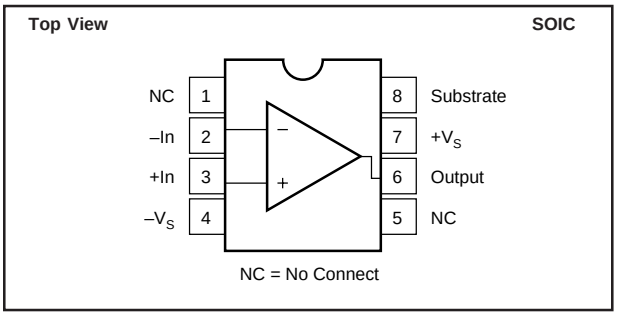
PARAMETER	CONDITION	OPA124U, P			OPA124UA, PA			OPA124PB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT NOISE											
Voltage, f_O = 10Hz[4]			40	80		*	*		*	*	nV/√Hz
f_O = 100Hz[4]			15	40		*	*		*	*	nV/√Hz
f_O = 1kHz[4]			8	15		*	*		*	*	nV/√Hz
f_O = 10kHz[5]			6	8		*	*		*	*	nV/√Hz
f_B = 10Hz to 10kHz[5]			0.7	1.2		*	*		*	*	µVrms
f_B = 0.1Hz to 10Hz			1.6	3.3		*	*		*	*	µVp-p
Current, f_B = 0.1Hz to 10Hz			9.5	15		*	*		*	*	fAp-p
f_O = 0.1Hz thru 20kHz			0.5	0.8		*	*		*	*	fA/√Hz
OFFSET VOLTAGE[1]											
Input Offset Voltage	V_{CM} = 0VDC		±200	±800		±150	±500		±100	±250	µV
vs Temperature	T_A = T_{MIN} to T_{MAX}		±4	±7.5		±2	±4		±1	±2	µV/°C
Supply Rejection	V_{CC} = ±10V to ±18V	88	110		90	*		100	*		dB
vs Temperature	T_A = T_{MIN} to T_{MAX}	84	100		86	*		90	*		dB
BIAS CURRENT[1]											
Input Bias Current	V_{CM} = 0VDC		±1	±5		±0.5	±2		±0.35	±1	pA
OFFSET CURRENT[1]											
Input Offset Current	V_{CM} = 0VDC		±1	±5		±0.5	±1		±0.25	±0.5	pA
IMPEDANCE											
Differential			10^{13} || 1			*			*		Ω || pF
Common-Mode			10^{14} || 3			*			*		Ω || pF
VOLTAGE RANGE											
Common-Mode Input Range		±10	±11		*	*		*	*		V
Common-Mode Rejection	V_{IN} = ±10VDC	92	110		94	*		100	*		dB
vs Temperature	T_A = T_{MIN} to T_{MAX}	86	100		*	*		90	*		dB
OPEN-LOOP GAIN, DC											
Open-Loop Voltage Gain	R_L ≥ 2kΩ	106	125		*	*		120	*		dB
FREQUENCY RESPONSE											
Unity Gain, Small Signal			1.5			*			*		MHz
Full Power Response	20Vp-p, R_L = 2kΩ	16	32		*	*		*	*		kHz
Slew Rate	V_O = ±10V, R_L = 2kΩ	1	1.6		*	*		*	*		V/µs
THD			0.0003			*			*		%
Settling Time, 0.1%	Gain = –1, R_L = 2kΩ		6			*			*		µs
0.01%	10V Step		10			*			*		µs
Overload Recovery, 50% Overdrive[2]	Gain = –1		5			*			*		µs
RATED OUTPUT											
Voltage Output	R_L = 2kΩ	±11	±12		*	*		*	*		V
Current Output	V_O = ±10VDC	±5.5	±10		*	*		*	*		mA
Output Resistance	DC, Open Loop		100			*			*		Ω
Load Capacitance Stability	Gain = +1		1000			*			*		pF
Short Circuit Current		10	40		*	*		*	*		mA
POWER SUPPLY											
Rated Voltage			±15			*			*		VDC
Voltage Range, Derated		±5		±18	*		*	*		*	VDC
Current, Quiescent	I_O = 0mADC		2.5	3.5		*	*		*	*	mA
TEMPERATURE RANGE											
Specification	T_{MIN} and T_{MAX}	–25		+85	*		*	*		*	°C
Storage		–65		+125	*		*	*		*	°C
θ Junction-Ambient: PDIP			90			*			*		°C/W
SOIC			100			*			*		°C/W

* Specification same as OPA124U, P

NOTES: (1) Offset voltage, offset current, and bias current are measured with the units fully warmed up. For performance at other temperatures see Typical Performance Curves. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (3) For performance at other temperatures see Typical Performance Curves. (4) Sample tested, 98% confidence. (5) Guaranteed by design.

CONNECTION DIAGRAMS





PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER[1]	TEMPERATURE RANGE	BIAS CURRENT pA, max	OFFSET DRIFT µV/°C, max
OPA124U	8-Lead SOIC	182	–25°C to +85°C	5	7.5
OPA124P	8-Pin Plastic DIP	006	–25°C to +85°C	5	7.5
OPA124UA	8-Lead SOIC	182	–25°C to +85°C	2	4
OPA124PA	8-Pin Plastic DIP	006	–25°C to +85°C	2	4
OPA124PB	8-Pin Plastic DIP	006	–25°C to +85°C	1	2

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS[1]

Supply	±18VDC
Internal Power Dissipation[2]	750mW
Differential Input Voltage[3]	±36VDC
Input Voltage Range[3]	±18VDC
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Output Short Circuit Duration[4]	Continuous
Junction Temperature	+175°C

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Packages must be derated based on θ_{JA} = 90°C/W for PDIP and 100°C/W for SOIC. (3) For supply voltages less than ±18VDC, the absolute maximum input voltage is equal to +18V > V_{IN} > $-V_{CC}$ – 6V. See Figure 2. (4) Short circuit may be to power supply common only. Rating applies to +25°C ambient. Observe dissipation limit and T_J.

ELECTROSTATIC DISCHARGE SENSITIVITY

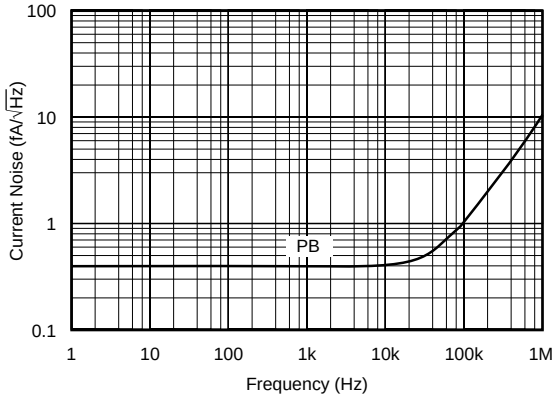
This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

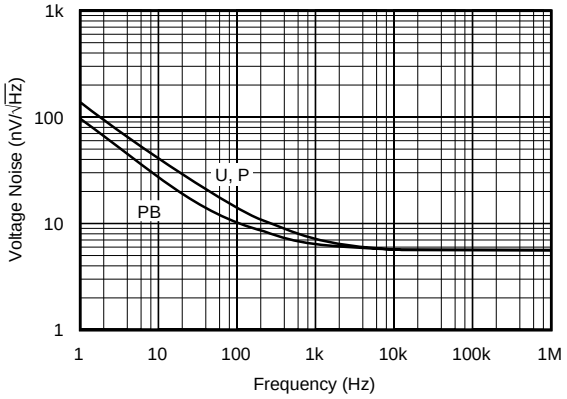
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, and V_{CC} = ±15VDC, unless otherwise noted.

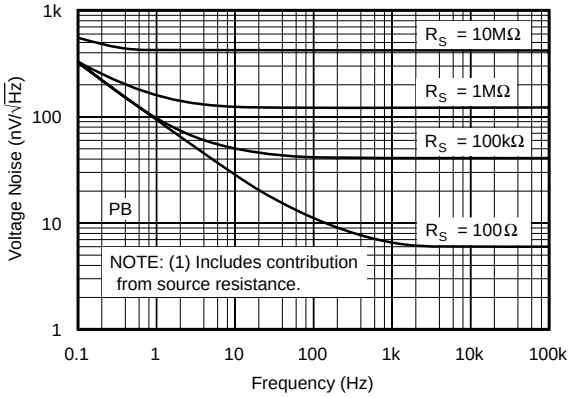
INPUT CURRENT NOISE SPECTRAL DENSITY



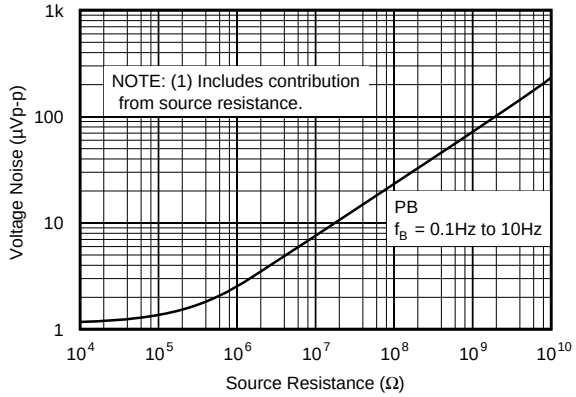
INPUT VOLTAGE NOISE SPECTRAL DENSITY



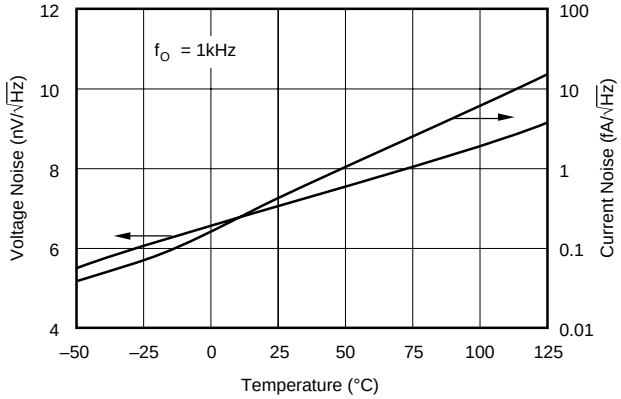
TOTAL[1] INPUT VOLTAGE NOISE SPECTRAL DENSITY vs SOURCE RESISTANCE



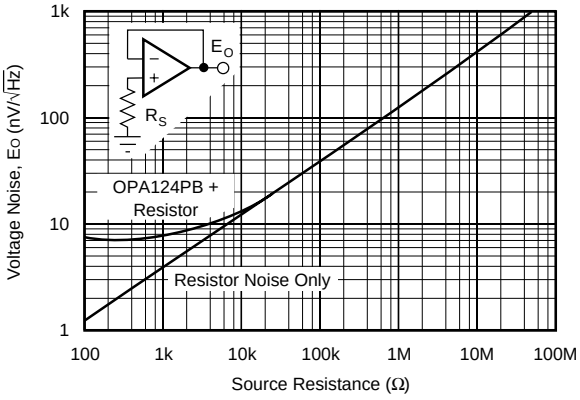
TOTAL[1] INPUT VOLTAGE NOISE (PEAK-TO-PEAK) vs SOURCE RESISTANCE



VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs TEMPERATURE



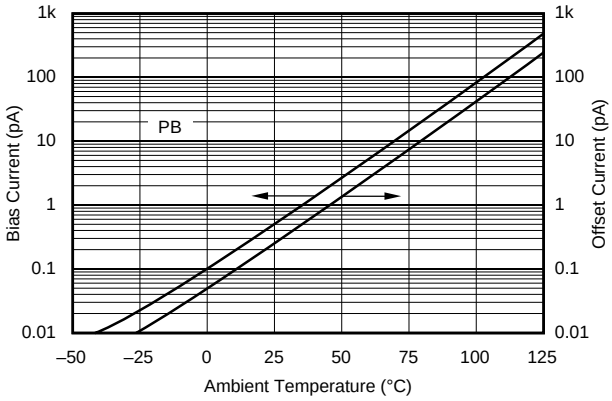
TOTAL INPUT VOLTAGE NOISE SPECTRAL DENSITY AT 1kHz vs SOURCE RESISTANCE



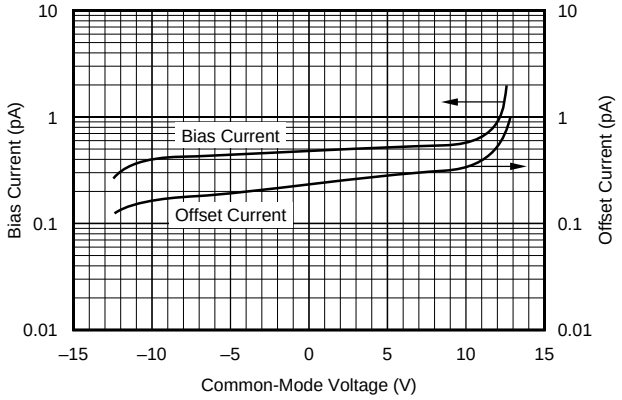
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_{CC} = ±15VDC, unless otherwise noted.

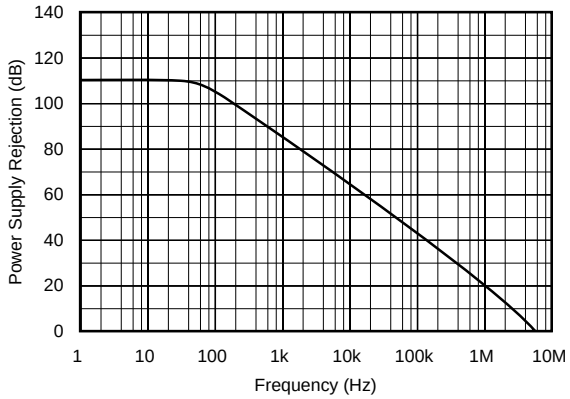
BIAS AND OFFSET CURRENT
vs TEMPERATURE



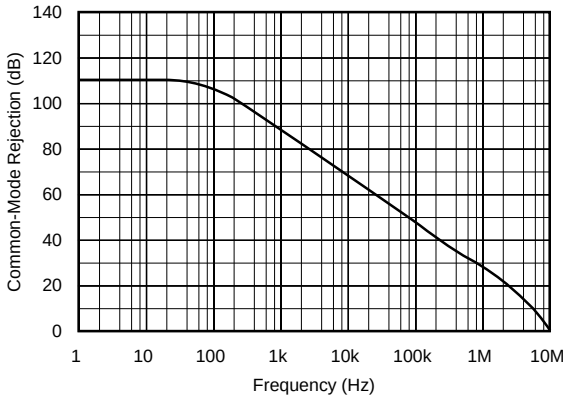
BIAS AND OFFSET CURRENT
vs INPUT COMMON-MODE VOLTAGE



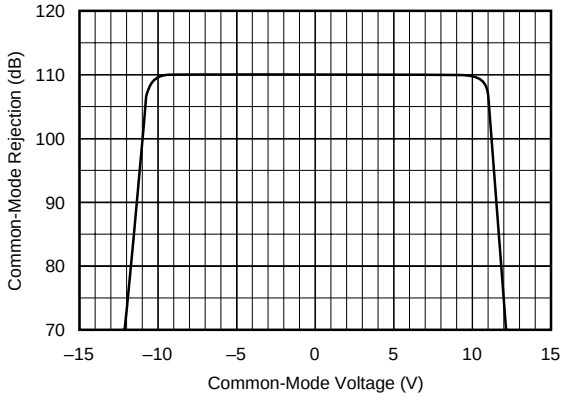
POWER SUPPLY REJECTION
vs FREQUENCY



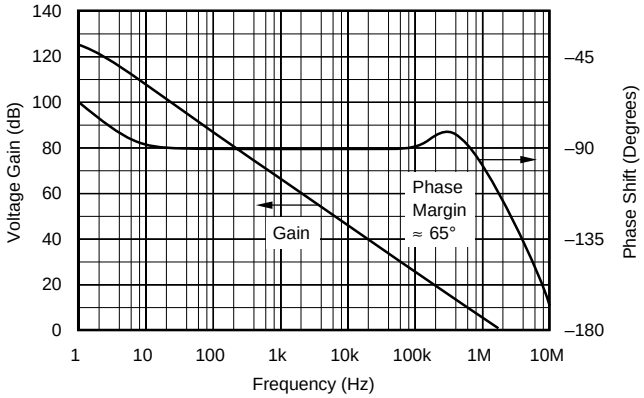
COMMON-MODE REJECTION
vs FREQUENCY



COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



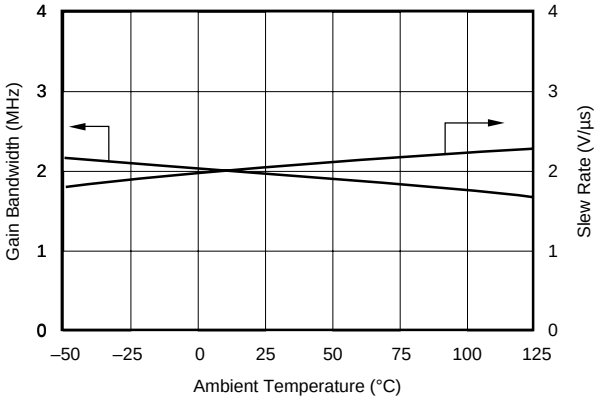
OPEN-LOOP FREQUENCY RESPONSE



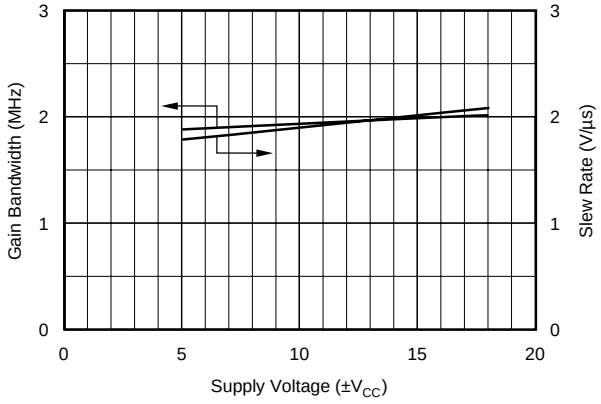
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_{CC} = ±15VDC, unless otherwise noted.

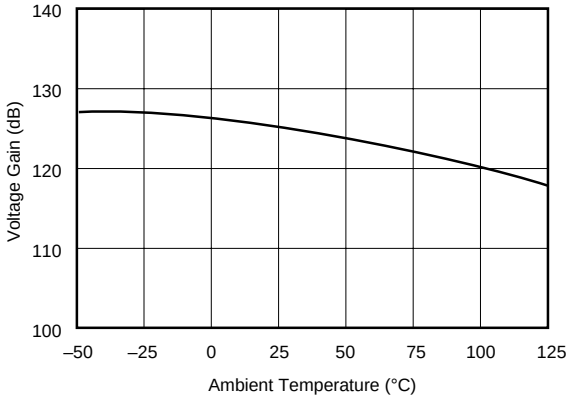
GAIN-BANDWIDTH AND SLEW RATE vs TEMPERATURE



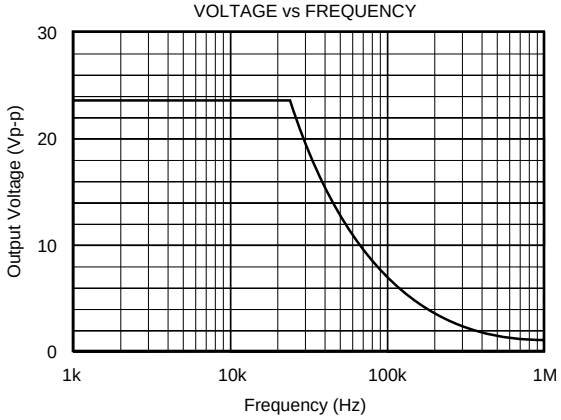
GAIN-BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



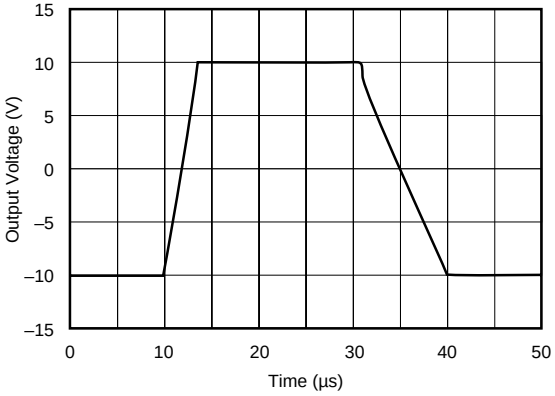
OPEN-LOOP GAIN vs TEMPERATURE



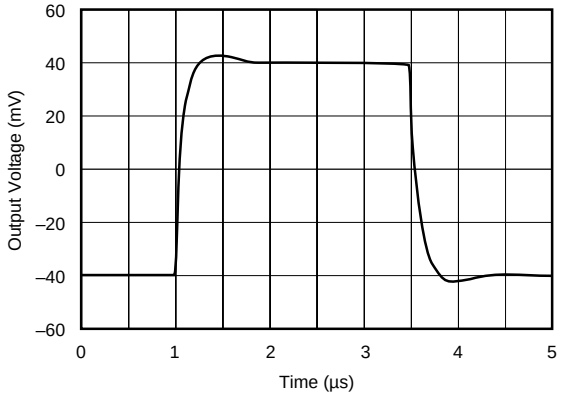
MAXIMUM UNDISTORTED OUTPUT VOLTAGE vs FREQUENCY



LARGE SIGNAL TRANSIENT RESPONSE



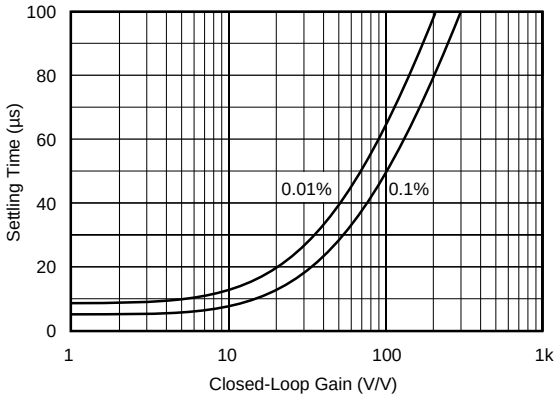
SMALL SIGNAL TRANSIENT RESPONSE



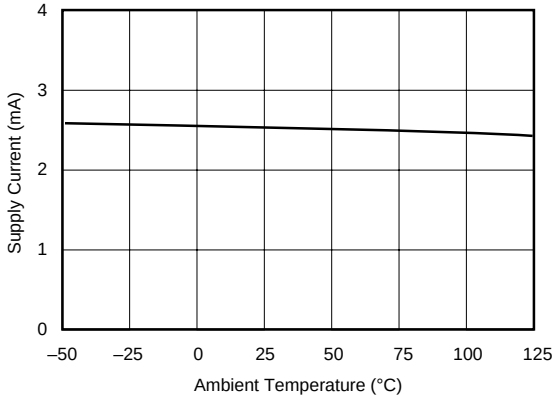
TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, and V_{CC} = ±15VDC, unless otherwise noted.

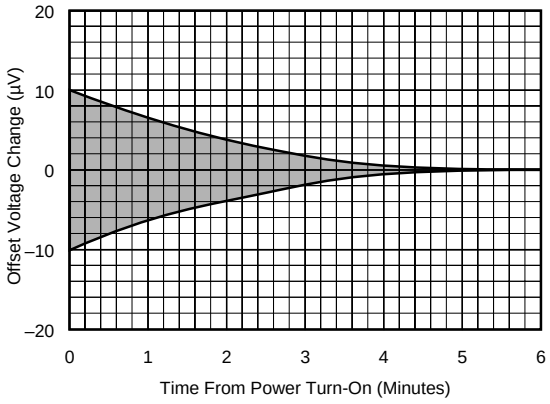
SETTLING TIME vs CLOSED-LOOP GAIN



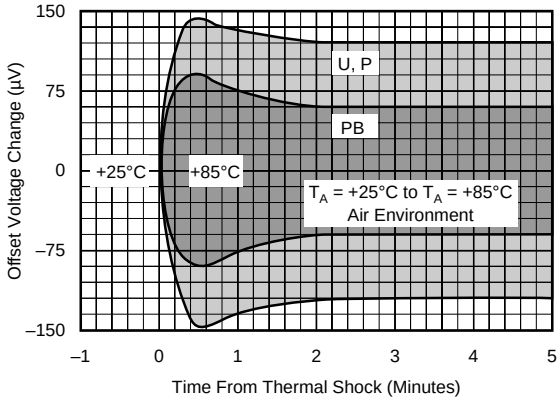
SUPPLY CURRENT vs TEMPERATURE



INPUT OFFSET VOLTAGE WARM-UP DRIFT



INPUT OFFSET VOLTAGE CHANGE
DUE TO THERMAL SHOCK



APPLICATIONS INFORMATION

OFFSET VOLTAGE ADJUSTMENT

The OPA124 offset voltage is laser-trimmed and will require no further trim for most applications. In order to reduce layout leakage errors, the offset adjust capability has been removed from the SOIC versions (OPA124UA and OPA124U). The PDIP versions (OPA124PB, OPA124PA, and OPA124P) do have pins available for offset adjustment. As with most amplifiers, externally trimming the remaining offset can change drift performance by about 0.3µV/°C for each 100µV of adjusted offset. The correct circuit configuration for offset adjust for the PDIP packages is shown in Figure 1.

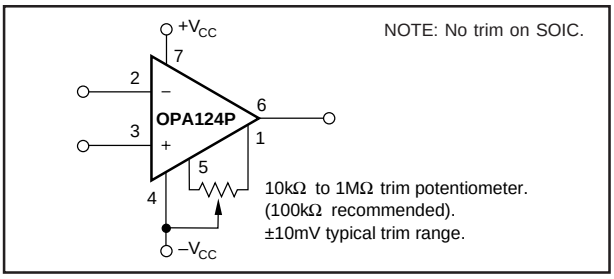


FIGURE 1. Offset Voltage Trim for PDIP packages.

INPUT PROTECTION

Conventional monolithic FET operational amplifiers require external current-limiting resistors to protect their inputs against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. Most BIFET amplifiers can be destroyed by the loss of $-V_{CC}$.

Unlike BIFET amplifiers, the ***Difet*** OPA124 requires input current limiting resistors only if its input voltage is greater than 6V more negative than $-V_{CC}$. A 10kΩ series resistor will limit input current to a safe level with up to ±15V input levels, even if both supply voltages are lost (Figure 2).

Static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers (both bipolar and FET types), this may cause a noticeable degradation of offset voltage and drift. Static protection is recommended when handling any precision IC operational amplifier.

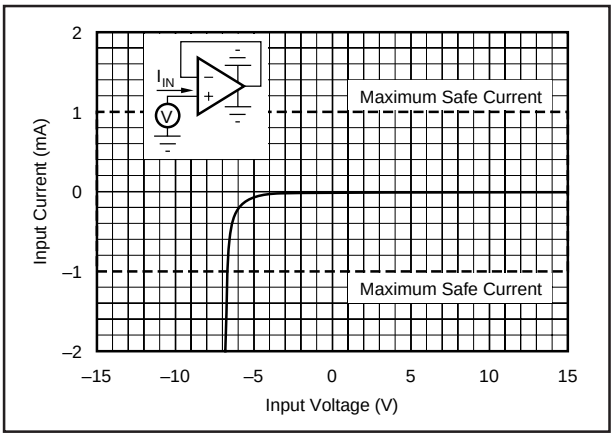


FIGURE 2. Input Current vs Input Voltage with $\pm V_{CC}$ Pins Grounded.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA124. To avoid leakage problems, the OPA124 should be soldered directly into a printed circuit board. Utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier substrate should be connected to any input shield or guard via pin 8 minimizing both leakage and noise pickup (see Figure 3).

If guarding is not required, pin 8 should be connected to ground.

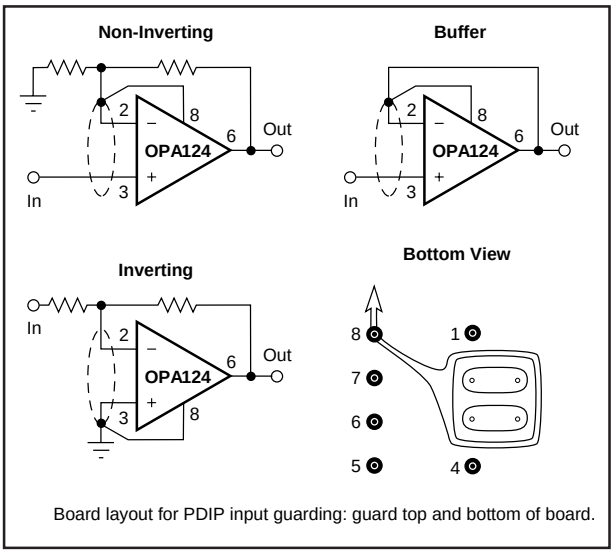


FIGURE 3. Connection of Input Guard.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA124P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA124PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA124PA2	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA124PB	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
OPA124U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA124UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

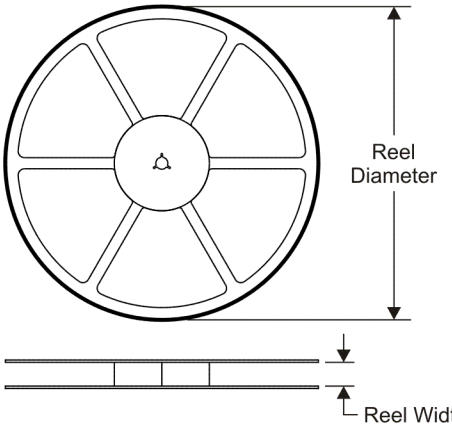
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

information may not be available for release.

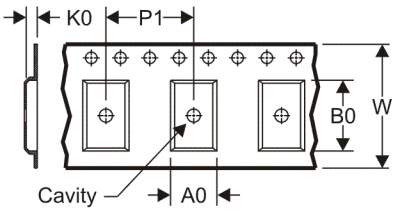
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

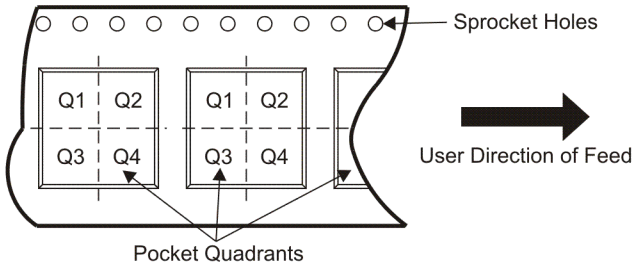


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

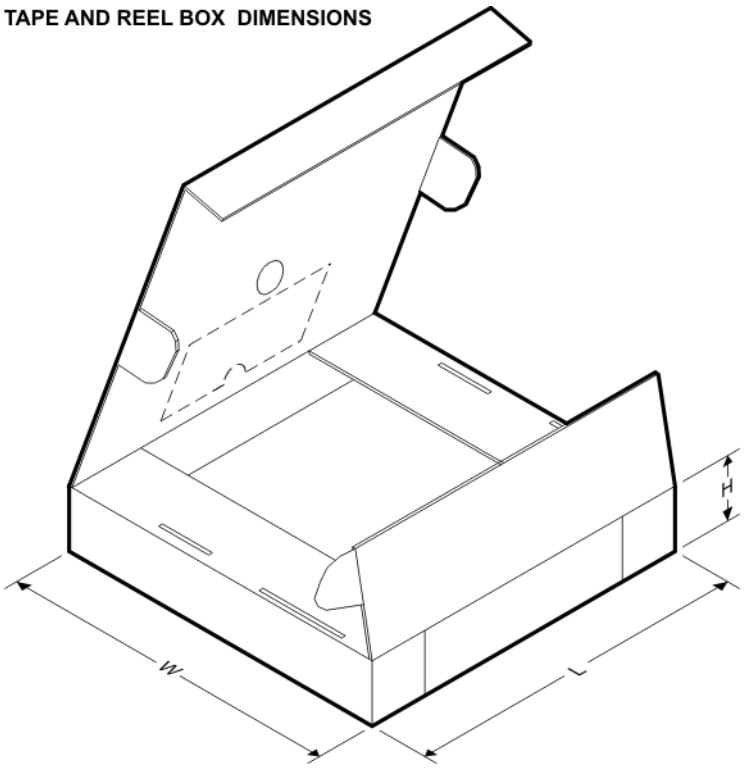
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA124U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA124UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA124U/2K5	SOIC	D	8	2500	346.0	346.0	29.0
OPA124UA/2K5	SOIC	D	8	2500	346.0	346.0	29.0

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