## 5V/3.3V 512K × 8 CMOS SRAM

### Features

- AS7C4096 (5V version)
- AS7C34096 (3.3V version)
- Industrial and commercial temperature
- Organization: 524,288 words × 8 bits
- Center power and ground pins
- High speed
  - 10/12/15/20 ns address access time
  - 5/6/7/8 ns output enable access time
- Low power consumption: ACTIVE
  - 1375 mW (AS7C4096) / max @ 12 ns
  - 468 mW (AS7C34096) / max @ 12 ns

- Low power consumption: STANDBY
  - 110 mW (AS7C4096) / max CMOS
  - 72 mW (AS7C34096) / max CMOS
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400 mil 36-pin SOJ
  - 44-pin TSOP 2
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
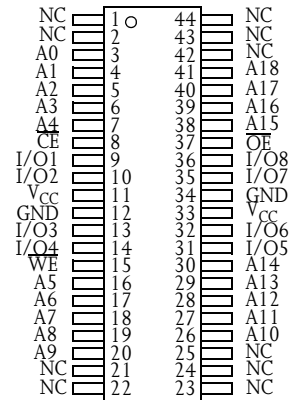
### Logic block diagram
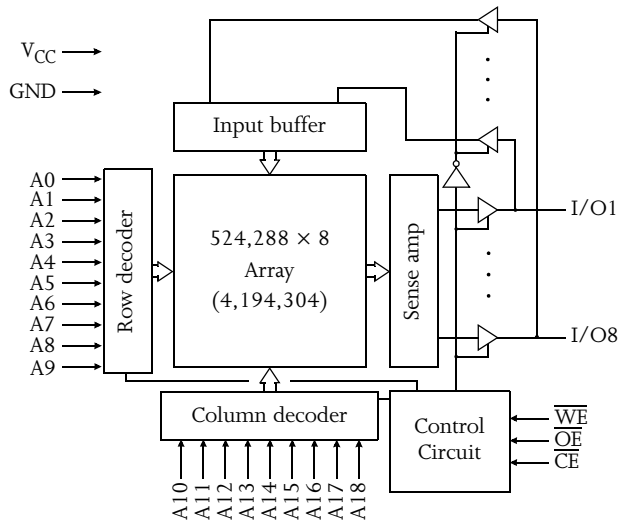


### Pin arrangements



36-pin SOJ (400 mil)
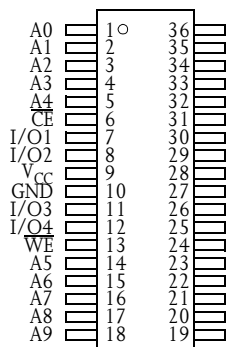
44-pin TSOP 2

### 48 BGA Package

|   | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | $A_0$ | $A_1$ | NC | $A_3$ | $A_6$ | $A_8$ |
| **B** | $I/O_5$ | $A_2$ | $\overline{WE}$ | $A_4$ | $A_7$ | $I/O_1$ |
| **C** | $I/O_6$ | NC | NC | $A_5$ | NC | $I/O_2$ |
| **D** | $V_{SS}$ | NC | NC | NC | NC | $V_{CC}$ |
| **E** | $V_{CC}$ | NC | NC | NC | NC | $V_{SS}$ |
| **F** | $I/O_7$ | NC | $A_{18}$ | $A_{17}$ | NC | $I/O_3$ |
| **G** | $I/O_8$ | $\overline{OE}$ | $\overline{CE}$ | $A_{16}$ | $A_{15}$ | $I/O_4$ |
| **H** | $A_9$ | $A_{10}$ | $A_{11}$ | $A_{12}$ | $A_{13}$ | $A_{14}$ |

### Selection guide

| | | −10 | −12 | −15 | −20 | Unit |
|---|---|---|---|---|---|---|
| Maximum address access time | | 10 | 12 | 15 | 20 | ns |
| Maximum outputenable access time | | 5 | 6 | 7 | 9 | ns |
| Maximum operating current | AS7C4096 | – | 250 | 220 | 180 | mA |
| | AS7C34096 | 160 | 130 | 110 | 100 | mA |
| Maximum CMOS standby current | AS7C4096 | – | 20 | 20 | 20 | mA |
| | AS7C34096 | 20 | 20 | 20 | 20 | mA |

## Functional description

The AS7C4096 and AS7C34096 are high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) devices organized as 524,288 words × 8 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ($t_{AA}$, $t_{RC}$, $t_{WC}$) of 10/12/15/20 ns with output enable access times ($t_{OE}$) of 5/6/7/8 ns are ideal for high-performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is high the device enters standby mode. The AS7C4096 is guaranteed not to exceed 110 mW power consumption in CMOS standby mode.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O1–I/O8 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single supply voltage. Both devices are available in the industry standard 400-mil 36-pin SOJ and 44-pin TSOP 2 packages.

## Absolute maximum ratings

| Parameter | Device | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Voltage on $V_{CC}$ relative to GND | AS7C4096 | $V_{t1}$ | −1 | +7.0 | V |
| | AS7C34096 | $V_{t1}$ | −0.5 | +5.0 | V |
| Voltage on any pin relative to GND | | $V_{t2}$ | −0.5 | $V_{CC}$ +0.5 | V |
| Power dissipation | | $P_D$ | − | 1.0 | W |
| Storage temperature (plastic) | | $T_{stg}$ | −65 | +150 | °C |
| Temperature with $V_{CC}$ applied | | $T_{bias}$ | −55 | +125 | °C |
| DC current unto output (low) | | $I_{OUT}$ | − | 20 | mA |

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Data | Mode |
|---|---|---|---|---|
| H | X | X | High Z | Standby ($I_{SB}$, $I_{SB1}$) |
| L | H | H | High Z | Output disable ($I_{CC}$) |
| L | H | L | $D_{OUT}$ | Read ($I_{CC}$) |
| L | L | X | $D_{IN}$ | Write ($I_{CC}$) |

Key: X = Don't care, L = Low, H = High

®

## Recommended operating condition

| Parameter | Device | Symbol | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | AS7C4096 | $V_{CC}(12/15/20)$ | 4.5 | 5.0 | 5.5 | V |
| | AS7C34096 | $V_{CC}(10)$ | 3.15 | 3.30 | 3.6 | V |
| | AS7C34096 | $V_{CC}(12/15/20)$ | 3.0 | 3.3 | 3.6 | V |
| Input voltage | AS7C4096 | $V_{IH}$ | 2.2 | – | $V_{CC} + 0.5$ | V |
| | AS7C34096 | $V_{IH}$ | 2.0 | – | $V_{CC} + 0.5$ | V |
| | | $V_{IL}$ | $-0.5^{1}$ | – | 0.8 | V |
| Ambient operating temperature | commercial | $T_A$ | 0 | – | 70 | °C |
| | industrial | $T_A$ | –40 | – | 85 | °C |

1 $V_{IL}$ min = –3.0V for pulse width less than $t_{RC}/2$.

## DC operating characteristics (over the operating range)[1]

| Parameter | Symbol | Test conditions | Device | −10 Min | −10 Max | −12 Min | −12 Max | −15 Min | −15 Max | −20 Min | −20 Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input leakage current | $|I_{LI}|$ | $V_{CC} = Max, V_{IN} = GND$ to $V_{CC}$ | | – | 1 | – | 1 | – | 1 | – | 1 | μA |
| Output leakage current | $|I_{LO}|$ | $V_{CC} = Max, \overline{CE} = V_{IH}$ $V_{OUT} = GND$ to $V_{CC}$ | | – | 1 | – | 1 | – | 1 | – | 1 | μA |
| Operating power supply current | $I_{CC}$ | $V_{CC} = Max, \overline{CE} < V_{IL}$ $f = f_{Max}, I_{OUT} = 0mA$ | AS7C4096 | – | – | – | 250 | – | 220 | – | 180 | mA |
| | | | AS7C34096 | – | 160 | – | 130 | – | 110 | – | 100 | |
| Standby power supply current | $I_{SB}$ | $V_{CC} = Max, \overline{CE} = V_{IH}$ $f = f_{Max}, I_{OUT} = 0mA$ | AS7C4096 | – | – | – | 60 | – | 60 | – | 60 | mA |
| | | | AS7C34096 | – | 60 | – | 60 | – | 60 | – | 60 | |
| | $I_{SB1}$ | $V_{CC} = Max,$ $\overline{CE} \geq V_{CC} - 0.2V, V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V, f = 0$ | AS7C4096 | – | – | – | 20 | – | 20 | – | 20 | mA |
| | | | AS7C34096 | – | 20 | – | 20 | – | 20 | – | 20 | |
| Output voltage | $V_{OL}$ | $I_{OL} = 8$ mA, $V_{CC} = Min$ | | – | 0.4 | – | 0.4 | – | 0.4 | – | 0.4 | V |
| | $V_{OH}$ | $I_{OH} = -4$ mA, $V_{CC} = Min$ | | 2.4 | – | 2.4 | – | 2.4 | – | 2.4 | – | V |

## Capacitance (f = 1MHz, $T_a$ = 25° C, $V_{CC}$ = NOMINAL)[2]

| Parameter | Symbol | Signals | Test conditions | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$ | $V_{IN} = 0V$ | 5 | pF |
| I/O capacitance | $C_{I/O}$ | I/O | $V_{IN} = V_{OUT} = 0V$ | 7 | pF |

® 

## Read cycle (over the operating range)[3,9]

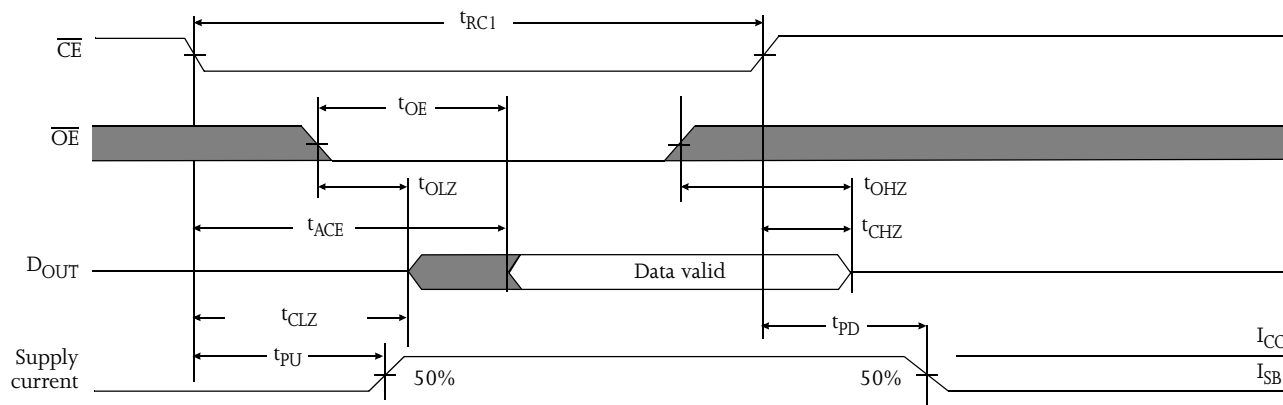| Parameter | Symbol | −10 | | −12 | | −15 | | −20 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Read cycle time | $t_{RC}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Address access time | $t_{AA}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | 3 |
| Chip enable ($\overline{CE}$) access time | $t_{ACE}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | 3 |
| Output enable ($\overline{OE}$) access time | $t_{OE}$ | – | 5 | – | 6 | – | 7 | – | 8 | ns | |
| Output hold from address change | $t_{OH}$ | 3 | – | 3 | – | 3 | – | 3 | – | ns | 5 |
| $\overline{CE}$ Low to output in low Z | $t_{CLZ}$ | 3 | – | 3 | – | 0 | – | 0 | – | ns | 4, 5 |
| $\overline{CE}$ High to output in high Z | $t_{CHZ}$ | – | 5 | – | 6 | – | 7 | – | 9 | ns | 4, 5 |
| $\overline{OE}$ Low to output in low Z | $t_{OLZ}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 4, 5 |
| $\overline{OE}$ High to output in high Z | $t_{OHZ}$ | – | 5 | – | 6 | – | 7 | – | 9 | ns | 4, 5 |
| Power up time | $t_{PU}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 4, 5 |
| Power down time | $t_{PD}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | 4, 5 |

## Key to switching waveforms

Rising input        Falling input        Undefined/don't care

## Read waveform 1 (address controlled)[3,6,7,9]
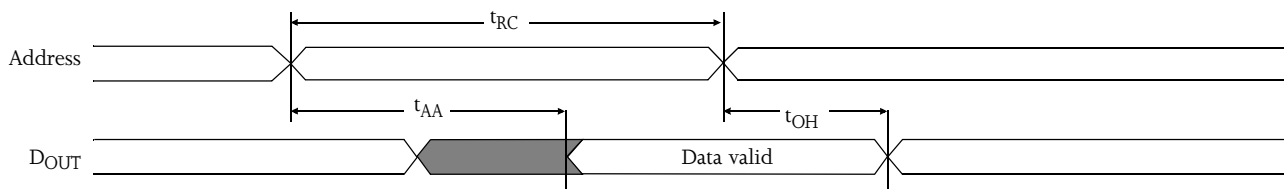


## Read waveform 2 ($\overline{CE}$, $\overline{OE}$ controlled)[3,6,8,9]

## Write cycle (over the operating range)[11]

| Parameter | Symbol | −10 Min | −10 Max | −12 Min | −12 Max | −15 Min | −15 Max | −20 Min | −20 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Write cycle time | $t_{WC}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Chip enable ($\overline{CE}$) to write end | $t_{CW}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | |
| Address setup to write end | $t_{AW}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | |
| Address setup time | $t_{AS}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Write pulse width ($\overline{OE}$ = high) | $t_{WP1}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | |
| Write pulse width ($\overline{OE}$ = low | $t_{WP2}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Address hold from end of write | $t_{AH}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Write recovery time | $t_{WR}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Data valid to write end | $t_{DW}$ | 5 | – | 6 | – | 7 | – | 9 | – | ns | |
| Data hold time | $t_{DH}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 4, 5 |
| Write enable to output in high Z | $t_{WZ}$ | 0 | 5 | 0 | 6 | 0 | 7 | 0 | 9 | ns | 4, 5 |
| Output active from write end | $t_{OW}$ | 3 | – | 3 | – | 3 | – | 3 | – | ns | 4, 5 |

## Write waveform 1 ($\overline{WE}$ controlled)[10,11]
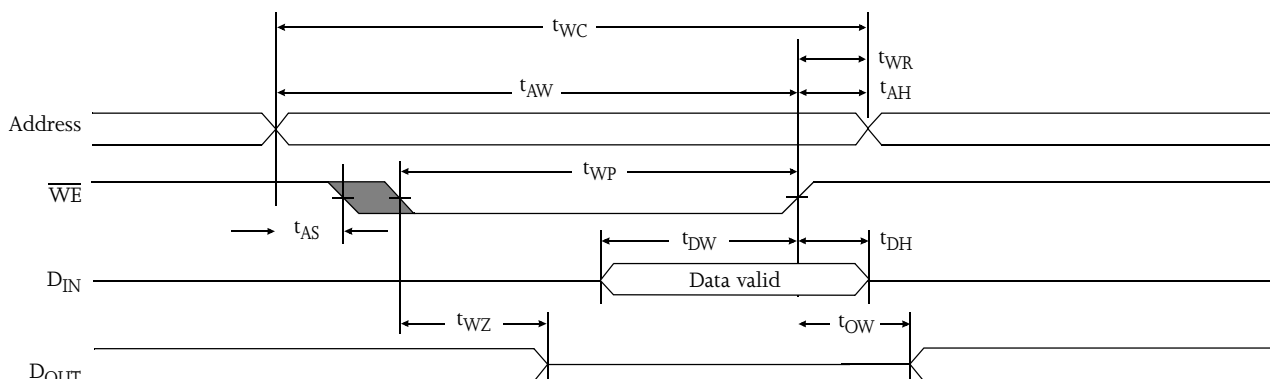


## Write waveform 2 ($\overline{CE}$ controlled)[10,11]
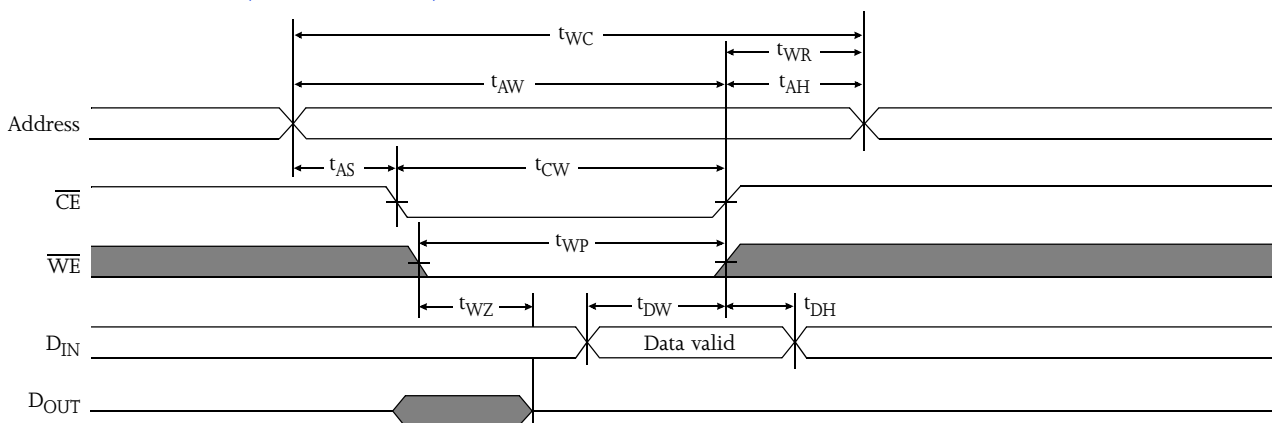
## AC test conditions

- Output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figures A, B, and C.
- Input rise and fall times: 2 ns. See Figure A.
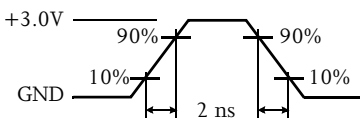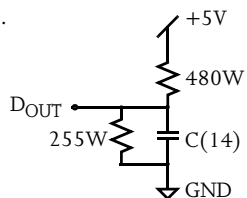- Input and output timing reference levels: 1.5V.

Thevenin equivalent:

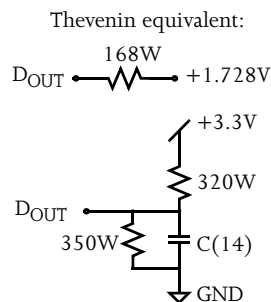$D_{OUT}$ —W\/W— +1.728V
168W

Figure A: Input pulse

Figure B: 5V Output load

Figure C: 3.3V Output load

### Notes

1. During $V_{CC}$ power-up, a pull-up resistor to $V_{CC}$ on $\overline{CE}$ is required to meet $I_{SB}$ specification.
2. This parameter is sampled, but not 100% tested.
3. For test conditions, see *AC Test Conditions*.
4. $t_{CLZ}$ and $t_{CHZ}$ are specified with $C_L$ = 5pF as in Figure C. Transition is measured ±500 mV from steady-state voltage.
5. This parameter is guaranteed, but not tested.
6. $\overline{WE}$ is HIGH for read cycle.
7. $\overline{CE}$ and $\overline{OE}$ are LOW for read cycle.
8. Address valid prior to or coincident with $\overline{CE}$ transition Low.
9. All read cycle timings are referenced from the last valid address to the first transitioning address.
10. $\overline{CE}$ or $\overline{WE}$ must be HIGH during address transitions. Either $\overline{CE}$ or $\overline{WE}$ asserting high terminates a write cycle.
11. All write cycle timings are referenced from the last valid address to the first transitioning address.
12. Not applicable.
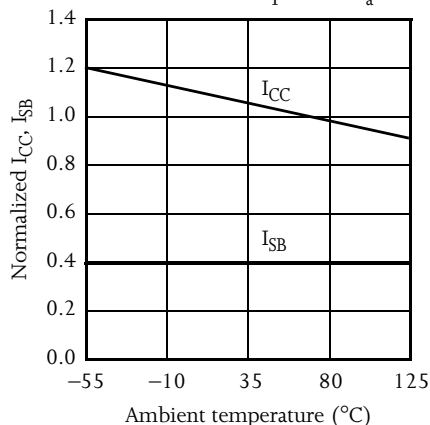13. C = 30pF, except at high Z and low Z parameters, where C = 5pF.

® 

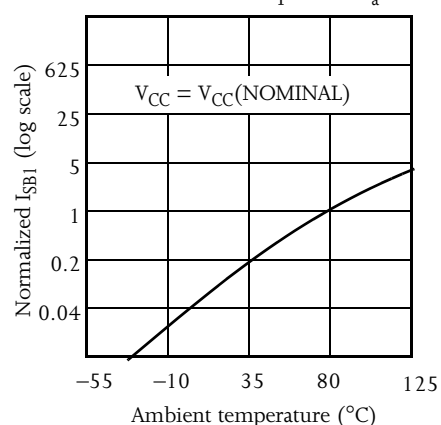## Typical DC and AC characteristics [12]



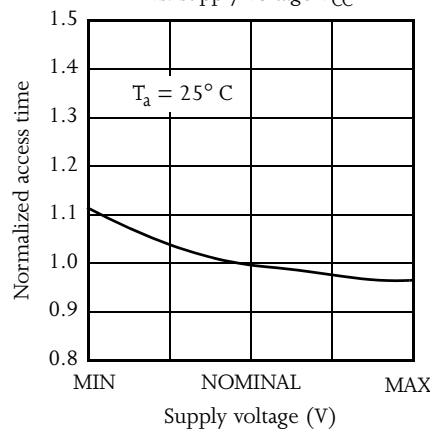Normalized supply current $I_{CC}$, $I_{SB}$ vs. supply voltage $V_{CC}$
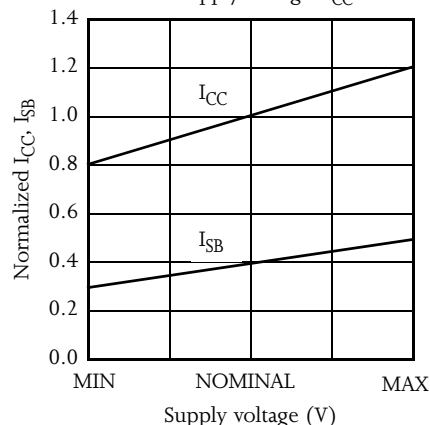


Normalized supply current $I_{CC}$, $I_{SB}$ vs. ambient temperature $T_a$

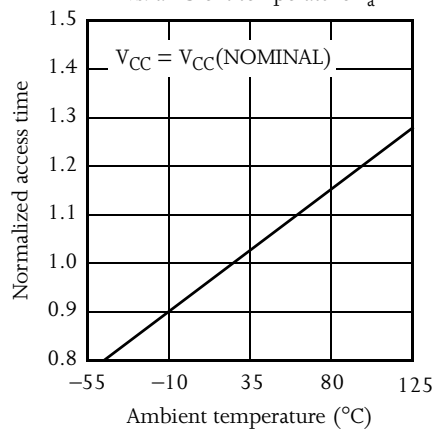

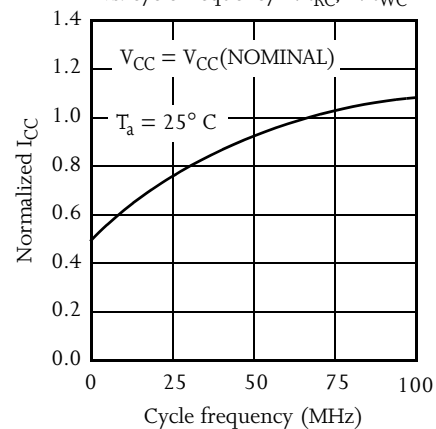Normalized supply current $I_{SB1}$ vs. ambient temperature $T_a$



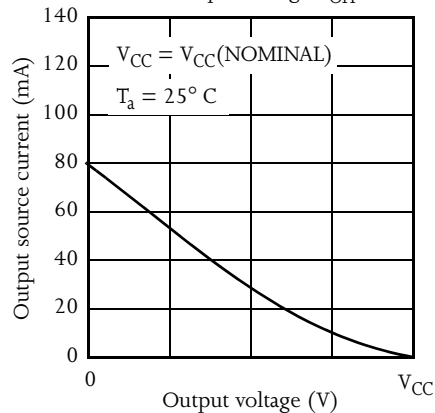Normalized access time $t_{AA}$ vs. supply voltage $V_{CC}$



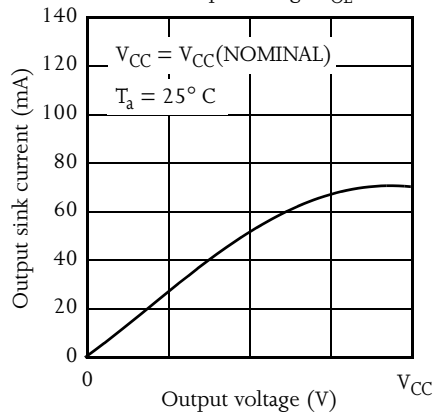Normalized access time $t_{AA}$ vs. ambient temperature $T_a$



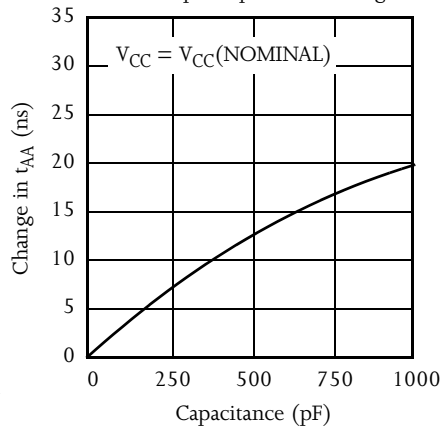Normalized supply current $I_{CC}$ vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



Output source current $I_{OH}$ vs. output voltage $V_{OH}$



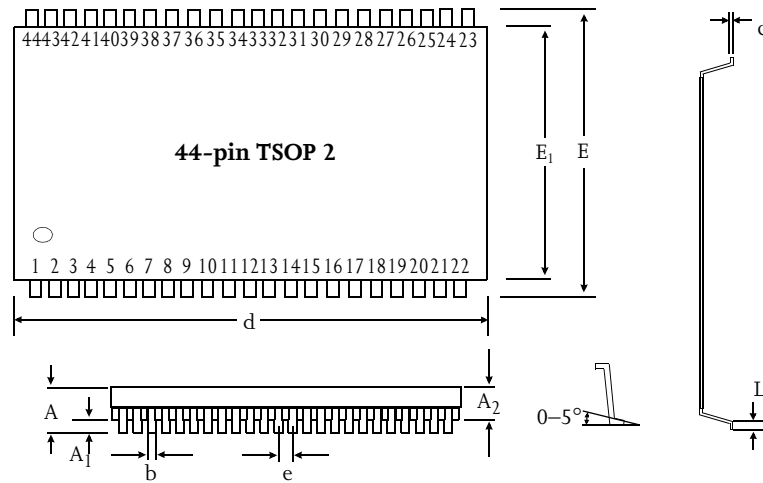Output sink current $I_{OL}$ vs. output voltage $V_{OL}$



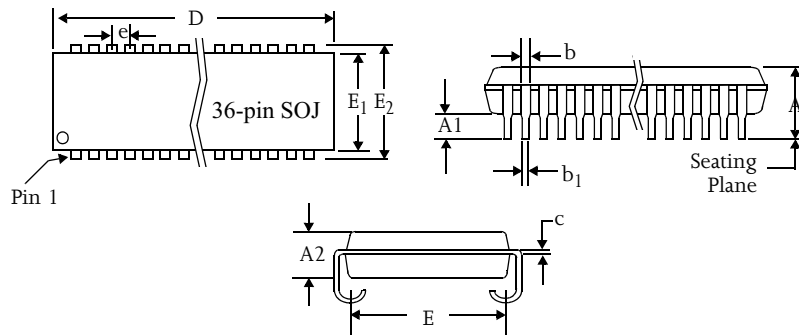Typical access time change $\Delta t_{AA}$ vs. output capacitive loading

## Package dimensions



44-pin TSOP 2

| | 44-pin TSOP 2 | |
|---|---|---|
| | **Min (mm)** | **Max (mm)** |
| **A** | | 1.2 |
| **A$_1$** | 0.05 | 0.15 |
| **A$_2$** | 0.95 | 1.05 |
| **b** | 0.30 | 0.45 |
| **c** | 0.15 (typical) | |
| **d** | 18.28 | 18.54 |
| **E$_1$** | 10.03 | 10.16 |
| **E** | 11.56 | 11.96 |
| **e** | 0.80 (typical) | |
| **L** | 0.40 | 0.60 |



36-pin SOJ

| | 36-pin SOJ 400 | |
|---|---|---|
| | **Min (mils)** | **Max (mils)** |
| **A** | .128 | 0.148 |
| **A$_1$** | 0.027 | – |
| **A$_2$** | 0.102 NOM | |
| **b** | 0.015 | 0.020 |
| **b$_1$** | 0.026 | 0.032 |
| **c** | 0.007 | 0.013 |
| **D** | .920 | .930 |
| **e** | 0.045 | 0.055 |
| **E** | 0.400 NOM | |
| **E** | 0.435 | 0.445 |

48-ball FBGA

Side View

E2

E

D

E1

Die

Detail View

A

E2

E

Die

Y

0.3/Typ

Bottom View

6 5 4 3 2 1

Ball #A1

A
B
C
D
E
F
G
H

C1

A

A

B1

Top View

Ball #A1 index

SRAM Die

C

Elastomer

B
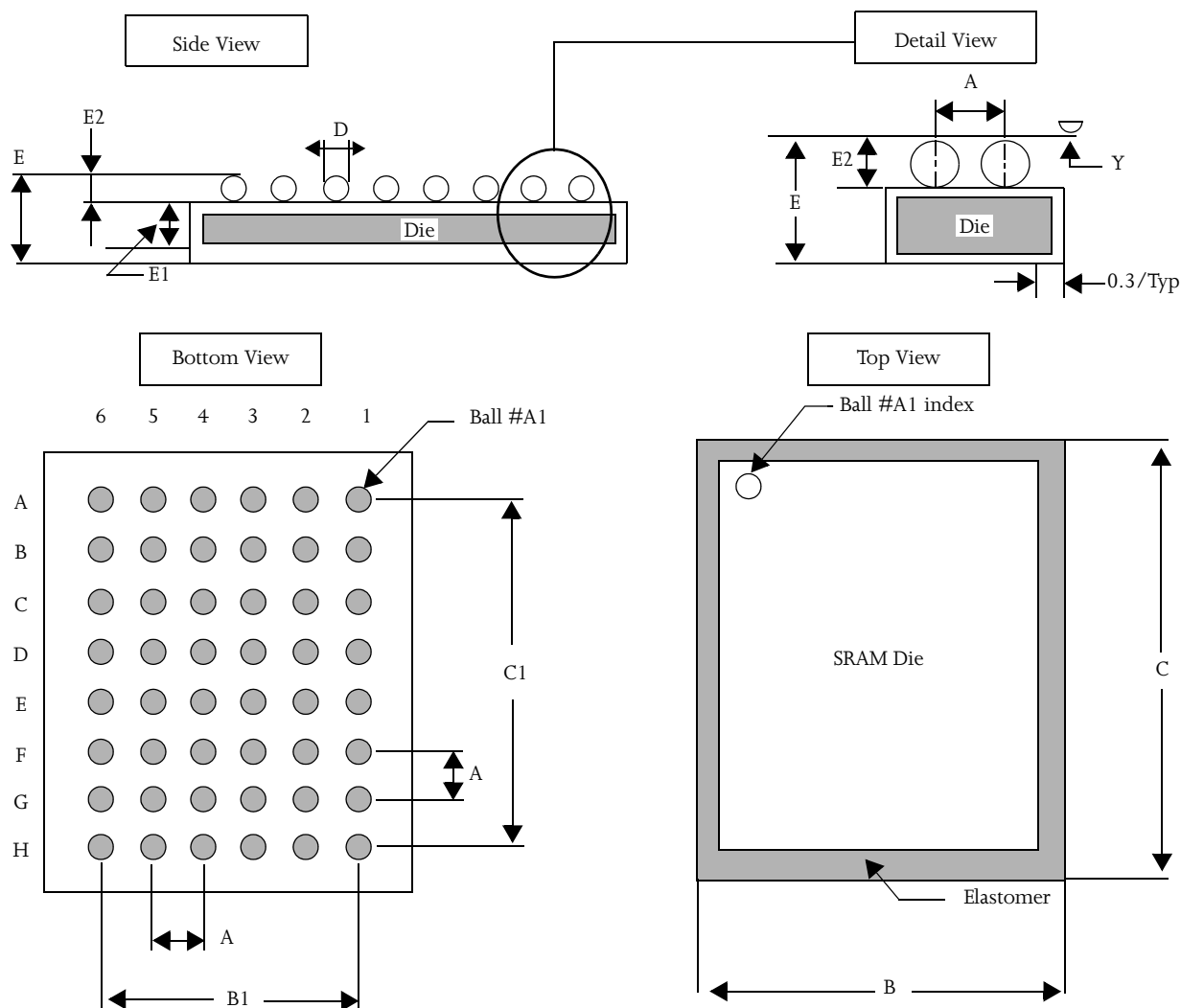
Notes

1. Bump counts: 48 (8 row × 6 column).

2. Pitch: (x,y) = 0.75 mm × 0.75 mm (typ).

3. Units: millimeters.

4. All tolerance are ±0.050 unless otherwise specified.

5. Typ: typical.

6. Y is coplanarity: 0.08 (max).

| 48-ball FBGA | | | |
|---|---|---|---|
| | **Minimum** | **Typical** | **Maximum** |
| **A** | – | 0.75 | – |
| **B** | 6.90 | 7.00 | 7.10 |
| **B1** | – | 3.75 | – |
| **C** | 10.90 | 11.00 | 11.10 |
| **C1** | – | 5.25 | – |
| **D** | 0.30 | 0.35 | 0.40 |
| **E** | – | – | 1.20 |
| **E1** | – | 0.68 | – |
| **E2** | 0.22 | 0.25 | 0.27 |
| **Y** | – | – | 0.08 |

## Ordering codes

| Package | Version | 10 ns | 12 ns | 15 ns | 20 ns |
|---|---|---|---|---|---|
| SOJ | 5V commercial | NA | AS7C4096-12JC | AS7C4096-15JC | AS7C4096-20JC |
| | 5V industrial | NA | AS7C4096-12JI | AS7C4096-15JI | AS7C4096-20JI |
| | 3.3V commercial | AS7C34096-10JC | AS7C34096-12JC | AS7C34096-15JC | AS7C34096-20JC |
| | 3.3V industrial | NA | AS7C34096-12JI | AS7C34096-15JI | AS7C34096-20JI |
| TSOP 2 | 5V commercial | NA | AS7C4096-12TC | AS7C4096-15TC | AS7C4096-20TC |
| | 5V industrial | NA | AS7C4096-12TI | AS7C4096-15TI | AS7C4096-20TI |
| | 3.3V commercial | AS7C34096-10TC | AS7C34096-12TC | AS7C34096-15TC | AS7C34096-20TC |
| | 3.3V industrial | NA | AS7C34096-12TI | AS7C34096-15TI | AS7C34096-20TI |
| BGA | 5V commercial | NA | AS7C4096-12BC | AS7C4096-15BC | AS7C4096-20BC |
| | 5V industrial | NA | AS7C4096-12BI | AS7C4096-15BI | AS7C4096-20BI |
| | 3.3V commercial | AS7C34096-10BC | AS7C34096-12BC | AS7C34096-15BC | AS7C34096-20BC |
| | 3.3V industrial | NA | AS7C34096-12BI | AS7C34096-15BI | AS7C34096-20BI |

## Part numbering system

| AS7C | X | 4096 | −XX | J, T, or B | X |
|---|---|---|---|---|---|
| SRAM prefix | Voltage: Blank: 5V CMOS 3: 3.3V CMOS | Device number | Access time | Packages: J: SOJ 400 mil T: TSOP 2 B: 48-ball FBGA 7x11 mm | Temperature ranges: C: Commercial, 0°C to 70°C I: Industrial, −40°C to 85°C |