

# Appendix A

## eZdsp™ F28335

### Schematics

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The schematics for the eZdsp™ F28335 can be found on the CD-ROM that accompanies this board. The schematics were drawn on ORCAD.

The schematics are correct for both the socketed and unsocketed version of the eZdsp™.

#### **WARNING !**

The TMS320F28335 supports +3.3V Input/Output levels which are NOT +5V tolerant. Connecting the eZdsp to a system with +5V Input/Output levels will damage the TMS320F28335. If the eZdsp is connected to another target then the eZdsp must be powered up first and powered down last to prevent latchup conditions.

#### **Design Notes:**

1. The TMS320F28335 X1/CLKIN pin is +1.8 volt input. The clock input is buffered with a SN74LVC1G14 whose supply is +1.8 volts. This provides +3.3 volts to the +1.8 volt clock translation. Refer to sheet 4 of the schematics.

|     |  |               |  |              |          |
|-----|--|---------------|--|--------------|----------|
| REV |  | DESCRIPTION   |  | DATE         | APPROVED |
| A   |  | ALPHA RELEASE |  | 29-July-2007 |          |

SCHEMATIC CONTENTS

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CHK

DATE

REV

DATE

DESIGN

DATE

POST-PCR

DATE

QA

DATE

RVN

DATE

RELEASE

DATE

REVISION STATUS OF SHEETS

REV

1

2

3

4

5

6

7

CHK

DATE

DESIGN

DATE

POST-PCR

DATE

QA

DATE

RVN

DATE

RELEASE

DATE

APPROVAL

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SPECTRUM DIGITAL INCORPORATED

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TMS320F28335 EzDSP

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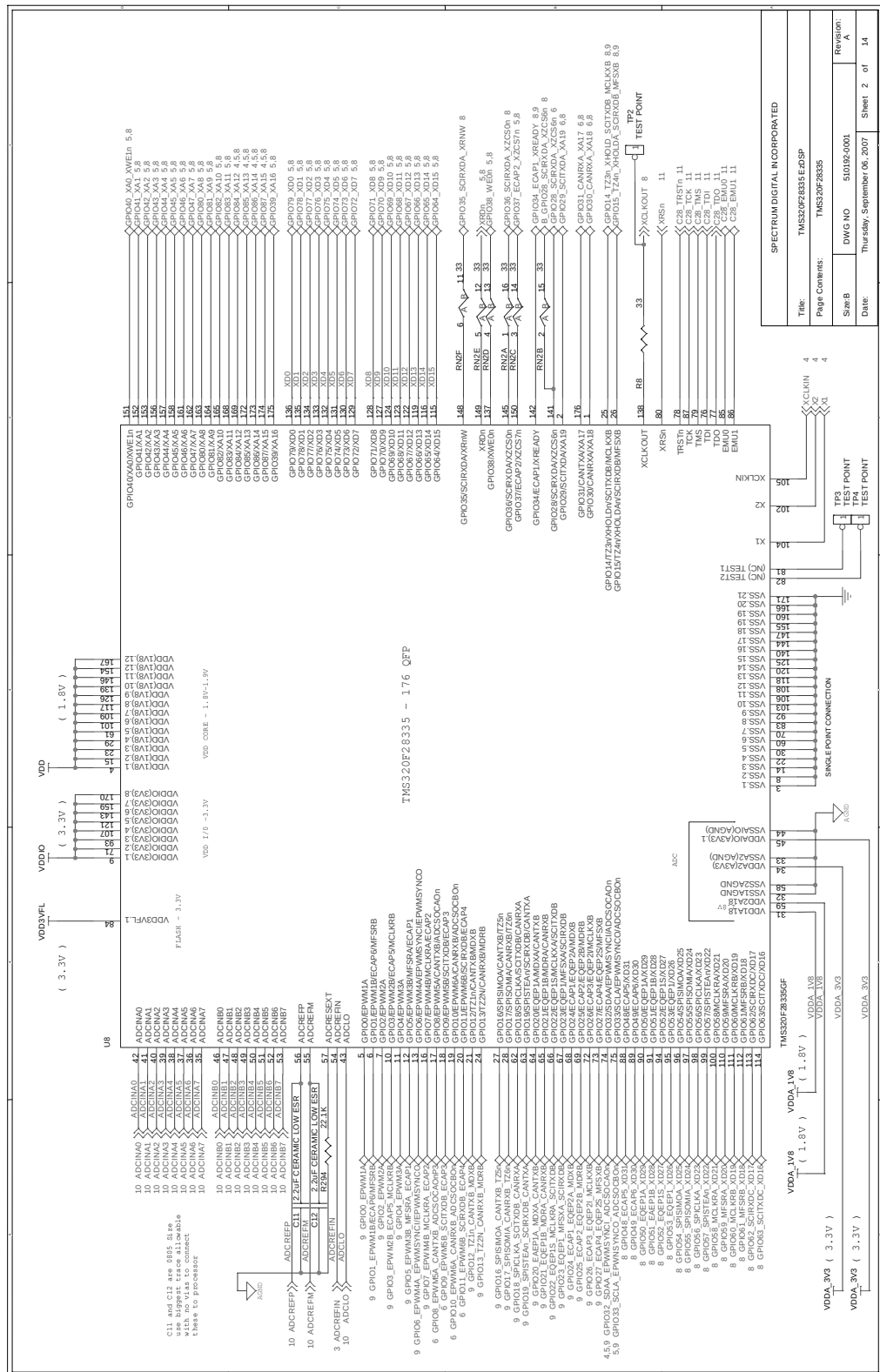
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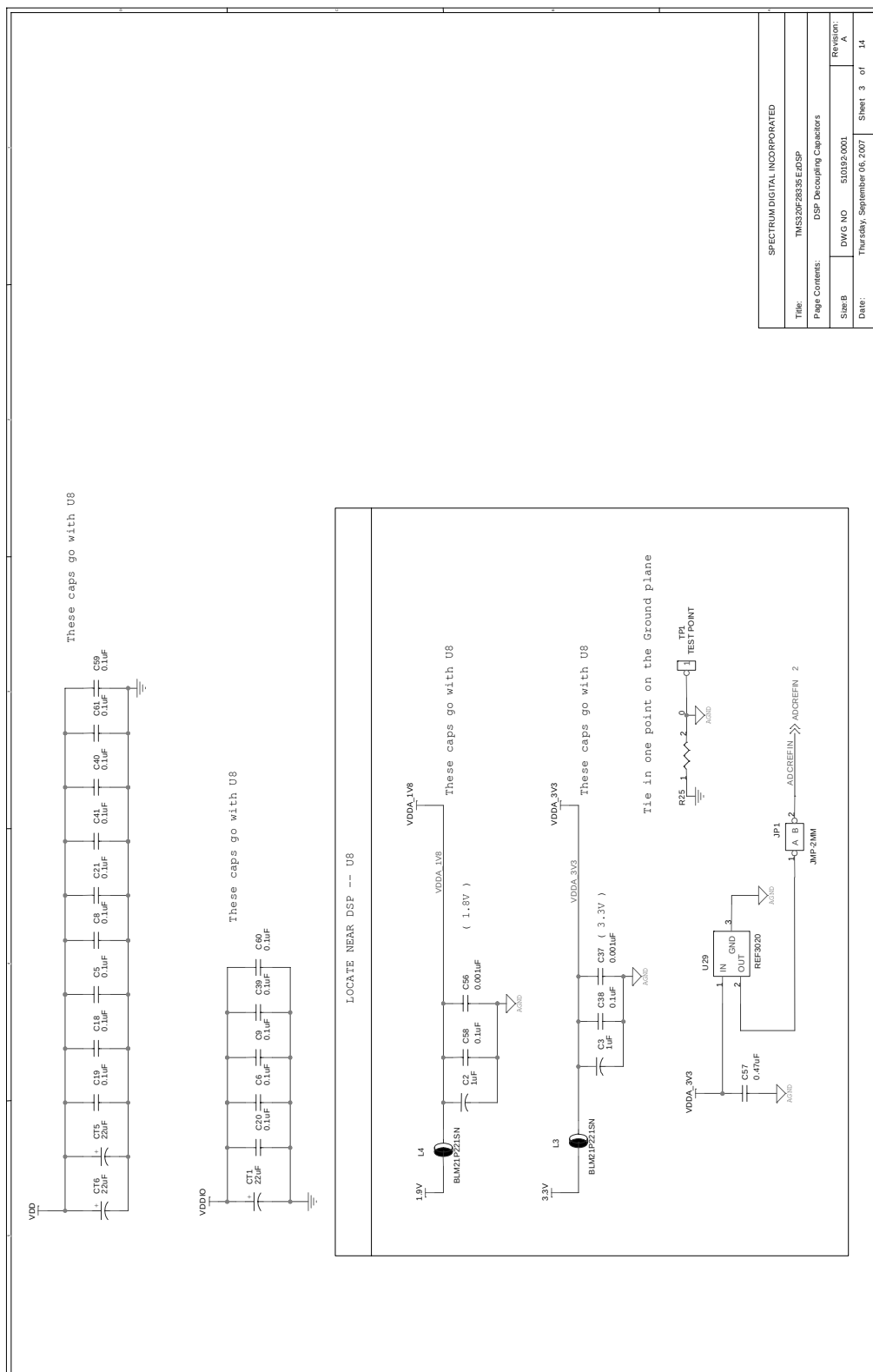
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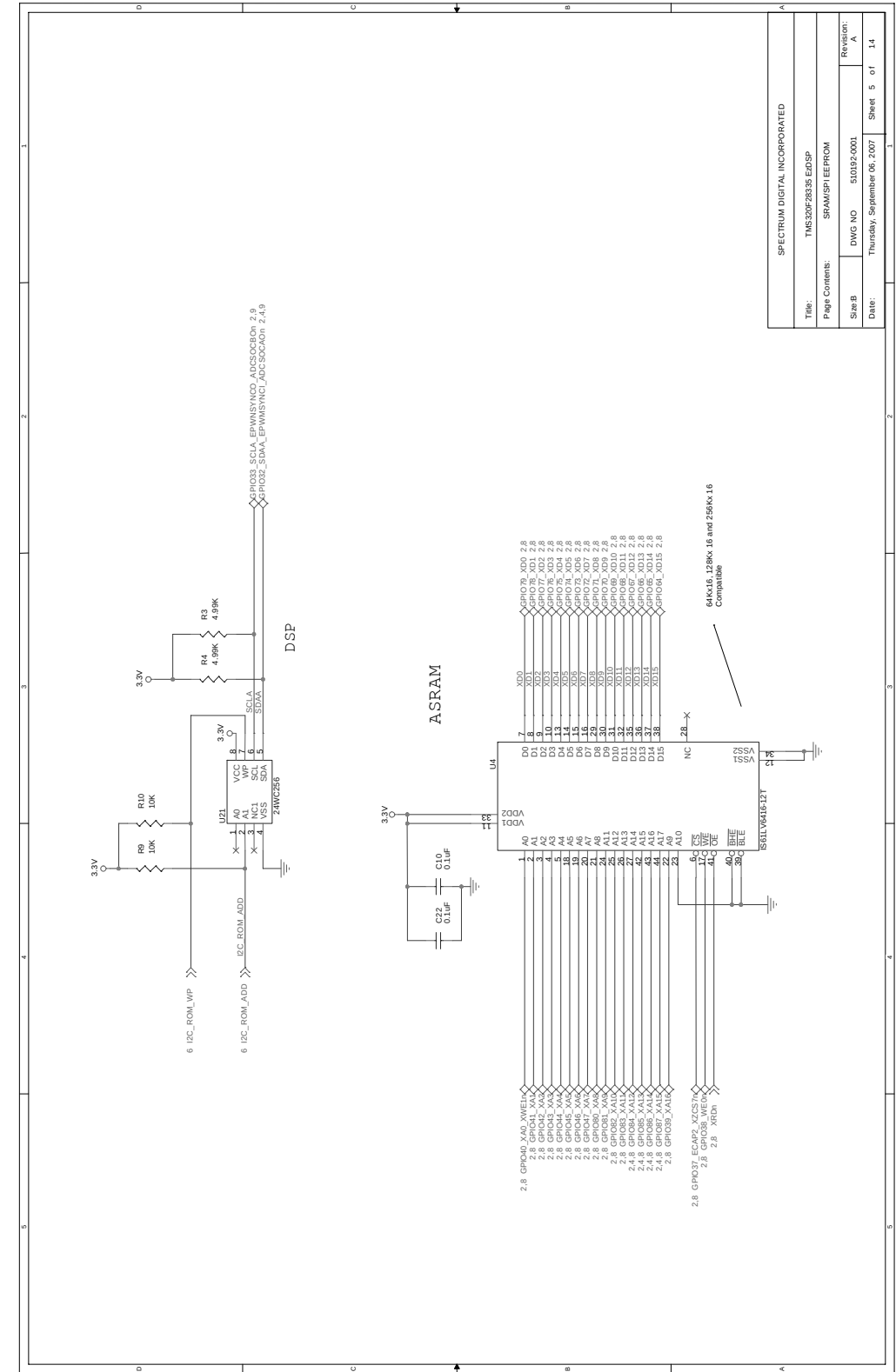
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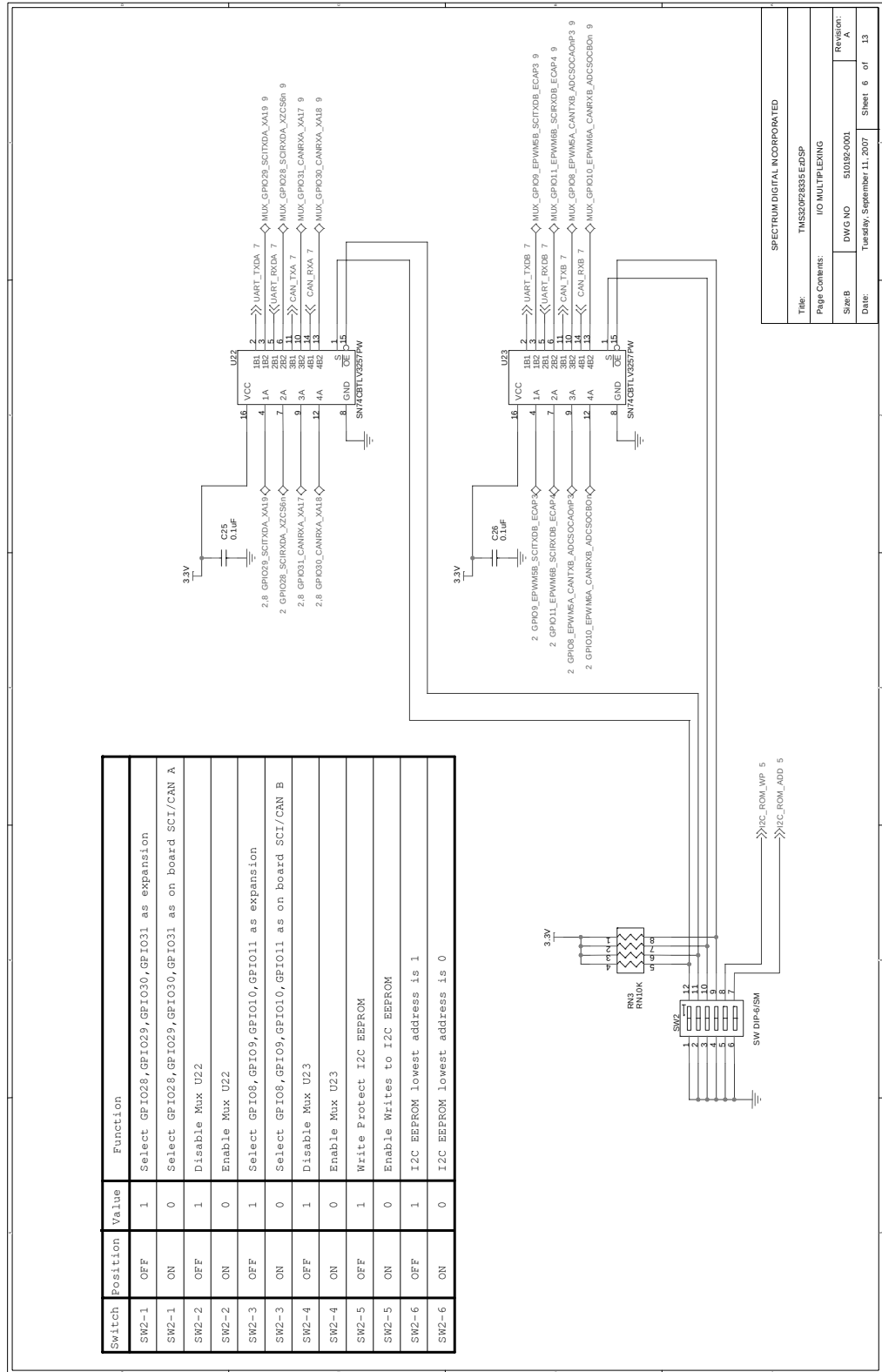
The TMS320F28335 EzDSP design is based on preliminary information (SPRS439 June 2007) for the TMS320F28335 device. This schematic is subject to change without notification. Spectrum Digital Inc. assumes no liability for applications assistance, customer product design or infringement of patents described herein.

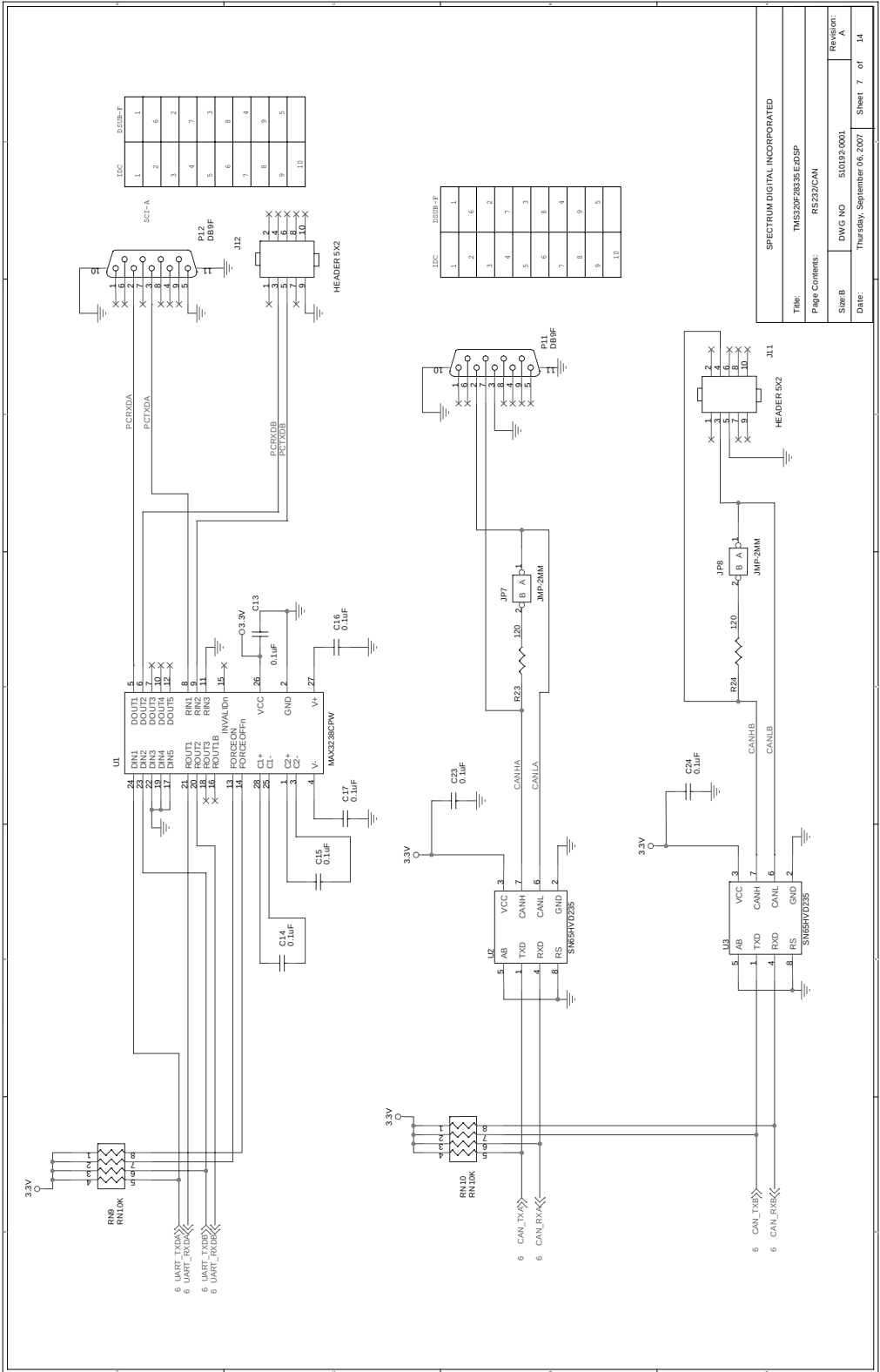




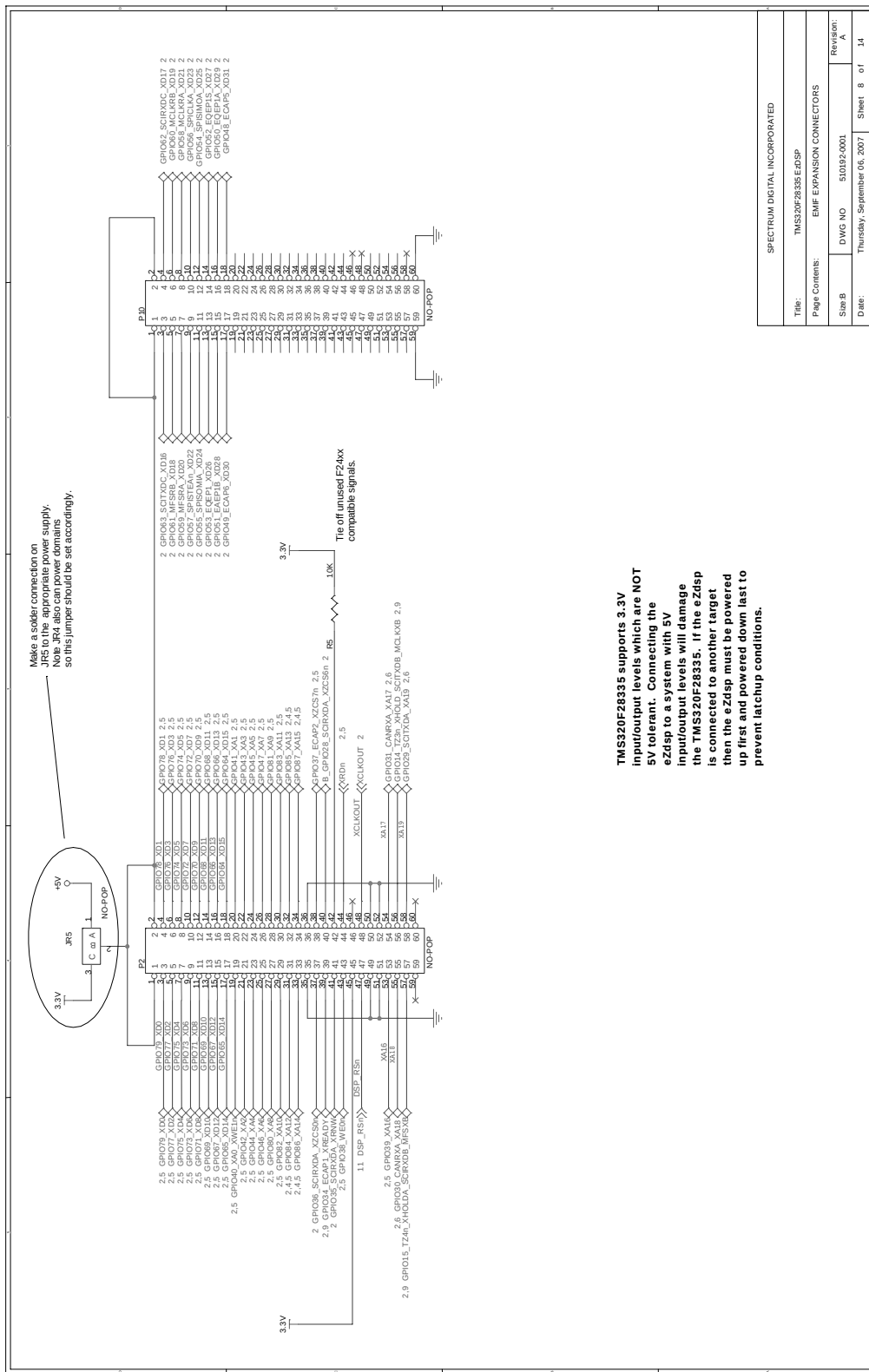


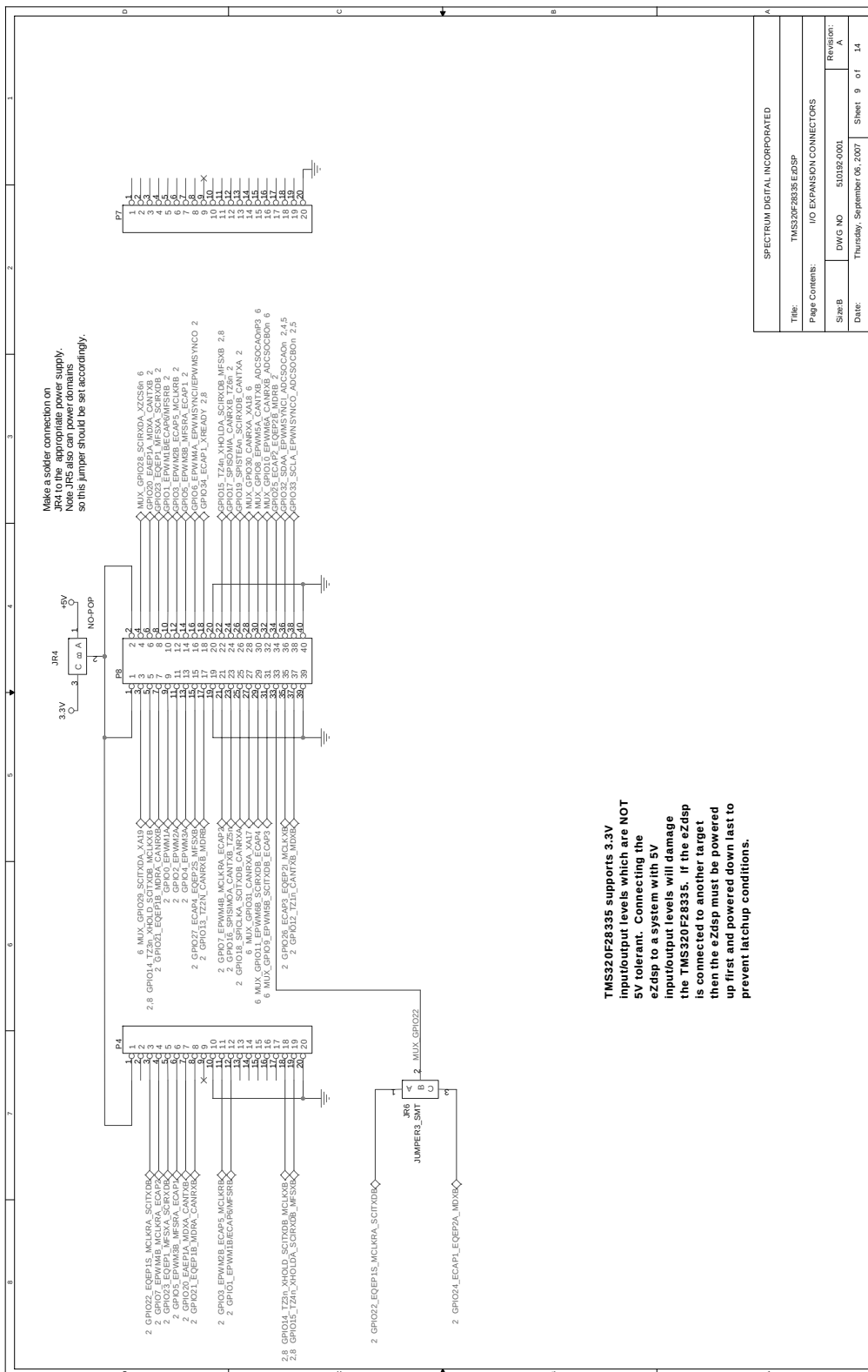












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