3-Axis Digital Angular Rate Gyroscope

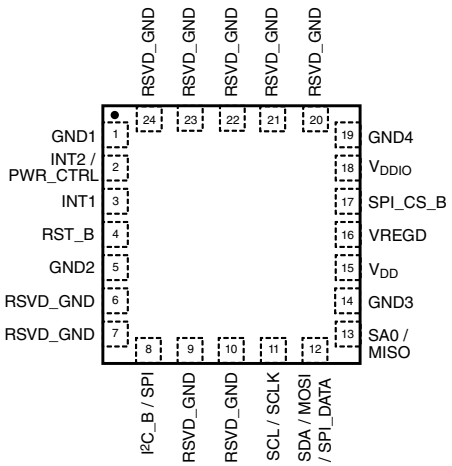
FXAS21002C

FXAS21002C is a small, low-power, yaw, pitch, and roll angular rate gyroscope with 16 bit ADC resolution. The full-scale range is adjustable from ±250°/s to ±2000°/s. It features both I^2C and SPI interfaces.

FXAS21002C is capable of measuring angular rates up to ±2000°/s, with output data rates (ODR) from 12.5 to 800 Hz. An integrated Low-Pass Filter (LPF) allows the host application to limit the digital signal bandwidth. The device may be configured to generate an interrupt when a user-programmable angular rate threshold is crossed on any one of the enabled axes.

FXAS21002C is available in a plastic, 24-lead QFN package; the device is guaranteed to operate over the extended temperature range of –40 °C to +85 °C.

24 QFN
4 mm x 4 mm x 1 mm
Case 2209-01



Pin Connections

Features

- Supply voltage (V_{DD}) from 1.95 V to 3.6 V
- Interface Supply voltage (V_{DDIO}) from 1.62 V to V_{DD} + 0.3 V
- 16-bit digital output resolution
- ±250/500/1000/2000°/s configurable full-scale dynamic ranges
- Full-Scale Range boost function enables FSR's up to ±4000 dps
- Angular rate sensitivity of 0.0625°/s in ±2000°/s FSR mode
- Noise spectral density of 25 mdps/√Hz at 64 Hz bandwidth (200 Hz ODR)
- Current consumption in Active mode is 2.7 mA
- Fast transition from Standby to Active mode (60 ms)
- Supported digital interfaces include:
  - I^2C Standard and Fast Mode (100/400 kHz)
  - SPI Interface (3- and 4-wire modes, up to 2 MHz)
- FIFO buffer is 192 bytes (32 X/Y/Z samples) with stop and circular operating modes
- Output Data Rates (ODR) from 12.5 to 800 Hz; programmable low-pass filter to further limit digital output data bandwidth
- Low power standby mode
- Power mode transition control via external pin for accelerometer-based power management (motion interrupt)
- Rate Threshold interrupt function
- Integrated self-test function
- 8-bit temperature sensor

Typical Applications

- Industrial and consumer grade robots, UAVs, and RC vehicles
- Game controller
- Gyro-stabilized electronic compass
- Orientation determination
- Gesture-based user interfaces and Human Machine Interface (HMI)
- Indoor navigation
- Mobile phones and tablets
- Virtual and augmented reality devices (including glasses)

Ordering Information

Part Number	Temperature Range	Package Description	Shipping
FXAS21002CQR1	–40 °C to +85 °C	QFN	Tape and reel (1 k)

Related Documentation

The FXAS21002C device features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents, go to freescale.com/FXAS21002C, and then click on the Documentation tab.

Table of Contents

1 General Description

1.1 Block Diagram

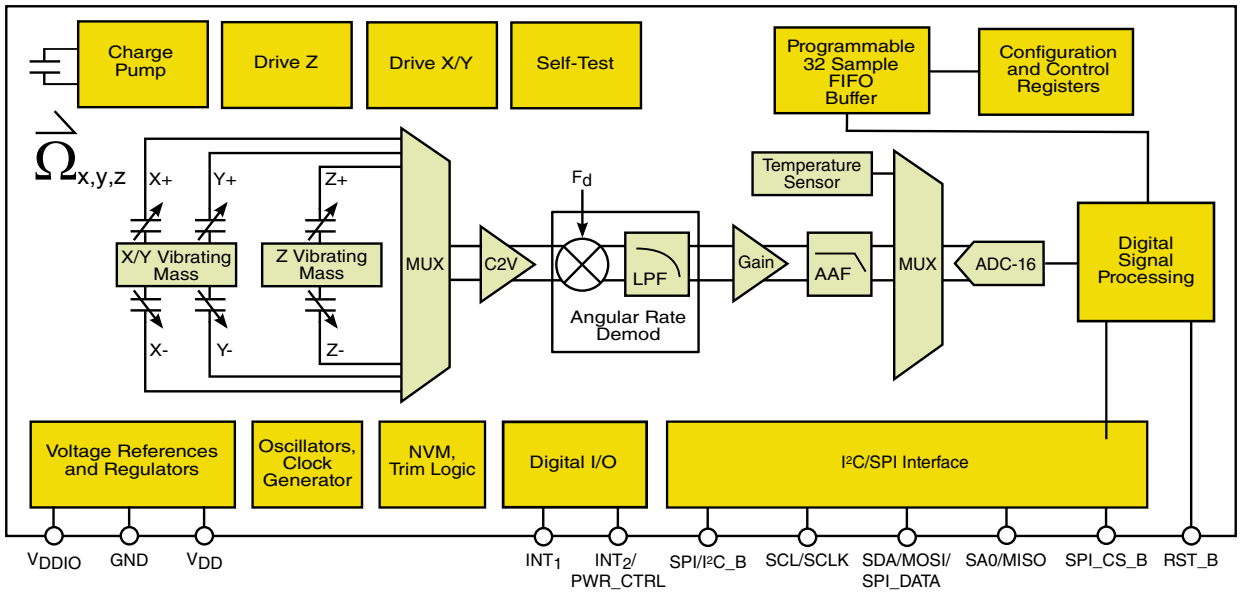


Figure 1. Block Diagram

1.2 Pinout

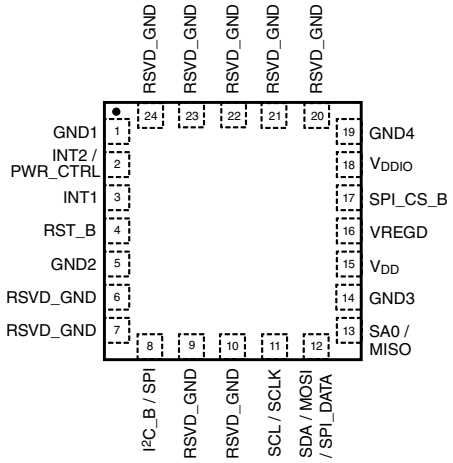


Figure 2. Device pinout (top view)

Table 1. Pin functions

Pin	Name	Function
1	GND1	Ground
2	INT2 / PWR_CTRL[1]	Interrupt Output 2 / Power state transition control input
3	INT1	Interrupt Output 1
4	RST_B	Reset input, active low. Connect this pin to V_{DDIO} if unused.
5	GND2	Ground
6	RSVD_GND	Reserved - Must be tied to ground
7	RSVD_GND	Reserved - Must be tied to ground
8	I^2C_B / SPI	Digital interface selection pin. This pin must be tied high to select SPI interface mode, or low to select I^2C interface mode.
9	RSVD_GND	Reserved pin—must be tied to ground
10	RSVD_GND	Reserved pin—must be tied to ground
11	SCL/SCLK	I^2C / SPI clock
12	SDA / MOSI / SPI_Data	I^2C data / SPI 4-wire Master Out Slave In / SPI 3-wire data In/Out[2]
13	SA0/MISO	I^2C address bit0 / SPI 4-wire Master In Slave Out
14	GND3	Ground
15	V_{DD}	Supply voltage
16	V_{REGD}	Digital regulator output. Connect a 0.1 µF capacitor between this pin and ground
17	SPI_CS_B	SPI chip select input, active low. This pin must be held logic high when operating in I^2C interface mode (I^2C_B/SPI set to ground) to ensure correct operation.
18	V_{DDIO}	Interface supply voltage
19	GND4	Ground
20	RSVD_GND	Reserved - Must be tied to ground
21	RSVD_GND	Reserved - Must be tied to ground
22	RSVD_GND	Reserved - Must be tied to ground
23	RSVD_GND	Reserved - Must be tied to ground
24	RSVD_GND	Reserved - Must be tied to ground

1. INT2/PWR_CTRL becomes a high-impedance input with weak internal pull-up resistor when **CTRLREG3[**EXTCTRLEN**]** = 1; the pull-up resistor is referenced to VDDIO.
2. MOSI becomes a bidirectional data pin when FXAS21002C is operated in 3-wire SPI mode with **CTRL_REG0[**SPIW**]**=1.

1.3 System Connections

The FXAS21002C offers the choice of interfacing with a host processor through either I^2C or SPI interfaces. Figure 3 and Figure 4 show the recommended circuit connections for implementing both interface options.

1.3.1 Typical Application Circuit—I²C Mode

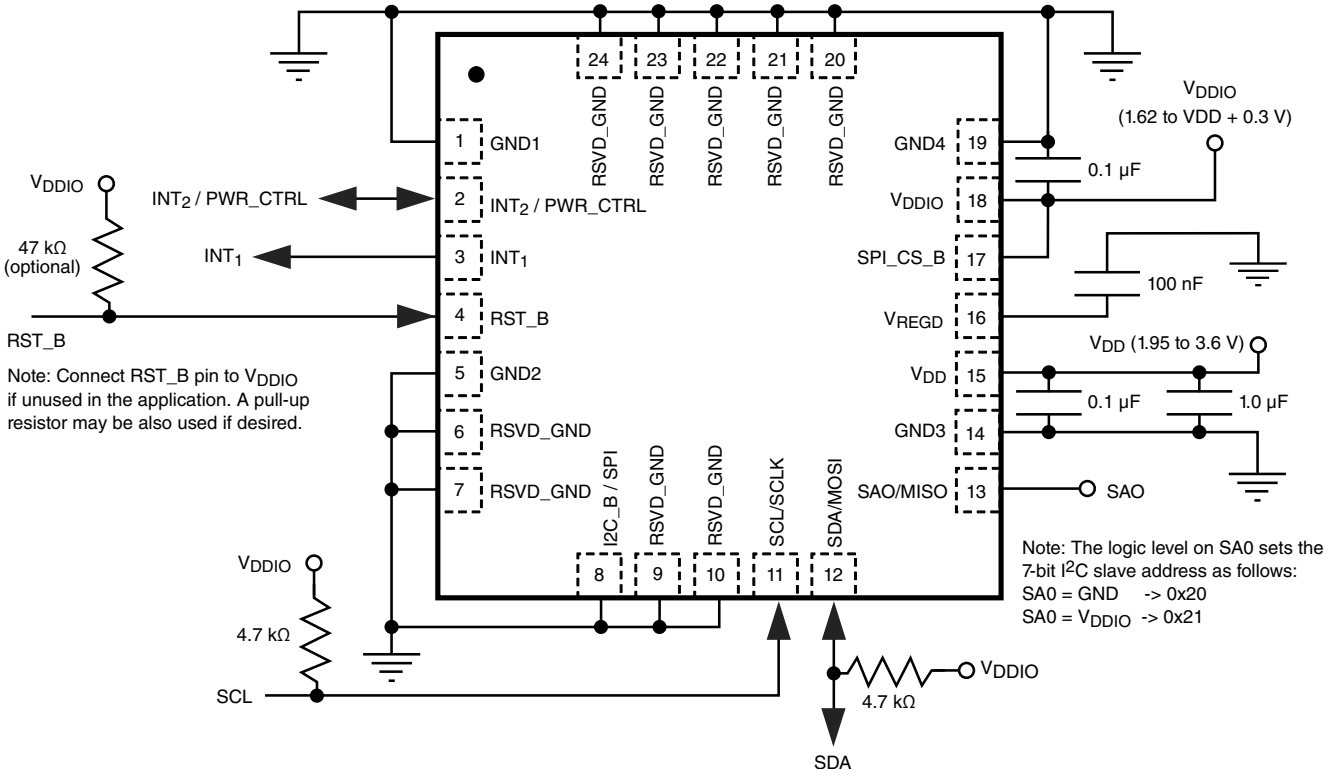


Figure 3. I²C mode electrical connections

1.3.2 Typical Application Circuit—SPI Mode

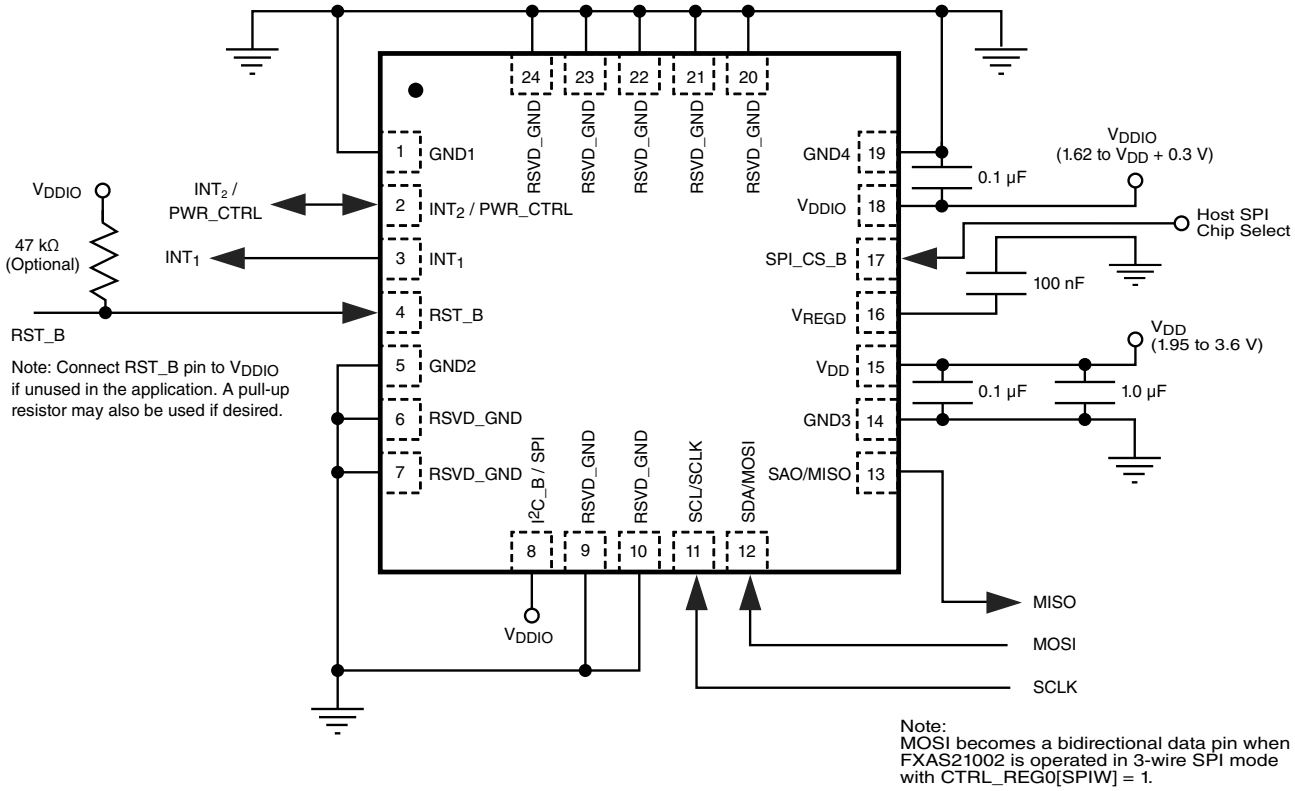


Figure 4. SPI mode electrical connections

1.4 Sensitive Axes Orientations and Polarities

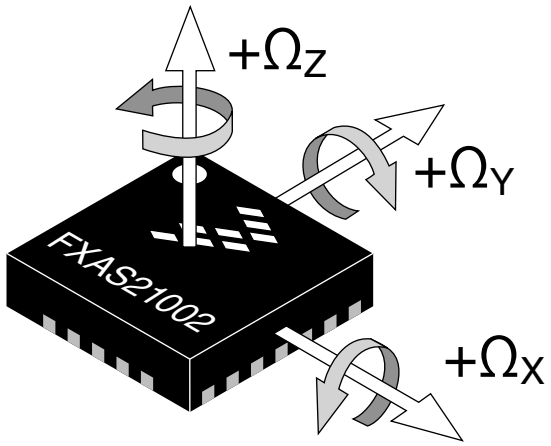


Figure 5. Reference frame for rotational measurement

2 Mechanical and Electrical Specifications

2.1 Absolute Maximum Ratings

Absolute maximum ratings are the limits the device can be exposed to without permanently damaging it. Absolute maximum ratings are stress ratings only; functional operation at these ratings is not guaranteed. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

This device contains circuitry to protect against damage due to high static voltage or electrical fields. It is advised, however, that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either GND or V_{DD}).

Table 2. Absolute maximum ratings

Rating	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	–0.3	3.6	V
Interface supply voltage	V_{DDIO}	–0.3	3.6	V
Input voltage on any control pin (SA0, SCL, SDA, RST_B, PWR_CTRL)	V_{IN}	–0.3	V_{DDIO} +0.3	V
Maximum Acceleration (all axes, 100 µs)	g_{max}	—	5000	*g*
Operating temperature	T_{OP}	–40	+85	°C
Storage temperature	T_{STG}	–40	+125	°C

Table 3. ESD and latch-up protection characteristics

Rating	Symbol	Value	Unit
Human body model (HBM)	V_{HBM}	±2000	V
Machine model (MM)	V_{MM}	±200	V
Charge device model (CDM)	V_{CDM}	±500	V
Latch-up current at T = 85 °C	I_{LU}	±100	mA

	Caution
	This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

	Caution
	This is an ESD sensitive device, improper handling can cause permanent damage to the part.

2.2 Operating Conditions

Table 4. Nominal operating conditions

Rating	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	1.95	—	3.6	V
Interface supply voltage	V_{DDIO}	1.62	—	V_{DD} + 0.3	V
Digital high level input voltage: SCL/SCLK, SDA/MOSI/SPI_DATA, SA0/MISO, SPI/ I^2C_B, RST_B, INT2/PWR_CTRL, SPI_CS_B pins	VIH	0.7 * V_{DDIO}	—	—	V
Digital low level input voltage: SCL/SCLK, SDA/MOSI/SPI_DATA, SA0/MISO, SPI/ I^2C_B, RST_B, INT2/PWR_CTRL, SPI_CS_B pins	VIL	—	—	0.3 * V_{DDIO}	V
Operating temperature	Top	–40	+25	+85	°C

2.3 Mechanical Characteristics

Table 5. Mechanical characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC Resolution	n	—	—	16	—	bits
Full-scale range	FSR	**CTRL_REG0**[FS] = 00 **CTRL_REG0**[FS] = 01 **CTRL_REG0**[FS] = 10 **CTRL_REG0**[FS] = 11	—	±2000 ±1000 ±500 ±250	—	dps
Sensitivity	S_o	**CTRL_REG0**[FS] = 00 **CTRL_REG0**[FS] = 01 **CTRL_REG0**[FS] = 10 **CTRL_REG0**[FS] = 11	—	62.5 31.25 15.625 7.8125	—	mdps/LSB
Sensitivity Temperature Coefficient	ε_T	–40 to +85 °C	—	XY: ±0.08 Z: ±0.01	—	%/°C
Zero-rate Offset	D_O	**CTRL_REG0**[FS] = 00	—	±25	—	LSB
Zero-rate Offset, Post-Board Mount[1]	$D_{O\text{-}PBM}$	**CTRL_REG0**[FS] = 00	—	±50	—	LSB

Table continues on the next page...

Table 5. Mechanical characteristics (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Zero Rate Bias Temperature Coefficient	D_T	–40 to +85 °C	—	XY: ±0.02 Z: ±0.01	—	dps/°C
Cross axis sensitivity	CAS	max(S_{XY}, S_{XZ}, S_{YX}, S_{YZ}, S_{ZX}, S_{ZY})	—	±1.5	—	%
Integral nonlinearity (deviation from linear response)	INL	**CTRL_REG0[**FS**]** = 00	—	±0.5	—	%FSR
Self-test output change[2]	STOC	**CTRL_REG0[**FS**]** = 00	7000	16000	25000	LSB
Maximum output data rate	ODR_{MAX}	—	—	800	—	Hz
Noise density	ND	ODR = 200 Hz, **CTRL_REG0[**FS**]** = 00, **CTRL_REG0[**BW**]** = 00	—	0.025	—	dps/√Hz
Test conditions (unless otherwise noted):						
• V_{DD} = 2.5 V • V_{DDIO} = 1.8 V • T = 25 °C						

1. Post Board Mount Offset Specifications are based on an eight-layer PCB.
2. The Self-Test function can be used to verify the correct functioning of the ASIC measurement chain and gyro drive circuitry. The Self-Test function will only produce a meaningful result when the device is maintained stationary during the test. The Self-Test output value will be either positive or negative due to factory trimming, therefore, the absolute value of the Self-Test result should be used.

2.4 Electrical Characteristics

Table 6. Electrical characteristics

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	—	1.95	2.5	3.6	V
Interface supply	V_{DDIO}	—	1.62	—	V_{DD}+0.3	V
Current consumption in Active mode	Idd_{Act}	Active mode	—	2.7	—	mA
Current consumption in Ready mode	Idd_{Rdy}	Ready mode	—	1.6	—	mA
Supply current drain in Standby mode	Idd_{Stby}	Standby mode	—	2.8	—	µA
Supply current in Standby mode over temperature	$IDD_{STBY-OT}$	–40 ≤ T ≤ 85 °C	—	—	7.5	µA
Digital high level input voltage SCL/SCLK, SDA/MOSI/ SPI_DATA, SA0/MISO, SPI/ I^2C_B, RST_B, INT2/ PWR_CTRL, SPI_CS_B	VIH	—	0.7 * V_{DDIO}	—	—	V

Table continues on the next page...

Table 6. Electrical characteristics (continued)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Digital low level input voltage SCL/SCLK, SDA/MOSI/SPI_DATA, SA0/MISO, SPI/I²C_B, RST_B, INT2/PWR_CTRL, SPI_CS_B	VIL	—	—	—	0.3 * V_{DDIO}	V
High-level output voltage INT1, INT2/PWR_CTRL, SDA/MOSI/SPI_DATA, SA0/MISO	VOH	I_O = 1 mA	0.9 * V_{DDIO}	—	—	V
Low-level output voltage INT1, INT2/PWR_CTRL, SDA/MOSI/SPI_DATA, SA0/MISO	VOL	I_O = 1 mA	—	—	0.1 * V_{DDIO}	V
Low-level output voltage SDA	VOL_{SDA1}	I_O = 3 mA, V_{DDIO} ≥ 2V	—	—	0.4 * V_{DDIO}	V
	VOL_{SDA2}	I_O = 3 mA, V_{DDIO} < 2V	—	—	0.2 * V_{DDIO}	
Output Data Rate frequency tolerance	ODR_{TOL}	—	—	±2.5	—	% ODR
Output Signal bandwidth	BW	—	4	< ODR/2	256	Hz
Standby to Active mode transition time	$T_{Stdy-Act}$	—	—	1/ODR + 60	—	ms
Ready to Active mode transition time	$T_{Rdy-Act}$	—	—	1/ODR + 5	—	ms
Test conditions (unless otherwise noted): • V_{DD} = 2.5 V • V_{DDIO} = 1.8 V • T = 25°C						

2.5 Temperature Sensor Characteristics

Table 7. Temperature sensor characteristics

Characteristic	Symbol	Condition(s)	Min	Typ	Max	Unit
Full-scale range	T_{FSR}	—	–40	—	+85	°C
Operating temperature	T_{OP}	—	–40	+25	+85	°C
Sensitivity	T_{SENS}	—	—	1	—	°C/LSB
Test conditions (unless otherwise noted): • V_{DD} = 2.5 V • V_{DDIO} = 1.8 V						

3 Digital Interfaces

The registers embedded inside the device are accessed through either an I^2C or an SPI serial interface. To enable either interface, the V_{DDIO} line must be connected to the interface supply voltage. If V_{DD} is not present and V_{DDIO} is present, FXAS21002C is in shutdown mode and communications on the interface are ignored. If V_{DDIO} is maintained, V_{DD} can be powered off and the communications pins will be in a high impedance state. This will allow communications to continue on the bus with other devices.

Table 8. Serial interface pin descriptions

Pin name	Pin description
V_{DDIO}	Digital interface power
SPI_CS_B	SPI chip select
SCL/SCLK	I^2C/SPI serial clock
SDA/MOSI/SPI Data	I^2C serial data/SPI master serial data out slave serial data in /SPI 3-wire data input/output
SA0/MISO	I^2C least significant bit of the device address/SPI master serial data in slave serial data out
I^2C_B/SPI	Digital interface mode selection pin

3.1 I²C Interface

To use the I^2C interface, the I^2C_B/SPI (pin 8) pin must be connected to GND (logic low) and the SPI_CS_B (pin 17) must be made logic high (by providing it a voltage equal to V_{DDIO}). FXAS21002C's I^2C interface is compliant with I^2C interface specification for Standard and Fast modes as outlined in the *I^2C-bus specification and user manual - Rev 4*, published by NXP Semiconductors. The 7-bit slave addresses that may be assigned to the device are 0x20 (with SA0 = 0) and 0x21 (with SA0 = 1). When I^2C_B/SPI is held low, the SA0/MISO pin is used to define the LSB of this I^2C address. This part does not implement clock stretching. See Table 9 for the I^2C slave addresses.

Table 9. I^2C Slave Addresses

Command	Device Address Bit[0] (SA0 pin state)	Slave Address Bits[6:0]	R/W Bit	Slave Address Byte Transmitted by Master
Read	0	0x20	1	0x41
Write	0	0x20	0	0x40
Read	1	0x21	1	0x43
Write	1	0x21	0	0x42

The key bus timing constraints are shown in Table 10. The I²C timing diagram is shown in Figure 6.

Table 10. Slave timing values

Parameter	Symbol	I²C Standard Mode[1, 2]		I²C Fast Mode[1, 2]		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Bus free time between STOP and START conditions	t_{BUF}	4.7	—	1.3	—	µs
Hold time (repeated) START condition	$t_{HD;STA}$	4.0	—	0.6	—	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	—	0.6	—	µs
Set-up time for a STOP condition	$t_{SU;STO}$	4.0	—	0.6	—	µs
SDA valid time[2]	$t_{VD;DAT}$	—	3.45[3]	—	0.9[3]	µs
SDA valid acknowledge time[4]	$t_{VD;ACK}$	—	3.45[3]	—	0.9[3]	µs
SDA setup time	$t_{SU;DAT}$	250	—	100[5]	—	ns
SCL clock low time	t_{LOW}	4.7	—	1.3	—	µs
SCL clock high time	t_{HIGH}	4.0	—	0.6	—	µs
SDA and SCL rise time	t_r	—	1000	20	300	ns
SDA and SCL fall time[6]	t_f	—	300	20*(V_{DDIO}/5.5 V)	300	ns
Capacitive load for each bus line[7]	C_b	—	400	—	400	pF
Pulse width of spikes on SDA and SCL that must be suppressed by the internal input filter	t_{SP}	0	50	0	50	ns

1. All values refer to VIH (min) and VIL (max) levels.
2. $t_{VD;DAT}$ refers to the time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
3. The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard mode and Fast mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time.
4. $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5. A Fast-mode I²C device can be used in a Standard-mode I²C system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. Also, the acknowledge timing must meet this set-up time.
6. The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
7. C_b is the total capacitance of one bus line in pF; the maximum bus capacitance allowable may vary from this value depending on the application operating voltage and frequency.

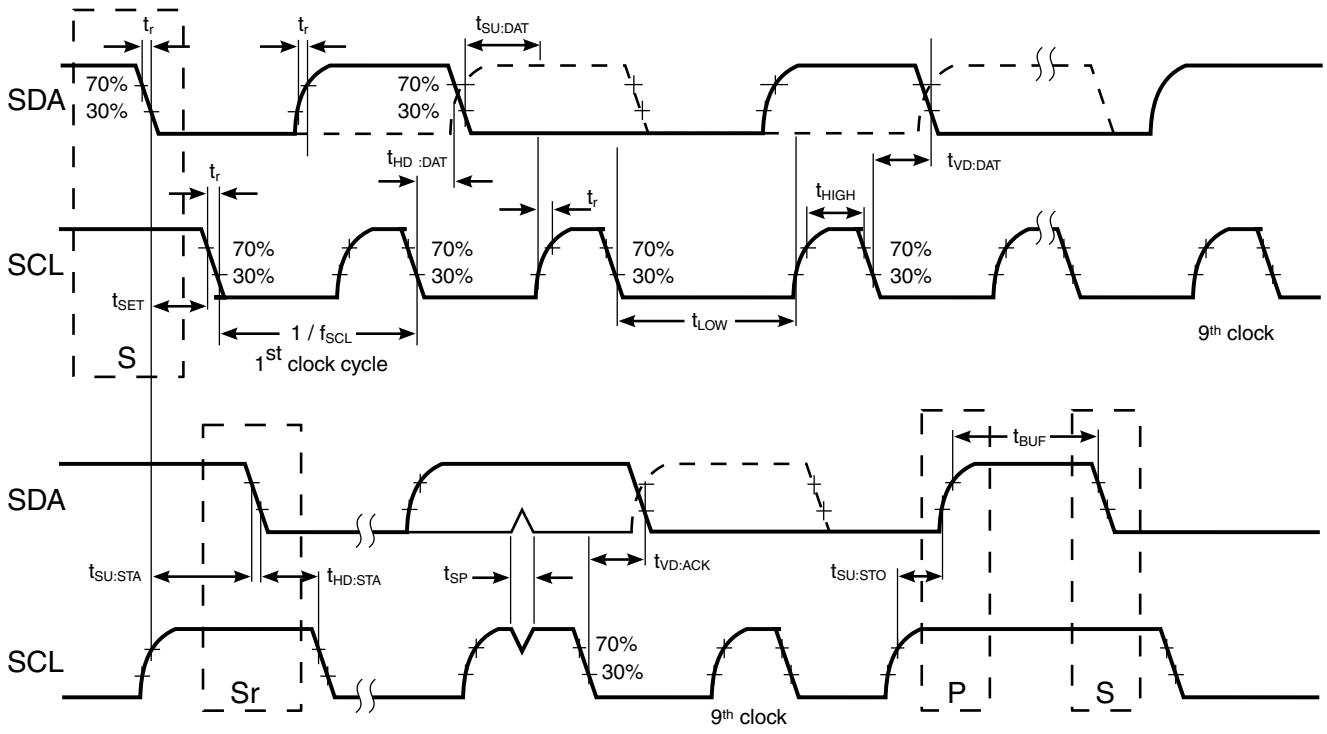


Figure 6. I²C timing diagram

3.1.1 I²C Operation

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The SDA is a bidirectional line used for sending and receiving the data to and from the interface. External pull-up resistors connected to V_{DDIO} are required for SDA and SCL. When the bus is free, the lines are high.

The maximum practical operating frequency for I²C in a given system implementation depends on several factors including the pull-up resistor values, and the total bus capacitance (trace + parasitic device capacitances).

A transaction on the bus is started through a start condition (ST) signal, which is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After the ST signal has been transmitted by the master, the bus is considered busy. The next byte of data transmitted contains the slave address in the first seven bits, and the eighth bit, the read/write bit, indicates whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after the ST condition with its own address. If they match, the device considers itself addressed by the master. The ninth clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK).

The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains consistently low during the high period of the acknowledge clock period. The number of bytes per transfer is unlimited. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. This delay action is called clock stretching. Not all receiver devices support clock stretching. Not all master devices recognize clock stretching.

A LOW-to-HIGH transition on the SDA line while SCL is high is defined as a stop condition (SP) signal. A write or burst write is always terminated by the master issuing the SP signal. A master should properly terminate a read by not acknowledging a byte at the appropriate time in the protocol. A master may also issue a repeated start signal (SR) during a transfer.

3.1.2 I²C Read Operations

3.1.2.1 Single-Byte Read

The master (or MCU) transmits an ST to the FXAS21002C, followed by the slave address, with the R/W bit set to “0” for a write, and the FXAS21002C sends an acknowledgement. Then, the MCU transmits the address of the register to read and the FXAS21002C sends an acknowledgement. The MCU transmits an SR, followed by the byte containing the slave address and the R/W bit set to “1” for a read from the previously selected register. The FXAS21002C then acknowledges and transmits the data from the requested register. The master transfers a NACK followed by an SP, signaling an end of transmission.

3.1.2.2 Multiple-Byte Read

When performing a multiple-byte or burst read, the FXAS21002C increments the register address read pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential registers after each FXAS21002C ACK is received. This continues until the master transfers a NACK followed by an SP, signaling an end of transmission.

3.1.3 I²C Write Operations

3.1.3.1 Single-Byte Write

To start a write command, the master transmits an ST to the FXAS21002C, followed by the slave address with the R/W bit set to “0” for a write, and the FXAS21002C sends an ACK. Then, the master transmits the address of the register to write to, and the FXAS21002C sends an ACK. Then, the master transmits the 8-bit data to write to the designated register and the FXAS21002C sends an ACK that it has received the data. Since this transmission is complete, the master transmits an SP to end the data transfer. The data sent to the FXAS21002C is now stored in the appropriate register.

3.1.3.2 Multiple-Byte Write

The FXAS21002C automatically increments the register address write pointer after a write command is received. Therefore, after following the steps of a single-byte write, multiple bytes of data can be written to sequential registers after each FXAS21002C ACK is received.

3.1.3.3 I²C Data Sequence Diagrams

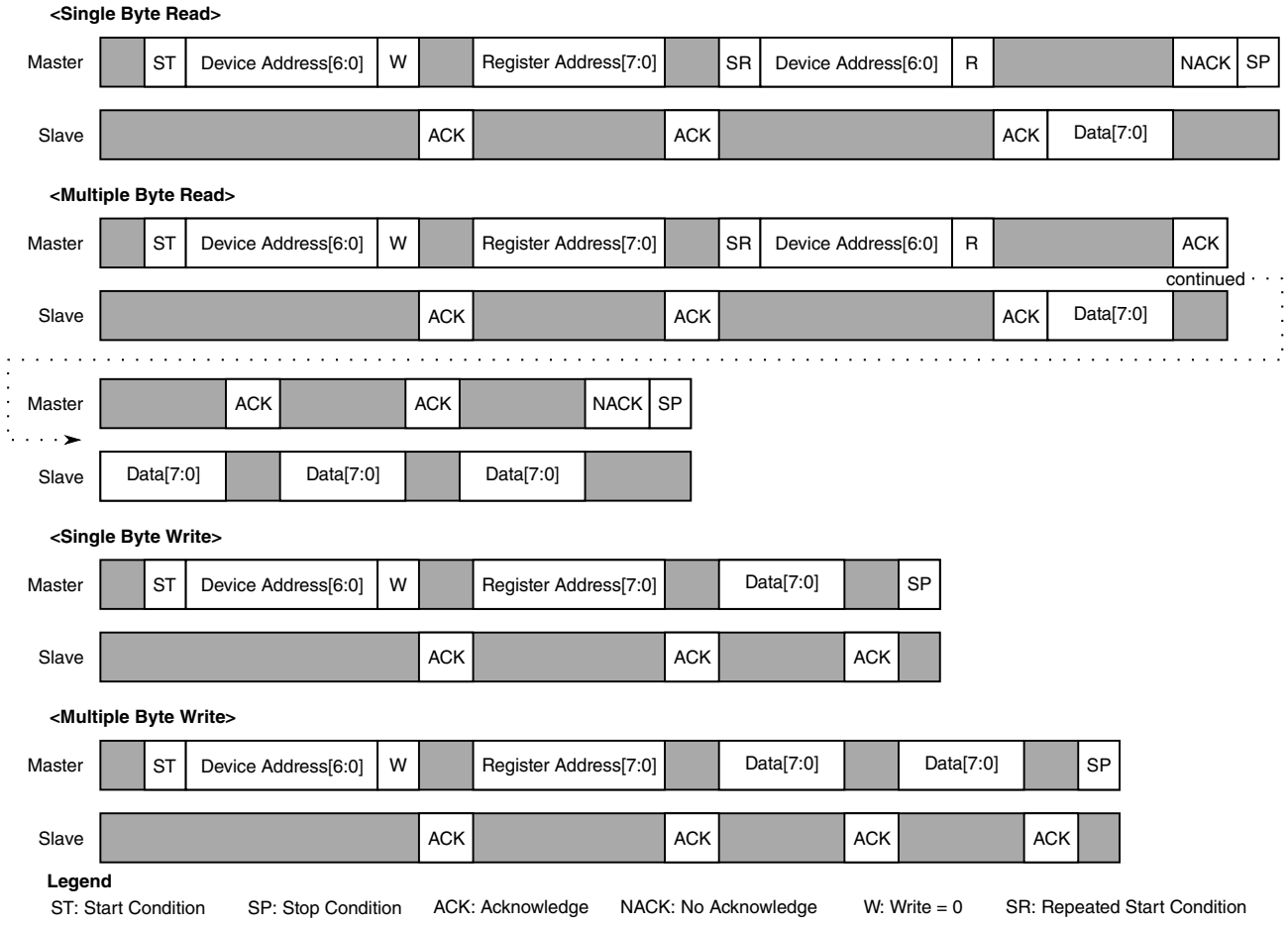


Figure 7. I²C data sequence diagram

3.2 SPI Interface

The SPI interface is a classical Master/Slave serial port. FXAS21002C is always considered to be the slave device and thus never initiates a communication with the host processor.

The SPI interface of FXAS21002C is compatible with SPI interface mode 00, corresponding to CPOL = 0 and CPHA = 0.

For CPOL = 0, the idle value of the clock is zero, and the active value of the clock is 1. For CPHA = 0, data is captured on the clock's rising edge (low to high transition) and data is propagated on the clock’s falling edge (high to low transition).

3.2.1 General SPI Operation

The SPI_CS_B pin is driven low at the start of a transaction, held low for the duration of the transfer, and then driven high again after the transaction is completed. During a transaction, the master toggles the clock (SCLK). The SCLK polarity is defined as having an idle value that is low, and an active phase that is high (CPOL = 0). Serial input and output data is captured on the clock's rising edge and propagated on the falling edge (CPHA = 0). Single byte read and single byte write operations are completed in 16 SCLK cycles; multiple byte reads and writes are completed in additional multiples of 8 SCLK cycles. The first SCLK cycle latches the most significant bit on MOSI to select whether the desired operation is a read (R/W = 1) or a write (R/W = 0). The following seven SCLK cycles are used to latch the slave register read or write address.

NOTE

4-wire SPI interface mode is the default out of POR or after a hard/soft reset. The 3-wire interface mode may be selected by setting **CTRL_REG0**[SPIW] = 1.

3.2.2 SPI Write Operations with 3- and 4-Wire Modes

A write operation is initiated by transmitting a 0 for the R/W bit. Then, the 7-bit register write address, A[6:0], is transmitted in MSb first order. The data byte to be written is then transferred during the second 8 SCLK cycle period (again, with MSb first). Figure 8 and Figure 9 shows the bus protocol for a single byte register write operation in either 3- or 4-wire SPI modes.

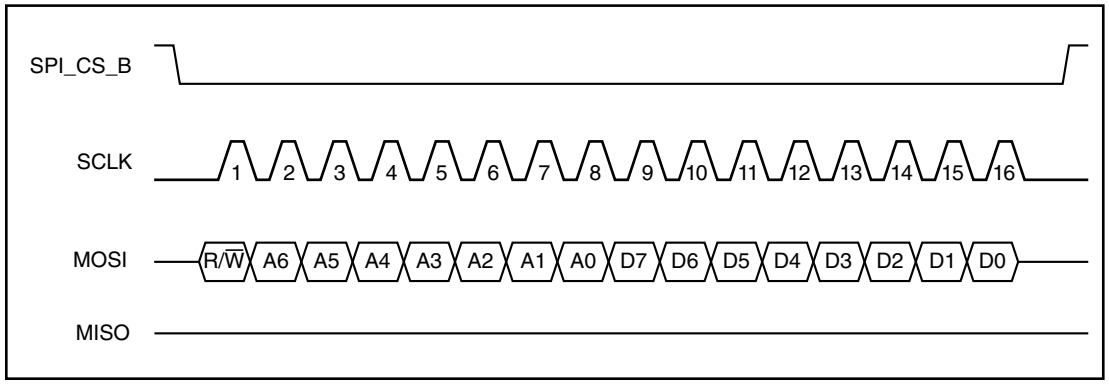


Figure 8. SPI single byte write protocol diagram (4-wire mode), R/W = 0

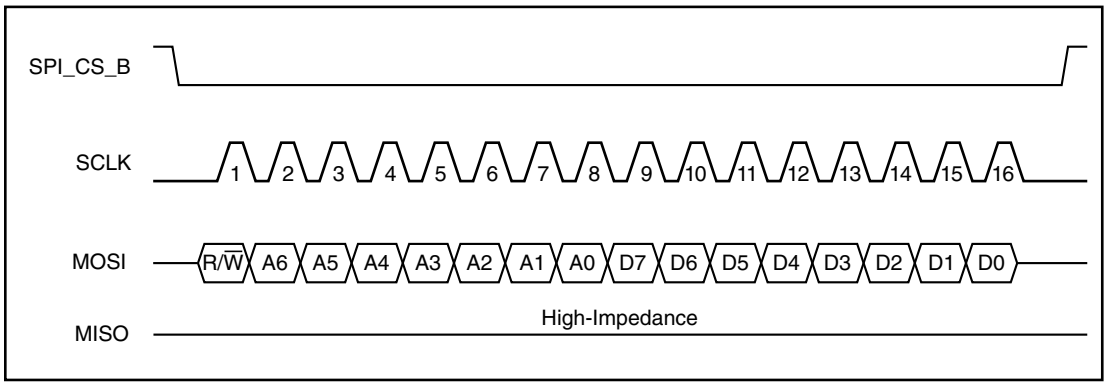


Figure 9. SPI single byte write protocol diagram (3-wire mode), R/W = 0

Multiple-byte write operations are performed similarly to the single-byte write sequence, but with additional data bytes transferred over every 8 SCLK cycle period. The register write address is internally auto-incremented by FXAS21002C so that every eighth clock edge will latch the address for the next register write address. When the desired number of bytes has been written, the rising edge on the SPI_CS_B pin terminates the transaction. Figure 10 and Figure 11 show the bus protocol for multiple byte register write operation in either 3- or 4-wire SPI modes.

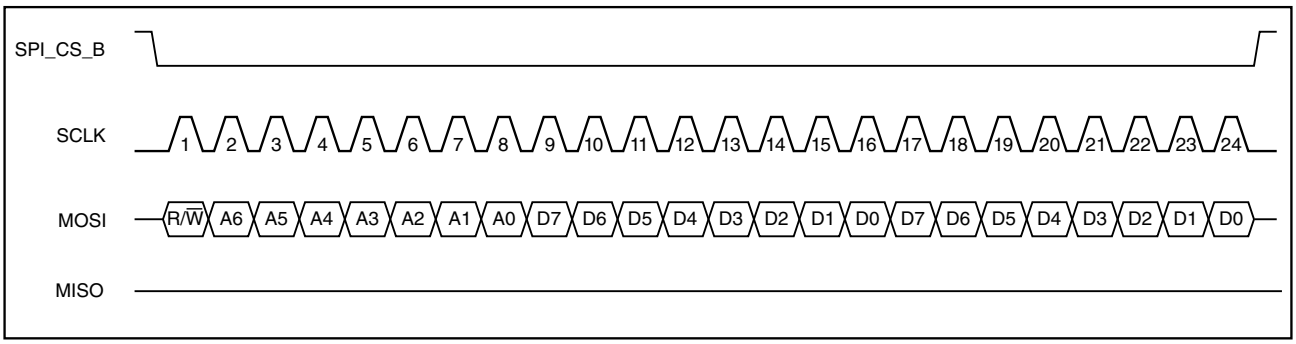


Figure 10. SPI multiple byte write protocol diagram (4-wire mode), R/W = 0

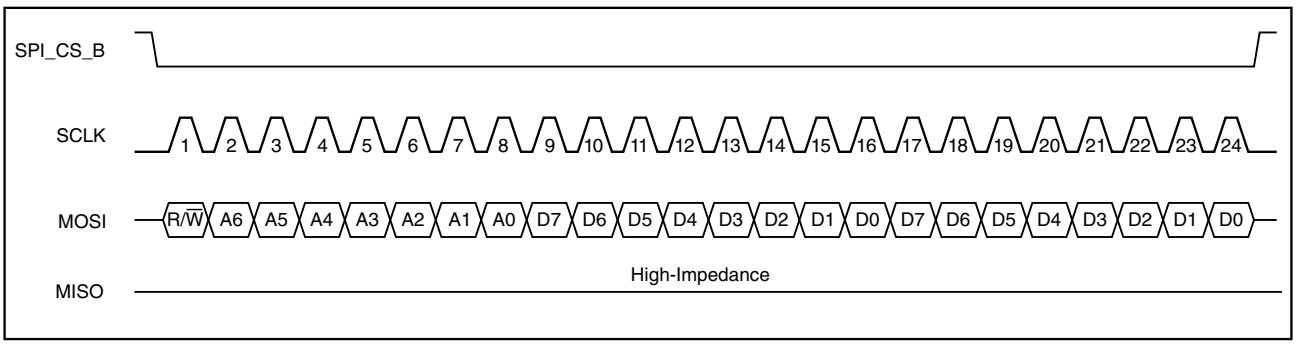


Figure 11. SPI multiple byte write protocol diagram (3-wire mode), R/W = 0

3.2.3 SPI Read Operations with 4-Wire Mode

NOTE

This description pertains only to the default SPI 4-wire interface mode (with CTRL_REG0[SPIW] = 0). This mode is the default out of POR, or after a hard/soft reset.

A register read operation is initiated by transmitting a 1 for the R/W bit. Then, the 7-bit register read address, A[6:0] is encoded in the first byte. The data is read from the MISO pin (MSB first). Figure 12 shows the bus protocol for a single byte read operation.

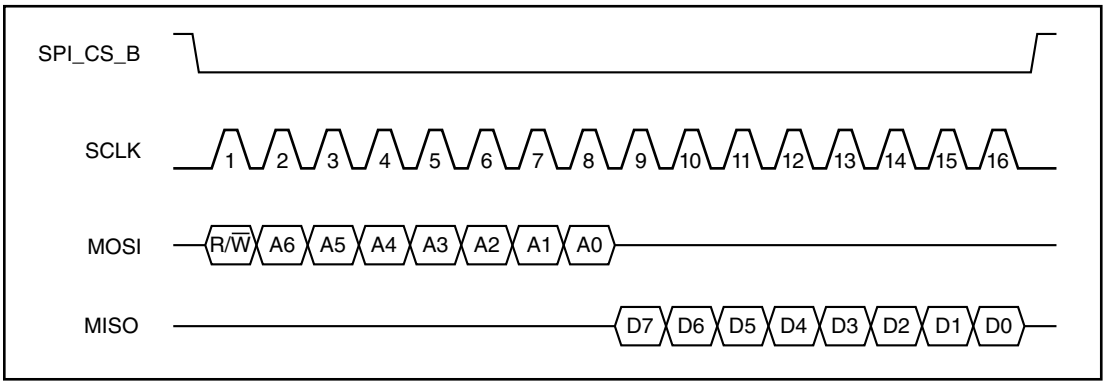


Figure 12. SPI single byte read protocol diagram (4-wire mode), R/W = 1

Multiple-byte read operations are performed similarly to single-byte reads; additional bytes are read in multiples of eight SCLK cycles. The register read address is auto-incremented by FXAS21002C so that every eighth clock edge will latch the address of the next register read address. When the desired number of bytes has been read, the rising edge on the SPI_CS_B terminates the transaction.

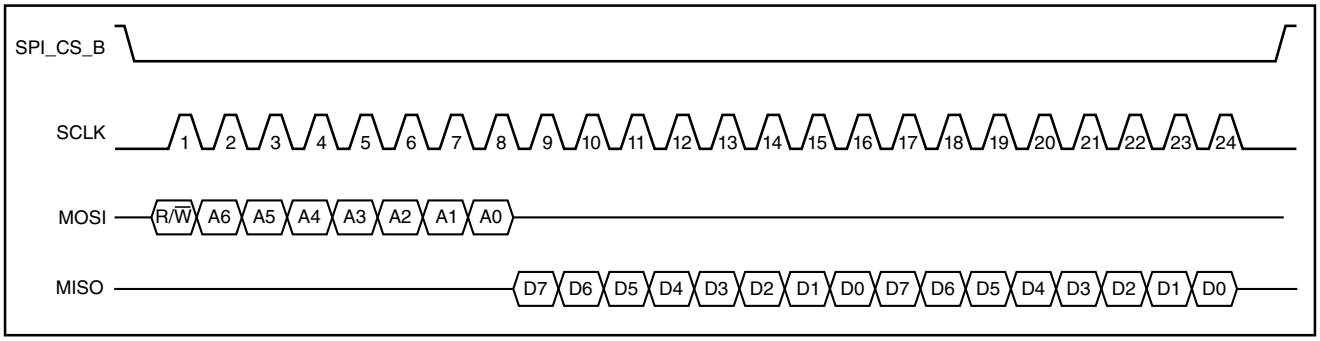


Figure 13. SPI multiple byte read protocol diagram (4-wire mode), R/W = 1

3.2.4 SPI Read Operations with 3-Wire Mode

NOTE

This description pertains only to the 3-wire SPI interface mode (with **CTRL_REG0**[SPIW] = 1). This interface mode is not the default and must be selected after a POR, or hard/soft reset.

FXAS21002C can be configured to operate in 3-wire SPI mode. In this mode the MISO pin is left unconnected or high-z, and the MOSI pin becomes a bi-directional input/output pin (SPI_DATA). 3-wire mode is selected by setting the SPIW bit in **CTRL_REG0**. Read operations in 3-wire mode are the same as in 4-wire mode except that at the end of address cycle, the MOSI (SPI_DATA) pin automatically switches from an input to an output.

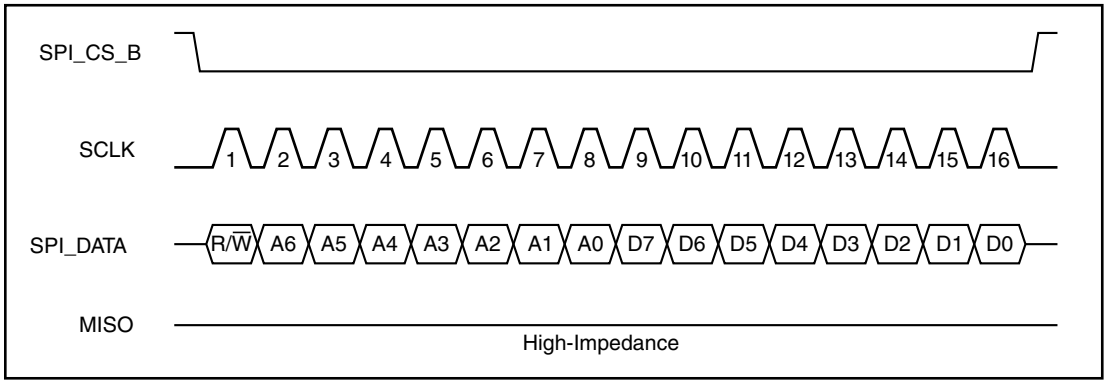


Figure 14. SPI single byte read protocol diagram (3-wire mode)

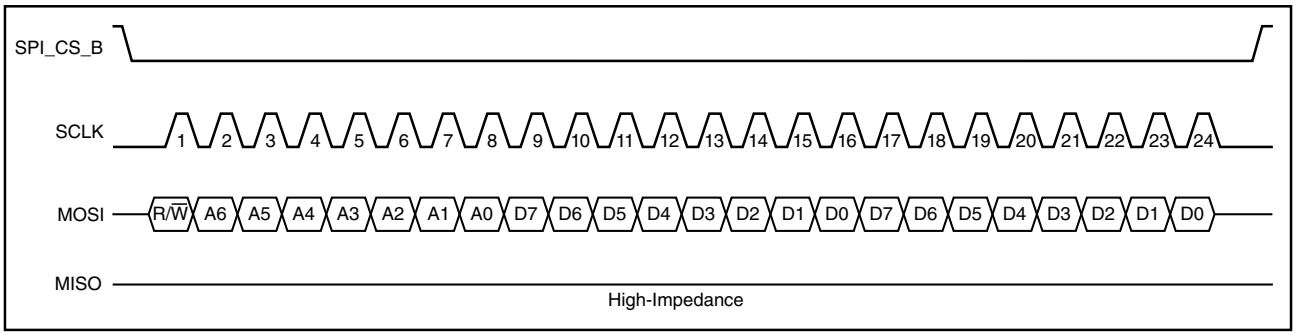


Figure 15. SPI multiple byte read protocol diagram (3-wire mode)

3.2.5 SPI Timing Specifications (4-wire mode)

Table 11 and Figure 16 specify and illustrate the minimum and maximum timing parameter values for correct SPI interface functionality when FXAS21002C is operated in 4-wire SPI mode. The timing delays given in Table 11 are taken at 70% of the rising edge and 30% of the falling edge. FXAS21002C only supports SPI mode 00, corresponding to CPOL = 0, and CPHA = 0. In this mode, the active state of the clock is high and the idle state is low. Data is latched on the rising edge of the clock and propagated on the falling edge. Please note that the timing parameters shown in Table 11 are based on simulations performed across process, voltage, and temperature with a total bus capacitance of 80 pF and a 10 kΩ pull-up resistor to VDDIO on each SPI interface pin (SCL/SCLK, SDA/MOSI/SPI_DATA, SA0/MISO, and SPI_CS_B).

NOTE

In 4-wire SPI mode the MISO pin is always placed in a high impedance state when CS_B is not asserted (logic high level).

Table 11. Slave timing values

Label	Description	Specifications		Unit
		Min.	Max.	
fSCLK	SCLK frequency	0	2	MHz
tSCLK	SCLK Period	500	—	ns
tSCLKH	SCLK high time	210	—	ns
tSCLKL	SCLK low time	210	—	ns
tSZ	Setup time for MISO signal (transition out of high-z state)	—	130	
tHZ	Hold time for MISO signal (transition back to high-z state)	—	110	
tSCS	Setup time for SPI_CS_B signal	250	—	ns
tHCS	Hold time for SPI_CS_B signal	200	—	ns
tWCS	Inactive time for SPI_CS_B signal	110	—	ns
tSET	Data setup time for MOSI signal	20	—	ns
tHOLD	Data hold time for MOSI signal	200	—	ns
tDDLY	Data setup time for MISO signal	—	210	ns

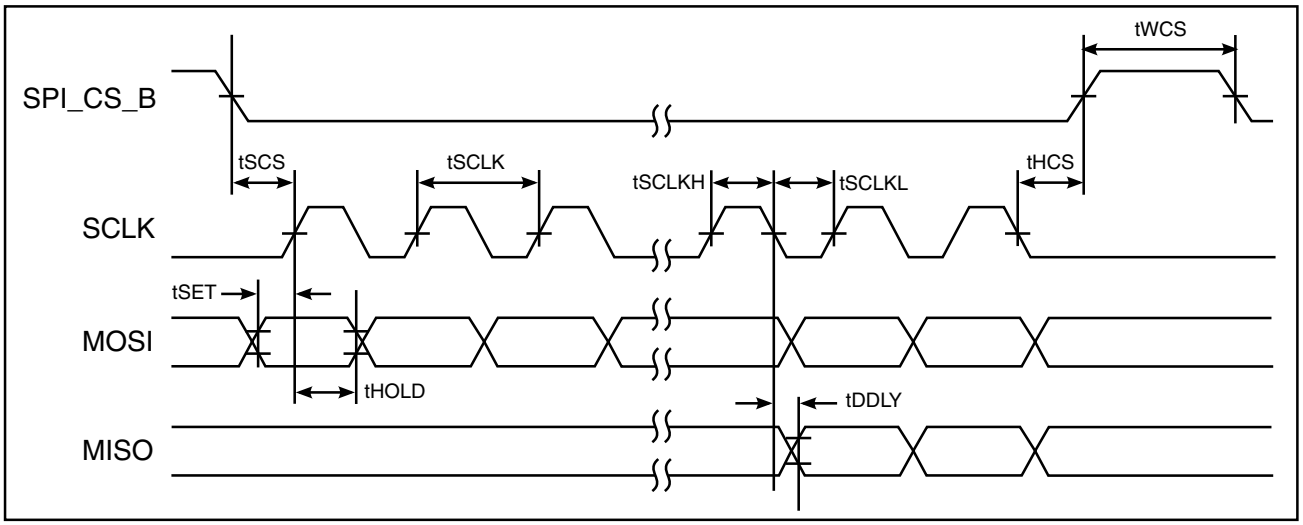


Figure 16. SPI timing diagram (4-wire mode)

3.2.6 SPI Timing Specifications (3-wire mode)

Table 12 and Figure 17 specify and illustrate the minimum and maximum timing parameter values for correct SPI interface functionality when FXAS21002C is operated in 3-wire SPI mode. The timing delays given in Table 12 are taken at 70% of the rising edge and 30% of the falling edge. FXAS21002C only supports SPI mode '00', corresponding to CPOL = 0, and CPHA = 0. In this mode, the active state of the clock is high and the idle state is low. Data is latched on the rising edge of the clock and propagated on the falling edge. Please note that the timing parameters shown in Table 12 are based on simulations performed across process, voltage, and temperature with a total bus capacitance of 80pF and a 10 kΩ pull-up resistor to VDDIO on each SPI interface pin (SCL/SCLK, SDA/MOSI/SPI_DATA, SA0/MISO, and SPI_CS_B).

NOTE

When FXAS21002C is operated in 3-wire SPI mode - by setting CTRL_REG0[SPIW] = 1 - the SA0/MISO pin is always placed in a high impedance (high-z) state.

Table 12. Slave timing values

Label	Description	Specifications		Unit
		Min.	Max.	
fSCLK	SCLK frequency	0	1.4	MHz
tSCLK	SCLK Period	714	—	ns
tSCLKH	SCLK high time	300	—	ns

Table continues on the next page...

Table 12. Slave timing values (continued)

Label	Description	Specifications		Unit
		Min.	Max.	
tSCLKL	SCLK low time	300	—	ns
tHZ	Hold time for MISO signal (transition back to high-z state)	—	200	
tSCS	Setup time for SPI_CS_B signal	250	—	ns
tHCS	Hold time for SPI_CS_B signal	200	—	ns
tWCS	Inactive time for SPI_CS_B signal	200	—	ns
tSET	Data setup time for MOSI signal	20	—	ns
tHOLD	Data hold time for MOSI signal	200	—	ns
tDDLY	Data setup time for MISO signal	—	280	ns

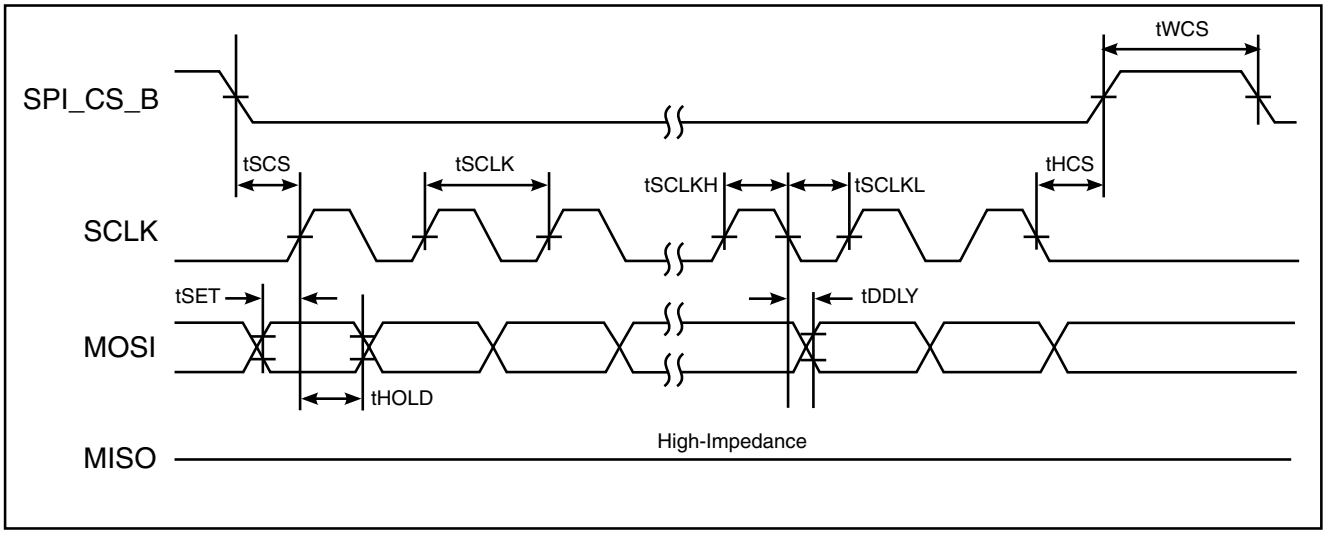


Figure 17. SPI timing diagram (3-wire mode)

4 Modes of Operation

The device may be placed into one of three functional modes:

- **Standby:** Some digital blocks are enabled; I^2C/SPI communication is possible. This mode is the minimum power consumption state for the device and is the default mode entered on POR or hard/soft reset. A transition from Standby mode to Active mode takes 1/ODR + 60 ms, typical.

- **Active:** All blocks are enabled (digital and analog); the device is actively measuring the angular rate at the ODR specified in 0x13: CTRL_REG1. This is the maximum power consumption state of the device.
- **Ready:** This mode is entered by setting **CTRL_REG1**[Ready] = 1. In this mode, the drive circuits are running but no measurements are being made. This mode offers the user the ability to significantly reduce the current draw of the device while providing a fast transition into Active mode within 1/ODR + 5 ms.

NOTE

When **CTRL_REG3**[EXTCTRLEN] = 0, the Active mode is entered/exited using the register interface (**CTRL_REG1**[ACTIVE] bit). When **CTRL_REG3**[EXTCTRLEN] = 1, the Active mode is entered/exited via the logic state on the PWR_CTRL input pin (pin 2).

The functional mode is selected using CTRL_REG1. After a POR (Power on Reset), a boot sequence is performed by the device and the registers are loaded with their preset values. After the boot sequence completes, the default operating mode of FXAS21002C is Standby mode.

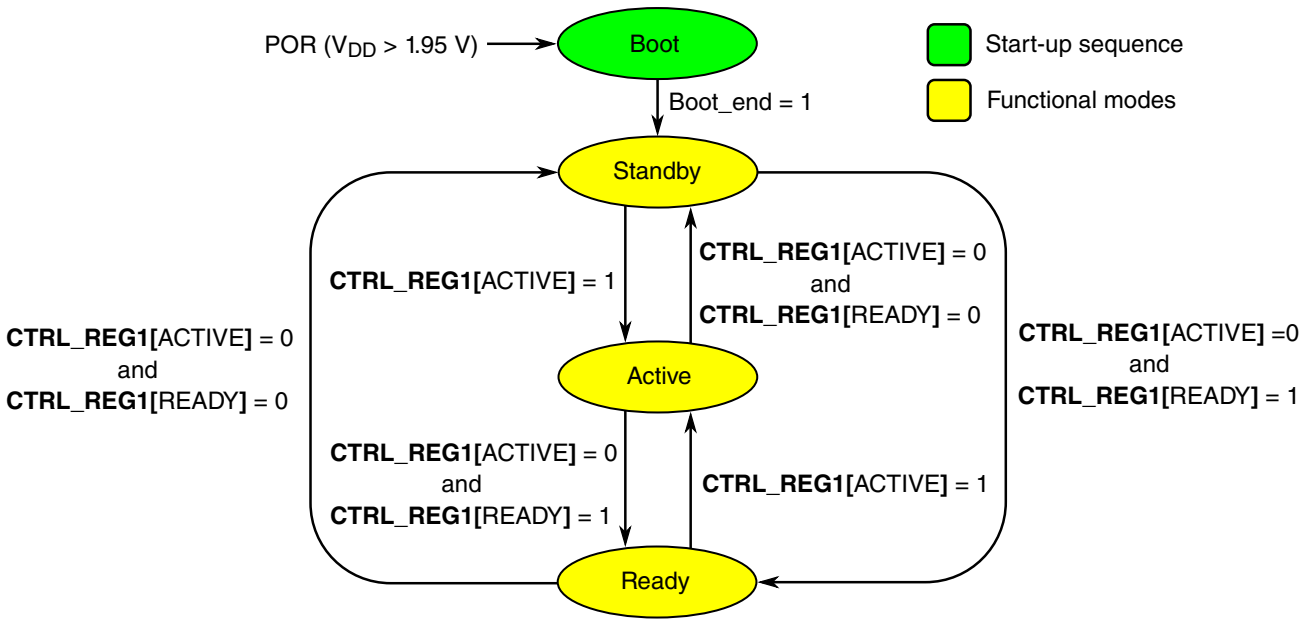


Figure 18. Functional mode transition diagram with CTRL_REG3[EXTCTRLEN] = 0

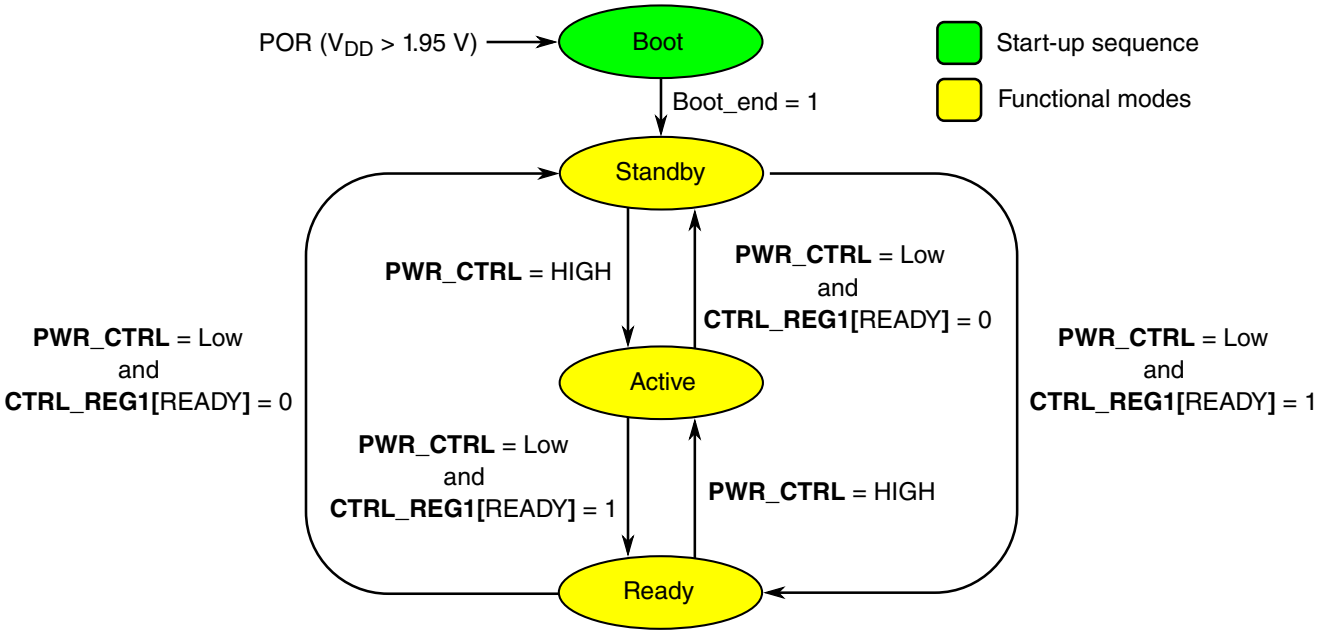


Figure 19. Functional mode transition diagram with CTRL_REG3[EXTCTRLEN] = 1

5 Functionality

The FXAS21002C is a low-power, digital-output, 3-axis gyroscope with both I^2C and SPI interfaces. The functionality includes the following:

- 16-bit output data presented in 2's complement format
- Configurable full scale ranges of ±250, ±500, ±1000 and ±2000 dps; optional FSRs of ±500, ±1000, ±2000 and ±4000 by setting **CTRL_REG3**[FS_DOUBLE] = 1
- Configurable output data rates from 12.5 to 800 Hz
- Internal low-pass filter with programmable cut-off frequency to limit the output data bandwidth
- Angular rate sensitivity of 0.0625°/s in ±2000°/s FSR mode
- Internal high-pass filter with programmable cut-off frequency
- Embedded rate threshold detection function with programmable debounce time
- 32-sample FIFO configurable in Circular or Stop data collection modes
- 2 external interrupt pins that are configurable to signal data-ready, Rate Threshold or FIFO events
- Self-test function for indication of device health

Data for each axis must be read from the respective data registers, two bytes at a time; for example, one byte for most significant byte and one byte for least significant. Combining these two bytes results in a 16-bit 2's complement signed integer with the sign bit in bit location #15 and the least significant bit in location 0. See the tables below:

Bit	**15**	14	13	12	11	10	9	8
Data bit	**D15**	D14	D13	D12	D11	D10	D9	D8
	Sign bit							

Bit	7	6	5	4	3	2	1	**0**
Data bit	D7	D6	D3	D4	D3	D2	D1	**D0**
								LSB

The conversion from counts to units of dps is done by first adjusting the byte order of the output data (if needed). On a big-endian processor, no byte order changes are needed. On a little-endian processor, the byte order (MSB, LSB) must be swapped. Following this step, the 16-bit value is multiplied by the appropriate sensitivity value for the selected full scale range. See Table 35 for nominal sensitivity values.

5.1 FIFO Data Buffer

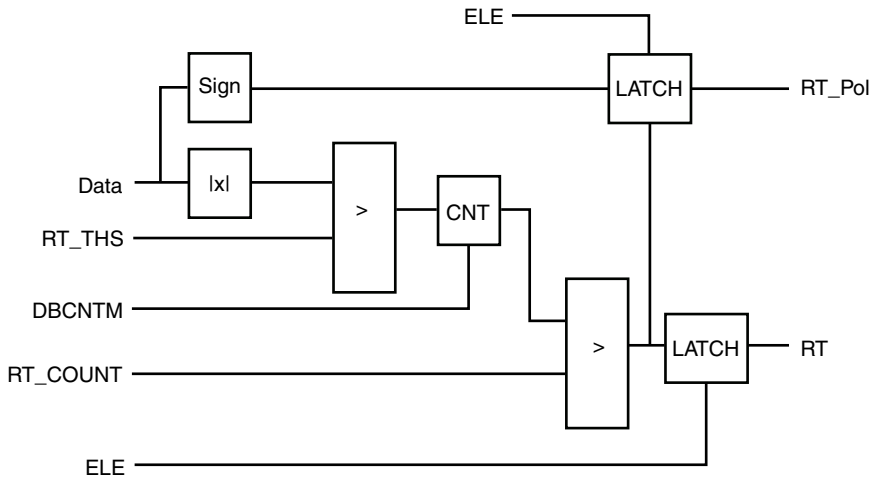
FXAS21002C contains a FIFO data buffer that is 192 bytes (32 X/Y/Z samples) and is useful for reducing the frequency of transactions on the I^2C/SPI bus. The FIFO can also provide system level power savings by allowing the host processor/MCU to go into a sleep/low-power mode while the FXAS21002C collects up to 32 samples of 3-axis angular rate data.

The FIFO is configured to operate in Circular Buffer mode or Stop mode, depending on the settings made in the 0x09: F_SETUP register. The Circular Buffer mode allows the FIFO to be filled with a new sample, replacing the oldest sample in the buffer. The most recent 32 samples will be stored in the buffer. This is useful in situations where the processor is waiting for a specific interrupt to indicate that the data must be flushed to analyze the event.

The FXAS21002C FIFO Buffer has a configurable watermark, allowing an interrupt to be signaled to the processor after a configurable number of samples enter the buffer (1 to 32).

5.2 Rate Threshold Detection Function

The embedded rate detection function can be used to detect an angular rate event that exceeds a programmed threshold on any one of the enabled axes for longer than the programmed debounce time, triggering an interrupt on one of the INT1/INT2 pins (if enabled).



Output data rate (Hz)	ODR and counter clock period (ms)	Event debounce time range (s)
800	1.25	0 – 0.32
400	2.5	0 – 0.64
200	5	0 – 1.28
100	10	0 – 2.56
50	20	0 – 5.12
25	40	0 – 10.24
12.5	80	0 – 20.48

If the debounce counter reaches the value stored in **RT_COUNT**, the rate threshold event is detected. The interrupt flag can be either latched or updated in real-time depending on the state of the **ELE** bit. The examples illustrated in Figure 20 through Figure 23 show the use of the rate threshold function with the various settings for the **DBCNTM** and **ELE** control bits:

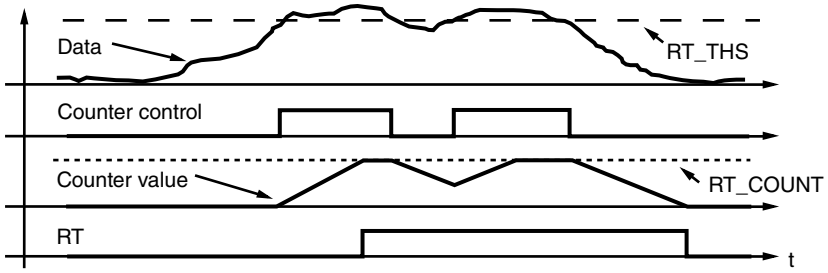


Figure 20. ELE = 0 and DBCNTM = 0

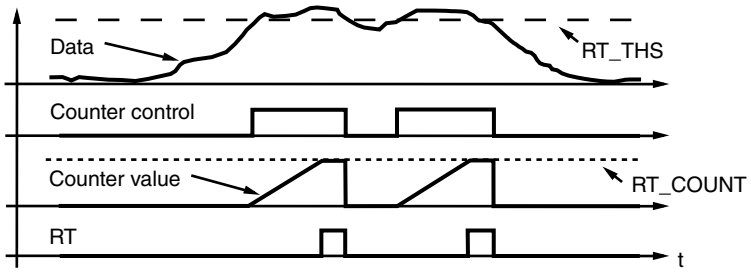


Figure 21. ELE = 0 and DBCNTM = 1

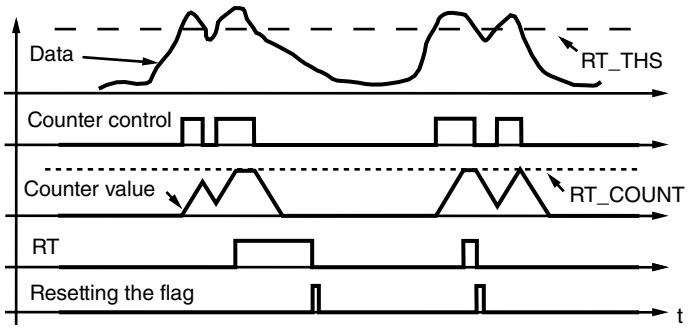


Figure 22. ELE = 1 and DBCNTM = 0

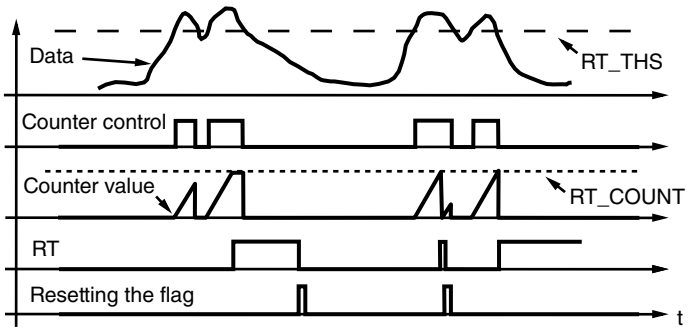


Figure 23. ELE = 1 and DBCNTM = 1

6 Register Descriptions

Table 13. Register address map

Name	Type	Register address	Auto-increment address	Default value	Comment
STATUS	R	0x00	0x01	0x00	Alias for DR_STATUS or F_STATUS
OUT_X_MSB	R	0x01	0x02	0x00[1]	[7:0] are 8 MSBs of 16 bit X-axis data sample
OUT_X_LSB	R	0x02	0x03	0x00[1]	[7:0] are 8 MSBs of 16 bit X-axis data sample
OUT_Y _MSB	R	0x03	0x04	0x00[1]	[7:0] are 8 MSBs of 16 bit Y-axis data sample
OUT_Y_LSB	R	0x04	0x05	0x00[1]	[7:0] are 8 MSBs of 16 bit Y-axis data sample
OUT_Z_MSB	R	0x05	0x06	0x00[1]	[7:0] are 8 MSBs of 16 bit Z-axis data sample
OUT_Z_LSB	R	0x06	0x00/0x01	0x00[1]	[7:0] are 8 MSBs of 16 bit Z-axis data sample; Auto-increment address depends on the setting made in CTRL_REG3[WRAPTOONE] (defaults to 0x00)
DR_STATUS	R	0x07	0x08	0x00	Data-ready status information
F_STATUS	R	0x08	0x09	0x00	FIFO Status
F_SETUP	R/W	0x09	0x0A	0x00	FIFO setup
F_EVENT	R	0x0A	0x0B	0x00	FIFO event
INT_SRC_FLAG	R	0x0B	0x0C	0x00	Interrupt event source status flags
WHO_AM_I	R	0x0C	0x0D	0xD7	Device ID
CTRL_REG0	R/W	0x0D	0x0E	0x00	Control register 0: Full-scale range selection, high-pass filter setting, SPI mode selection
RT_CFG	R/W	0x0E	0x0F	0x00	Rate threshold function configuration
RT_SRC	R	0x0F	0x10	0x00	Rate threshold event flags status register
RT_THS	R/W	0x10	0x11	0x00	Rate threshold function threshold register
RT_COUNT	R/W	0x11	0x12	0x01	Rate threshold function debounce counter
TEMP	R	0x12	0x13	0x00	Device temperature in °C
CTRL_REG1	R/W	0x13	0x14	0x00	Control register 1: Operating mode, ODR selection, self-test and soft reset
CTRL_REG2	R/W	0x14	0x15	0x00	Control register 2: Interrupt configuration settings
CTRL_REG3	R/W	0x15	0x00	0x00	Control Register 3: Auto-increment address configuration, external power control, FSR expansion
RESERVED	—	0x16 – 0xFF	address + 1	—	Factory reserved register space

1. As shown on POR. On hard/soft reset, the default value cannot be determined.

6.1 0x00: STATUS

The STATUS register content depends on the FIFO mode setting. It is a copy of either 0x07: DR_STATUS or 0x08: F_STATUS. This allows for easy reading of the relevant status register before reading the current sample output data, or the first sample stored in the FIFO.

6.2 0x01–0x06: OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, OUT_Z_LSB

The X-axis, Y-axis, and Z-axis output rate data are represented in 16-bit, 2's complement format. The output data registers are arranged in a contiguous big endian format, with the MSB of each axis's data located at the lower register address. The output data registers are either updated at the selected output data rate (with **F_SETUP[**F_MODE**]** equal to 0b00), or alternately, point to the head of the FIFO buffer (with **F_SETUP[**F_MODE**]** greater than 0b00). When reading a data sample with **F_MODE** equal to 0b00, the host must always start by reading the MSB of each axis first to ensure that the corresponding LSB register is also updated with the current sample data. When F_MODE is greater than 0b00, the OUT_X_MSB register must be read out first in order for the other five output data registers (OUT_X_LSB through OUT_Z_LSB) to be updated with sample data stored at the head of the FIFO. The FIFO head pointer is only incremented to point to the next stored sample when the host reads the OUT_Z_MSB register.

NOTE

To avoid the loss of data, the user must burst-read all six bytes of sample data (three axes) in a single I^2C or SPI transaction.

Table 14. 0x01: OUT_X_MSB

Bit	7	6	5	4	3	2	1	0
Read	XD[15:8]							
Write								
Reset[1]	0	0	0	0	0	0	0	0

1. As shown on POR. On hard/soft reset, the default value cannot be determined.

Table 15. 0x02: OUT_X_LSB

Bit	7	6	5	4	3	2	1	0
Read	XD[7:0]							
Write								
Reset[1]	0	0	0	0	0	0	0	

1. As shown on POR. On hard/soft reset, the default value cannot be determined.

Table 16. 0x03: OUT_Y_MSB

Bit	7	6	5	4	3	2	1	0
Read	YD[15:8]							
Write								
Reset[1]	0	0	0	0	0	0	0	0

1. As shown on POR. On hard/soft reset, the default value cannot be determined.

Table 17. 0x04: OUT_Y_LSB

Bit	7	6	5	4	3	2	1	0
Read	YD[7:0]							
Write								
Reset[1]	0	0	0	0	0	0	0	0

1. As shown on POR. On hard/soft reset, the default value cannot be determined.

Table 18. 0x05: OUT_Z_MSB

Bit	7	6	5	4	3	2	1	0
Read	ZD[15:8]							
Write								
Reset[1]	0	0	0	0	0	0	0	0

1. As shown on POR. On hard/soft reset, the default value cannot be determined.

Table 19. 0x06: OUT_Z_LSB

Bit	7	6	5	4	3	2	1	0
Read	ZD[7:0]							
Write								
Reset[1]	0	0	0	0	0	0	0	0

1. As shown on POR. On hard/soft reset, the default value cannot be determined.

NOTE

After this register is read, the next read register by the auto-increment process is STATUS at 0x00, when CTRL_REG3[WRAPTOONE] = 0, or OUT_X_MSB when CTRL_REG3[WRAPTOONE] = 1.

Data output LSB registers only contain valid data after a read of the corresponding axis MSB data register. When **F_SETUP**[F_MODE] > 0b00, a data read operation must start by reading the OUT_X_MSB register in order for the contents of the other output data registers to be updated for the currently indexed buffered sample. With **F_SETUP**[F_MODE] > 0b00, the OUT_Z_MSB register must be read in order to advance the internal buffer read pointer to index the next sample stored in the FIFO.

6.3 0x07: DR_STATUS

The DR_STATUS register provides the sample data acquisition status and reflects the real-time updates to the OUT_X, OUT_Y, and OUT_Z registers. The content of this register is reset upon a transition from Standby to Active or from Ready to Active modes.

Table 20. DR_STATUS register

Bit	7	6	5	4	3	2	1	0
Read	ZYXOW	ZOW	YOW	XOW	ZYXDR	ZDR	YDR	XDR
Write								
Reset	0	0	0	0	0	0	0	0

Table 21. DR_STATUS field descriptions

Field	Description
7 ZYXOW	X-, Y-, Z-axis data overwrite • Asserted whenever new X-, Y-, and Z-axis data is acquired before completing the retrieval of the previous set. • Cleared after the high-bytes of the data of all channels (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) are read. 0: No data overwrite has occurred 1: X, Y, and Z data overwrite occurred before the previous data was read

Table continues on the next page...

Table 21. DR_STATUS field descriptions (continued)

Field	Description
6 ZOW	Z-axis data overwrite • Asserted whenever a new Z-axis acquisition is completed before the retrieval of the previous data. When this occurs, the previous data is overwritten. • Cleared anytime the OUT_Z_MSB (and respectively OUT_Y_MSB, OUT_X_MSB) register is read. 0: No data overwrite has occurred 1: Z-axis data overwrite occurred before the previous data was read
5 YOW	Y-axis data overwrite • Asserted whenever a new Y-axis acquisition is completed before the retrieval of the previous data. When this occurs, the previous data is overwritten. • Cleared anytime the OUT_Z_MSB (and respectively OUT_Y_MSB, OUT_X_MSB) register is read. 0: No data overwrite has occurred 1: Y-axis data overwrite occurred before the previous data was read
4 XOW	X-axis data overwrite • Asserted whenever a new X-axis acquisition is completed before the retrieval of the previous data. When this occurs, the previous data is overwritten. • Cleared anytime the OUT_Z_MSB (and respectively OUT_Y_MSB, OUT_X_MSB) register is read. 0: No data overwrite has occurred 1: X-axis data overwrite occurred before the previous data was read
3 ZYXDR	X-, Y-, and Z-axis data available • Signals that a new acquisition for any of the channels is available. • Cleared when the high-bytes of the data of all channels (OUT_X_MSB, OUT_Y_MSB, OUT_Z_MSB) are read. 0: No new data is ready 1: New data is ready
2 ZDR	Z-axis new data available • Asserted whenever a new Z-axis data acquisition is completed. • Cleared anytime the OUT_Z_MSB register is read. 0: No new Z-axis data is ready 1: New Z-axis data is ready
1 YDR	Y-axis new data available • Asserted whenever a new Y-axis data acquisition is completed. • Cleared anytime the OUT_Y_MSB register is read. 0: No new Y-axis data is ready 1: New Y-axis data is ready
0 XDR	X-axis new data available • Asserted whenever a new X-axis data acquisition is completed. • Cleared anytime the OUT_X_MSB register is read. 0: No new X-axis data is ready 1: New X-axis data is ready

6.4 0x08: F_STATUS

When the FIFO is enabled, the F_STATUS register indicates the current status of the FIFO. Also, the STATUS register (address 0x00) contains the same content as F_STATUS to facilitate the emptying of the FIFO by the host processor. The content of this register is reset upon a transition from Standby to Active or from Ready to Active modes.

Table 22. F_STATUS register

Bit	7	6	5	4	3	2	1	0
Read	F_OVF	F_WMKF	F_CNT[5:0]					
Write								
Reset	0	0	0	0	0	0	0	0

Table 23. F_Status field descriptions

Field	Description
7 F_OVF	FIFO overflow flag • A FIFO overflow event, such as when F_CNT = 32 and a new sample arrives, asserts the F_OVF flag. • Cleared when the FIFO sample count goes below 32. 0: No overflow detected 1: Overflow detected
6 F_WMKF	FIFO watermark flag • A FIFO sample count greater than or equal to the sample count watermark (determined by the F_WMRK field in register 0x09: F_SETUP) asserts the F_WMKF event flag. • Cleared when FIFO sample count goes below the sample count watermark (set by the value of F_SETUP[F_WMRK] field). 0: No watermark event detected 1: Watermark event detected
5:0 F_CNT	FIFO sample counter • Indicates the number of samples currently stored in the FIFO. • A count value of 0b000000 indicates that the FIFO is empty.

6.5 0x09: F_SETUP

The F_SETUP register is used to configure the FIFO. The FIFO update rate is set by the selected system ODR (DR bits in 0x13: CTRL_REG1). The contents should be modified only when the device is in Standby mode.

Table 24. F_Setup register

Bit	7	6	5	4	3	2	1	0
Read	F_MODE[1:0]		F_WMRK[5:0]					
Write								
Reset	0	0	0	0	0	0	0	0

Table 25. F_SETUP field descriptions

Field	Description
7:6 F_MODE	FIFO operating mode selection: 00: FIFO is disabled 01: Circular Buffer mode 1x: Stop mode Note: • Used to select the FIFO operating mode. • In the Circular Buffer mode, the oldest sample is discarded and replaced by the newest sample when the buffer is full with **F_STATUS[**F_CNT**]** = 32. • In the Stop mode, the FIFO will stop accepting new samples when the buffer is full with **F_STATUS[**F_CNT**]** = 32. • The FIFO operating mode cannot be switched between Circular and Stop modes while the FIFO is enabled. • To change the FIFO operating mode, the FIFO function must first be disabled by setting F_MODE[1:0] = 00. • The FIFO is cleared whenever the FIFO is disabled.
5:0 F_WMRK	FIFO sample count watermark setting • Used to set the watermark level. • To suppress FIFO watermark event flag generation, F_WMRK[5:0] can be set to 0x00. • Disabling the FIFO clears F_WMKF • A FIFO sample count exceeding the watermark level does not stop the FIFO from accepting new data. Default value is 0b000000.

6.6 0x0A: F_EVENT

The F_EVENT register is used to monitor the FIFO event status. The content of this register is reset upon a transition from Standby to Active or from Ready to Active modes.

Table 26. F_Event register

Bit	7	6	5	4	3	2	1	0
Read	0	0	F_EVENT	FE_TIME[4:0]				
Write								
Reset	0	0	0	0	0	0	0	0

Table 27. F_EVENT field descriptions

Field	Description
5 F_EVENT	FIFO Event • Indicates if either F_OVF or F_WMKF flags are set (logical OR). • The F_STATUS register must be read to determine which event(s) occurred. • To clear this flag, both F_OVF and F_WMKF flags must be cleared. See F_STATUS for details. 0: FIFO Event not detected 1: FIFO Event was detected
4:0 FE_TIME	Number of ODR periods elapsed since F_EVENT was set • Indicates the number of samples acquired since a FIFO event flag (overflow or watermark) was asserted. • Reset when F_OVF and F_WMKF fall. • To clear this field, the F_EVENT flag must be cleared.

6.7 0x0B: INT_SOURCE_FLAG

The INT_SOURCE_FLAG register provides the event-flag status for the interrupt generating functions within the device. Reading the INT_SRC_FLAG register does not reset any event-flag source bits; they are reset by reading the appropriate event source register.

Table 28. INT_SRC register

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	BOOTEND	SRC_FIFO	SRC_RT	SRC_DRDY
Write								
Reset	0	0	0	0	0	0	0	0

Table 29. INT_SRC_FLAG field descriptions

Field	Description
3 BOOTEND	Boot sequence complete event flag • Asserted as soon as the device boot sequence has completed and remains at '1' thereafter. 1: Boot sequence is complete 0: When one of the following occurs: • A hard or soft reset event is triggered • A POR event occurs

Table continues on the next page...

Table 29. INT_SRC_FLAG field descriptions (continued)

Field	Description
2 SRC_FIFO	FIFO event source flag • Indicates that the FIFO event flags triggered the interrupt 1: When the FIFO event flag **F_Event[**F_Event**]** is set (F_OVF or F_WMKF are set), provided the FIFO interrupt is enabled (**CTRL_REG2[**INT_EN_FIFO**]** = 1). 0: Cleared when F_Event flag gets cleared (whenever both F_OVF and F_WMKF get cleared).
1 SRC_RT	Rate threshold event source flag • Indicates that the rate threshold event flag(s) triggered the interrupt 1: When the event active flag **RT_SRC[**EA**]** is set, provided the Rate Threshold interrupt is enabled (**CTRL_REG2[**INT_EN_RT**]** = 1). 0: Cleared when the event active flag **RT_SRC[**EA**]** is cleared.
0 SRC_DRDY	Data-ready event source flag • Indicates that a data-ready event triggers the interrupt 1: When any of the data-ready flags from **DR_STATUS** are set, provided the Data Ready interrupt is enabled (**CTRL_REG2[**INT_EN_DRDY**]** = 1). 0: Cleared by reading the MSBs of the X, Y, and Z axes sample data.

6.8 0x0C: WHO_AM_I

The WHO_AM_I register contains the device identifier which is factory programmed to 0xD7.

Table 30. WHO_AM_I

Bit	7	6	5	4	3	2	1	0
Read	WHO_AM_I[7:0]							
Write								
Reset	1	1	0	1	0	1	1	1

6.9 0x0D: CTRL_REG0

CTRL_REG0 is used for general control and configuration of the device. The bit fields in CTRL_REG0 should be changed only in Standby or Ready modes. Accuracy of the output data is not guaranteed if these bits are changed when the device is in Active mode.

Table 31. CTRL_REG0

Bit	7	6	5	4	3	2	1	0
Read Write	BW[1:0]		SPIW	SEL[1:0]		HPF_EN	FS[1:0]	
Reset	0	0	0	0	0	0	0	0

Table 32. CTRL_REG0 field descriptions

Field	Description
7:6 BW	Bandwidth • Selects the cut-off frequency of the digital low-pass filter, limiting the bandwidth of the digital output data as shown in Table 33.
5 SPIW	SPI interface mode selection 0: SPI 4-wire mode (default) 1: SPI 3-wire mode (MOSI pin is used for SPI input and output signals)
4:3 SEL	High-pass filter cutoff frequency selection • Details of the high-pass filter settings are shown in Table 34.
2 HPF_EN	High-pass filter enable • The high-pass filter is initialized on operating mode and ODR change. • When enabled, the HPF is applied to the angular rate data supplied to the output registers/FIFO and the embedded rate threshold function. 0: High-pass filter disabled (default) 1: High-pass filter enabled
1:0 FS	Full-scale range selection • See Table 35

Table 33. FXAS21002C LPF cutoff frequency

BW	ODR = 800 Hz	ODR = 400 Hz	ODR = 200 Hz	ODR = 100 Hz	ODR = 50 Hz	ODR = 25 Hz	ODR = 12.5 Hz
0b00	256	128	64	32	16	8	4
0b01	128	64	32	16	8	4	—
0b1x	64	32	16	8	4	—	—

Table 34. High-pass filter cutoff frequency selection

SEL1	SEL0	Cutoff Frequency in Hz versus ODR						
		800 Hz	400 Hz	200 Hz	100 Hz	50 Hz	25 Hz	12.5 Hz
0	0	15	7.5	3.75	1.875	0.937	0.468	0.234
0	1	7.7	3.85	1.925	0.963	0.481	0.241	0.120
1	0	3.9	1.95	0.975	0.488	0.244	0.122	0.061
1	1	1.98	0.99	0.495	0.248	0.124	0.062	0.031

HPF_EN enables the high pass filter. Note that high-pass filter is initialized on mode change, ODR change, and assertion of the zero rate register bit. When enabled, the high-pass filtered data is input to both the output data registers/FIFO and the rate threshold function.

FS[1:0] selects the full scale range of the device as shown in Table 35.

Table 35. Selectable Full Scale Ranges

FS1	FS0	Range (dps)	Nominal Sensitivity (mdps/LSB)
0	0	±2000	62.5
0	1	±1000	31.25
1	0	±500	15.625
1	1	±250	7.8125

NOTE

Setting the **CTRL_REG3**[FS_DOUBLE] increases the dynamic range for each **CTRL_REG0**[FS] selection by a factor of two, from ±250/500/1000/2000°/s to ±500/1000/2000/4000°/s.

6.10 0x0E: RT_CFG

The RT_CFG register is used to enable the Rate Threshold interrupt generation. The internal state of the Rate Threshold function is reset when a transition from Standby to Active or Ready to Active modes occurs. The contents should only be modified when the device is in Standby mode.

Table 36. RT_ CFG Register

Bit	7	6	5	4	3	2	1	0
Read	0	0	0	0	ELE	ZTEFE	YTEFE	XTEFE
Write								
Reset	0	0	0	0	0	0	0	0

Table 37. RT_CFG field descriptions

Field	Description
3 ELE	Event latch enable • See Functionality for more details. 0: Event flag latch disabled 1: Event flag latch enabled
2 ZTEFE	Event flag enable on Z-axis rate • Enable bits for rate threshold event detection on the Z axis 0: Z event detection disabled 1: Z Event detection enabled
1 YTEFE	Event flag enable on Y-axis rate • Enable bits for rate threshold event detection on the Y axis 0: Y event detection disabled 1: Y Event detection enabled
0 XTEFE	Event flag enable on X-axis rate • Enable bits for rate threshold event detection on the X axis 0: X event detection disabled 1: X Event detection enabled

6.11 0x0F: RT_SRC

This register indicates the source of the Rate Threshold event. The content of RT_SRC is reset upon a transition from Standby to Active or from Ready to Active modes.

Table 38. RT_ SRC Register

Bit	7	6	5	4	3	2	1	0
Read	0	EA	ZRT	Z_RT_POL	YRT	Y_RT_POL	XRT	X_RT_POL
Write								
Reset	0	0	0	0	0	0	0	0

Table 39. RT_SRC field descriptions

Field	Description
6 EA	Event active flag • EA indicates that a rate threshold event has been detected on at least one of the axes (OR condition). This bit is cleared after a read of this register only if it has been latched (ELE =1). 0: No event flags have been asserted 1: One or more event flags have been asserted (XRT, YRT or ZRT)
5 ZRT	Z rate event • Indicates that a rate threshold event (as defined in Functionality) has been detected on the Z-axis (only if RT_CFG[ZTEFE] is 1). • Flag is asserted a few samples (RT_COUNT) after the absolute value of the Z output rate data goes above the RT_THS value. • Cleared a few samples (RT_COUNT) after the absolute value of Z rate output goes below the RT_THS value. Also cleared when the register is read, if it has been latched (ELE = 1). 0: No rate threshold event detected on Z axis 1: Rate Threshold event detected on Z axis
4 Z_RT_POL	Polarity of Z event • Indicates the rate polarity on the Z-axis (if **RT_CFG[**ZTEFE**]** =1). If **RT_CFG[**ZTEFE**]** =1, this bit indicates the polarity of the Z data irrespective of the rate threshold event detected on Z-axis. • Cleared when read if it has been latched (ELE =1) 0: Z rate event was Positive 1: Z rate event was Negative
3 YRT	Y rate event • Indicates that a rate threshold event (as defined in Functionality) has been detected on the Y-axis (only if **RT_CFG[**YTEFE**]** =1). • Flag is asserted few samples(RT_COUNT) after the absolute value of the Y output rate data goes above the RT_THS value. • Cleared a few samples (RT_COUNT) after the absolute value of Y rate output goes below the RT_THS value. Also cleared when the register is read if it has been latched (ELE = 1). 0: No Rate Threshold event detected on Y axis 1: Rate Threshold event detected on Y axis
2 Y_RT_POL	Polarity of Y event • Indicates the rate polarity on the Y-axis (if **RT_CFG[**YTEFE**]** =1). If **RT_CFG[**YTEFE**]** =1, this bit indicates the polarity of the Y data irrespective of the rate threshold event detected on Y-axis. • Cleared when read if it has been latched (ELE =1) 0: Y rate event was Positive 1: Y rate event was Negative

Table continues on the next page...

Table 39. RT_SRC field descriptions (continued)

Field	Description
1 XRT	X rate Event • Indicates that a rate threshold event (as defined in Functionality) has been detected on the X-axis (only if RT_CFG[XTEFE] =1). • Flag is asserted few samples (RT_COUNT) after the absolute value of the X output rate data goes above the RT_THS value. • Cleared a few samples (RT_COUNT) after the absolute value of X rate output goes below the RT_THS value. Also cleared when the register is read if it has been latched (ELE = 1). 0: No Rate Threshold event detected on X axis 1: Rate Threshold event detected on X axis.
0 X_RT_POL	Polarity of X event • Indicates the rate polarity on the X axis (if **RT_CFG[**XTEFE**]** =1). If **RT_CFG[**XTEFE**]** =1, this bit indicates the polarity of the X-data irrespective of the rate threshold event detected on X-axis. • Cleared when read if it has been latched (ELE =1) 0: X rate event was positive 1: X rate event was negative

6.12 0x10: RT_THS

The RT_THS register sets the threshold limit for the detection of the rate and the debounce counter mode. See Functionality for more details.

Table 40. RT_THS register

Bit	7	6	5	4	3	2	1	0
Read	DBCNTM	THS[6:0]						
Write								
Reset	0	0	0	0	0	0	0	0

Table 41. RT_THS field descriptions

Field	Description
7 DBCNTM	Debounce counter mode selection • The contents should only be modified when the device is in Standby mode 1: Clear counter when angular rate is below the threshold value 0: Decrement counter on every ODR cycle that the angular rate is below the threshold value

Table continues on the next page...

Table 41. RT_THS field descriptions (continued)

Field	Description
6:0 THS	Unsigned 7-bit rate threshold value • The contents should only be modified when the device is in Standby mode • The internal state of the Rate Threshold function is reset when a transition from Standby to Active or Ready to Active modes occurs. • The rate threshold in dps is given by the following formula: *Rate Threshold (dps) = (THS+1) * 256 * Sensitivity (dps/LSB)* *Rate Threshold (LSB) = (THS+1) * 256*

NOTE

The sensitivity (dps/LSB) varies with the FSR setting: **CTRL_REG0**[FS] and also with the FS_DOUBLE setting: **CTRL_REG3**[FS_DOUBLE]. See Table 54 for more sensitivity details on enabling FS_DOUBLE.

6.13 0x11: RT_COUNT

RT_COUNT sets the number of debounce counts. See Functionality for more details.

Table 42. RT_COUNT register

Bit	7	6	5	4	3	2	1	0
Read Write	RT_CNT[7:0]							
Reset	0	0	0	0	0	0	0	1

Table 43. RT_COUNT field descriptions

Field	Description
7:0 RT_CNT	Debounce counter value • The contents should only be modified when the device is in Standby mode • The internal state of the Rate Threshold function debounce counter is reset when a transition from Standby to Active or Ready to Active modes occurs • Stores the number of counts with the angular rate above the threshold needed before asserting the rate threshold event flag • The counter period is the same as the selected ODR period, allowing for a debounce time to be calculated. For example, an RT_COUNT value of 10 (decimal) and an ODR of 100 Hz would result in a debounce time of 100 ms.

6.14 0x12: TEMP

The TEMP register contains an 8-bit 2's complement temperature value with a range of –128 °C to +127 °C and a scaling of 1 °C/LSB. The temperature data is only compensated (factory trim values applied) when the device is operating in the Active mode and actively measuring the angular rate.

Table 44. TEMP register

Bit	7	6	5	4	3	2	1	0
Read	TEMP[7:0]							
Write								
Reset	0	0	0	0	0	0	0	0

6.15 0x13: CTRL_REG1

The CTRL_REG1 register is used to configure the device ODR, set the operating mode, soft-reset the device, and exercise the Self-Test function.

NOTE

Control bits in CTRL_REG1 should be changed only in Standby or Ready mode. Accuracy of the output data is not guaranteed if these bits are changed while the device is in Active mode.

Table 45. CTRL_REG1 register

Bit	7	6	5	4	3	2	1	0
Read	—	RST	ST	DR[2:0]			ACTIVE	READY
Write								
Reset	0	0	0	0	0	0	0	0

Table 46. CTRL_REG1 field descriptions

Field	Description
6 RST	Software Reset: • Used to trigger a reset of the device. • On reset, all registers except 0x01 through 0x06 revert to their default values. Register addresses 0x01 through 0x06 contain values that cannot be determined. • This bit is self cleared after assertion. 0: Device reset not triggered/completed 1: Device reset triggered

Table continues on the next page...

Table 46. CTRL_REG1 field descriptions (continued)

Field	Description
5 ST	Self-Test enable • When ST is set, a data output change will occur even if no angular rate is applied. This allows the host application to check the functionality of the sensor and the entire measurement signal chain. The expected Self-Test delta value is summarized in Table 4 0: Self-Test disabled 1: Self-Test enabled
4:2 DR	Output Data Rate selection • Selects the output data rate as per Table 47
1 Active	Standby/Active mode selection, see Table 48
0 Ready	Standby/Ready mode selection, see Table 48

NOTE

On issuing a Software Reset command over an I^2C interface, the device immediately resets and does not send any acknowledgment (ACK) of the written byte to the Master.

Table 47. Digital output data bandwidth settings

Decimal number	CTRL_REG1[DR]	ODR (Hz)
0	000	800
1	001	400
2	010	200
3	011	100
4	100	50
5	101	25
6	110	12.5
7	111	12.5

The **ACTIVE** and **READY** bits are used to control the device operating mode. In Standby mode (**ACTIVE** = 0), the device is only capable of communication on the I^2C or SPI digital interfaces. In Ready mode (**READY** = 1), the device is ready to measure angular rate but no data acquisitions are being made. The Ready mode can be used to reduce the device power consumption and allow for a fast transition into the Active mode when needed. In Active mode (**ACTIVE** = 1), the device is fully functional. The **ACTIVE** bit has a higher priority than the **READY** bit as shown in Table 48.

Table 48. Device operating mode

Active	Ready	Operating mode
0	0	Standby
0	1	Ready
1	X	Active

When **CTRL_REG3**[EXTCTRLEN] = 1, the **ACTIVE** bit is directly controlled by the logic level input to the INT2/PWR_CTRL pin and becomes read-only via the register interface. Thus, the device operating mode can be directly controlled by the INT2/PWR_CTRL pin when **CTRL_REG3**[EXTCTRLEN] =1. The weak pull-up resistor is internal to the IC and automatically enabled when **CTRL_REG3**[EXTCTRLEN] is set to 1, hence setting the Active bit high.

6.16 0x14: CTRL_REG2

This register enables and assigns the output pin(s) and logic polarities for the various interrupt sources available on the device.

Table 49. CTRL_REG2 register

Bit	7	6	5	4	3	2	1	0
Read Write	INT_CFG_FIFO	INT_EN_FIFO	INT_CFG_RT	INT_EN _RT	INT_CFG_DRDY	INT_EN_DRDY	IPOL	PP_OD
Reset	0	0	0	0	0	0	0	0

Table 50. Interrupt Enable register descriptions

Register	Description
7 INT_CFG_FIFO	FIFO interrupt pin routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
6 INT_EN_FIFO	FIFO Interrupt Enable 0: FIFO interrupt disabled 1: FIFO interrupt enabled

Table continues on the next page...

Table 50. Interrupt Enable register descriptions (continued)

Register	Description
5 INT_CFG_RT	Rate threshold interrupt pin routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
4 INT_EN_RT	Rate threshold interrupt enable 0: Rate threshold interrupt disabled 1: Rate threshold interrupt enabled
3 INT_CFG_DRDY	Data-ready interrupt pin routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
2 INT_EN_DRDY	Data ready interrupt enable 0: Data-ready interrupt disabled 1: Data-ready interrupt enabled
1 IPOL	Interrupt logic polarity 0: Active low 1: Active high
0 PP_OD	INT1 and INT2 pin output driver configuration 0: Push-pull output driver 1: Open-drain/open-source buffer with IPOL = 0/1, respectively

Table 51. INT pin behavior as a function of PP_OD and IPOL bit settings

INT pin configuration	PP_OD	IPOL	INT asserted value	INT deasserted value
CMOS output	0	0	0	1
CMOS output	0	1	1	0
External pull-up resistor added	1	0	0	High-z[1]
External pull-down resistor added	1	1	1	High-z[1]

1. High-z = tri-state (high impedance) condition; the state of the INT pin will be defined by the external pull-up or pull-down resistor.

6.17 0x15:CTRL_REG3

This register is used to enable the FSR expansion, external power control input, and options to modify the auto-increment read address pointer behavior when doing burst reads of the FIFO data.

Table 52. CTRL_REG3 register

Bit	7	6	5	4	3	2	1	0
Read	—	—	—	—	WRAPTOONE	EXTCTRLEN	—	FS_DOUBLE
Write								
Reset	—	—	—	—	0	0	—	0

NOTE

Control bits in CTRL_REG3 should only be changed when operating in Standby or Ready mode. Accuracy of the output data is not guaranteed if any of these bits are changed while the device is operating in Active mode.

Table 53. CTRL_REG3 register descriptions

Register	Description
3 WRAPTOONE	Auto-increment read address pointer roll-over behavior: 0: The auto-increment read address pointer rolls over to address 0x00 (STATUS) after the Z-axis LSB is read (default). 1: The auto-increment pointer rolls over to address 0x01 (X-axis MSB) in order to facilitate the faster read out of the FIFO data in a single burst read operation (STATUS register only needs to be read once).
2 EXTCTRLEN	External power mode control input: 0: INT2 pin is used as an interrupt output (default) 1: INT2 pin becomes an input pin that may be used to control the power mode. Note that when EXTCTRLEN is set, the interrupt outputs and related settings for the INT2 pin are ignored. EXTCTRLEN allows the device operating mode to be controlled using the INT2 pin (the pin becomes a high impedance input when this bit is set high). The input is level sensitive, and allows the host to transition the device operating mode from either Standby to Active or from Ready to Active (and vice-versa) depending on the operating mode, Standby or Ready, that was configured at the time this bit was set.
0 FS_DOUBLE	Full-scale range expansion enable: 0: Maximum full-scale range selections are as per Table 37, selected via the **CTRL_REG0[**FS**]** field. 1: Maximum full-scale range selections are doubled from what is shown in Table 37. FS_DOUBLE increases the dynamic range for each **CTRL_REG0[**FS**]** selection by a factor of two, from ±250/500/1000/2000°/s to ±500/1000/2000/4000°/s. This feature is provided to enable a higher dynamic range for applications such as sports equipment monitoring (e.g. golf club or tennis racket swings). While the full-scale range is doubled in this mode, the noise and nonlinearity of the signal are also increased.

Table 54. Rate sensitivity changes with FSR_DOUBLE setting

FSR Selection	Sensitivity (mdps/LSB) FSR_DOUBLE = 0	Sensitivity (mdps/LSB) FSR_DOUBLE = 1
CTRL_REG0[FS] = 00	62.50	125.0
CTRL_REG0[FS] = 01	31.25	62.50
CTRL_REG0[FS] = 10	15.625	31.25
CTRL_REG0[FS] = 11	7.8125	15.625

7 Printed Circuit Board Layout and Device Mounting

Printed Circuit Board (PCB) layout and device mounting are critical to the overall performance of the design. The footprint for the surface mount packages must be the correct size as a base for a proper solder connection between the PCB and the package. This, along with the recommended soldering materials and techniques, will optimize assembly and minimize the stress on the package after board mounting.

Freescale application note AN1902, "Assembly Guidelines for QFN and DFN Packages" discusses the QFN package used by the FXAS21002C.

7.1 Printed Circuit Board Layout

The following recommendations are meant to serve as general guidelines for realizing an effective PCB layout. See Figure 24 for component PCB footprint dimensions.

- The PCB land pattern should be designed with Non-Solder Mask Defined (NSMD) as shown in Figure 24.
- On the layer that the device is soldered, there should be no trace routing or vias underneath the device's component package.
- No components or vias should be placed at a distance less than 2 mm from the package land area. This may cause additional package stress if it is too close to the package land area.
- Signal traces connected to pads should be as symmetric as possible. Put dummy traces on the NC pads in order to have same length of exposed trace for all pads.
- No copper traces should be on the top layer of the PCB under the package, as this will cause planarity issues with the board mount. Freescale QFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide-free molding compound (green) and lead-free terminations. These terminations are

compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

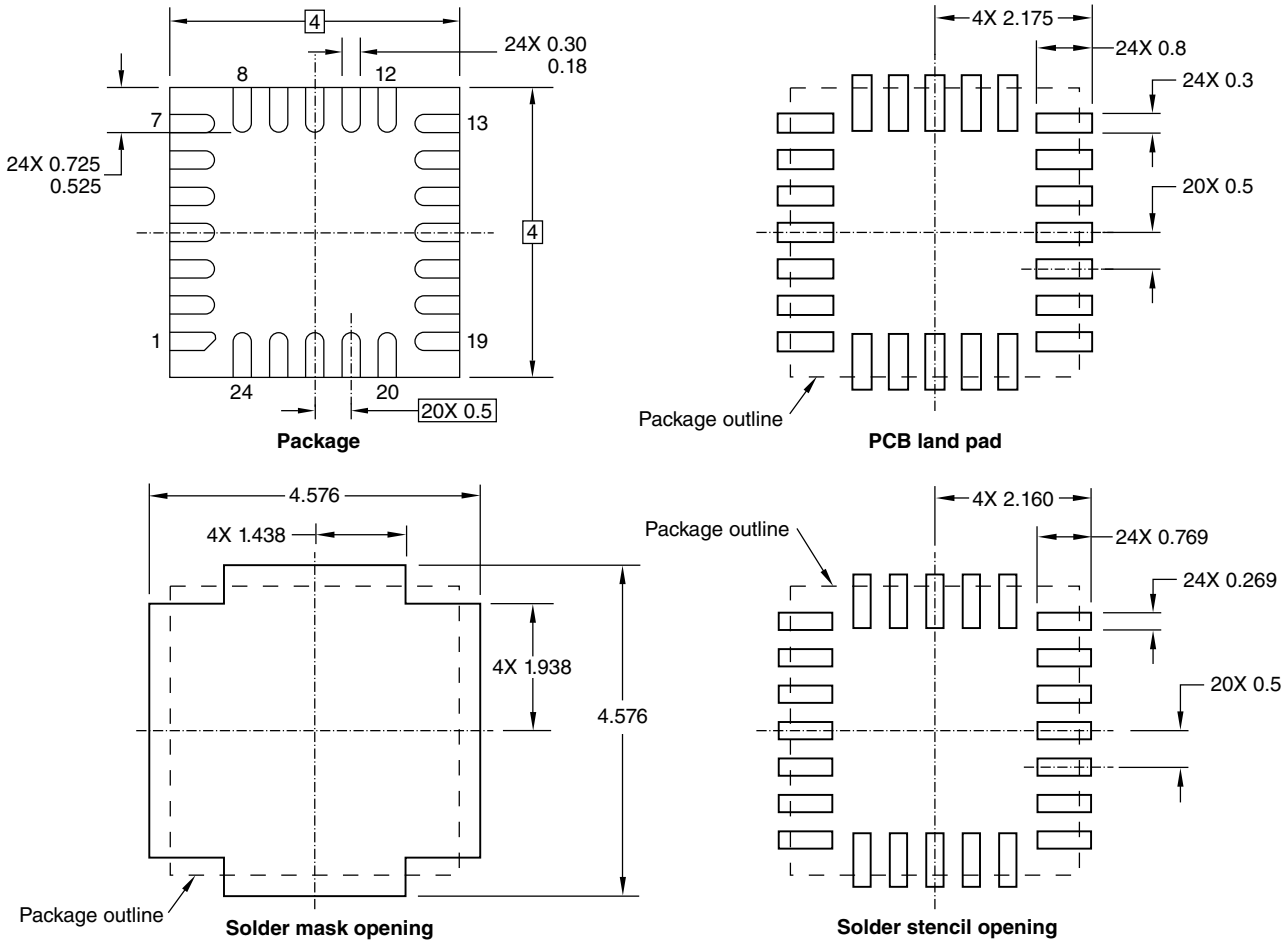


Figure 24. Footprint

7.2 Overview of Soldering Considerations

The information provided here is based on experiments executed on QFN devices. These experiments cannot represent exact conditions present at a customer site. Therefore, information herein should be used for guidance purposes only. Process and design optimizations are recommended to develop an application-specific solution. With the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

- Stencil thickness should be 100 or 125 µm.

- The PCB should be rated for the multiple lead-free reflow condition with a maximum 260 °C temperature.
- Use a standard pick-and-place process and equipment. Do not use a hand soldering process.
- Do not use a screw-down or stacking to mount the PCB into an enclosure. These methods could bend the PCB, which would put stress on the package.

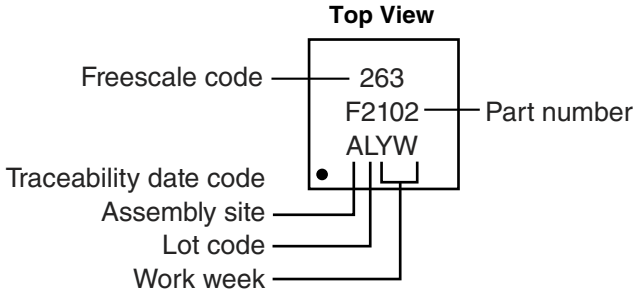
7.3 Halogen Content

This package is designed to be Halogen Free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembled package will contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

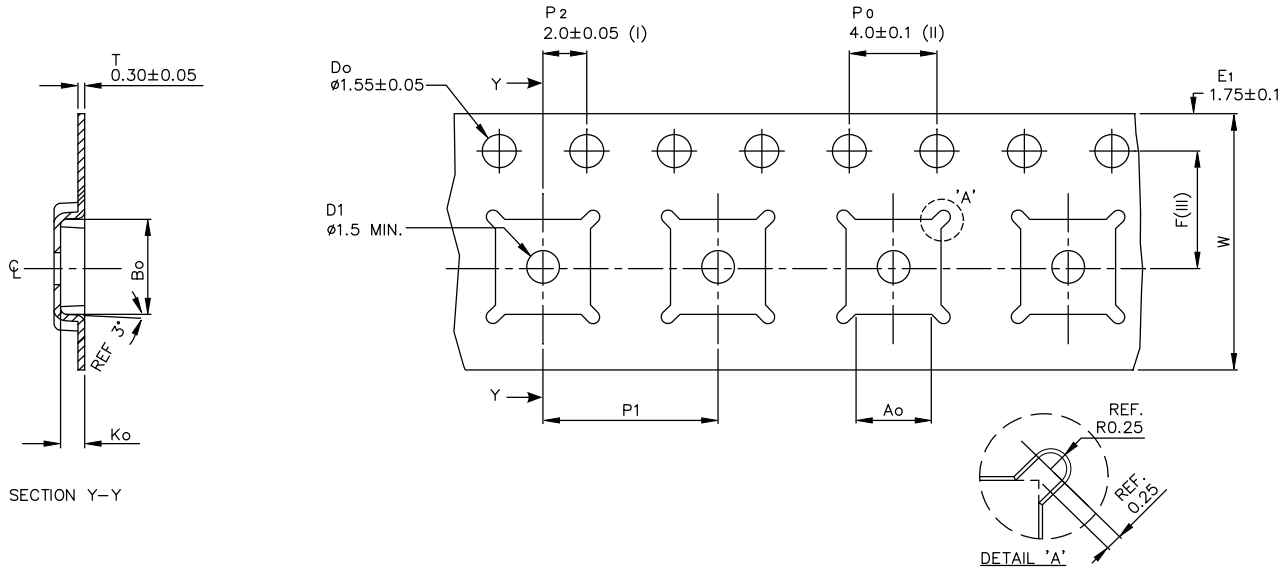
8 Package Information

The FXAS21002C platform uses a 24-lead QFN package, case number 2209-01.

8.1 Product Identification Markings



8.2 Tape and Reel Information



Ao	4.35 +/– 0.1
Bo	4.35 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.05
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centerline of sprocket hole to centerline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centerline of sprocket hole to centerline of pocket.
(IV) Other material available.
(V) Typical SR value Max 10^9 OHM/SQ
ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

Figure 25. Tape dimensions

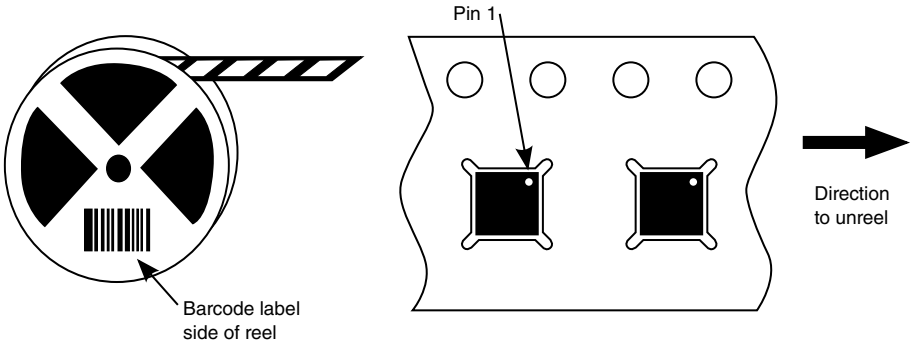
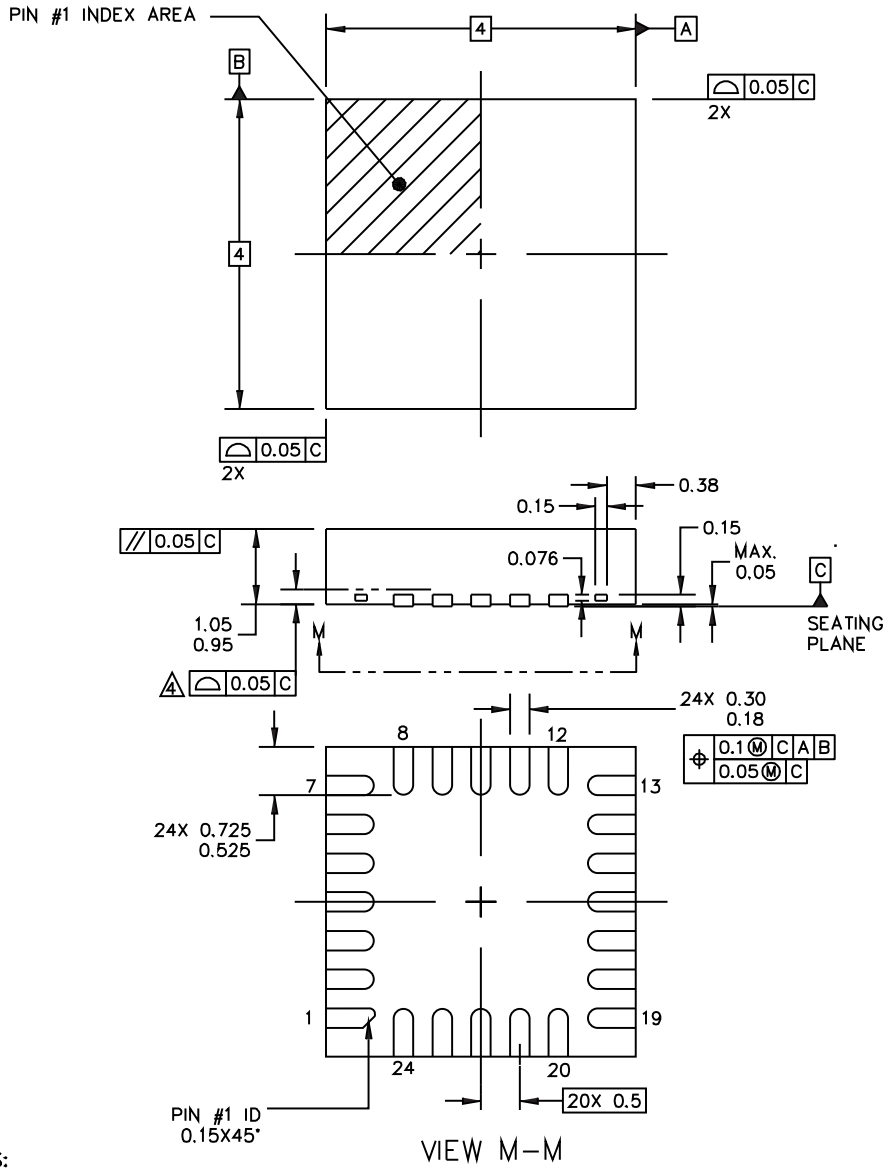


Figure 26. Tape and reel orientation

8.3 Package Description



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

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TITLE: QFN, CHIP ON LEAD (COL), 4 X 4 X 1, 0.5 PITCH, 24 TERMINAL	DOCUMENT NO: 98ASA00356D	REV: O	
	CASE NUMBER: 2209-01	15 DEC 2011	
	STANDARD: NON-JEDEC		

This drawing is located at www.freescale.com/files/shared/doc/package_info/98ASA00356D.pdf.

9 Revision History

Revision number	Revision date	Description
0.3	3/2014	Initial release of document
1.0	8/2014	Added the following sections: • Mechanical and Electrical Specifications • Digital Interfaces • Modes of Operation • Functionality • Register Descriptions • Printed Circuit Board Layout and Device Mounting
1.1	11/2014	• Figure 1, removed BYP • Table 2, removed T = 25°C from Test conditions • Table 6, removed "Sensitivity error due to linear acceleration removed Zero Rate Offset error due to linear acceleration Added footnote to Zero-rate Offset, Post-Board Mount" • Section 5.2, image, added Latch and ELE connection • Section 6.4, removed "Reading F_STATUS clears the SRC_FIFO bit in the 0x0B: INT_SOURCE_FLAG register." • Table 27, F_EVENT field, added bullet: To clear this flag, both F_OVF and F_WMKF flags must be cleared. See F_STATUS for details. • Table 27, F_EVENT field, added bullet: To clear this field, the F_EVENT flag must be cleared. • Table 29, SRC_FIFO field, changed flag descriptions from 1: F_OVF or F_WMKF are set, provided the FIFO interrupt is enabled (**CTRL_REG2[**INT_EN_FIFO=1**]**) 0: Cleared by reading the register to 1: When F_Event flag is set (F_OVF or F_WMKF are set), provided the FIFO interrupt is enabled (**CTRL_REG2[**INT_EN_FIFO=1**]**) 0: Cleared when F_Event Flag gets cleared (whenever both F_OVF and F_WMKF get cleared) • Table 29, SRC_RT field, changed bullets from ◦ Indicates that the rate threshold event flag triggered the interrupt ◦ Cleared by reading RT_SRC register to ◦ Indicates that the rate threshold event flag(s) triggered the interrupt (when XRT or YRT or ZRT(logical OR) event threshold flags go high) ◦ Cleared when XRT, YRT or ZRT event threshold flags are cleared. • Section 6.11, added: "It also clears the RT_SRC flag in the 0x0B: INT_SOURCE_FLAG register." • Added Table 54, *Rate sensitivity changes with FSR_DOUBLE setting*
1.2	11/2014	• Removed last two features items • Minor changes to table 2, Temperature Sensor Characteristics • In Mechanical Characteristics table, changed typical parameters for Zero-rate Offset, Zero-rate Offset, Post-board Mount and Integral nonlinearity and updated table footnotes.

Table continues on the next page...

Revision number	Revision date	Description
		• Updated Electrical Charactristics table, for Supply current drain in Standby mode, and Supply current drain in Standby mode over Temperature parameters. Also removed test condition on Output Data Rate frequency tolerance parameter. • Changed Table 8 Serial interface pin descriptions, pin currently named SDA/MOSI/ SPI_Data and modified pin description. • changed Table 9, Slave timing values, for parameter SDA and SCL fall time, minimum values for I^2C Fast Mode. • Added table title to Table 10. I^2C Register Data Address Map. • Section 3.1.1, I^2C Operation, changed first paragraph to read “External pull-up resistors connected to V_{DDIO}”... • Section 5, functionality, changed seventh bullet to read “Embedded rate threshold detection function with programmable debounce time” • Added new column “Auto-Increment Address” to Table 13 Register address map and populated the column with data. Removed last two rows of table, Auto-Increment address and Fast-read increment address. • Modified note after Table 19 to read “After this register is read, the next read register by the autoincrement process is STATUS at 0x00, when CTRL_REG3[WRAPTOONE] = 0, or OUT_X_MSB when CTRL_REG3[WRAPTOONE] = 1.”
2.0	2/2015	• Moved Section 2.1 to 2.5 • Figure 12, changed "SPI_DIO" to "SPI_DATA" • Register 0x09: F_SETUP, added "The contents should only be modified when the device is in Standby mode." • Table 29, Field 1, changed "...XRT, YRT or ZRT..." to "...XRT, YRT and ZRT..." • Register 0x0E: RT_CFG, added "The internal state of the Rate Threshold function is reset when..." • Table 37, Field 3, deleted second and third bullet • Register 0x0F: RT_SRC, added "The content of this register is reset upon a transition from Standy to Active or from Ready to Active modes. • Table 39: Field 6 • added "only if it has been latched (ELE =1)" • added to bit 1 "(XRT, YRT or ZRT)" Field 5 • changed second bullet to "Flag is asserted few samples (RT_COUNT)..." • added third bullet "Cleared when the absolute value of Z..." • changed bit 0 from "Z rate lower than RT_THS value" to "No rate threshold event detected on Z-axis" • changed bit 1 from "Z rate greater than RT_THS event has occured" to "Rate Threshold event detected on Z axis" Field 4 • changed first bullet from "Indicates the rate polarity on the Z-axis (if ZTEFE =1). If ZTEFE =1, this bit indicates the polarity of the Z data irrespective of the rate threshold event detected on Z-axis." to "Indicates the rate polarity on the Z-axis (if **RT_CFG[**ZTEFE**]** =1). If **RT_CFG[**ZTEFE**]** =1, this bit indicates the polarity of the Z data irrespective of the rate threshold event detected on Z-axis." Field 3 • changed second bullet to "Flag is asserted few samples (RT_COUNT)..." • added third bullet "Cleared when the absolute value of Y..." • changed bit 0 from "Y rate lower than RT_THS value" to "No rate threshold event detected on Y-axis" • changed bit 1 from "Y rate greater than RT_THS event has occured" to "Rate Threshold event detected on Y-axis" Field 2

Table continues on the next page...

Revision number	Revision date	Description
		• changed first bullet from "Indicates the rate polarity on the Y-axis (if YTEFE =1). If YTEFE =1, this bit indicates the polarity of the Y data irrespective of the rate threshold event detected on Y-axis." to "Indicates the rate polarity on the Y-axis (if **RT_CFG[**YTEFE**]** =1). If **RT_CFG[Y**TEFE**]** =1, this bit indicates the polarity of the Y data irrespective of the rate threshold event detected on Y-axis." Field 1 • changed second bullet to "Flag is asserted few samples (RT_COUNT)..." • added third bullet "Cleared when the absolute value of X..." • changed bit 0 from "X rate lower than RT_THS value" to "No rate threshold event detected on X-axis" • changed bit 1 from "X rate greater than RT_THS event has occured" to "Rate Threshold event detected on X-axis" Field 0 • changed first bullet from "Indicates the rate polarity on the X-axis (if XTEFE =1). If XTEFE =1, this bit indicates the polarity of the X data irrespective of the rate threshold event detected on X-axis." to "Indicates the rate polarity on the X-axis (if **RT_CFG[**XTEFE**]** =1). If **RT_CFG[**XTEFE**]** =1, this bit indicates the polarity of the X data irrespective of the rate threshold event detected on X-axis." • Table 41, Field 6:0, changed formula from "Rate_threshold=THS*(Full_scale/128)" to "Rate Threshold (in dps) = (THS + 1)* 256 * Sensitivity (in dps/LSB)" and "Rate_Threshold(in LSB) = (THS + 1)* 256"
2.1	5/2015	• Table 5, Self-test output change, Min value of 7000 added and Max value of 25000 added • Table 6 • Digital high level input voltage, added SCLK • Low-level output voltage, added test condition of I_o = 1 mA • Section 5, second bullet, changed **CTRL_REG3[**FSR_DOUBLE**]** = 1 to **CTRL_REG3[**FS_DOUBLE**]** = 1 • Table 13 • F_EVENT, added the default value of 0x00 • INT_SRC_FLAG, added the default value of 0x00 • CTRL_REG3, changed Auto-increment address from 0x16 to 0x00 • RESERVED, added Auto-increment address of address + 1

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Revision 2.1, 5/2015