CS4244

4 In/4 Out Audio CODEC with PCM and TDM Interfaces

DAC Features

- Advanced multibit delta-sigma modulator
- 24-bit resolution
- Differential or single-ended outputs
- Dynamic range (A-weighted)
  - -109 dB differential
  - -105 dB single-ended
- THD+N
  - -90 dB differential
  - -88 dB single ended
- 2 Vrms full-scale output into 3-kΩ AC load
- Rail-to-rail operation

ADC Features

- Advanced multibit delta-sigma modulator
- 24-bit resolution
- Differential inputs
- -105 dB dynamic range (A-weighted)
- -88 dB THD+N
- 2 Vrms full-scale input

System Features

- TDM, left justified, and I²S serial inputs and outputs
- I²C host control port
- Supports logic levels between 5 and 1.8 V
- Supports sample rates up to 96 kHz

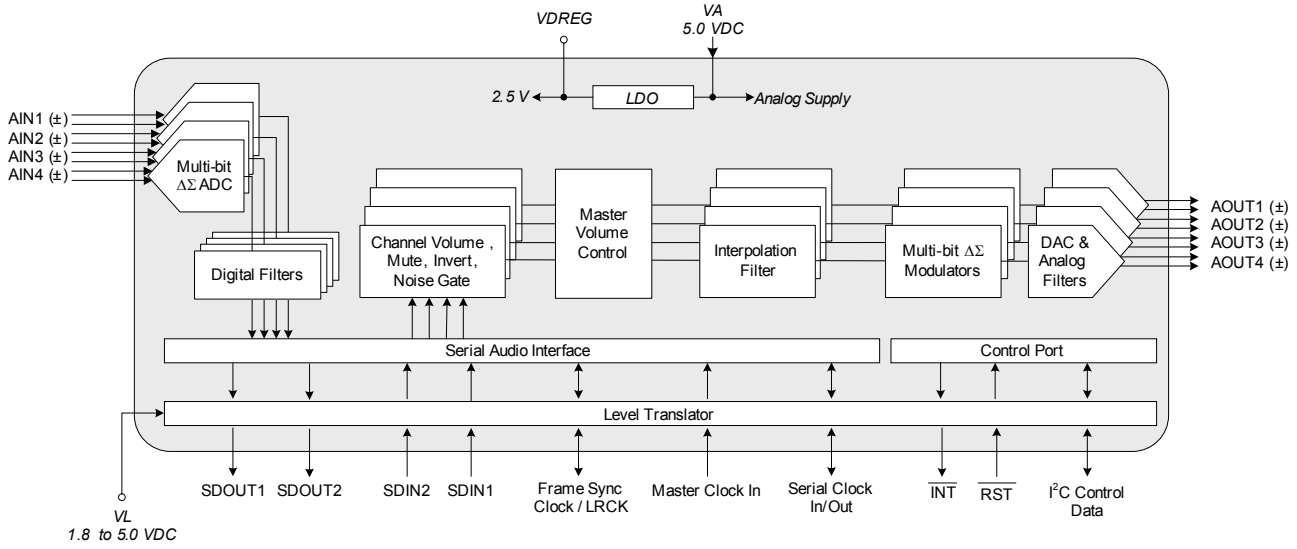
Common Applications

- Automotive audio systems
- AV, Blu-Ray® Disc, and DVD receivers
- Audio interfaces, mixing consoles, and effects processors

General Description

The CS4244 provides four multibit analog-to-digital and four multi-bit digital-to-analog Δ-Σ converters and is compatible with differential inputs and either differential or single-ended outputs. Digital volume control, noise gating, and muting is provided for each DAC path. A selectable high-pass filter is provided for the 4 ADC inputs. The CS4244 supports master and slave modes and TDM, left-justified, and I²S modes.

This product is available in a 40-pin QFN package in Automotive (-40°C to +85°C) and Commercial (0°C to +70°C) temperature grades. The CDB4244 Customer Demonstration Board is also available for device evaluation and implementation suggestions. See "Ordering Information" on page 64 for complete details.



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1. PIN DESCRIPTIONS

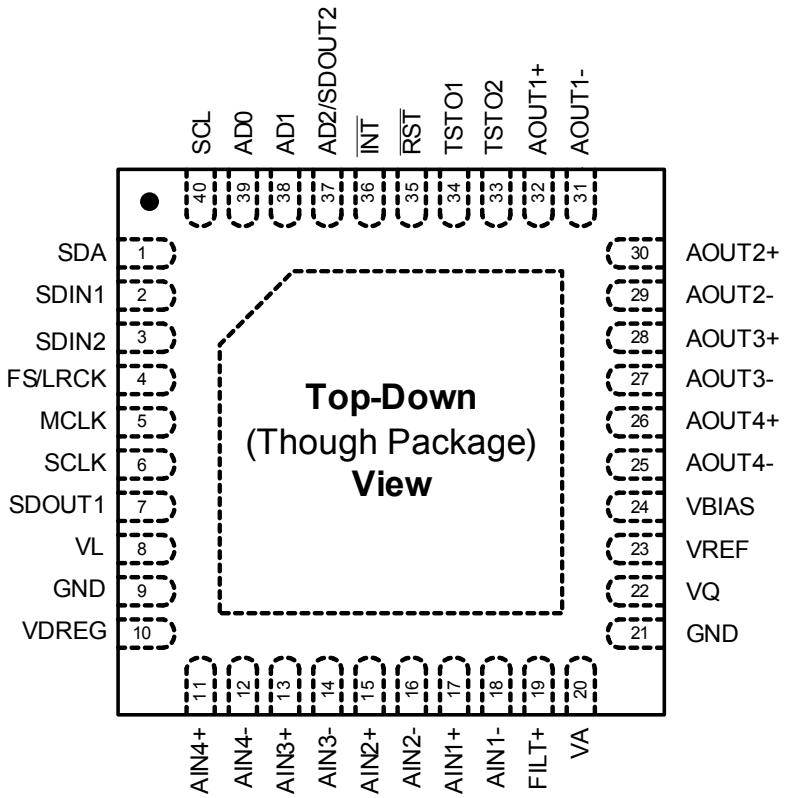


Figure 1. CS4244 Pinout

Pin Name	Pin #	Pin Description
SDA	1	**Serial Control Data** (*Input/Output*) - Bi-directional data I/O for the I²C control port.
SDINx	2,3	**Serial Data Input** (*Input*) - Input channels serial audio data.
FS/LRCK	4	**Frame Synchronization Clock/Left/Right Clock** (*Input/Output*) - Determines which channel or frame is currently active on the serial audio data line.
MCLK	5	**Master Clock** (*Input*) -Clock source for the internal logic, processing, and modulators.
SCLK	6	**Serial Clock** (*Input*/Output) -Serial Clock for the serial data port.
SDOUT1	7	**Serial Data Output 1** (*Output*) - ADC data output into a multi-slot TDM stream or AIN1 and AIN2 ADC data output in Left Justified and I²S modes.
VL	8	**Interface Power** (*Input*) - Positive power for the digital interface level shifters.
GND	9,21	**Ground** (*Input*) - Ground reference for the I/O and digital, analog sections.
VDREG	10	**Digital Power** (*Output*) - Internally generated positive power supply for digital section.
AINx+	11,13,15, 17	**Positive Analog Input** (*Input*) - Positive input signals to the internal analog to digital converters. The full scale analog input level is specified in the Analog Input Characteristics tables on pages 12 and 13.
AINx-	12,14,16, 18	**Negative Analog Input** (*Input*) - Negative input signals to the internal analog to digital converters. The full scale analog input level is specified in the Analog Input Characteristics tables on pages 12 and 13.
FILT+	19	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal ADCs.

VA	20	**Analog Power** (*Input*) - Positive power for the analog sections.
VQ	22	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
VREF	23	**Analog Power Reference** (*Input*) - Return pin for the VBIAS cap.
VBIAS	24	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal DACs.
AOUTx-	25,27,29, 31	**Negative Analog Output** *(Output)* - Negative output signals from the internal digital to analog converters. The full scale analog output level is specified in the Analog Output Characteristics tables on pages 16 and 17.
AOUTx+	26,28,30, 32	**Positive Analog Output** *(Output)* - Positive output signals from the internal digital to analog converters. The full scale analog output level is specified in the Analog Output Characteristics tables on pages 16 and 17.
TSTOx	33,34	**Test Outputs** *(Output)* - Test outputs. These pins should be left unconnected.
$\overline{\text{RST}}$	35	**Reset** (*Input*) - Applies reset to the internal circuitry when pulled low.
$\overline{\text{INT}}$	36	**Interrupt (Output)** - Sent to DSP to indicate an interrupt condition has occurred.
AD2/SDOUT2	37	**I²C Address Bit 2/Serial Data Output 2** (*Input/Output*) - Sets the I²C address bit 2 at reset. Functions as Serial Data Out 2 for AIN3 and AIN4 ADC data output in Left Justified and I²S modes. High impedance in TDM mode. See Section 4.3 I²C Control Port for more details concerning this mode of operation.
AD1	38	**I²C Address Bit 1** (*Input*) - Sets the I²C address bit 1.
AD0	39	**I²C Address Bit 0** (*Input*) - Sets the I²C address bit 0.
SCL	40	**Serial Control Port Clock** (*Input*) - Serial clock for the I²C control port.
GND	-	**Thermal Pad** - The thermal pad on the bottom of the device should be connected to the ground plane via an array of vias.

1.1 I/O Pin Characteristics

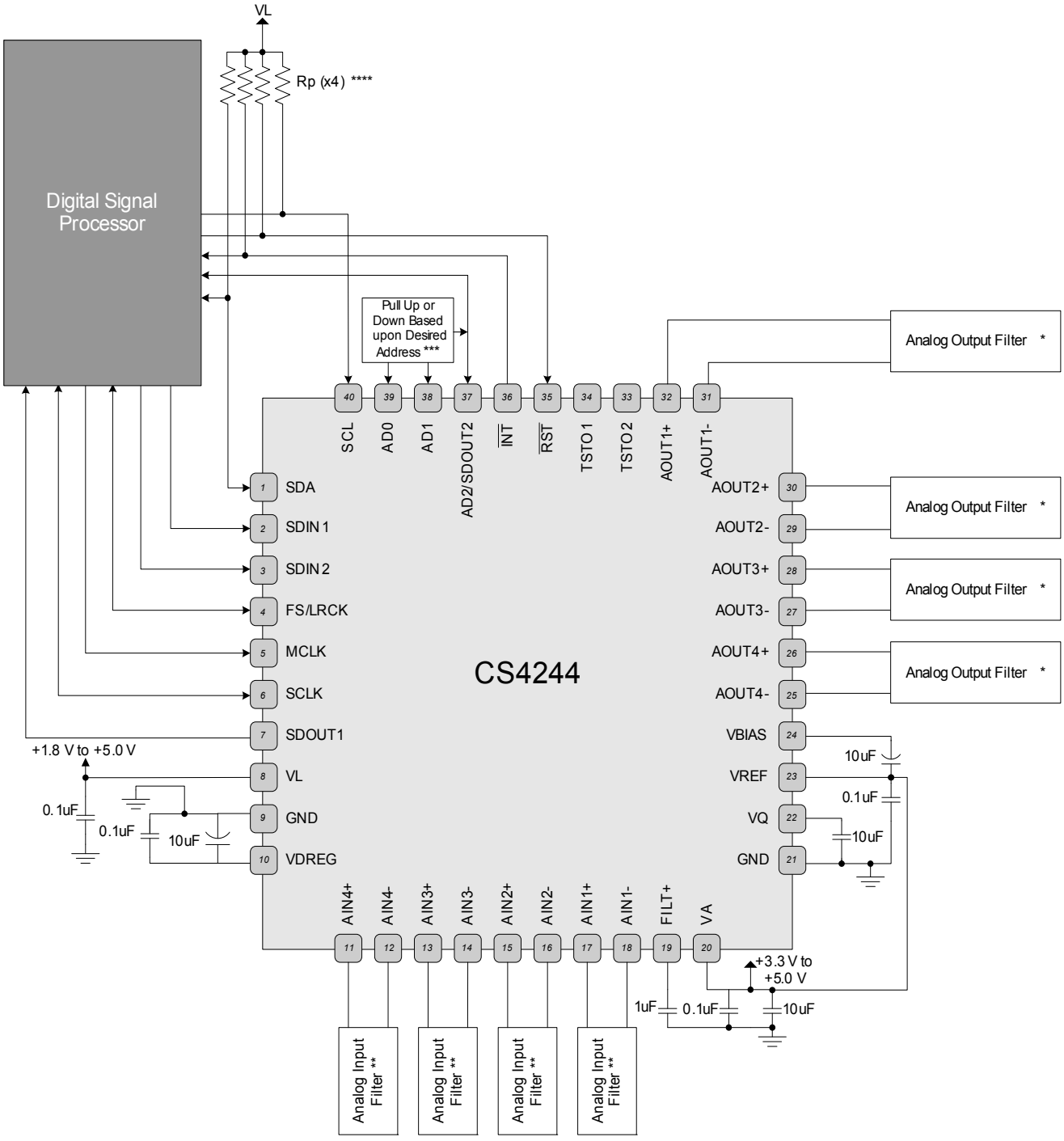
Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

Power Supply	Pin Name	I/O	Driver	Internal Connections (Note 1)	Receiver
VL	SCL	Input	-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	SDA	Input/Output	CMOS/Open Drain	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	$\overline{\text{INT}}$	Output	CMOS/Open Drain	(Note 2)	-
	$\overline{\text{RST}}$	Input	-	(Note 2)	5.0 V CMOS, with Hysteresis
	MCLK	Input	-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	FS/LRCK	Input/Output	5.0 V CMOS	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	SCLK	Input/Output	5.0 V CMOS	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	SDOUT1	Output	5.0 V CMOS	Weak Pull-down (~500kΩ)	
	SDINx	Input	-	Weak Pull-down (~500kΩ)	5.0 V CMOS, with Hysteresis
	AD0,1	Input	-	(Note 2)	5.0 V CMOS
	AD2/SDOUT2	Input/Output	5.0 V CMOS	(Note 2)	5.0 V CMOS

Notes:

1. Internal connection valid when device is in reset.
2. This pin has no internal pull-up or pull-down resistors. External pull-up or pull-down resistors should be added in accordance with Figure 2.

2. TYPICAL CONNECTION DIAGRAM



* See Section 4.6.4
** See Section 4.6.2.2
*** See Section 4.3
**** See Switching Specifications - Control Port

Figure 2. Typical Connection Diagram

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = 0 V; all voltages with respect to ground. (Note 3)

Parameters		Symbol	Min	Typ	Max	Units
DC Power Supply						
Analog Core		VA	3.135 4.75	3.3 5	3.465 5.25	V V
Level Translator		VL	1.71	-	5.25	V
Temperature						
Ambient Operating Temperature - Power Applied	Automotive Commercial	T_A	-40 0	- -	+85 +70	°C °C
Junction Temperature		T_J	-40	-	+150	°C

Notes: 3. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC Power Supply					
Analog Core		VA	-0.3	5.5	V
Level Translator		VL	-0.3	5.5	V
VDREG Current	(Note 4)	I_{VDREG}	-	10	µA
Inputs					
Input Current	(Note 5)	I_{in}	-	±10	mA
Analog Input Voltage	(Note 6)	V_{INA}	- 0.3	VA + 0.4	V
Logic Level Input Voltage	(Note 6)	V_{IND}	-0.3	VL + 0.4	V
Temperature					
Ambient Operating Temperature - Power Applied		T_A	-55	+125	°C
Storage Temperature		T_{stg}	-65	+150	°C

WARNING: OPERATION BEYOND THESE LIMITS MAY RESULT IN PERMANENT DAMAGE TO THE DEVICE.

Notes: 4. No external loads should be connected to the VDREG pin. Any connection of a load to this point may result in errant operation or performance degradation in the device.

5. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.

6. The maximum over/under voltage is limited by the input current.

DC ELECTRICAL CHARACTERISTICS

GND = 0 V; all voltages with respect to ground.

Parameters	Min	Typ	Max	Units
VDREG (Note 7)				
Nominal Voltage	-	2.5	-	V
Output Impedance	-	0.5	-	Ω
FILT+				
Nominal Voltage	-	VA	-	V
Output Impedance	-	23	-	kΩ
DC Current Source/Sink	-	-	1	µA
VQ				
Nominal Voltage	-	0.5•VA	-	V
Output Impedance	-	77	-	kΩ
DC Current Source/Sink	-	-	0	µA

Notes:

7. No external loads should be connected to the VDREG pin. Any connection of a load to this point may result in errant operation or performance degradation in the device.

TYPICAL CURRENT CONSUMPTION

This table represents the power consumption for individual circuit blocks within the CS4244. CS4244 is configured as shown in Figure 2 on page 8. VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC; F_S = 100 kHz; MCLK = 25.6 MHz; DAC load is 3 kΩ; All input signals are zero (digital zero for SDINx inputs and AC coupled to ground for AINx inputs) .

	Functional Block	**VA/VL**	**Typical Current [mA] (unless otherwise noted)** (Note 9), (Note 12)	
			i_{VA}	i_{VL}
1	Reset Overhead (All lines held static, $\overline{RST}$ line pulled low.)	5	0.030	0.001
		3.3	0.020	0.001
2	Power Down Overhead (All lines clocks and data lines active, $\overline{RST}$ line pulled high, All PDNx bits set high.)	5	5	0.101
		3.3	5	0.101
3	PLL (Note 10) (Current drawn resulting from PLL being active. PLL is active for 256x and 384x)	5	1	-
		3.3	1	-
4	DAC Overhead (Current drawn whenever any of the four DACs are powered up.)	5	50	-
		3.3	45	-
5	DAC Channel (Note 8) (Current drawn per each DAC powered up.)	5	5	-
		3.3	4	-
6	ADC Overhead (Current drawn whenever any of the four ADCs are powered up.)	5	11	-
		3.3	11	-
7	ADC Group (Current drawn due to an ADC “group” being powered up. See (Note 11))	5	2	-
		3.3	2	-
8	ADC Channel (Current drawn per each ADC powered up.)	5	2	0.109
		3.3	2	0.066

Notes:

8. Full-scale differential output signal.
9. Current consumption increases with increasing F_S and increasing MCLK. Values are based on F_S of 100 kHz and MCLK of 25.6 MHz. Current variance between speed modes is small.
10. PLL is activated by setting the MCLK RATE bit to either 000 (operating in 256x mode) or 001 (operating in 384kHz).
11. Internal to the CS4244, the analog to digital converters are grouped together in stereo pairs. ADC1 and ADC2 are grouped together as are ADC3 and ADC4. The ADC group current draw is the current that is drawn whenever one of these groups become active.
12. To calculate total current draw for an arbitrary amount of ADCs or DACs, the following equations apply:

Total Running Current Draw from VA Supply = *Power Down Overhead + PLL (If Applicable)+ DAC Current Draw + ADC Current Draw*
where
DAC Current Draw = DAC Overhead + (Number of DACs x DAC Channel)
ADC Current Draw = ADC Overhead + (Number of active ADC Groups x ADC Group) + (Number of active ADC Channels x ADC Channel)

and

Total Running Current Draw from VL Supply = *PDN Overhead + (Number of active ADC Channels x ADC Channel)*

ANALOG INPUT CHARACTERISTICS (COMMERCIAL GRADE)

Test Conditions (unless otherwise specified): Device configured as shown in Section 2. on page 8. Input sine wave: 1 kHz; VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = 25 °C; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Sample Rate = 48 kHz; all Power Down ADCx bits = 0.

Parameter	VA, VREF = 3.3 V			VA, VREF = 5.0 V			Unit
	Min	Typ	Max	Min	Typ	Max	
Dynamic Range							
A-weighted	95	101	-	99	105	-	dB
unweighted	92	98	-	96	102	-	dB
Total Harmonic Distortion + Noise							
-1 dBFS	-	-95	-89	-	-88	-82	dB
-60 dBFS	-	-38	-32	-	-42	-36	dB
Other Analog Characteristics							
Interchannel Gain Mismatch	-	0.2	-	-	0.2	-	dB
Gain Drift	-	±100	-	-	±100	-	ppm/°C
Offset Error (Note 13)							
High Pass Filter On	-	0.0001	-	-	0.0001	-	% Full Scale
High Pass Filter Off	-	0.25	-	-	0.25	-	% Full Scale
Interchannel Isolation	-	90	-	-	90	-	dB
Full-scale Input Voltage (Differential Inputs)	1.58•VA	1.66•VA	1.74•VA	1.58•VA	1.66•VA	1.74•VA	Vpp
Input Impedance	-	40	-	-	40	-	kΩ
Common Mode Rejection (Differential Inputs)	-	60	-	-	60	-	dB
PSRR (Note 14) 1 kHz	-	45	-	-	45	-	dB
60 Hz	-	20	-	-	20	-	dB

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE GRADE)

Test Conditions (unless otherwise specified): Device configured as shown in Section 2. on page 8. Input sine wave: 1 kHz; VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = -40 to +85 °C; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified; Sample Rate = 48 kHz; all Power Down ADCx bits = 0.

Parameter	VA, VREF = 3.3 V Min	Typ	Max	VA, VREF = 5.0 V Min	Typ	Max	Unit
Dynamic Range							
A-weighted	93	101	-	97	105	-	dB
unweighted	90	98	-	94	102	-	dB
Total Harmonic Distortion + Noise							
-1 dBFS	-	-95	-87	-	-88	-80	dB
-60 dBFS	-	-38	-30	-	-42	-34	dB
Other Analog Characteristics							
Interchannel Gain Mismatch	-	0.2	-	-	0.2	-	dB
Gain Drift	-	±100	-	-	±100	-	ppm/°C
Offset Error (Note 13)							
High Pass Filter On	-	0.0001	-	-	0.0001	-	% Full Scale
High Pass Filter Off	-	0.25	-	-	0.25	-	% Full Scale
Interchannel Isolation	-	90	-	-	90	-	dB
Full-scale Input Voltage (Differential Inputs)	1.58•VA	1.66•VA	1.74•VA	1.58•VA	1.66•VA	1.74•VA	Vpp
Input Impedance	-	40	-	-	40	-	kΩ
Common Mode Rejection (Differential Inputs)	-	60	-	-	60	-	dB
PSRR (Note 14) 1 kHz	-	45	-	-	45	-	dB
60 Hz	-	20	-	-	20	-	dB

Notes:

13. AINx+ connected to AINx-.
14. Valid with the recommended capacitor values on FILT+ and VQ. See Figure 4 for test configuration.

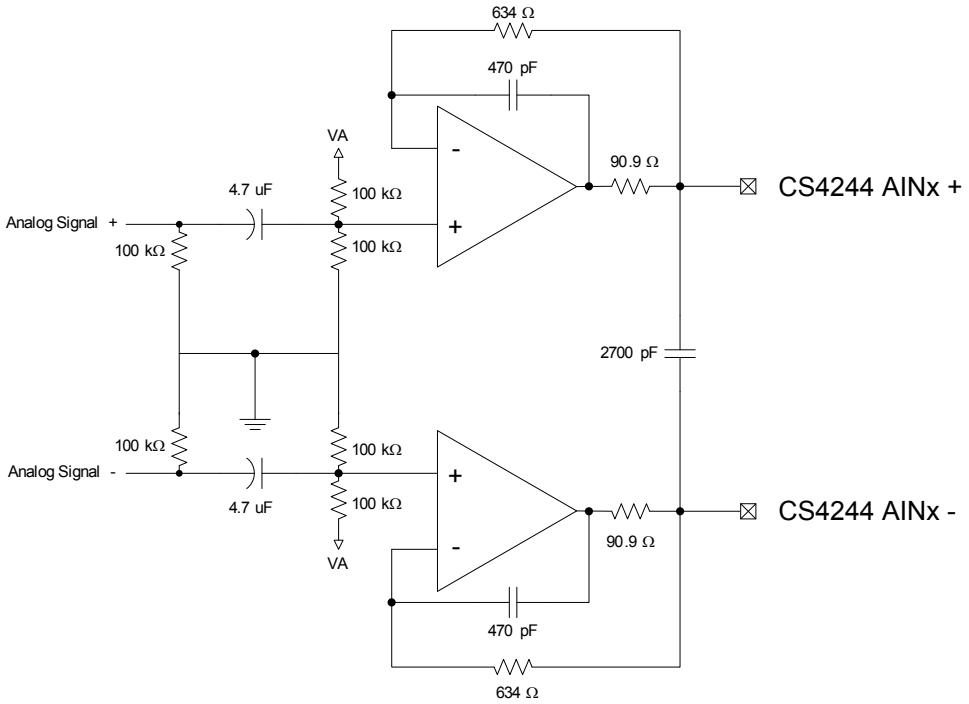


Figure 3. Test Circuit for ADC Performance Testing

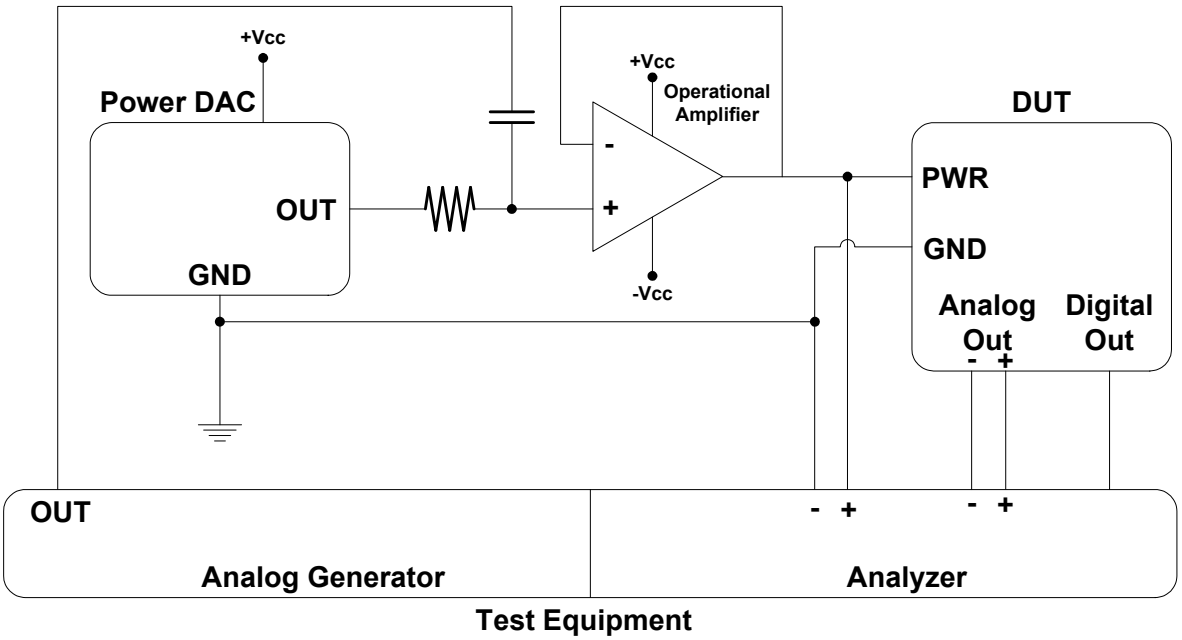


Figure 4. PSRR Test Configuration

ADC DIGITAL FILTER CHARACTERISTICS

Test Conditions (unless otherwise specified): Device configured as shown in Section 2. on page 8. Input sine wave: 1 kHz; VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; Measurement Bandwidth is 20 Hz to 20 kHz unless otherwise specified. See filter plots in Section 7. on page 60.

Parameter (Note 15)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	0.4535	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		70	-	-	dB
Single-Speed Mode					
ADC Group Delay (Note 16)		-	9.5/Fs	-	s
***High-Pass Filter Characteristics* (48 kHz Fs)**					
Frequency Response	-3.0 dB -0.13 dB	- -	2 11	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-0.09	-	0.17	dB
Filter Settling Time (Note 17)		-	25000/Fs	0	s
Double-Speed Mode					
ADC Group Delay (Note 16)		-	9.5/Fs	-	s
***High-Pass Filter Characteristics* (96 kHz Fs)**					
Frequency Response	-3.0 dB -0.13 dB	- -	4 22	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-0.15	-	0.17	dB
Filter Settling Time (Note 17)		-	25000/Fs	0	s

Note:

15. Response is clock-dependent and will scale with Fs.
16. The ADC group delay is measured from the time the analog inputs are sampled on the AINx pins to the FS/LRCK transition (rising or falling) after the last bit of that (group of) sample(s) has been transmitted on SDOUTx.
17. The amount of time from input of half-full-scale step function until the filter output settles to 0.1% of full scale.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL GRADE)

Test Conditions (unless otherwise specified). Device configured as shown in Section 2. on page 8. VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = 25 °C; Full-scale 1 kHz input sine wave; Sample Rate = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Specifications apply to all channels unless otherwise indicated; all Power Down DACx bits = 0. See (Note 19) on page 17.

Parameter		VA, VREF= 3.3 V (Differential/Single-ended) Min	Typ	Max	VA, VREF= 5.0 V (Differential/Single-ended) Min	Typ	Max	Unit
Dynamic Performance								
Dynamic Range								
18 to 24-Bit	A-weighted	100/96	106/102	-	103/99	109/105	-	dB
	unweighted	97/93	103/99	-	100/96	106/102	-	dB
16-Bit	A-weighted	89	95	-	89	95	-	dB
	unweighted	86	92	-	86	92	-	dB
Total Harmonic Distortion + Noise		-	-90/-88	-84/-82	-	-90/-88	-84/-82	dB
Full-scale Output Voltage		1.48•VA/ 0.74•VA	1.56•VA/ 0.78•VA	1.64•VA/ 0.82•VA	1.48•VA/ 0.74•VA	1.56•VA/ 0.78•VA	1.64•VA/ 0.82•VA	Vpp
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)(Note 19)		3	-	-	3	-	-	kΩ
Load Capacitance (C_L)(Note 19)		-	-	100	-	-	100	pF
Parallel DC-Load Resistance(Note 20)		10	-	-	10	-	-	kΩ
Output Impedance		-	100	-	-	100	-	Ω
PSRR (Note 21)	1 kHz	-	60	-	-	60	-	dB
	60 Hz	-	60	-	-	60	-	dB

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE GRADE)

Test Conditions (unless otherwise specified): Device configured as shown in Section 2. on page 8. VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.; T_A = -40 to +85 °C; Full-scale 1 kHz input sine wave; Sample Rate = 48 kHz; Measurement Bandwidth is 20 Hz to 20 kHz; Specifications apply to all channels unless otherwise indicated; all Power Down DACx bits = 0. See (Note 19).

Parameter		VA, VREF= 3.3 V (Differential/Single-ended) Min	Typ	Max	VA, VREF= 5.0 V (Differential/Single-ended) Min	Typ	Max	Unit
Dynamic Performance								
Dynamic Range								
18 to 24-Bit	A-weighted	98/94	106/102	-	101/97	109/105	-	dB
	unweighted	95/91	103/99	-	98/94	106/102	-	dB
16-Bit	A-weighted	87	95	-	87	95	-	dB
	unweighted	84	92	-	84	92	-	dB
Total Harmonic Distortion + Noise		-	-90/-88	-82/-80	-	-90/-88	-82/-80	dB
Full-scale Output Voltage		1.48•VA/ 0.74•VA	1.56•VA/ 0.78•VA	1.64•VA/ 0.82•VA	1.48•VA/ 0.74•VA	1.56•VA/ 0.78•VA	1.64•VA/ 0.82•VA	Vpp
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)(Note 19)		3	-	-	3	-	-	kΩ
Load Capacitance (C_L)(Note 19)		-	-	100	-	-	100	pF
Parallel DC-Load Resistance(Note 20)		10	-	-	10	-	-	kΩ
Output Impedance		-	100	-	-	100	-	Ω
PSRR (Note 21)	1 kHz	-	60	-	-	60	-	dB
	60 Hz	-	60	-	-	60	-	dB

Notes:

18. One LSB of triangular PDF dither added to data.
19. Loading configuration is given in Figure 5 below.

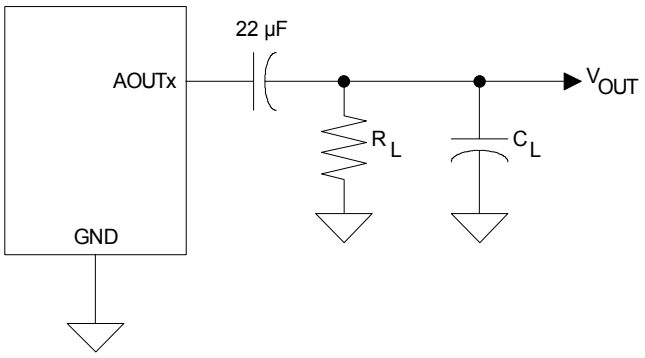


Figure 5. Equivalent Output Test Load

20. Parallel combination of all DAC DC loads. See Section 4.2.3.
21. Valid with the recommended capacitor values on FILT+ and VQ. See Figure 4 for test configuration.

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Test Conditions (unless otherwise specified): VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC. The filter characteristics have been normalized to the sample rate (F_S) and can be referenced to the desired sample rate by multiplying the given characteristic by F_S.

Parameter		Min	Typ	Max	Unit
Single-Speed Mode					
Passband (Note 22)	to -0.05 dB corner	0	-	0.4780	F_S
	to -3 dB corner	0	-	0.4996	F_S
Frequency Response 20 Hz to 20 kHz		-0.01	-	+0.12	dB
StopBand		0.5465	-	-	F_S
StopBand Attenuation	(Note 23)	102	-	-	dB
DAC1-4 Group Delay (Note 24)		-	11/Fs	-	s
Double-Speed Mode					
Passband (Note 22)	to -0.1 dB corner	0	-	0.4650	F_S
	to -3 dB corner	0	-	0.4982	F_S
Frequency Response 20 Hz to 20 kHz		-0.05	-	+0.2	dB
StopBand		0.5770	-	-	F_S
StopBand Attenuation	(Note 23)	80	-	-	dB
DAC1-4 Group Delay (Note 24)		-	7/Fs	-	s

Notes:

22. Response is clock-dependent and will scale with F_S.
23. For Single-Speed Mode, the measurement bandwidth is 0.5465 F_S to 3 F_S.
    For Double-Speed Mode, the measurement bandwidth is 0.577 F_S to 1.4 F_S.
24. The DAC group delay is measured from the FS/LRCK transition (rising or falling) before the first bit of a (group of) sample(s) is transmitted on the SDINx pins to the time it appears on the AOUTx pins.

DIGITAL I/O CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage (all input pins except $\overline{RST}$) (VL = 1.8 V)	(% of VL)	V_{IH}	75%	-	-	V
High-Level Input Voltage (all input pins except $\overline{RST}$) (VL = 2.5 V, 3.3 V, or 5 V)	(% of VL)	V_{IH}	70%	-	-	V
Low-Level Input Voltage (all input pins except $\overline{RST}$)	(% of VL)	V_{IL}	-	-	30%	V
High-Level Input Voltage ($\overline{RST}$ pin)		V_{IH}	1.2	-	-	V
Low-Level Input Voltage ($\overline{RST}$ pin)		V_{IL}	-	-	0.3	V
High-Level Output Voltage at I_o = 2 mA	(% of VL)	V_{OH}	80%	-	-	V
Low-Level Output Voltage at I_o = 2 mA	(% of VL)	V_{OL}	-	-	20%	V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF

SWITCHING CHARACTERISTICS - SERIAL AUDIO INTERFACE

VA_SEL = 0 for VA = 3.3 VDC, 1 for VA = 5.0 VDC.

Parameters		Symbol	Min	Max	Units
$\overline{RST}$ pin Low Pulse Width	(Note 25)		1	-	ms
MCLK Frequency	(Note 26)		7.68	25.6	MHz
MCLK Duty Cycle			45	55	%
SCLK Duty Cycle			45	55	%
Input Sample Rate (FS/LRCK pin)	Single-Speed Mode	F_S	30	50	kHz
	Double-Speed Mode	F_S	60	100	kHz
SCLK Falling Edge to SDOUTx Valid (VL = 1.8 V)		t_{dh2}	-	31	ns
SCLK Falling Edge to SDOUTx Valid (VL = 2.5 V)		t_{dh2}	-	22	ns
SCLK Falling Edge to SDOUTx Valid (VL = 3.3 V or 5 V)		t_{dh2}	-	17	ns
TDM Slave Mode					
SCLK Frequency	(Note 27)		256x	512x	F_S
FS/LRCK High Time Pulse	(Note 28)	t_{lpw}	$1/f_{SCLK}$	$(n-1)/f_{SCLK}$ (Note 29)	ns
FS/LRCK Rising Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SDINx Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
SDINx Hold Time After SCLK Rising Edge		t_{dh1}	5	-	ns
PCM Slave Mode					
SCLK Frequency			32x	64x	F_S
FS/LRCK Duty Cycle			45	55	%
FS/LRCK Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SDINx Setup Time Before SCLK Rising Edge		t_{ds}	3	-	ns
SDINx Hold Time After SCLK Rising Edge		t_{dh1}	5	-	ns
PCM Master Mode					
SCLK Frequency			64x	64x	F_S
FS/LRCK Duty Cycle			45	55	%
FS/LRCK Edge to SCLK Rising Edge		t_{lcks}	5	-	ns
SDINx Setup Time Before SCLK Rising Edge		t_{ds}	5	-	ns
SDINx Hold Time After SCLK Rising Edge (VL = 1.8 V)		t_{dh1}	11	-	ns
SDINx Hold Time After SCLK Rising Edge (VL = 2.5 V, 3.3 V, or 5 V)		t_{dh1}	10	-	ns

Notes:

25. After applying power to the CS4244, $\overline{RST}$ should be held low until after the power supplies and MCLK are stable.
26. MCLK must be synchronous to and scale with F_S.
27. The SCLK frequency must remain less than or equal to the MCLK frequency. For this reason, SCLK may range from 256x to 512x only in single speed mode. In double speed mode, 256x is the only ratio supported.
28. The MSB of CH1 is always aligned with the second SCLK rising edge following FS/LRCK rising edge.
29. Where “n” is equal to the MCLK to LRCK ratio (set by the Master Clock Rate register bits), i.e. in 256x mode, n = 256, in 512x mode, n = 512, etc.

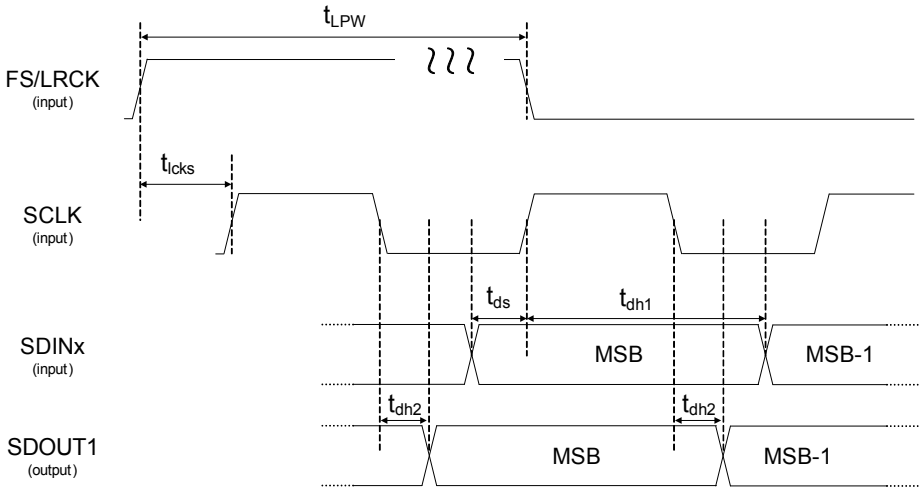


Figure 6. TDM Serial Audio Interface Timing

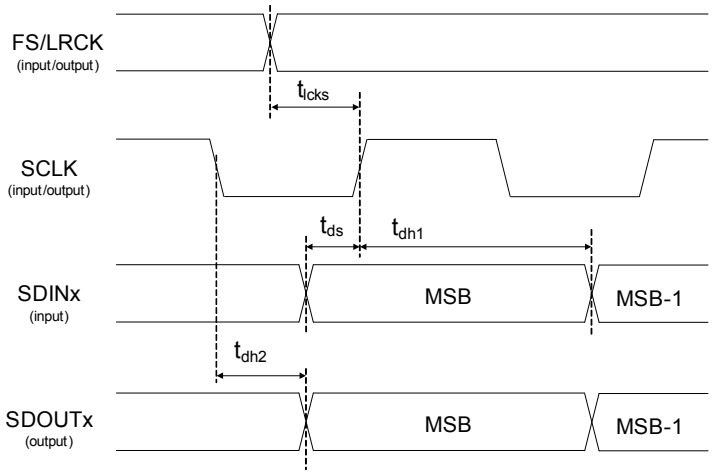


Figure 7. PCM Serial Audio Interface Timing

SWITCHING SPECIFICATIONS - CONTROL PORT

Test conditions (unless otherwise specified): Inputs: Logic 0 = GND = 0 V, Logic 1 = VL; SDA load capacitance equal to maximum value of C_b specified below (Note 30).

Parameters	Symbol	Min	Max	Unit
SCL Clock Frequency	f_{scl}	-	550	kHz
$\overline{\text{RESET}}$ Rising Edge to Start	t_{irs}	(Note 31)	-	ns
Bus Free Time Between Transmissions	t_{buf}	1.3	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	0.6	-	µs
Clock Low time	t_{low}	1.3	-	µs
Clock High Time	t_{high}	0.6	-	µs
Setup Time for Repeated Start Condition	t_{sust}	0.6	-	µs
SDA Input Hold Time from SCL Falling (Note 32)	t_{hddi}	0	0.9	µs
SDA Output Hold Time from SCL Falling	t_{hddo}	0.2	0.9	µs
SDA Setup time to SCL Rising	t_{sud}	100	-	ns
Rise Time of SCL and SDA	t_r	-	300	ns
Fall Time SCL and SDA	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	0.6	-	µs
SDA Bus Load Capacitance	C_b	-	400	pF
SDA Pull-Up Resistance	R_p	500	-	Ω

Notes:

30. All specifications are valid for the signals at the pins of the CS4244 with the specified load capacitance.
31. 2 ms + (3000/MCLK). See Section 4.2.1.
32. Data must be held for sufficient time to bridge the transition time, t_f, of SCL.

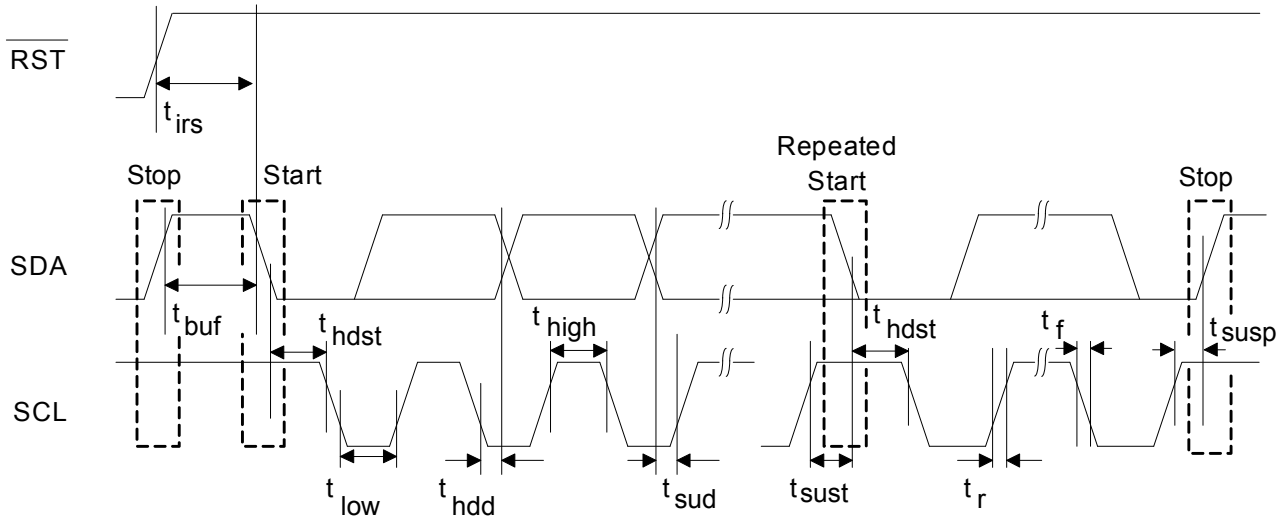


Figure 8. I²C Control Port Timing

4. APPLICATIONS

4.1 Power Supply Decoupling, Grounding, and PCB Layout

As with any high-resolution converter, the CS4244 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 2 shows the recommended power arrangements, with VA connected to clean supplies. VDREG, which powers the digital circuitry, is generated internally from an on-chip regulator from the VA supply. The VDREG pin provides a connection point for the decoupling capacitors, as shown in Figure 2.

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as near to the pins of the CS4244 as possible. The low value ceramic capacitor should be the nearest to the pin and should be mounted on the same side of the board as the CS4244 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+, VBIAS, and VQ pins in order to avoid unwanted coupling into the modulators. The FILT+, VBIAS, and VQ decoupling capacitors, particularly the 0.1 µF, must be positioned to minimize the electrical path from their respective pins and GND.VA_SEL

For optimal heat dissipation from the package, it is recommended that the area directly under the device be filled with copper and tied to the ground plane. The use of vias connecting the topside ground to the backside ground is also recommended.

4.2 Recommended Power-up & Power-down Sequence

The initialization and Power-Up/Down sequence flow chart is shown in Figure 9. For the CS4244 Reset is defined as all lines held static, $\overline{\text{RST}}$ line is pulled low. Power Down is defined as all lines (excluding MCLK) held static, $\overline{\text{RST}}$ line is high, all PDNx bits are ‘1’. Running is defined as $\overline{\text{RST}}$ line high, all PDNx bits are ‘0’.

4.2.1 Power-up

The CS4244 enters a reset state upon the initial application of VA and VL. When these power supplies are initially applied to the device, the audio outputs, AOUTxx, are clamped to VQ which is initially low. Additionally, the interpolation and decimation filters, delta-sigma modulators and control port registers are all reset and the internal voltage reference, multi-bit digital-to-analog and analog-to-digital converters and low-pass filters are powered down. The device remains in the reset state until the $\overline{\text{RST}}$ pin is brought high.

Once $\overline{\text{RST}}$ is brought high, the control port address is latched after 2 ms + (3000/MCLK). Until this latching transition is complete, the device will not respond to I²C reads or writes, but the I²C bus may still be used during this time. Once the latching transition is complete, the address is latched and the control port is accessible. At this point and the desired register settings can be loaded per the interface descriptions detailed in the Section 4.3 I²C Control Port. To ensure specified performance and timing, the VA_SEL must be set to “0” for VA = 3.3 VDC and “1” for VA = 5.0 VDC before audio output begins.

After the $\overline{\text{RST}}$ pin is brought high and MCLK is applied, the outputs begin to ramp with VQ towards the nominal quiescent voltage. VQ will charge to VA/2 upon initial power up. The time that it takes to charge up to VA/2 is governed by the size of the capacitor attached to the VQ pin. With the capacitor value shown in the typical connection diagram, the charge time will be approximately 250 ms. The gradual voltage ramping allows time for the external DC-blocking capacitors to charge to VQ, effectively blocking the quiescent DC voltage. Once FS/LRCK is valid, MCLK occurrences are counted over one F_S period to determine the MCLK/F_S ratio. With MCLK valid and any of the PDNx bits cleared, the internal voltage references will transition to their nominal voltage. Power is applied to the D/A converters and filters, and the analog outputs are un-clamped from the quiescent voltage, VQ. Afterwards, normal operation begins.

4.2.2 Power-down

To prevent audio transients at power-down, the DC-blocking capacitors must fully discharge before turning off the power. In order to do this in a controlled manner, it is recommended that all the converters be muted to start the sequence. Next, set PDNx for all converters to 1 to power them down internally. Then, FS/LRCK and SCLK can be removed if desired. Finally, the "VQ RAMP" bit in the "DAC Control 4" register must be set to '1' for a period of 50 ms before applying reset or removing power or MCLK. During this time, voltage on VQ and the audio outputs discharge gradually to GND. If power is removed before this 50 ms time period has passed, a transient will occur and a slight click or pop may be heard. There is no minimum time for a power cycle. Power may be re-applied at any time.

It is important to note that all clocks should be applied and removed in the order specified in Figure 9. If MCLK is removed or applied before $\overline{\text{RST}}$ has been pulled low, audible pops, clicks and/or distortion can result. If either SCLK or FS/LRCK is removed or applied before all PDNx bits are set to 1, audible pops, clicks and/or distortion can result.

Note: Timings are approximate and based upon the nominal value of the passive components specified in the "Typical Connection Diagram" on page 8. See Section 4.6.5.2 for volume ramp behavior.

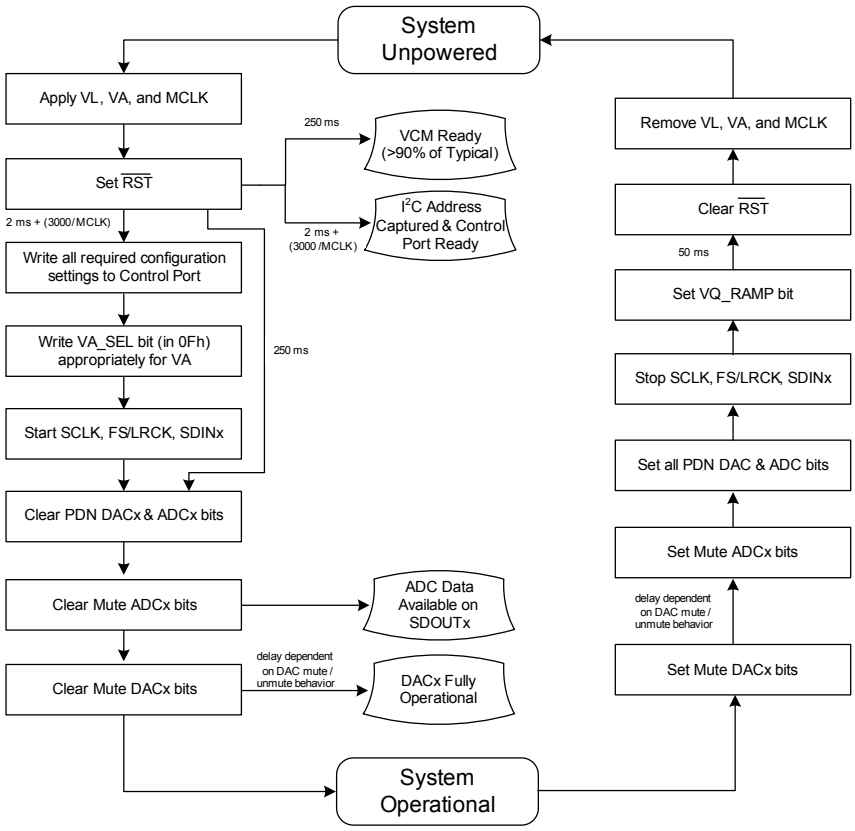


Figure 9. System Level Initialization and Power-Up/Down Sequence

4.2.3 DAC DC Loading

Figure 10 shows the analog output configuration during power-up, with the AOUTx± pins clamped to VQ to prevent pops and clicks. Thus any DC loads (RL_x) on the output pins will be in parallel when the switches are closed. These DC loads will pull the VQ voltage down towards ground. If the parallel combination of all DC loads exceeds the specification shown in the Analog Output Characteristics tables on pages 16

and 17, the VQ voltage will never rise to its minimum operating voltage. If the VQ voltage never rises above this minimum operating voltage, the device will not finish the power-up sequence and normal operation will not begin.

Also note that any AOUTx± pin(s) with a DC load must remain powered up (PDN DACx = 0) to keep the VQ net at its nominal voltage during normal operation, otherwise clipping may occur on the outputs.

Note that the load capacitors (CL_x) are also in parallel during power-up. The amount of total capacitance on the VQ net during power-up will affect the amount of time it takes for the VQ voltage to rise to its nominal operating voltage after VA power is applied. The time period can be calculated using the time constant given by the internal series resistor and the load capacitors.

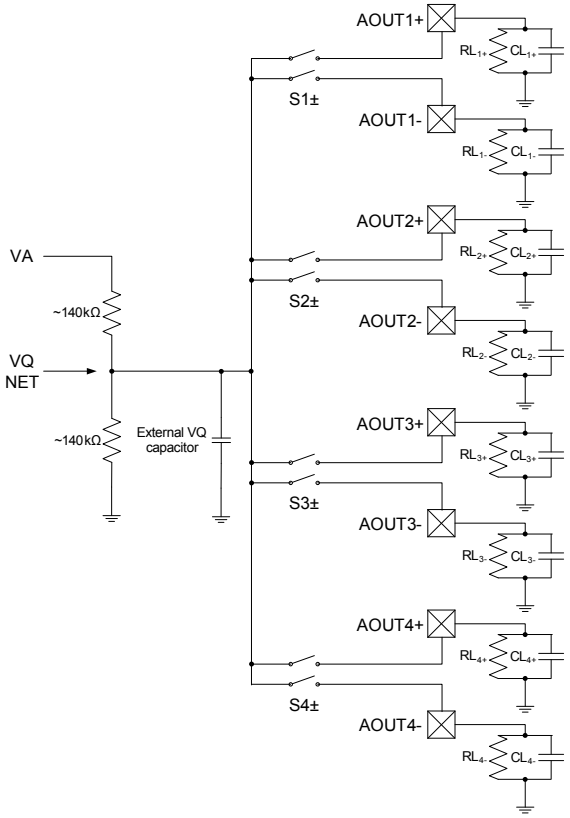


Figure 10. DAC DC Loading

4.3 I²C Control Port

All device configuration is achieved via the I²C control port registers as described in the Switching Specifications - Control Port table. The operation via the control port may be completely asynchronous with respect to the audio sample rates. However, to avoid potential interference problems, the I²C pins should remain static if no operation is required. The CS4244 acts as an I²C slave device.

SDA is a bidirectional data line. Data is clocked into and out of the device by the clock, SCL. The AD0 and AD1 pins form the two least significant bits of the chip address and should be connected through a resistor to VL or GND as desired. The SDOUT2 pin is used to set the AD2 bit by connecting a resistor from the SDOUT2 pin to VL or to GND. The state of these pins are sensed after the CS4244 is released from reset.

The signal timings for a read and write cycle are shown in Figure 11 and Figure 12. A Start condition is defined as a falling transition of SDA while the clock is high. A Stop condition is a rising transition while the clock is high. All other transitions of SDA occur while the clock is low. The first byte sent to the CS4244 after a Start condition consists of a 7-bit chip address field and a R/$\overline{W}$ bit (high for a read, low for a write). The upper 4 bits of the 7-bit address field are fixed at 0010. To communicate with a CS4244, the chip address field, which is the first byte sent to the CS4244, should match 0010 followed by the settings of the ADx pins. The eighth bit of the address is the R/$\overline{W}$ bit. If the operation is a write, the next byte is the Memory Address Pointer (MAP) which selects the register to be read or written. If the operation is a read, the contents of the register pointed to by the MAP will be output. Setting the auto increment bit in MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit. The ACK bit is output from the CS4244 after each input byte is read, and is input to the CS4244 from the microcontroller after each transmitted byte.

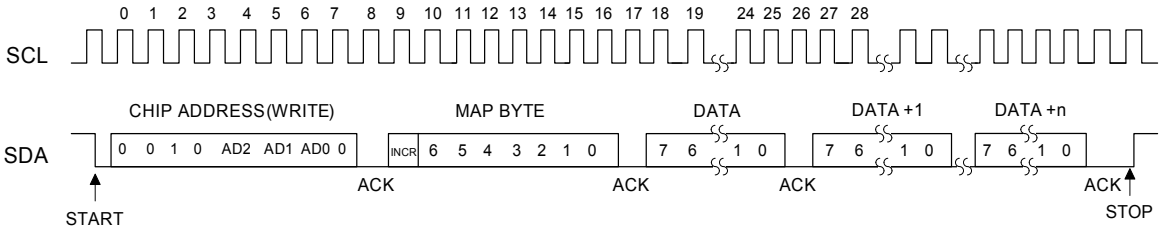


Figure 11. Timing, I²C Write

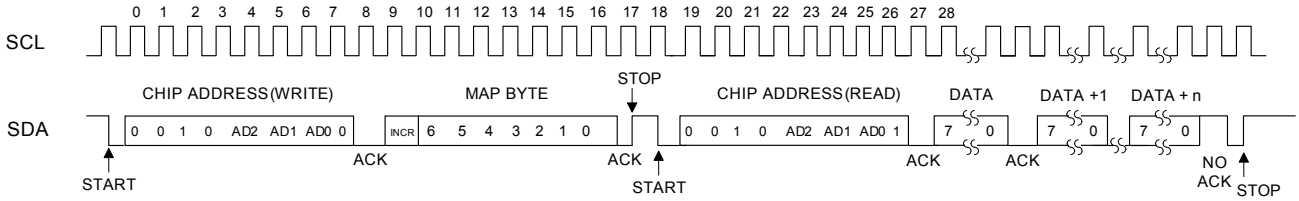


Figure 12. Timing, I²C Read

Since the read operation can not set the MAP, an aborted write operation is used as a preamble. As shown in Figure 12, the write operation is aborted after the acknowledge for the MAP byte by sending a stop condition. The following pseudocode illustrates an aborted write operation followed by a read operation.

Send start condition.
Send 0010xxx0 (chip address & write operation).
Receive acknowledge bit.
Send MAP byte, auto increment off.
Receive acknowledge bit.
Send stop condition, aborting write.
Send start condition.
Send 0010xxx1 (chip address & read operation).
Receive acknowledge bit.
Receive byte, contents of selected register.
Send acknowledge bit.
Send stop condition.

Setting the auto increment bit in the MAP allows successive reads or writes of consecutive registers. Each byte is separated by an acknowledge bit.

4.3.1 Memory Address Pointer (MAP)

The MAP byte comes after the address byte and selects the register to be read or written. Refer to the pseudocode above for implementation details.

4.3.1.1 Map Increment (INCR)

The CS4244 has MAP auto-increment capability enabled by the INCR bit (the MSB) of the MAP. If INCR is set to '0', MAP will stay constant for successive I²C reads or writes. If INCR is set to '1', MAP will auto-increment after each byte is read or written, allowing block reads or writes of successive registers.

4.4 System Clocking

The CS4244 will operate at sampling frequencies from 30 kHz to 100 kHz. This range is divided into two speed modes as shown in Table 1.

Mode	Sampling Frequency
Single-Speed	30-50 kHz
Double-Speed	60-100 kHz

Table 1. Speed Modes

The serial port clocking must be changed while all PDNx bits are set. If the clocking is changed otherwise, the device will enter a mute state, see Section 4.8 on page 43.

4.4.1 Master Clock

The ratio of the MCLK frequency to the sample rate must be an integer. The FS/LRCK frequency is equal to F_S, the frequency at which all of the slots of the TDM stream or channels in Left Justified or I²S formats are clocked into or out of the device. The Speed Mode and Master Clock Rate bits configure the device to generate the proper clocks in Master Mode and receive the proper clocks in Slave Mode. Table 2 illustrates several standard audio sample rates and the required MCLK and FS/LRCK frequencies.

The CS4244 has an internal fixed ratio PLL. This PLL is activated when the "MCLK RATE[2:0]" bits in the "Clock & SP Sel." register are set to either 000 or 001, corresponding to 256x or 384x. When in either of these two modes, the PLL will activate to adjust the frequency of the incoming MCLK to ensure that the internal state machines operate at a nominal 24.576 MHz rate. As is shown in the Typical Current Consumption table, activation of the PLL will increase the power consumption of the CS4244.

FS/LRCK **(kHz)**	**MCLK (MHz)**				
	128x (Note 33)	**192x** (Note 33)	**256x**	**384x**	**512x**
32	-	-	8.1920	12.2880	16.3840
44.1	-	-	11.2896	16.9344	22.5792
48	-	-	12.2880	18.4320	24.5760
64	8.1920	12.2880	16.3840	-	-
88.2	11.2896	16.9344	22.5792	-	-
96	12.2880	18.4320	24.5760	-	-
Mode	**DSM**			**SSM**	

Table 2. Common Clock Frequencies

Note:

33. 128x and 192x ratios valid only in Left Justified or I²S formats.

4.4.2 Master Mode Clock Ratios

As a clock master, FS/LRCK and SCLK will operate as outputs internally derived from MCLK. FS/LRCK is equal to F_S and SCLK is equal to 64x F_S as shown in Figure 13. TDM format is not supported in Master Mode.

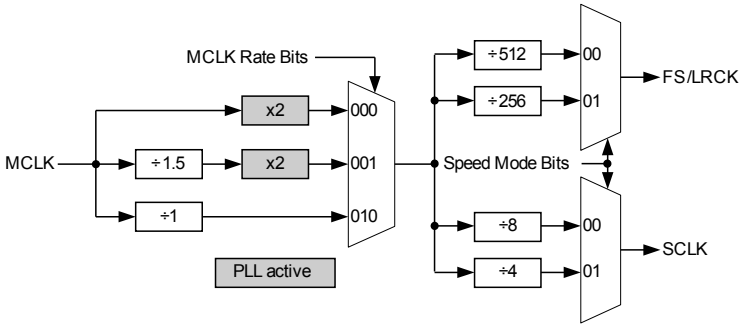


Figure 13. Master Mode Clocking

The resulting valid master mode clock ratios are shown in Table 3 below.

	SSM	DSM
MCLK/F_S	256x, 384x, 512x	128x, 192x, 256x
SCLK/F_S	64x	64x

Table 3. Master Mode Left Justified and I²S Clock Ratios

4.4.3 Slave Mode Clock Ratios

In Slave Mode, SCLK and FS/LRCK operate as inputs. The FS/LRCK clock frequency must be equal to the sample rate, F_S, and must be synchronously derived from the supplied master clock, MCLK.

The serial bit clock, SCLK, must be synchronously derived from the master clock, MCLK, and be equal to 512x, 256x, 128x, 64x, 48x or 32x F_S, depending on the desired format and speed mode. Refer to Table 4 and Table 5 for required clock ratios.

	SSM	DSM
MCLK/F_S	256x, 384x, 512x	128x, 192x, 256x
SCLK/F_S	32x, 48x, 64x, 128x	32x, 48x, 64x

Table 4. Slave Mode Left Justified and I²S Clock Ratios

(Note 34)	SSM		DSM
MCLK/F_S	256x, 384x, 512x	512x	256x
SCLK/F_S	256x	512x	256x

Table 5. Slave Mode TDM Clock Ratios

Note:

34. For all cases, the SCLK frequency must be less than or equal to the MCLK frequency.

4.5 Serial Port Interface

The serial port interface format is selected by the Serial Port Format register bits. The TDM format is available in Slave Mode only.

4.5.1 TDM Mode

The serial port of the CS4244 supports the TDM interface format with varying bit depths from 16 to 24 as shown in Figure 15. Data is clocked out of the ADC on the falling edge of SCLK and clocked into the DAC on the rising edge.

As indicated in Figure 15, TDM data is received most significant bit (MSB) first, on the second rising edge of the SCLK occurring after a FS/LRCK rising edge. All data is valid on the rising edge of SCLK. All bits are transmitted on the falling edge of SCLK. Each slot is 32 bits wide, with the valid data sample left justified within the slot. Valid data lengths are 16, 18, 20, or 24 bits.

FS/LRCK identifies the start of a new frame and is equal to the sample rate, F_S. As shown in Figure 14, FS/LRCK is sampled as valid on the rising SCLK edge preceding the most significant bit of the first data sample and must be held valid for at least 1 SCLK period.

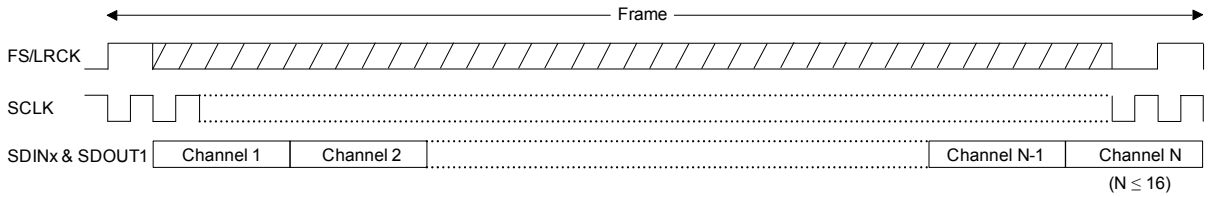


Figure 14. TDM System Clock Format

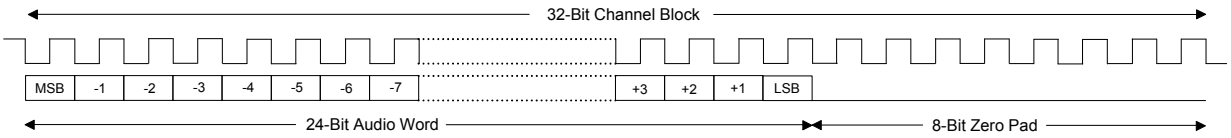


Figure 15. 32-bit Receiver Channel Block

The structure in which the serial data is coded into the TDM slots is shown in Figure 16. SDOUT2 is unused in TDM mode and is placed in a high-impedance state. When using a 48 kHz sample rate with a 24.576 MHz MCLK and SCLK, a 16 slot TDM structure can be realized. When using a 48 kHz sample rate with 12.288 MHz SCLK and 24.576 MHz MCLK, or a 96 kHz sample rate with a 24.576 MHz MCLK and SCLK, an 8 slot TDM structure can be realized. The data that is coded into the TDM slots is extracted into the appropriate signal path via the settings in the Control port. Please refer to Section 4.6.1 Routing the Serial Data within the Signal Paths for more details.

MCLK = 12.288/24.576MHz FS/LRCK = 48/96kHz SCLK = 12.288/24.576MHz																
	Slot 1 [31:0]		Slot 2 [31:0]		Slot 3 [31:0]		Slot 4 [31:0]		Slot 5 [31:0]		Slot 6 [31:0]		Slot 7 [31:0]		Slot 8 [31:0]	
SDIN1	Input Data 1.1 [31:8]	x [7:0]	Input Data 1.2 [31:8]	x [7:0]	Input Data 1.3 [31:8]	x [7:0]	Input Data 1.4 [31:8]	x [7:0]	Input Data 1.5 [31:8]	x [7:0]	Input Data 1.6 [31:8]	x [7:0]	Input Data 1.7 [31:8]	x [7:0]	Input Data 1.8 [31:8]	x [7:0]
SDIN2	Input Data 2.1 [31:8]	x [7:0]	Input Data 2.2 [31:8]	x [7:0]	Input Data 2.3 [31:8]	x[7:0]	Input Data 2.4 [31:8]	x [7:0]	Input Data 2.5 [31:8]	x [7:0]	Input Data 2.6 [31:8]	x[7:0]	Input Data 2.7 [31:8]	x[7:0]	Input Data 2.8 [31:8]	x[7:0]
SDOUT1	ADC1 Data[31:8]	0's [7:0]	ADC2 Data [31:8]	0's [7:0]	ADC3 Data [31:8]	0's [7:0]	ADC4 Data[31:8]	0's [7:0]	0's [31:0]		0's [31:0]		0's [31:0]		0's [31:0]	
SDOUT1 with Sidechain	ADC1 Data[31:8]	0's [7:0]	ADC2 Data [31:8]	0's [7:0]	ADC3 Data [31:8]	0's [7:0]	ADC4 Data [31:8]	0's [7:0]	Output Data (SDIN2 Slot 1)		Output Data (SDIN2 Slot 2)		Output Data (SDIN2 Slot 3)		Output Data (SDIN2 Slot 4)	

MCLK = 24.576MHz FS/LRCK = 48kHz SCLK = 24.576MHz																				
	Slot 1 [31:0]			Slot 4 [31:0]		Slot 5 [31:0]			Slot 8 [31:0]		Slot 9 [31:0]			Slot 12 [31:0]		Slot 13 [31:0]			Slot 16 [31:0]	
SDIN1	Input Data 1.1 [31:8]	x [7:0]		Input Data 1.4 [31:8]	x [7:0]	Input Data 1.5 [31:8]	x [7:0]		Input Data 1.8 [31:8]	x [7:0]	Input Data 1.9 [31:8]	x [7:0]		Input Data 1.12 [31:8]	x [7:0]	Input Data 1.13 [31:8]	x [7:0]		Input Data 1.16 [31:8]	x [7:0]
SDIN2	Input Data 2.1 [31:8]	x [7:0]	...→...	Input Data 2.4 [31:8]	x [7:0]	Input Data 2.5 [31:8]	x [7:0]	...→...	Input Data 2.8 [31:8]	x [7:0]	Input Data 2.9 [31:8]	x [7:0]	...→...	Input Data 2.12 [31:8]	x [7:0]	Input Data 2.13 [31:8]	x [7:0]	...→...	Input Data 2.16 [31:8]	x [7:0]
SDOUT1	ADC1 Data [31:8]	0's [7:0]		ADC4 Data [31:8]	0's [7:0]	0's [31:0]			0's [31:0]		0's [31:0]			0's [31:0]		0's [31:0]			0's [31:0]	
SDOUT1 with Sidechain	ADC1 Data [31:8]	0's [7:0]		ADC4 Data [31:8]	0's [7:0]	Output Data (SDIN2 Slot 1)			Output Data (SDIN2 Slot 4)		Output Data (SDIN2 Slot 5)			Output Data (SDIN2 Slot 8)		Output Data (SDIN2 Slot 9)			Output Data (SDIN2 Slot 12)	

Figure 16. Serial Data Coding and Extraction Options within the TDM Streams

4.5.2 Left Justified and I²S Modes

The serial port of the CS4244 supports the Left Justified and I²S interface formats with valid bit depths of 16, 18, 20, or 24 bits for the SDOUTx pins and 24 bits for the SDINx pins. All data is valid on the rising edge of SCLK. Data is clocked out of the ADC on the falling edge of SCLK and clocked into the DAC on the rising edge. In Master Mode each slot is 32 bits wide.

In Left Justified mode (see Figure 17) the data is received or transmitted most significant bit (MSB) first, on the first rising edge of the SCLK occurring after a FS/LRCK edge. The left channel is received or transmitted while FS/LRCK is logic high.

In I²S mode (see Figure 18) the data is received or transmitted most significant bit (MSB) first, on the second rising edge of the SCLK occurring after a FS/LRCK edge. The left channel is received or transmitted while FS/LRCK is logic low.

The AIN1 and AIN2 signals are transmitted on the SDOUT1 pin; the AIN3 and AIN4 signals are transmitted on the SDOUT2 pin. The data on the SDIN1 pin is routed to AOUT1 and AOUT2; the data on the SDIN2 pin is routed to AOUT3 and AOUT4.

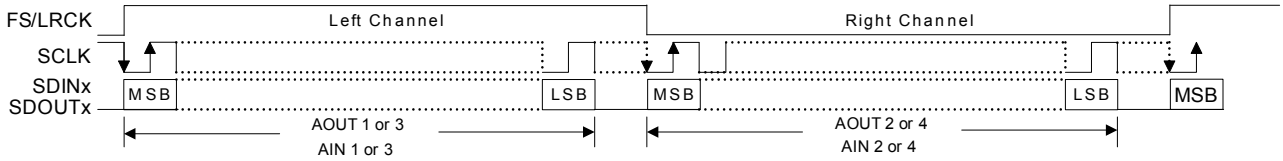


Figure 17. Left Justified Format

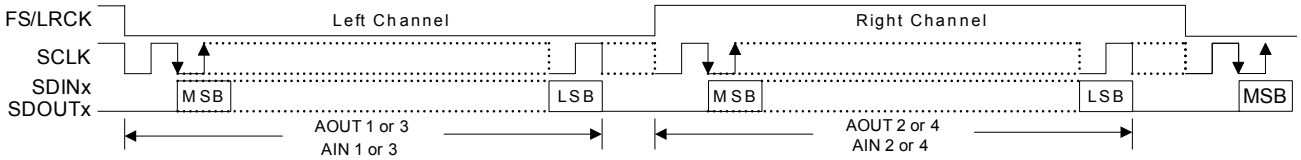


Figure 18. I²S Format

4.6 Internal Signal Path

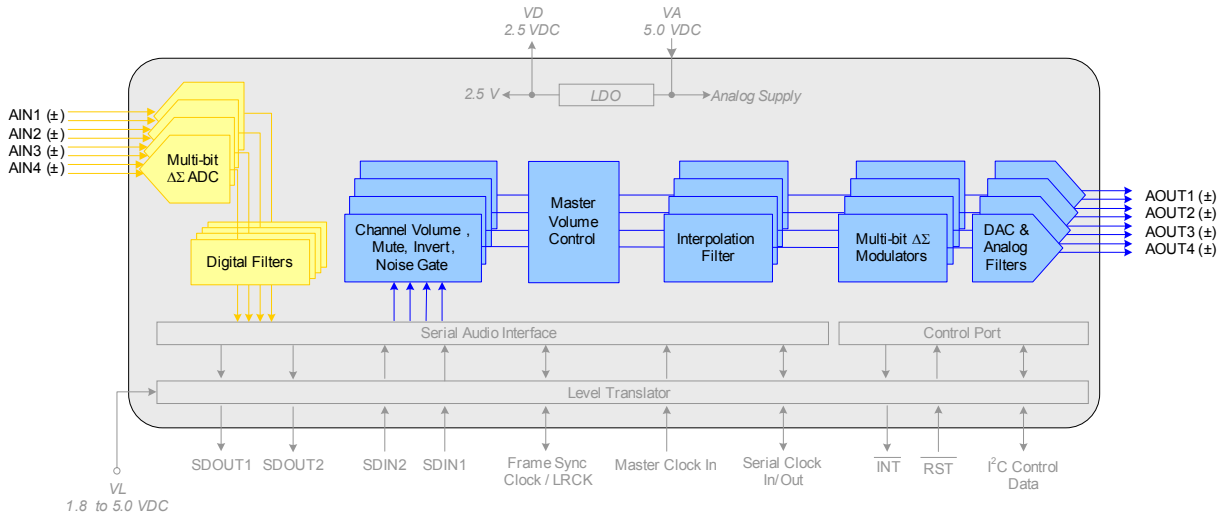


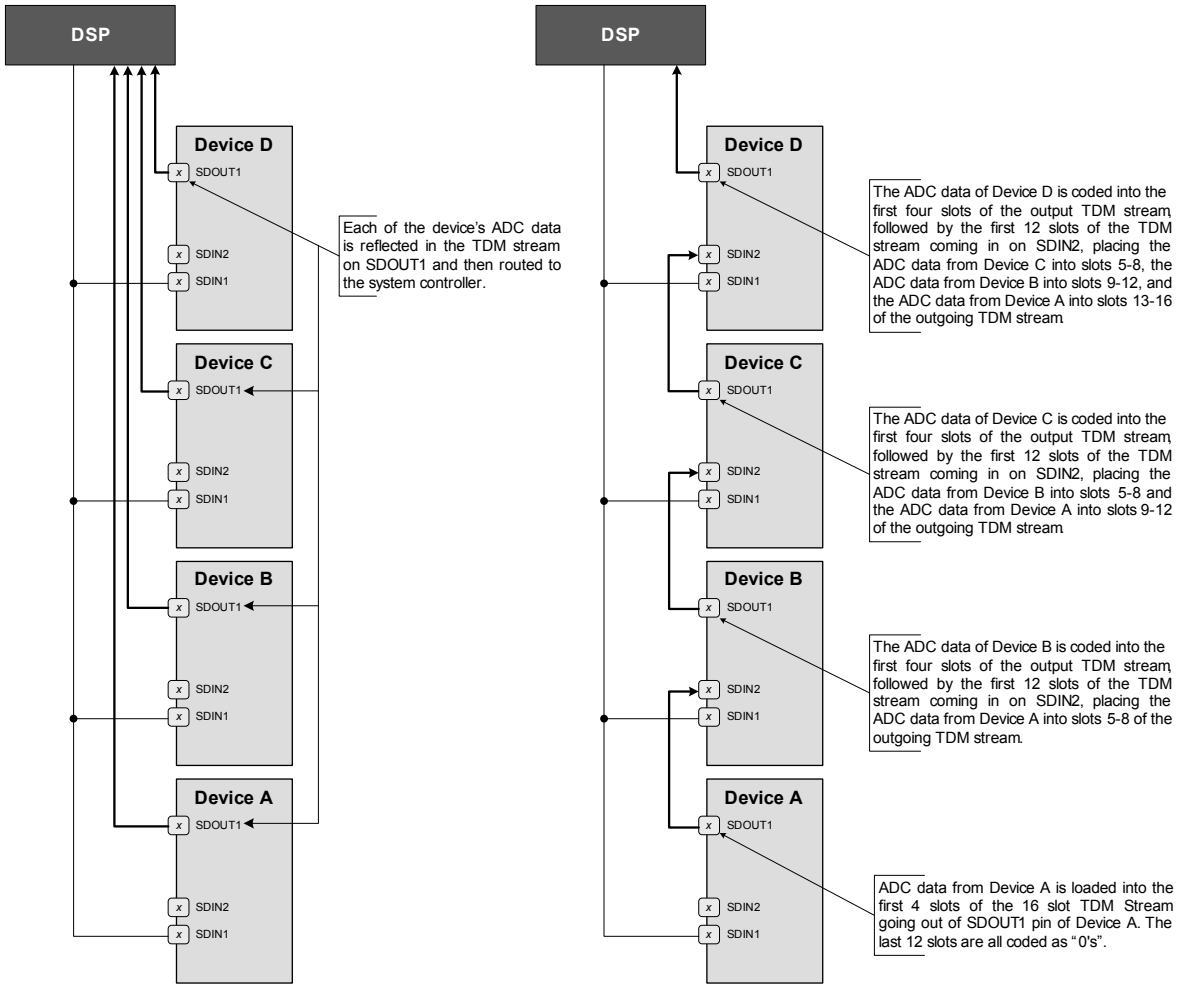
Figure 19. Audio Path Routing

The CS4244 device includes two paths in which audio data can be routed. The analog input path, shown in yellow, allows up to four analog signals to be combined into a single TDM stream on the SDOUT1 pin or output as stereo pairs on the SDOUT1 and SDOUT2 pins. The DAC1-4 path, highlighted in blue, converts serial audio data to analog audio data.

4.6.1 Routing the Serial Data within the Signal Paths

4.6.1.1 ADC Signal Routing

In TDM mode, the CS4244 is designed to load the first four slots of the TDM stream on the SDOUT1 pin with the internal ADC data. Additionally, in order to minimize the number of SDOUT lines that must be run to the system controller in a multiple IC application, the SDOUT data for up to 4 devices can be loaded into a single TDM stream by side chaining the devices together, as shown in Figure 20. To enable the sidechain feature, the “SDO CHAIN” bit in the "SP Control" register must be set.



Note:
This diagram shows the configuration for 16 slot TDM streams. If 8 slot TDM streams are used, two separate serial data lines will need to be connected from the DSP. One would carry the serial data for Devices C&D and the other would carry the serial data for Devices A&B

Figure 20. Conventional SDOUT (Left) vs. Sidechain SDOUT (Right) Configuration

In Left Justified or I²S mode, the CS4244 transmits the AIN1 and AIN2 signals on the SDOUT1 pin and the AIN3 and AIN4 signals on the SDOUT2 pin.

4.6.1.2 DAC1-4 Signal Routing

In TDM mode, the "DAC1-4 SOURCE[2:0]" bits in the "SP Data Sel." register advise the CS4244 where data for the DAC1-4 path is located within the incoming TDM streams. Details for this register and the bit settings can be found in Figures 21 and 22.

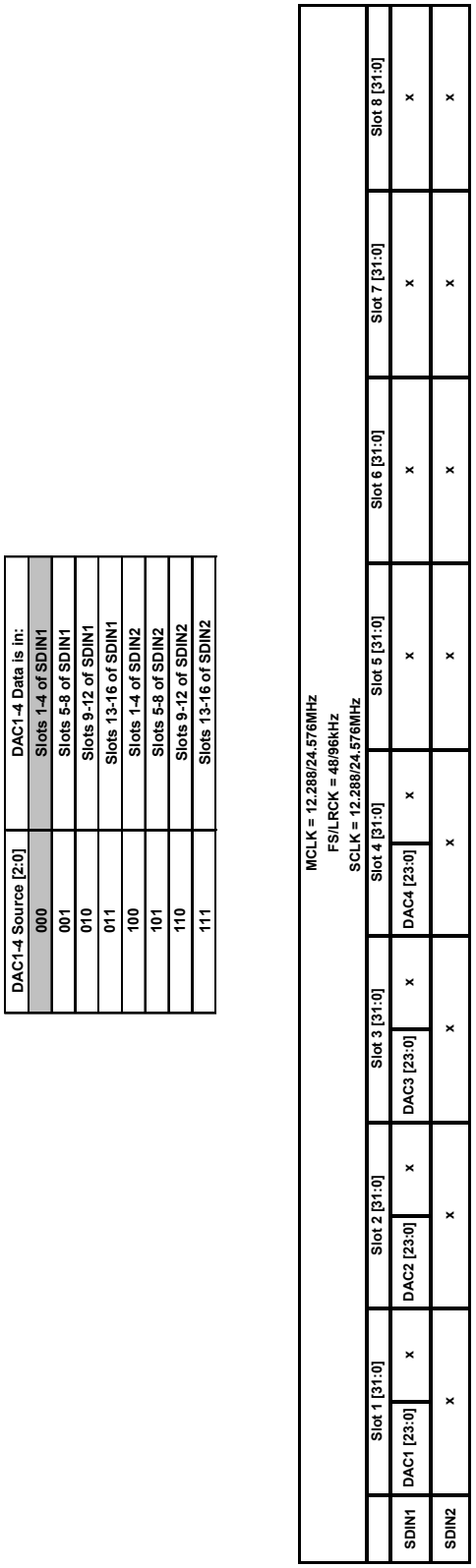
In Left Justified or I²S mode, the CS4244 routes the data on the SDIN1 pin to DAC1 and DAC2 and the data on the SDIN2 pin to DAC3 and DAC4.

DAC1-4 Source [2:0]	DAC1-4 Data is in:
000	Slots 1-4 of SDIN1
001	Slots 5-8 of SDIN1
010	Slots 9-12 of SDIN1
011	Slots 13-16 of SDIN1
100	Slots 1-4 of SDIN2
101	Slots 5-8 of SDIN2
110	Slots 9-12 of SDIN2
111	Slots 13-16 of SDIN2

MCLK = 12.288/24.576MHz FS/LRCK = 48/96kHz SCLK = 12.288/24.576MHz								
SDIN1	Slot 1 [31:0]	Slot 2 [31:0]	Slot 3 [31:0]	Slot 4 [31:0]	Slot 5 [31:0]	Slot 6 [31:0]	Slot 7 [31:0]	Slot 8 [31:0]
SDIN2	Slot 1 [31:0]	Slot 2 [31:0]	Slot 3 [31:0]	Slot 4 [31:0]	Slot 5 [31:0]	Slot 6 [31:0]	Slot 7 [31:0]	Slot 8 [31:0]

MCLK = 24.576MHz FS/LRCK = 48kHz SCLK = 24.576MHz											
SDIN1	Slot 1 [31:0]	...→...	Slot 4 [31:0]	Slot 5 [31:0]	...→...	Slot 8 [31:0]	Slot 9 [31:0]	...→...	Slot 12 [31:0]	Slot 13 [31:0]	...→...	Slot 16 [31:0]
SDIN2	Slot 1 [31:0]		Slot 4 [31:0]	Slot 5 [31:0]		Slot 8 [31:0]	Slot 9 [31:0]		Slot 12 [31:0]	Slot 13 [31:0]		Slot 16 [31:0]

Figure 21. DAC1-4 Serial Data Source Selection



DAC1-4 Source [2:0]	DAC1-4 Data is in:
000	Slots 1-4 of SDIN1
001	Slots 5-8 of SDIN1
010	Slots 9-12 of SDIN1
011	Slots 13-16 of SDIN1
100	Slots 1-4 of SDIN2
101	Slots 5-8 of SDIN2
110	Slots 9-12 of SDIN2
111	Slots 13-16 of SDIN2

Figure 22. Example Serial Data Source Selection

4.6.2 ADC Path

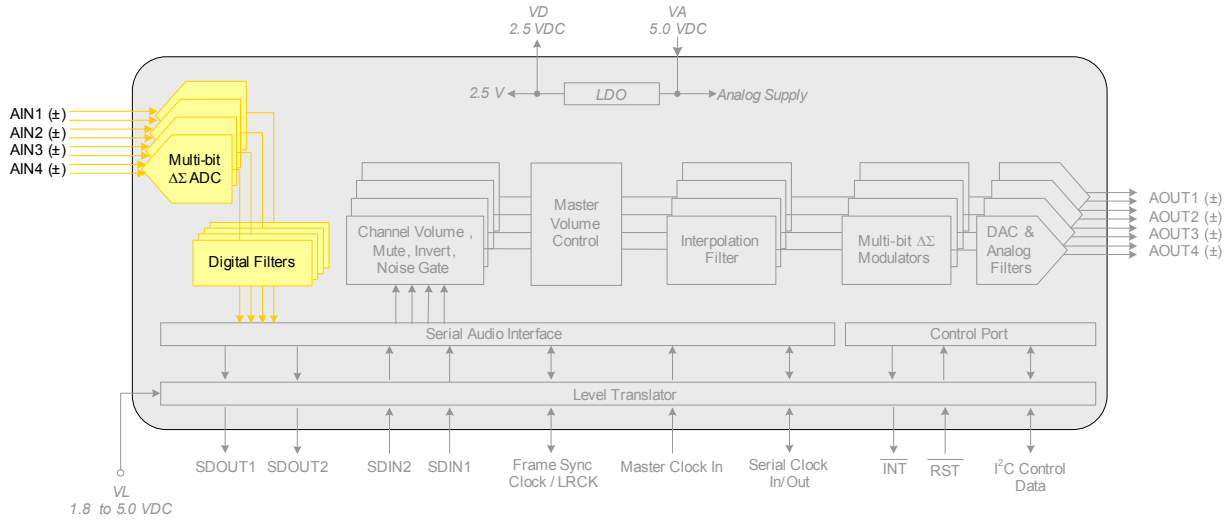


Figure 23. ADC Path

4.6.2.1 Analog Inputs

AINx+ and AINx- are line-level differential analog inputs. The analog input pins do not self-bias and must be externally biased to VA/2 to avoid clipping of the input signal. The full-scale analog input levels are scaled according to VA and can be found in the Analog Input Characteristics tables on pages 12 and 13.

The ADC output data is in two's complement binary format. For inputs above positive full scale or below negative full scale, the ADC will output 7FFFFFH or 800000H, respectively, and cause the ADC Overflow bit in the Interrupt Notification 1 register to be set to a '1'.

4.6.2.2 Active ADC Input Filter

The analog modulator samples the input at 6.144 MHz (internal MCLK = 12.288 MHz). The digital filter will reject signals within the stopband of the filter. However, there is no rejection for input signals which are multiples of the digital passband frequency (n × 6.144 MHz), where n = 0,1,2,... Refer to Figure 24 for a recommended analog input filter that will attenuate any noise energy at 6.144 MHz, in addition to providing the optimum source impedance for the modulators. The use of capacitors that have a large voltage coefficient (such as general-purpose ceramics) must be avoided since these can degrade signal linearity.

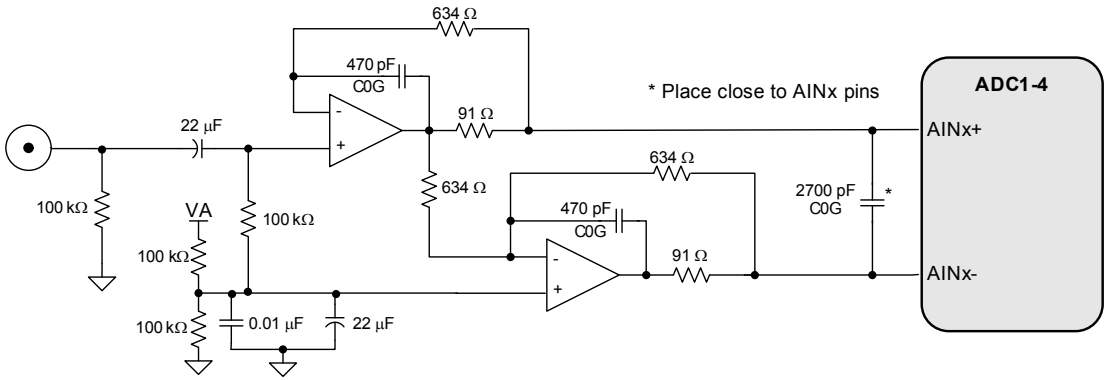


Figure 24. Single-Ended to Differential Active Input Filter

4.6.2.3 ADC HPF

The ADC path contains an optional HPF which can be enabled or disabled for all four ADCs via the "ENABLE HPF" bit in the "ADC Control 1" register. The HPF should only be disabled when the DC component of the input signal needs to be preserved in the digital output data. The HPF characteristics are given in the ADC Digital Filter Characteristics table and plotted in Section 7. The Analog Input Characteristics tables on pages 12 and 13 specify the DC offset error when the HPF is enabled or disabled.

The following figure shows how the recommended single-ended to differential active input filter (Figure 24) can be modified to allow for DC coupled inputs when the HPF is disabled. Note that the voltage swing should not exceed the ADC full-scale input specification.

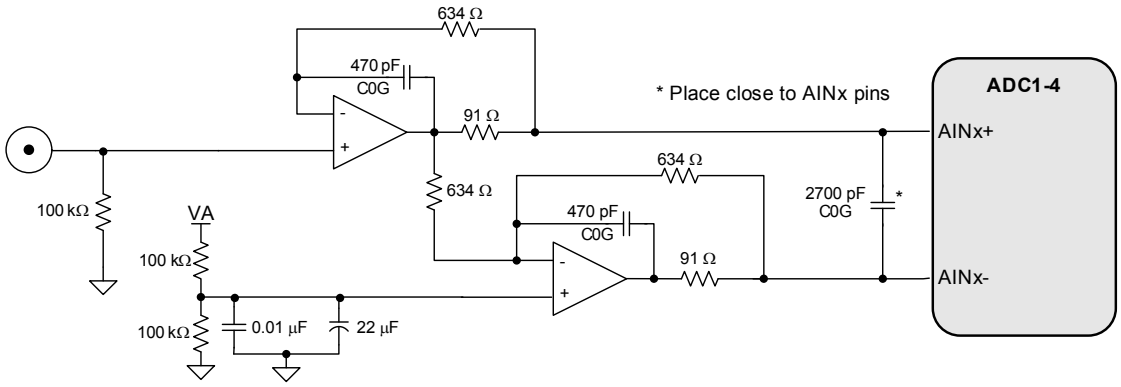


Figure 25. Single-Ended to Differential Active Input Filter - DC Coupled Input Signal (VA/2 Centered)

4.6.3 DAC1-4 Path

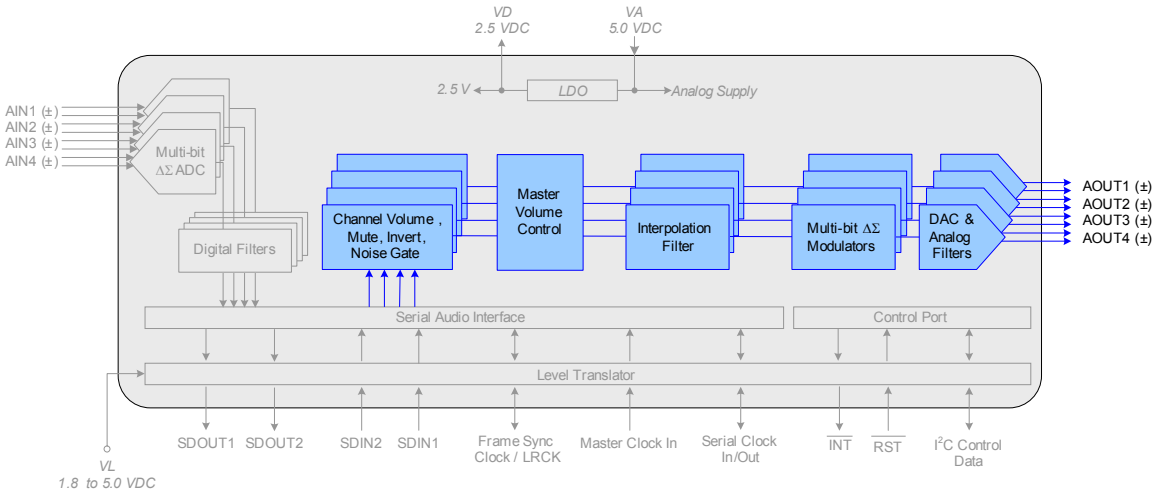


Figure 26. DAC1-4 Path

The AOUT1-4 signals are driven by the data placed into the DAC1-4 path. This data can be placed into the DAC1-4 path via the DAC1-4 Data Source settings in the control port. These settings allow the input source to be selected from any of the up to 32 slots of data on the incoming TDM streams on SDIN1 and SDIN2.

The DAC1-4 path also includes individual channel mutes. Separate volume controls are available for each channel, along with a master volume control that simultaneously attenuates all four channels. The master volume attenuation is added to any channel attenuation that is applied.

4.6.3.1 De-emphasis Filter

The CS4244 includes on-chip digital de-emphasis for 32, 44.1, and 48 kHz sample rates. It is not supported for 96 kHz or for any settings in Double-speed Mode. The filter response is adjusted to be appropriate for a particular base rate by the Base Rate Advisory bits. This filter response, shown in Figure 27, will vary if these bits are not set appropriately for the given base rate. The frequency response of the de-emphasis curve scales proportionally with changes in sample rate, F_S. Please see Section 6.9.2 DAC1-4 De-emphasis for de-emphasis control.

The de-emphasis feature is included to accommodate audio recordings that utilize 50/15 μs pre-emphasis equalization as a means of noise reduction.

De-emphasis is only available in Single-speed Mode.

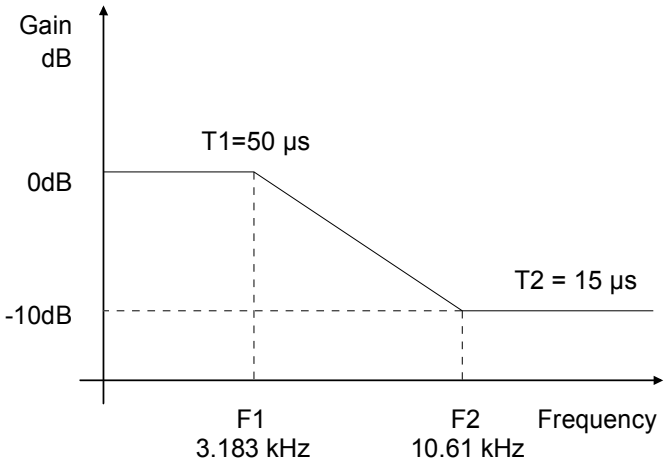


Figure 27. De-emphasis Curve

4.6.4 Analog Outputs

The recommended differential passive output filter is shown below. The filter has a flat frequency response in the audio band while rejecting as much signal energy outside of the audio band as possible. The filter has a single-pole high-pass filter to AC-couple the output signal to the load and a single-pole low-pass filter to attenuate high-frequency energy resulting from the CS4244 DAC's noise shaping function.

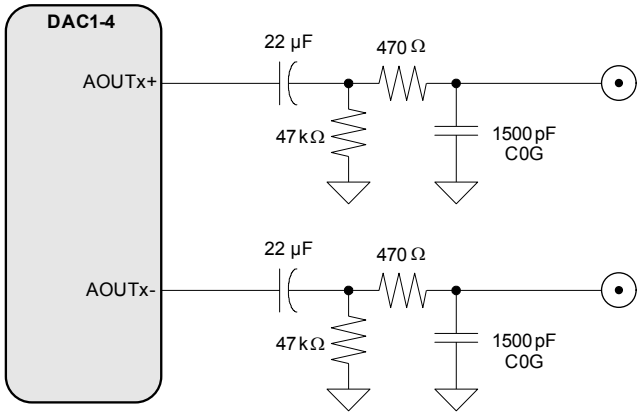


Figure 28. Passive Analog Output Filter

4.6.5 Volume Control

The CS4244 includes a volume control for the DAC1-4 signal path. The implementation details for the volume control and other associated peripheries for DAC1-4 is shown in Figure 29 below. Digital volume steps, adjustable noise gating, muting, and soft ramping are provided on each DAC channel.

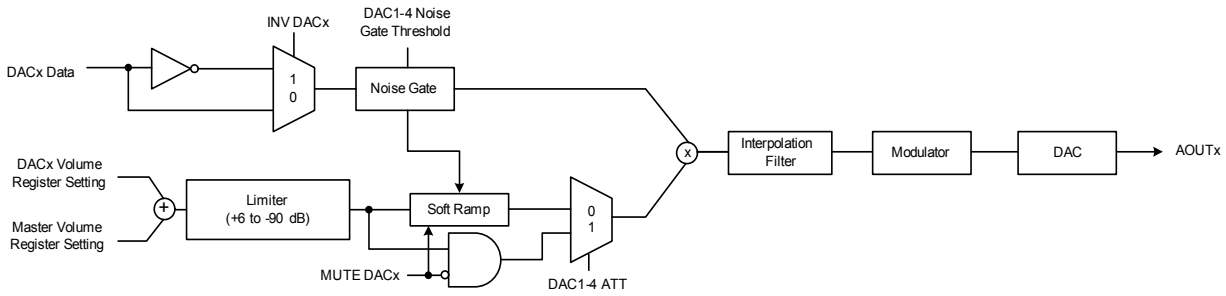


Figure 29. Volume Implementation for the DAC1-4 Path

4.6.5.1 Mute Behavior

Each DAC channel volume is controlled by the sum (in dB) of the individual channel volume and the master volume registers. The channel and master volume control registers have a range of +6 dB to -90 dB with a nominal resolution of $^{6.02}/_{16}$ dB per each bit, which is approximately 0.4 dB. The sum of the two volume settings is limited to a range of +6 dB to -90 dB. Any volume setting below this range will result in infinite attenuation thus muting the channel.

A DAC channel may alternatively be muted by using the mute register bits, the power down bits, or the Noise Gate feature. For any case when the mute engages (volume is less than -90 dB, power down bit is set, mute bit is set, or Noise Gate is engaged), the CS4244 will mute the channel immediately or soft-ramp the volume down at a rate specified by the MUTE DELAY[1:0] bits depending on the settings of the DAC1-4 ATT. bit in the "DAC Control 3" register. This behavior also applies when unmuting a channel.

4.6.5.2 Soft Ramp

The CS4244 soft ramp feature (enabled using the DAC1-4 ATT. bit) is activated on mute and unmute transitions as well as any normal volume register changes. To avoid any potential audible artifacts due to the soft ramping, the volume control algorithm implements the ramping function differently based upon how the user attempts to control the volume.

If the user changes the volume in distant discrete steps such as what would happen if a button were pressed on a user interface to temporarily add attenuation to or mute a channel, then the volume is ramped from the current setting to the new setting at a constant rate set by the MUTE DELAY[1:0] bits.

Alternatively, if the user controls the volume through a knob or slider interface, a volume envelope is sampled at a slow, not-necessarily uniform rate (typically 1-20 Hz) and sent to the CS4244. In this case the ramping algorithm detects a short succession of volume changes attempting to track the volume envelope and dynamically adjusts the soft-ramp rate.

If the CS4244 were to use a constant ramp rate between the volume changes it receives, its output volume envelope may either lag behind the user-generated envelope if the ramp rate is set too low (possibly not reaching the peaks and dulling the envelope) or the output volume envelope may cause a stair-case effect resulting in audible zipper noise if the ramp rate is set too high. By instead adapting the soft-ramp rate to fit the envelope given by the incoming volume samples, the envelope lag time is limited and the zipper

noise is avoided. In this mode the soft ramp algorithm linearly interpolates the volume between the volume changes. There is a lag of one volume change sample since two samples are required to calculate the first ramp rate.

See Figure 30 for the soft ramp diagram. On the first volume sample received, the CS4244 only detects the possible beginning of a volume envelope sequence and resets an envelope counter. The volume starts ramping to the new volume setting at a constant rate controlled by the MUTE DELAY[1:0] setting. If the envelope counter times out before a new volume sample is received, the next received sample is treated in the same way as the previous sample and the ramp rate is kept constant. In this way, as long as the volume samples are distant from each other by more than the envelope counter time out, the rate is kept constant resulting in the soft-ramp behavior described in the button-press example.

However if the next volume sample is received before the envelope counter times out, then it is assumed to be part of a volume envelope sequence. The envelope counter is reset and as long as new samples are received in succession before a time out occurs, the sequence is continued. Starting at the second volume sample of an envelope sequence, the ramp rate is adjusted using the equation shown in Figure 30.

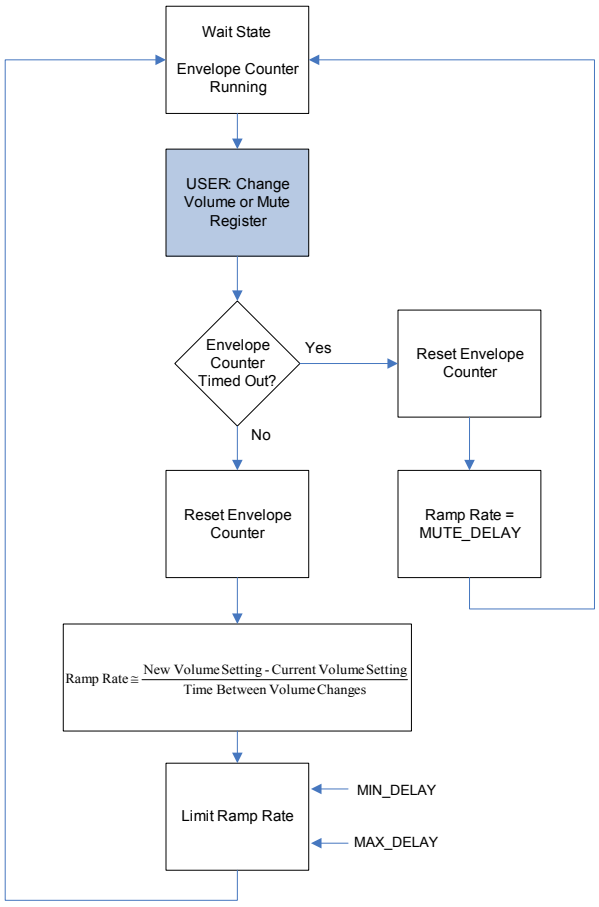


Figure 30. Soft Ramp Behavior

Two control parameters allow the user to limit the ramp-rate range to achieve optimum effect. The MIN DELAY[2:0] setting limits the maximum ramp rate; higher values will introduce more lag in the envelope tracking while providing a smoother ramp. The MAX DELAY[2:0] setting limits the minimum ramp rate; lower values will permit closer tracking of the envelope but may re-introduce zipper noise. The default values of these registers are recommended as a starting point. It is possible to disable the volume envelope

tracking and always produce a constant ramp rate. To accomplish this, set the MIN DELAY[2:0] and MAX DELAY[2:0] values to match the MUTE DELAY[1:0] setting.

The envelope counter time out period which defines the boundary between the two soft-ramping behaviors depends on the base rate. It is equal to approximately 100,000/Fs.

The MUTE DELAY[1:0], MIN DELAY[2:0], and MAX DELAY[2:0] bits specify a delay equal to a multiple of the base period between volume steps of $^{6.02}/_{64}$ dB, which is approximately 0.1 dB. This is the internal resolution of the volume control engine. Consequently the soft-ramp rate can be expressed in ms/dB as shown in Table 6.

	Fs = 48 kHz or 96 kHz (Base = 48 kHz)			Fs = 32 kHz or 64 kHz (Base = 32 kHz)		
Ramp Rate	Time to Ramp to Full Scale (ms)	Time to Ramp 6 dB (ms)	ms/dB	Time to Ramp to Full Scale (ms)	Time to Ramp 6 dB (ms)	ms/dB
1 x Base	21.33	1.33	0.22	32	2	0.33
2 x Base	42.67	2.67	0.44	64	4	0.66
4 x Base	85.33	5.33	0.89	128	8	1.33
8 x Base	170.67	10.67	1.77	256	16	2.66
16 x Base	341.33	21.33	3.54	512	32	5.32
32 x Base	682.67	42.67	7.09	1024	64	10.63
64 x Base	1365.33	85.33	14.17	2048	128	21.26
128 x Base	2730.67	170.67	28.35	4096	256	42.52

Table 6. Soft Ramp Rates

Full-scale ramp is 96 dB (-90 dB to +6 dB)

4.6.5.3 Noise Gate

The CS4244 is equipped with a Noise Gate feature that mutes the output if the signal drops below a given bit depth for 8192 samples. While the enabling or disabling of the Noise Gate feature is done for the entire DAC1-4 output path, each of the channels within the path have separate monitoring circuitry that will trigger the Noise Gate function independently of the other channels. For instance, if the Noise Gate were enabled for and one of the channels were to exhibit a pattern of more than 8192 samples of either all “1’s” or all “0’s”, the output for that particular channel would be muted (and subsequently unmuted), independently of the other channels. To enable the Noise Gate feature, set the DAC1-4 NG[2:0] bits to the desired bit depth. The available bit depth settings are shown in Table 7.

DAC1-4 NG[2:0] Setting	Channel is muted after “x” bits
000	Upper 13 Bits (-72 dB)
001	Upper 14 Bits (-78 dB)
010	Upper 15 Bits (-82 dB)
011	Upper 16 Bits (-90 dB)
100	Upper 17 Bits (-94 dB)
101	Upper 18 Bits (-102 dB)
110	Upper 24 Bits (-138 dB)
111	Noise Gate Disabled

Table 7. Noise Gate Bit Depth Settings

When the upper “x” bits, as dictated by the DAC1-4 NG[2:0] settings, are either all “1’s” or all “0’s” for 8192 consecutive samples, the Noise Gate will engage for that channel. Setting these bits to ‘111’ will disable the Noise Gate feature. If the Noise Gate feature engages, it will transition into and out of mute as dictated by the DAC1-4 ATT. bit in the "DAC Control 3" register.

4.7 Reset Line

The reset line of the CS4244 is used to place the device into a reset condition. In this condition, all of the values of the CS4244 control port are set to their default values. This mode of operation is the lowest power mode of operation for the CS4244 and should be used whenever the device is not operating in order to save power. During the power up and power down sequence, it is often necessary for the CS4244 devices to be placed into (and taken out of) reset at a different moment in time than the amplifiers to which they are connected in order to minimize audible clicks and pops during the sequence. For this reason, it is advisable to run separate reset lines for each type of device, i.e. one reset line for the CS4244 devices and one for the amplifier devices.

4.8 Error Reporting and Interrupt Behavior

The CS4244 is equipped with a suite of error reporting and protection. The types of errors that are detected, the notification method for these errors, and the steps needed to clear the errors are detailed in Table 8.

It is important to note that the interrupt notification bits for all of the errors are triggered on the edge of the occurrence of the event. They are not level-triggered and therefore do not indicate the presence of an error in real time. This means that, a “1” in the error’s respective field inside the Interrupt Notification register only indicates that the error has occurred since the last time the register was cleared and not necessarily that the error is currently occurring.

Name of Error	Event(s) that Caused the Error	Outputs Muted Upon Occurrence?	All PDNx bits must be set and then cleared to resume normal operation?
Disallowed Test Mode Entry (Note 35)	Device has entered test mode due to an errant I²C write.	No	No
Serial Port Error	FS/LRCK, or SCLK has become invalid.	Yes	Yes
Clocking Error	The speed mode which the device is receiving is different than the speed mode set in the SPEED MODE bits, or the PLL is unlocked from input signal.	Yes	Yes
ADCx Overflow	ADC inputs are larger than the permitted full scale signal.	No	No (Normal operation will continue but audible distortion will occur.)
DACx Clip	DAC output level is larger than the available rail voltage.	No	No Normal operation will continue but audible distortion will occur.

Table 8. Error Reporting and Interrupt Behavior Details

Note:

35. This error is provided to aid in trouble shooting during software development. Entry into the test mode of the device may cause permanent damage to the device and should not be done intentionally.

4.8.1 Interrupt Masking

An occurrence of any of the errors mentioned above will cause the interrupt line to engage in order to notify the system controller that an error has occurred. If it is preferred that the error not cause the interrupt line to engage, this error can be masked in its respective mask register. It is important to note that, in the event of an error, the interrupt notification bit for the respective error will reflect the occurrence of the event, regardless of the setting of the mask bit. Setting the mask bit only prevents the interrupt pin from being flagged upon the occurrence.

4.8.2 Interrupt Line Operation

As mentioned previously, the interrupt line of the CS4244 will be pulled low or high (depending on the settings of the “INT PIN[1:0]” bits in the "Interrupt Control" register) after an interrupt condition occurs, provided that the event is not masked in the mask register. If the CS4244’s interrupt line is to be connected onto a single bus with other devices, it is advisable to use it in the open drain mode of operation. If no other devices are connected to the interrupt line, it may be used in the CMOS mode of operation. When used in the open drain configuration, it is necessary to connect a pull-up resistor to this net, which will ensure a known state on the net when no error is present. Please refer to the typical connection diagram for the appropriate pull-up resistor value.

4.8.3 Error Reporting and Clearing

In the event of an error, the interrupt line will be engaged - provided the mask bit for that error is not set. When the interrupt notification registers are read to determine the source of the error, the mask bit for whichever error occurred will be set automatically by the CS4244. The system controller should begin to take corrective action to clear the error. Once the error has been cleared, the system controller should clear the mask bit in the appropriate mask register to ensure that a subsequent occurrence of the error will cause the interrupt line to engage appropriately. This behavior is detailed in Figure 31 on page 45.

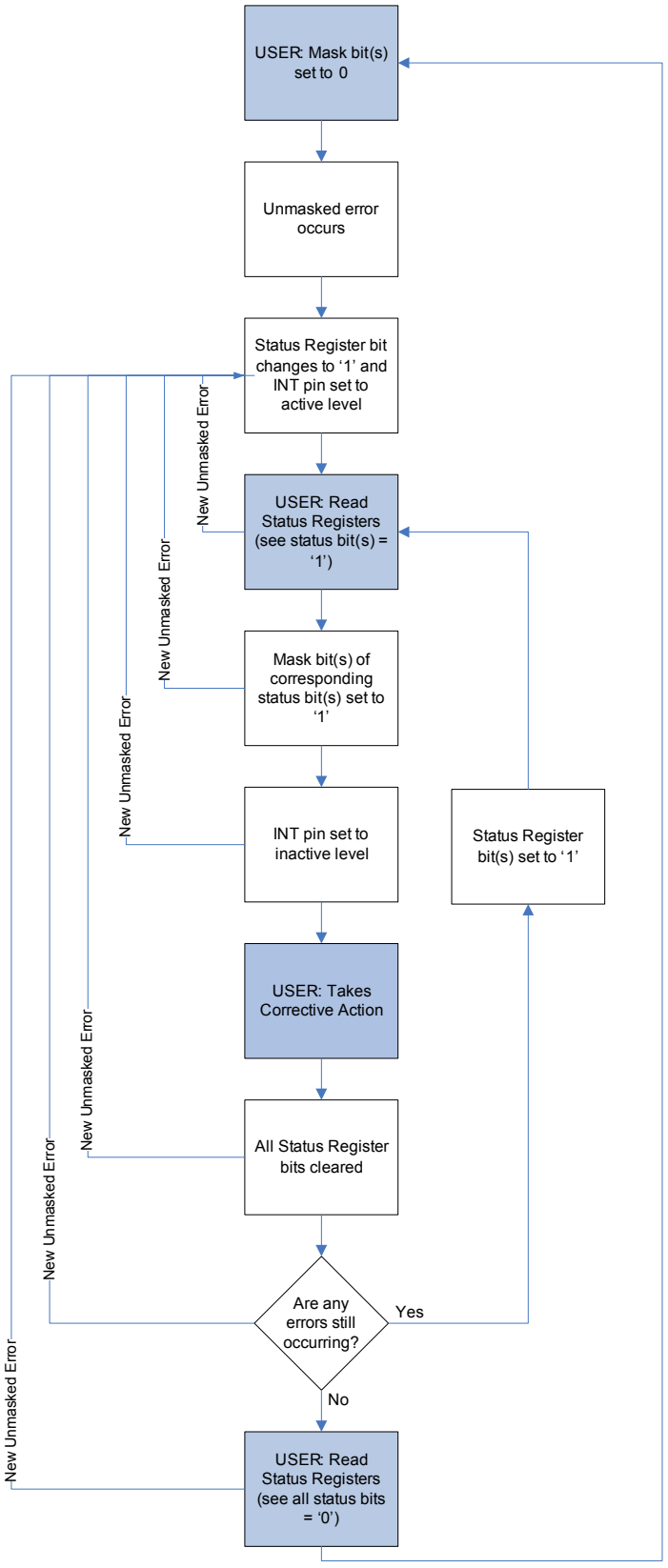


Figure 31. Interrupt Behavior and Example Interrupt Service Routine

5. REGISTER QUICK REFERENCE

Default values are shown below the bit names.

AD	Function	7	6	5	4	3	2	1	0
		(Read Only Bits are shown in Italics)							
01h p 48	Device ID A & B	*DEV. ID A[3:0]* 0	1	0	0	*DEV. ID B[3:0]* 0	0	1	0
02h p 48	Device ID C & D	*DEV. ID C[3:0]* 0	0	1	1	*DEV. ID D[3:0]* 0	1	0	0
03h p 48	Device ID E & F	*DEV. ID E[3:0]* 0	0	0	0	*DEV. ID F[3:0]* 0	0	0	0
04h	Variant ID	Reserved [3:0] 0	0	0	0	Reserved [3:0] 0	0	0	0
05h p 48	Revision ID	*ALPHA REV. ID[3:0]* x	x	x	x	*NUMERIC REV. ID[3:0]* x	x	x	x
06h p 49	Clock & SP Sel.	BASE RATE[1:0] 0	0	SPEED MODE[1:0] 0	0	MCLK RATE[2:0] 0	1	0	Reserved 0
07h p 50	Sample Width Sel.	SDOUTx SW[1:0] 1	1	INPUT SW[1:0] 1	1	Reserved[1:0] 1	1	Reserved[1:0] 1	1
08h p 50	SP Control	INV SCLK 0	Reserved[2:0] 1	0	0	SP FORMAT[1:0] 1	0	SDO CHAIN 0	MSTR/SLV 0
09h p 51	SP Data Sel.	Reserved 0	Reserved 0	DAC1-4 SOURCE[2:0] 0	0	0	Reserved[2:0] 0	0	1
0Ah	Reserved	Reserved[7:0] 1	1	1	1	1	1	1	1
0Bh	Reserved	Reserved[7:0] 1	1	1	1	1	1	1	1
0Ch	Reserved	Reserved[7:0] 1	1	1	1	1	1	1	1
0Dh	Reserved	Reserved[7:0] 1	1	1	1	1	1	1	1
0Eh	Reserved	Reserved 0	Reserved[2:0] 0	0	0	Reserved[3:0] 0	0	0	0
0Fh p 52	ADC Control 1	Reserved 1	Reserved 1	VA_SEL 0	ENABLE HPF 0	INV. ADC4 0	INV. ADC3 0	INV. ADC2 0	INV. ADC1 0
10h p 52	ADC Control 2	MUTE ADC4 1	MUTE ADC3 1	MUTE ADC2 1	MUTE ADC1 1	PDN ADC4 1	PDN ADC3 1	PDN ADC2 1	PDN ADC1 1
11h	Reserved	Reserved[2:0] 1	1	1	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
12h p 53	DAC Control 1	DAC1-4 NG[2:0] 1	1	1	DAC1-4 DE 0	Reserved 0	Reserved 0	Reserved 0	0
13h p 53	DAC Control 2	Reserved[2:0] 1	1	1	Reserved 0	INV. DAC4 0	INV. DAC3 0	INV. DAC2 0	INV. DAC1 0
14h p 54	DAC Control 3	Reserved 1	DAC1-4 ATT. 0	Reserved 1	Reserved 1	MUTE DAC4 1	MUTE DAC3 1	MUTE DAC2 1	MUTE DAC1 1
15h p 54	DAC Control 4	VQ RAMP 0	Reserved[1:0] 0	0	Reserved 1	PDN DAC4 1	PDN DAC3 1	PDN DAC2 1	PDN DAC1 1

AD	Function	7	6	5	4	3	2	1	0
(Read Only Bits are shown in Italics)									
16h p 55	Volume Mode	MUTE DELAY[1:0] 1	 0	MIN DELAY[2:0] 0	 0	 0	MAX DELAY[2:0] 1	 1	 1
17h p 56	Master Volume	MASTER VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
18h p 56	DAC1 Volume	DAC1 VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
19h p 56	DAC2 Volume	DAC2 VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
1Ah p 56	DAC3 Volume	DAC3 VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
1Bh p 56	DAC4 Volume	DAC4 VOLUME[7:0] 0	 0	 0	 1	 0	 0	 0	 0
1Ch	Reserved	Reserved[7:0] 0	 0	 0	 1	 0	 0	 0	 0
1Dh	Reserved	Reserved[3:0] 1	 0	 1	 1	Reserved[3:0] 1	 0	 1	 0
1Eh p 56	Interrupt Control	INT MODE 0	INT PIN[1:0] 1	 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0	Reserved 0
1Fh p 57	Interrupt Mask 1	MASK TST MODE ERR 0	MASK SP ERR 0	MASK CLK ERR 0	Reserved 1	MASK ADC4 OVFL 0	MASK ADC3 OVFL 0	MASK ADC2 OVFL 0	MASK ADC1 OVFL 0
20h p 58	Interrupt Mask 2	Reserved 0	Reserved 0	Reserved 1	Reserved 0	MASK DAC4 CLIP 0	MASK DAC3 CLIP 0	MASK DAC2 CLIP 0	MASK DAC1 CLIP 0
21h p 58	Interrupt Notification 1	*TST MODE* x	*SP ERR* x	*CLK ERR* x	*Reserved* x	*ADC4 OVFL* x	*ADC3 OVFL* x	*ADC2 OVFL* x	*ADC1 OVFL* x
22h p 59	Interrupt Notification 2	*Reserved* x	*Reserved* x	*Reserved* x	*Reserved* x	*DAC4 CLIP* x	*DAC3 CLIP* x	*DAC2 CLIP* x	*DAC1 CLIP* x

6. REGISTER DESCRIPTIONS

All registers are read/write unless otherwise stated. All “Reserved” bits must maintain their default state. Default values are shaded.

6.1 Device I.D. A–F (Address 01h–03h) *(Read Only)*

7	6	5	4	3	2	1	0
DEV. ID A[3:0]				DEV. ID B[3:0]			
7	6	5	4	3	2	1	0
DEV. ID C[3:0]				DEV. ID D[3:0]			
7	6	5	4	3	2	1	0
DEV. ID E[3:0]				DEV. ID F[3:0]			

6.1.1 Device I.D. (Read Only)

Device I.D. code for the CS4244. Example:.

DEV. ID A[3:0]	DEV. ID B[3:0]	DEV. ID C[3:0]	DEV. ID D[3:0]	DEV. ID E[3:0]	DEV. ID F[3:0]	Part Number
4h	2h	3h	4h	0h	0h	CS4244

6.2 Revision I.D. (Address 05h) *(Read Only)*

7	6	5	4	3	2	1	0
AREVID3	AREVID2	AREVID1	AREVID0	NREVID3	NREVID2	NREVID1	NREVID0

6.2.1 Alpha Revision (Read Only)

CS4244 Alpha (silicon) revision level.

AREVID[3:0]	Alpha Revision Level
Ah	A
...	...

6.2.2 Numeric Revision (Read Only)

CS4244 Numeric (metal) revision level.

NREVID[3:0]	Numeric Revision Level
0h	0
...	...

Note: The Alpha and Numeric revision I.D. are used to form the complete device revision I.D. Example: A0, A1, B0, B1, B2, etc.

6.3 Clock & SP Select (Address 06h)

7	6	5	4	3	2	1	0
BASE RATE[1:0]		SPEED MODE[1:0]		MCLK RATE[2:0]			Reserved

6.3.1 Base Rate Advisory

Advises the CS4244 of the base rate of the incoming base rate. This allows for the de-emphasis filters to be adjusted appropriately. The CS4244 includes on-chip digital de-emphasis for 32, 44.1, and 48 kHz base rates. It is not supported for 96 kHz or for any settings in Double Speed Mode.

BASE RATE	Base Rate is:
00	48 kHz
01	44.1 kHz
10	32 kHz
11	Reserved

6.3.2 Speed Mode

Sets the speed mode in which the CS4244 will operate..

SPEED MODE	Speed Mode is:
00	Single Speed Mode
01	Double Speed Mode
10	Reserved
11	Auto Detect (Slave Mode only)

6.3.3 Master Clock Rate

Sets the rate at which the master clock is entering the CS4244. Settings are given in “x” multiplied by the incoming sample rate, as MCLK must scale directly with incoming sample rate.

MCLK RATE	MCLK is:
000	$256xF_S$ in Single Speed Mode or $128xF_S$ in Double Speed Mode
001	$384xF_S$ in Single Speed Mode or $192xF_S$ in Double Speed Mode
010	$512xF_S$ in Single Speed Mode or $256xF_S$ in Double Speed Modex
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Reserved

6.4 Sample Width Select (Address 07h)

7	6	5	4	3	2	1	0
SDOUTx SW[1:0]		INPUT SW[1:0]		Reserved[1:0]		Reserved[1:0]	

6.4.1 Output Sample Width

These bits set the width of the samples placed into the outgoing SDOUTx streams.

OUTPUT SW	Sample Width is:
00	16 bits
01	18 bits
10	20 bits
11	24 bits

Note: Bits wider than the Output Sample Width setting are cleared within the SDOUTx data stream.

6.4.2 Input Sample Width

These bits set the width of the samples coming into the CS4244 through the SDINx TDM streams.

INPUT SW	Sample Width is:
00	16 bits
01	18 bits
10	20 bits
11	24 bits

Note: In Left Justified or I²S mode, the Input Sample Width is fixed to 24 bits.

6.5 Serial Port Control (Address 08h)

7	6	5	4	3	2	1	0
INV SCLK	Reserved[2:0]			SP FORMAT[1:0]		SDO CHAIN	MASTER/ SLAVE

6.5.1 Invert SCLK

When set, this bit inverts the polarity of the SCLK signal.

INV SCLK	SCLK is:
0	Not Inverted
1	Inverted

6.5.2 Serial Port Format

Sets the format of both the incoming serial data signals and outgoing serial data signals.

SP FORMAT	Format is:
00	Left Justified
01	I²S
10	TDM (Slave Mode Only)
11	Reserved

6.5.3 Serial Data Output Sidechain

Setting this bit enables the SDOUT1 side chain feature. In this mode, the samples from multiple devices can be coded into one TDM stream. See Section 4.6.2 ADC Path for details.

SDO CHAIN	Sidechain is:
0	Disabled
1	Enabled

6.5.4 Master/Slave

Setting this bit places the CS4244 in master mode, clearing it places it in slave mode.

MASTER/SLAVE	CS4244 is in:
0	Slave Mode
1	Master Mode

Note: I²S and Left Justified are the only serial port formats available if the CS4244 is in Master Mode.

6.6 Serial Port Data Select (Address 09h)

7	6	5	4	3	2	1	0
Reserved	Reserved	DAC1-4 SOURCE[2:0]			Reserved[2:0]		

6.6.1 DAC1-4 Data Source

Sets which portion of data is to be routed to the DAC1-4 data paths.

DAC1-4 SOURCE	Data is routed into the DAC1-4 path from:
000	Slots 1-4 of the TDM stream on SDIN1
001	Slots 5-8 of the TDM stream on SDIN1
010	Slots 9-12 of the TDM stream on SDIN1
011	Slots 13-16 of the TDM stream on SDIN1
100	Slots 1-4 of the TDM stream on SDIN2
101	Slots 5-8 of the TDM stream on SDIN2
110	Slots 9-12 of the TDM stream on SDIN2
111	Slots 13-16 of the TDM stream on SDIN2

6.7 ADC Control 1 (Address 0Fh)

7	6	5	4	3	2	1	0
Reserved	Reserved	VA_SEL	ENABLE HPF	INV. ADC4	INV. ADC3	INV. ADC2	INV. ADC1

6.7.1 VA Select

Scales internal operational voltages appropriately for VA level. Configuring this bit appropriately for the VA voltage level used in the application is imperative to ensure proper operation of the device.

VA_SEL	Must be set when VA is:
0	3.3 VDC
1	5 VDC

6.7.2 Enable High-pass Filter

Enables high-pass filter for the ADC path.

ENABLE HPF	High Pass Filter is:
0	Disabled
1	Enabled

6.7.3 Inv. ADCx

Inverts the polarity of the ADCx signal.

INV. ADCx	ADCx Polarity is:
0	Not Inverted
1	Inverted

6.8 ADC Control 2 (Address 10h)

7	6	5	4	3	2	1	0
MUTE ADC4	MUTE ADC3	MUTE_ADC2	MUTE ADC1	PDN ADC4	PDN ADC3	PDN ADC2	PDN ADC1

6.8.1 Mute ADCx

Mutes the ADCx signal

MUTE ADCx	ADC is:
0	Not Muted
1	Muted

6.8.2 Power Down ADCx

Powers down the ADCx path.

PDN ADCx	ADC is:
0	Powered Up
1	Powered Down

6.9 DAC Control 1 (Address 12h)

7	6	5	4	3	2	1	0
DAC1-4 NG			DAC1-4 DE	Reserved	Reserved	Reserved	

6.9.1 DAC1-4 Noise Gate

This sets the bit depth at which the Noise Gate feature should engage for the DAC1-4 path.

DAC1-4 NG[2:0]	Noise Gate is set at: [b]
000	Upper 13 Bits (72 dB)
001	Upper 14 Bits (78 dB)
010	Upper 15 Bits (84 dB)
011	Upper 16 Bits (90 dB)
100	Upper 17 Bits (96 dB)
101	Upper 18 Bits (102 dB)
110	Upper 24 Bits (138 dB)
111	Noise Gate Disabled

6.9.2 DAC1-4 De-emphasis

Enables or disables de-emphasis for the DAC1-4 path. See Section 4.6.3.1 for details. The CS4244 includes on-chip digital de-emphasis for 32, 44.1, and 48 kHz base rates. It is not supported for 96 kHz or for any settings in Double-speed Mode.

DAC1-4 DE	De-emphasis is:
0	Disabled
1	Enabled

6.10 DAC Control 2 (Address 13h)

7	6	5	4	3	2	1	0
Reserved[2:0]			Reserved	INV. DAC4	INV. DAC3	INV. DAC2	INV. DAC1

6.10.1 Inv. DACx

Inverts the polarity of the DACx signal.

INV. DACx	DACx Polarity is:
0	Not Inverted
1	Inverted

6.11 DAC Control 3 (Address 14h)

7	6	5	4	3	2	1	0
Reserved	DAC1-4 ATT	Reserved	Reserved	MUTE DAC4	MUTE DAC3	MUTE DAC2	MUTE DAC1

6.11.1 DAC1-4 Attenuation

Sets the mode of attenuation used for the DAC1-4 path.

DAC1-4 ATT	Attenuation events happen:
0	On a soft ramp
1	Immediately

Note: Please see Section 4.6.5 Volume Control for more details regarding the attenuation modes.

6.11.2 Mute DACx

Mutes the DACx signal.

MUTE DACx	DACx is:
0	Not Muted
1	Muted

6.12 DAC Control 4 (Address 15h)

7	6	5	4	3	2	1	0
VQ RAMP	Reserved[1:0]		Reserved	PDN DAC4	PDN DAC3	PDN DAC2	PDN DAC1

6.12.1 VQ Ramp

Ramps common mode voltage “VQ” down to ground. This bit needs to be set before asserting reset pin.

VQ RAMP	Effect:
0	VQ is set at nominal level (VA/2)
1	VQ is ramped from nominal level to ground.

6.12.2 Power Down DACx

Powers down the DACx path.

PDN DACx	DACx is:
0	Powered Up
1	Powered Down

6.13 Volume Mode (Address 16h)

7	6	5	4	3	2	1	0
MUTE DELAY[1:0]		MIN DELAY[2:0]			MAX DELAY[2:0]		

6.13.1 Mute Delay

Sets the delay between the volume steps during muting and unmuting of a signal when attenuation mode is set to soft ramp. Each step of the ramp is equal to $^{6.02}/_{64}$ dB ~= 0.094 dB. Settings are given as "x" times the base period.

MUTE DELAY	Delay is:
00	1x
01	4x
10	16x
11	64x

6.13.2 Minimum Delay

Sets the minimum delay before each volume transition. Settings are given in "x" times the base period. See Section 4.6.5 Volume Control for more details regarding the operation of the volume control.

MIN DELAY	Minimum Delay is:
000	1x
001	2x
010	4x
011	8x
100	16x
101	32x
110	64x
111	128x

6.13.3 Maximum Delay

Sets the maximum delay before the volume transition. Settings are given in "x" times the base period. See Section 4.6.5 Volume Control for more details regarding the operation of the volume control.

MAX DELAY	Maximum Delay is:
000	1x
001	2x
010	4x
011	8x
100	16x
101	32x
110	64x
111	128x

6.14 Master and DAC1-4 Volume Control (Address 17h, 18h, 19h, 1Ah, & 1Bh)

7	6	5	4	3	2	1	0
x VOLUME[7:0]							

6.14.1 x Volume Control

Sets the level of the x Volume Control. Each volume step equals $^{6.02}/_{16}$ dB ~= 0.38 dB. See Section 4.6.5.1 on page 40 for the muting behavior of these volume registers.

x VOLUME	x Volume is: [dB]
00000000	+6.02
00001111	+0.38
00010000	0
00010001	-0.38
00011000	-3.01
...	...
11111110	-89.55 (most total attenuation before mute)
11111111	-89.92 (least total attenuation before unmute)

6.15 Interrupt Control (Address 1Eh)

7	6	5	4	3	2	1	0
INT MODE	INT POL [1:0]		Reserved	Reserved	Reserved	Reserved	Reserved

6.15.1 INT MODE

Sets the behavior mode of the interrupt registers of the device. In the default configuration, if the interrupt notification registers are read and any error is found to have occurred since the last clearing of that register, the device will automatically set the corresponding mask bit in the appropriate mask register. In the nondefault configuration, mask bits are not set automatically.

INT MODE	Upon the reading of an error out of the interrupt notification bits, the CS4244 will:
0	Automatically set the corresponding mask bit.
1	Not set the corresponding mask bit.

6.15.2 Interrupt Pin Polarity

Sets the output mode of the interrupt pin.

INT POL	Output mode of the interrupt pin is:
00	Active High
01	Active Low
10	Active Low/Open Drain
11	Reserved

6.16 Interrupt Mask 1 (Address 1Fh)

7	6	5	4	3	2	1	0
MASK TST MODE ERR	MASK SP ERR	MASK CLK ERR	Reserved	MASK ADC4 OVFL	MASK ADC3 OVFL	MASK ADC2 OVFL	MASK ADC1 OVFL

6.16.1 Test Mode Error Interrupt Mask

Controls whether a Test Mode Error event flags the interrupt pin. A test mode error occurs when an inadvertent I²C write places the device in test mode.

MASKTSTMOD ERR	In the event of a Test Mode Error event, Interrupt Pin will:
0	Be Flagged
1	Not be flagged

6.16.2 Serial Port Error Interrupt Mask

Controls whether the interrupt pin if flagged when any of the following parameters are changed without first powering down the device (i.e., setting all Power Down ADCx and Power Down DACx bits):

- Serial Port Format: SP FORMAT[1:0]
- Speed Mode: SPEED MODE (In slave mode, changing the MCLK/F_S ratio without powering down the device, flags this error and the Clocking Error. In master mode, changing MCLK frequency without the device being powered down does not flag this or the Clocking Error since MCLK/F_S does not change.)
- Master/Slave: MSTR/SLV

MASK SP ERR	In the event of a Serial Port Error event, Interrupt Pin will:
0	Be Flagged
1	Not be flagged

6.16.3 Clocking Error Interrupt Mask

Allows or prevents a Clocking Error event from flagging the interrupt pin. See Section 4.8 for details.

MASK CLK ERR	In the event of a Clocking Error event, Interrupt Pin will:
0	Be Flagged
1	Not be flagged

6.16.4 ADCx Overflow Interrupt Mask

Allows or prevents an ADCx Overflow event from flagging the interrupt pin.

MASK ADCx OVFL	In the event of an ADCx Overflow event, Interrupt Pin will:
0	Be Flagged
1	Not be flagged

6.17 Interrupt Mask 2 (Address 20h)

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	MASK DAC4 CLIP	MASK DAC3 CLIP	MASK DAC2 CLIP	MASK DAC1 CLIP

6.17.1 DACx Clip Interrupt Mask

Allows or prevents a DACx Clip event from flagging the interrupt pin.

MASK DACx CLIP	In the event of a DACx Clip event, Interrupt Pin will:
0	Be Flagged
1	Not be flagged

6.18 Interrupt Notification 1 (Address 21h) *(Read Only)*

7	6	5	4	3	2	1	0
TST MODE ERR	SP ERR	CLK ERR	Reserved	ADC4 OVFL	ADC3 OVFL	ADC2 OVFL	ADC1 OVFL

6.18.1 Test Mode Error

A Test Mode Error has occurred since the last clearing of the Interrupt Notification register.

TSTMOD ERR	Since the last clearing of the Interrupt Notification Register, a Test Mode Error:
0	Has Not Occurred
1	Has Occurred

6.18.2 Serial Port Error

A Serial Port Error has occurred since the last clearing of the Interrupt Notification register.

SP ERR	Since the last clearing of the Interrupt Notification Register, a Serial Port Error:
0	Has Not Occurred
1	Has Occurred

6.18.3 Clocking Error

A Clocking Error has occurred since the last clearing of the Interrupt Notification register.

CLK ERR	Since the last clearing of the Interrupt Notification Register, a Clocking Error:
0	Has Not Occurred
1	Has Occurred

6.18.4 ADCx Overflow

An ADCx Overflow has occurred since the last clearing of the Interrupt Notification register.

ADCx OVFL	Since the last clearing of the Interrupt Notification Register, a ADCx Overflow Error:
0	Has Not Occurred
1	Has Occurred

6.19 Interrupt Notification 2 (Address 22h) *(Read Only)*

7	6	5	4	3	2	1	0
Reserved	Reserved	Reserved	Reserved	DAC4 CLIP	DAC3 CLIP	DAC2 CLIP	DAC1 CLIP

6.19.1 DACx Clip

A DACx Clip has occurred since the last clearing of the Interrupt Notification register.

DACx CLIP	Since the last clearing of the Interrupt Notification Register, a DACx Clip Error:
0	Has Not Occurred
1	Has Occurred

7. ADC FILTER PLOTS

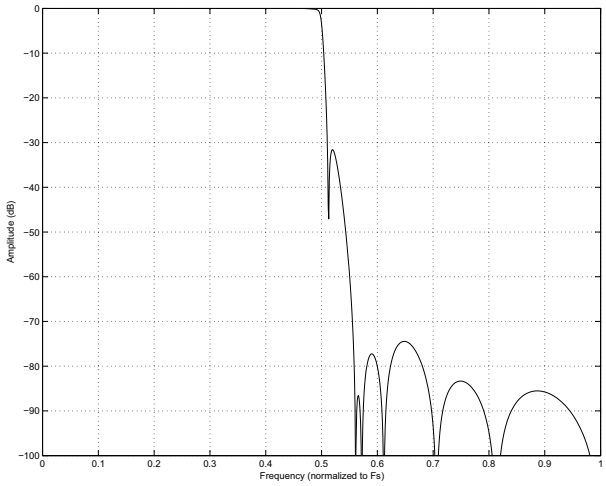


Figure 32. ADC Stopband Rejection

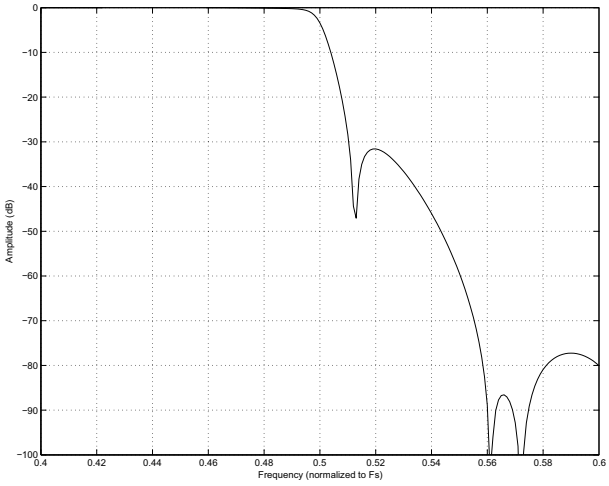


Figure 33. ADC Transition Band

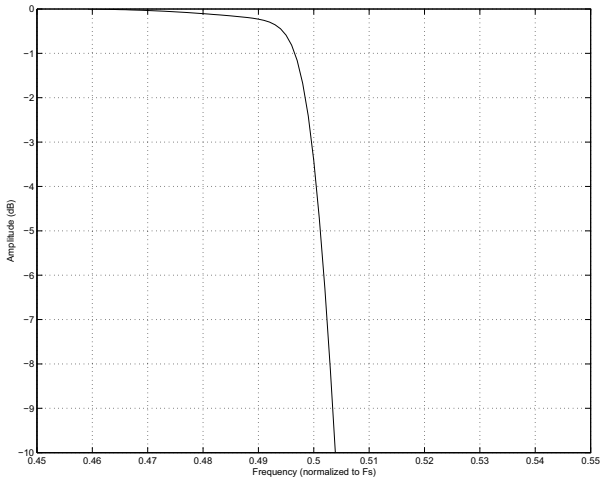


Figure 34. ADC Transition Band (Detail)

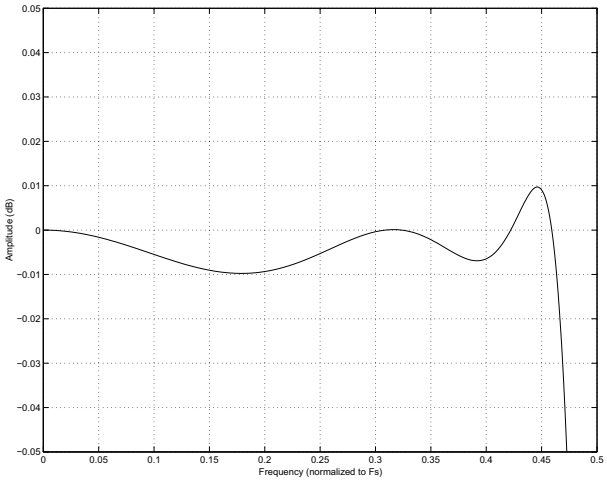


Figure 35. ADC Passband Ripple

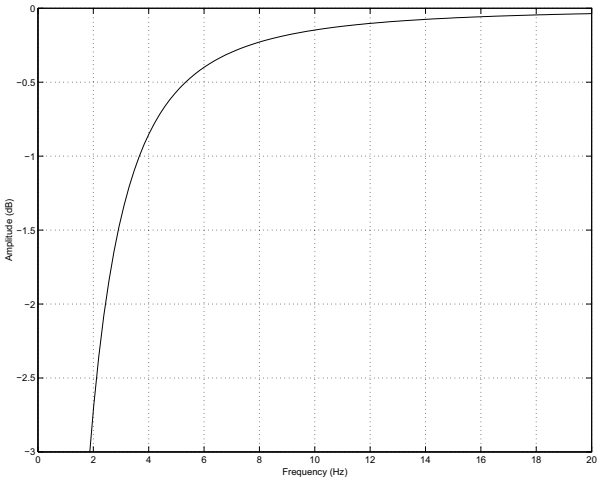


Figure 36. ADC HPF (48 kHz)

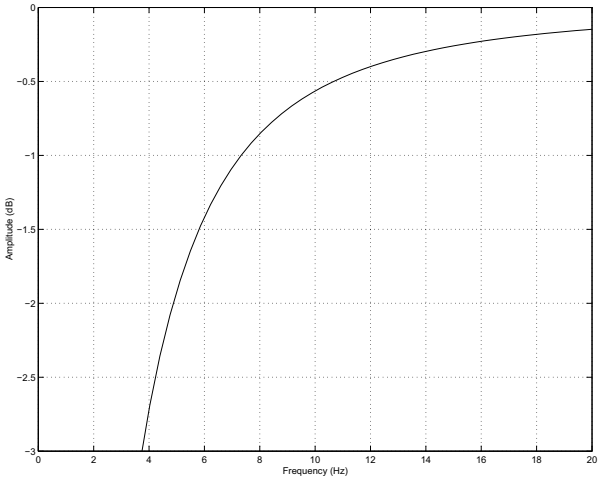


Figure 37. ADC HPF (96 kHz)

8. DAC FILTER PLOTS

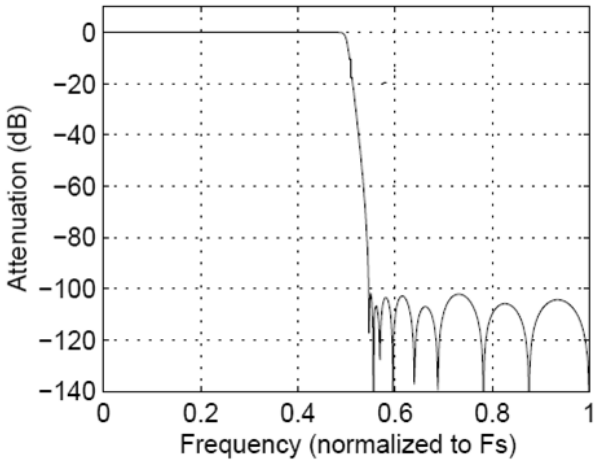


Figure 38. SSM DAC Stopband Rejection

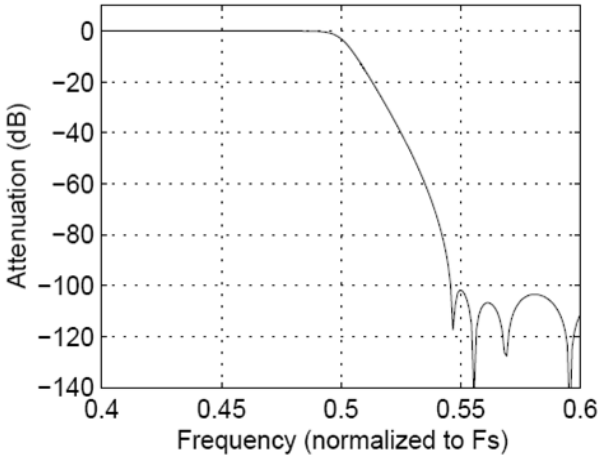


Figure 39. SSM DAC Transition Band

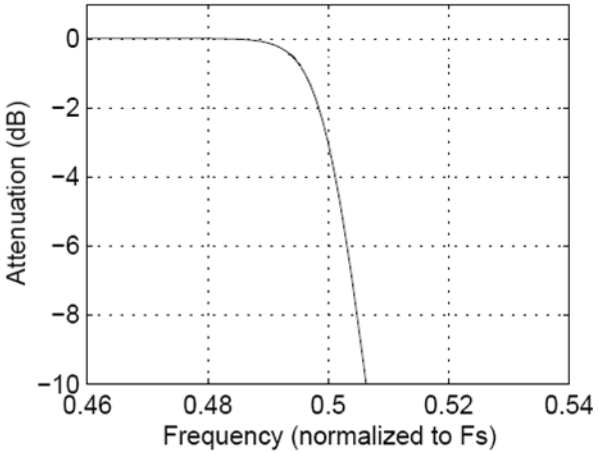


Figure 40. SSM DAC Transition Band (Detail)

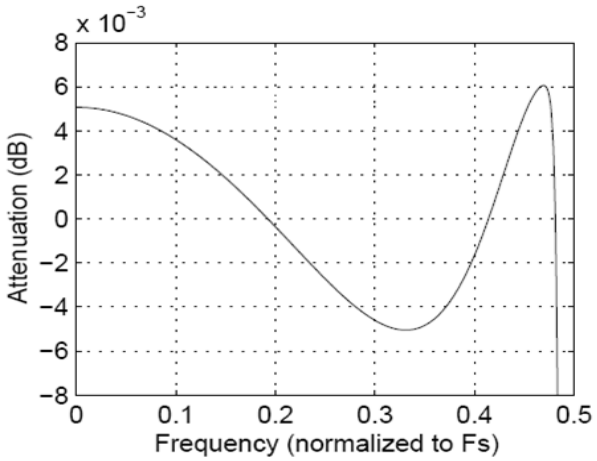


Figure 41. SSM DAC Passband Ripple

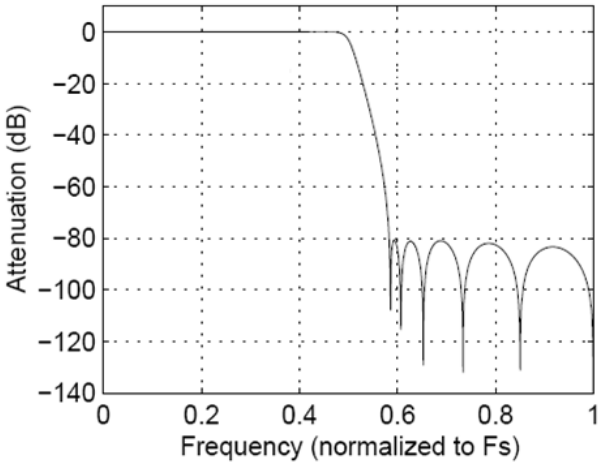


Figure 42. DSM DAC Stopband Rejection

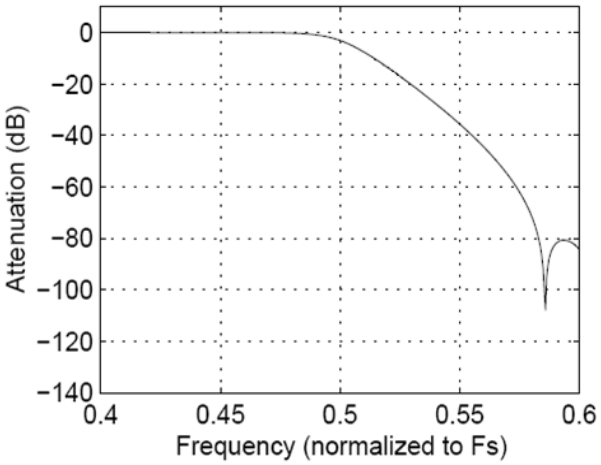


Figure 43. DSM DAC Transition Band

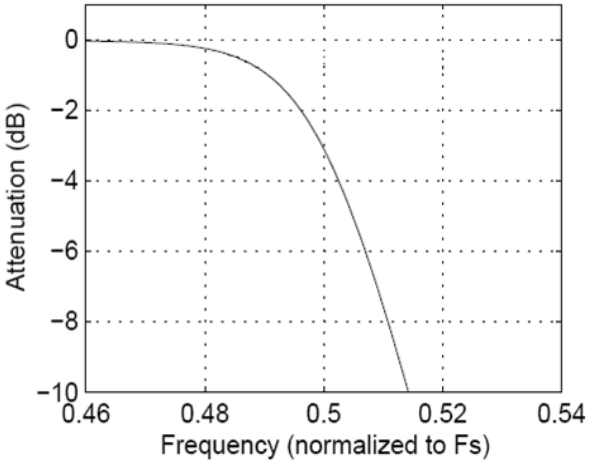


Figure 44. DSM DAC Transition Band (Detail)

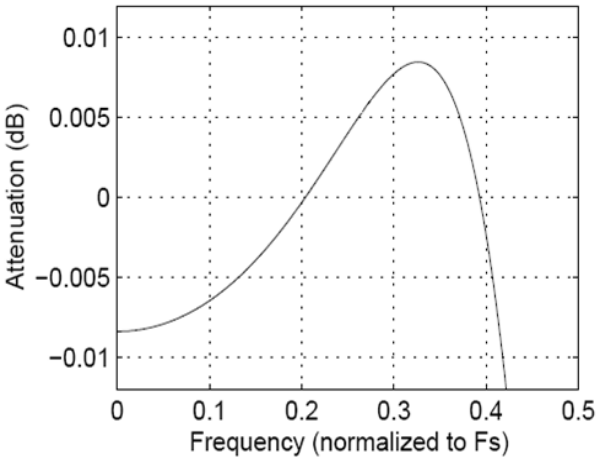


Figure 45. DSM DAC Passband Ripple

9. PACKAGE DIMENSIONS

40L QFN (6 × 6 MM BODY) PACKAGE DRAWING

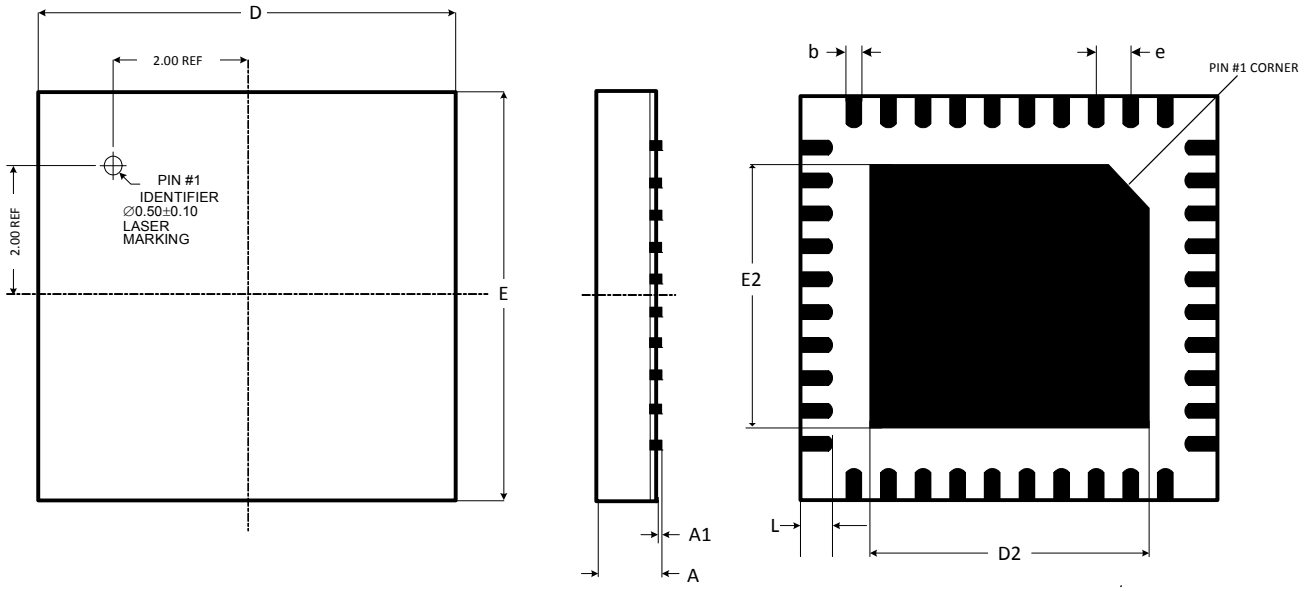


Figure 46. Package Drawing

	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	0.0315	0.0354	0.0354	0.8	0.85	0.9	1
A1	0	0.0014	0.002	0	0.035	0.05	1
b	0.0078	0.0098	0.011	0.2	0.25	0.3	1,2
D		0.2362 BSC			6 BSC		1
D2	0.1594	0.1614	0.1634	4	4.1	4.2	1
E		0.2362 BSC			6 BSC		1
E2	0.1594	0.1614	0.1634	4	4.1	4.2	1
e		0.0197 BSC			0.5 BSC		1
L	0.0118	0.0177	0.0197	0.3	0.45	0.5	1

JEDEC #: MO-220

Controlling Dimension is Millimeters.

Notes: 1. Dimensioning and tolerance per ASME Y4.5M - 1994.

2. Dimensioning lead width applies to the plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.

10.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order#
CS4244	4 In/4 Out CODEC	40-QFN	Yes	Commercial	0° to +70°C	Rail	CS4244-CNZ
						Tape and Reel	CS4244-CNZR
				Automotive	-40° to +85°C	Rail	CS4244-DNZ
						Tape and Reel	CS4244-DNZR
CDB4244	CS4244 Evaluation Board		-	-	-	-	CDB4244

11.REVISION HISTORY

Release	Changes
F1 MAR '12	– Updated the Commercial temperature ranges from -40 to +85°C to 0 to +70°C and the Automotive temperature ranges from -40 to +105°C to -40 to +85°C in the following sections: "General Description" on page 1, "Recommended Operating Conditions" on page 9, "Analog Input Characteristics (Automotive Grade)" on page 13, "ADC Digital Filter Characteristics" on page 15, "Analog Output Characteristics (Automotive Grade)" on page 17, and Section 10. Ordering Information. – Updated PSRR specification in the Analog Input Characteristics (Commercial Grade) and Analog Input Characteristics (Automotive Grade) tables. – Removed note about ADC CM bits in the Analog Input Characteristics (Commercial Grade) and Analog Input Characteristics (Automotive Grade) tables. – Removed T_A test condition from "ADC Digital Filter Characteristics" on page 15. – Added analog input pins must be externally biased to Section 4.6.2.1. – Changed ADC CM bits to reserved in Section 5 and Section 6.6. – Changed part number for automotive grade in Section 10. Ordering Information from ENZ to DNZ.
F2 OCT '14	– Updated dimensions and figure in Section 9. Package Dimensions. (Data sheet change only; no change has been made to the physical device.)

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.