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NTE985
Integrated Circuit
TV Luminance Processor

Description:
The NTE985is a monolithic silicon integrated circuit that performs the luminance processing functions of amplification; contrast, brightness and peaking control; blanking; and black–level clamping.

Features:
- Black–Level Clamping
- Linear DC Controls for Brightness, Contrast and Peaking
- Horizontal and Vertical Blanking
- "Hermetic Chip" Construction
- Silicon Nitride Passivated
- Platinum Silicide Ohmic Contacts
- Operates with Standard or Tapped Delay Line

Absolute Maximum Ratings:
DC Supply Current 57mA
Device Dissipation:
Up to T_A = +55°C 750mW
Above T_A = +55°C . . . . derate linearly 7.9mW/°C
Operating Ambient Temperature Range, T_A . . . . −40° to +85°C
Storage Temperature Range, T_{stg} . . . . −65° to +150°C
Lead Temperature (During Soldering, 1/16" ±1/32" from case, 10sec max), T_L . . . . +265°C

Electrical Characteristics: (T_A = +25°C unless otherwise specified)

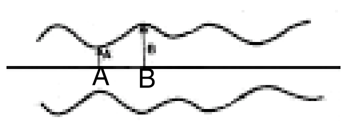
Parameter	Bias Volts	Test Conditions											Limits			Unit
		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	Min	Typ	Max	
		Switching Positions for Characteristics Measurements														
Static Characteristics																
Voltage At Term. 13	6.5	2	1	1	2	2	4	1	2	2	1	1	11	12.3	13.2	V
Quiescent Voltage At Term. 4	6.5	2	1	1	2	2	3	1	2	2	1	1	3.3	4	5.7	V
Quiescent Voltage At Term 7	6.5	2	1	1	2	2	2	1	2	2	1	1	7.1	7.7	8.3	V
Current into Term. 13 (Term 13 Connected to 11V)	6.5	2	1	1	2	2	3	1	2	2	1	2	10	18	30	mA
Dynamic Characteristics																
Wide–Band Gain (Note 1)	7.3	1	1	1	2	1	2	1	1	1	2	1	1	3	5	dB
Contrast Gain Reduction (Note 2)	7.3	1	1	1	2	1	2	1	1	2	2	1	27	30	–	dB
Peaking Gain (Note 1)	7.3	1	1	2	2	1	2	1	1	1	2	1	9	13	17	dB
Peaking Gain Reduction (Note 3)	7.3	1	1	2	2	1	2	1	1	1	2	1	16	18	–	dB
Max. Intermodulation Distortion 3.8V (Note 4)	7.3	1	–	1	1	1	2	–	2	1	2	1	–	20	–	%
5V (Note 5)	7.3	1	–	1	1	1	2	–	2	1	2	1	–	40	–	%

Note 1 Set 50kHz generator for 200mV_{rms}. Adjust R1 Peaking control for minimum setting, measure wide–band gain at terminal 7.

Note 2 Set 50kHz generator for 200mV_{rms}. Adjust R1 for minimum setting, measure contrast gain reduction at terminal 7.

Note 3 Set 50kHz generator for 200mV_{rms}. Adjust R1 for minimum setting, measure peaking gain reduction at terminal 7.

Note 4 Adjust R1 for minimum setting. With S2 at switch position 1 and S7 at switch position 3, set 50kHz generator for 3.8V_{p-p}. Then with S2, set 1MHz generator for 200mV_{rms}. Then with S7 at switch position 2, measure downward modulation of the 1MHz signal due to the 50kHz signal.



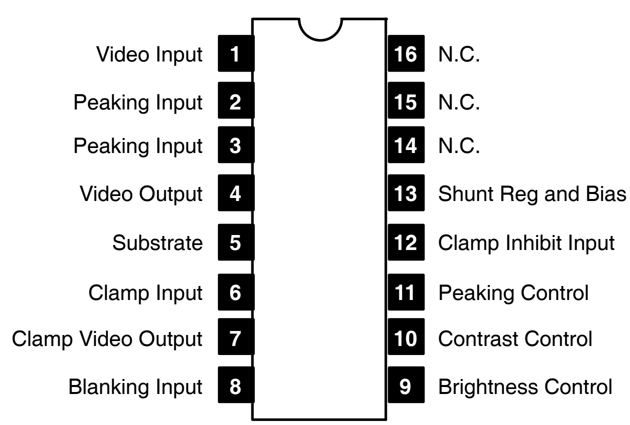
Modulated
I–MHz Signal

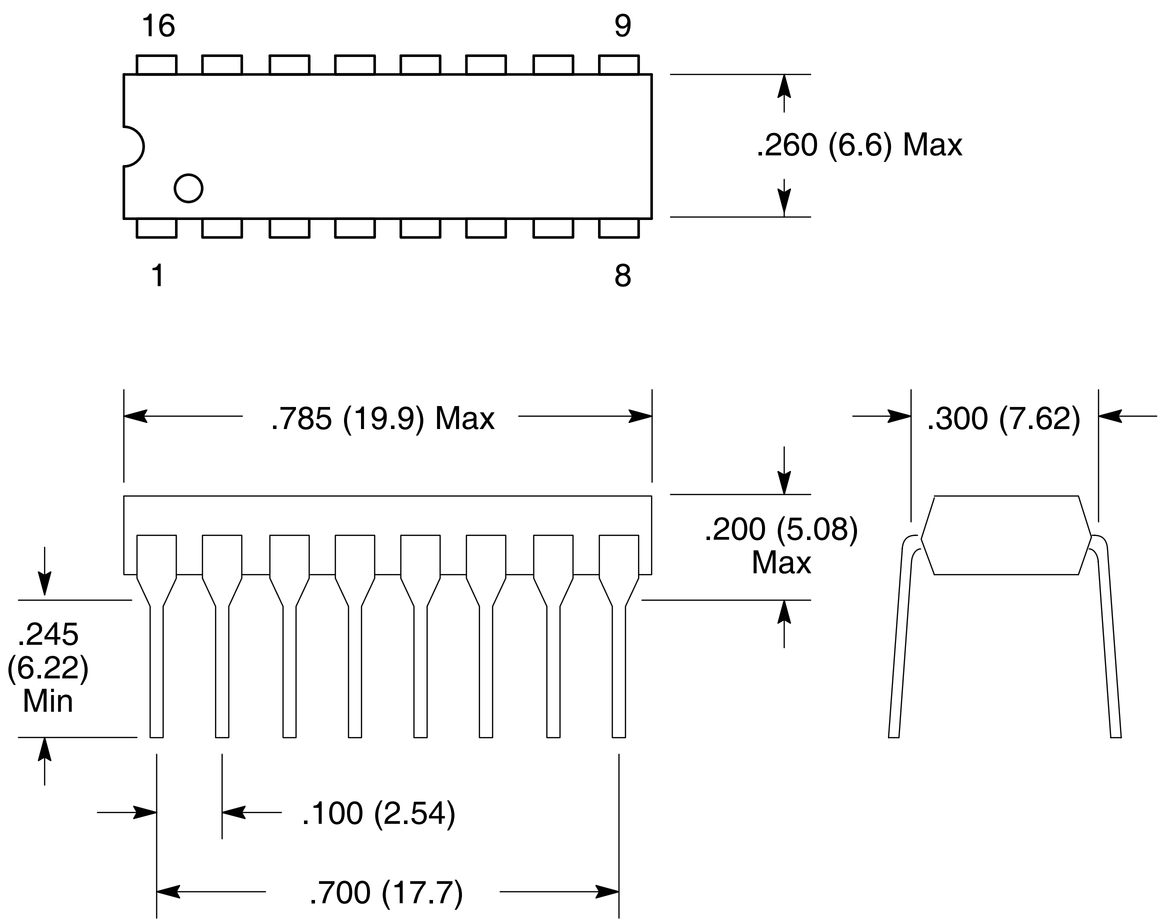
A = Amplitude of 50kHz signal at deepest trough
B = Peak amplitude of 50kHz signal

$$\text{Downward Modulation} = \frac{B-A}{B}$$

Note 5 Repeat step 4 except that the 50kHz generartor must be set at 5V_{p-p}

Pin Connection Diagram




16
9
1
8
.260 (6.6) Max
.785 (19.9) Max
.300 (7.62)
.200 (5.08)
Max
.245
(6.22)
Min
.100 (2.54)
.700 (17.7)