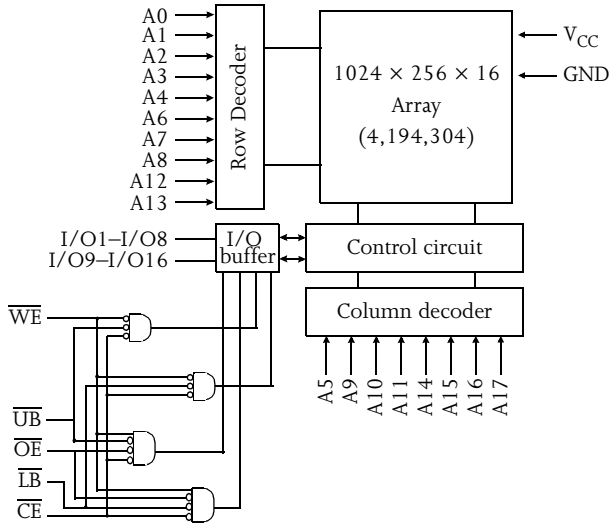
# AS7C4098
# AS7C34098

## 5V/3.3V 256K × 16 CMOS SRAM

## Features

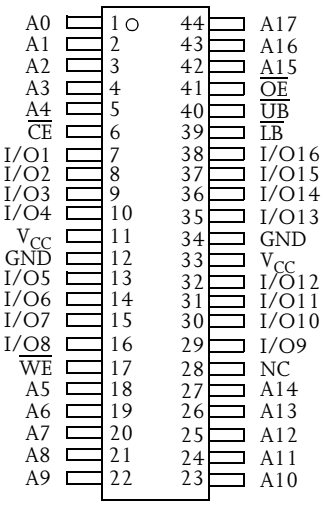
- AS7C4098 (5V version)
- AS7C34098 (3.3V version)
- Industrial and commercial temperature
- Organization: 262,144 words × 16 bits
- Center power and ground pins
- High speed
  - 10/12/15/20 ns address access time
  - 5/6/7/8 ns output enable access time
- Low power consumption: ACTIVE
  - 1375 mW (AS7C4098)/max @ 12 ns
  - 468 mW (AS7C34098)/max @ 12 ns
- Low power consumption: STANDBY
  - 110 mW (AS7C4098)/max CMOS
  - 72 mW (AS7C34098)/max CMOS
- Individual byte read/write controls
- 2.0V data retention
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- TTL- and CMOS-compatible, three-state I/O
- 44-pin JEDEC standard packages
  - 400-mil SOJ
  - 400-mil TSOP II
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

## Logic block diagram




## Pin arrangement

44-pin SOJ, TSOP II (400 mil)




## Selection guide

| | | AS7C34098 −10 | AS7C4098 AS7C34098 −12 | AS7C4098 AS7C34098 −15 | AS7C4098 AS7C34098 −20 | Unit |
|---|---|---|---|---|---|---|
| Maximum address access time | | 10 | 12 | 15 | 20 | ns |
| Maximum output enable access time | | 5 | 6 | 7 | 9 | ns |
| Maximum operating current | AS7C4098 | – | 250 | 220 | 180 | mA |
| | AS7C34098 | 160 | 130 | 110 | 100 | mA |
| Maximum CMOS standby current | AS7C4098 | – | 20 | 20 | 20 | mA |
| | AS7C34098 | 20 | 20 | 20 | 20 | mA |

## Functional description

The AS7C4098 and AS7C34098 are high-performance CMOS 4,194,304-bit Static Random Access Memory (SRAM) devices organized as 262,144 words × 16 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ($t_{AA}$, $t_{RC}$, $t_{WC}$) of 10/12/15/20 ns with output enable access times ($t_{OE}$) of 5/6/7/8 ns are ideal for high-performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is High the device enters standby mode. The standard AS7C4098 is guaranteed not to exceed 110 mW power consumption in CMOS standby mode. Both devices offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O1–I/O16 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) High. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

These devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O1–I/O8, and $\overline{UB}$ controls the higher bits, I/O9–I/O16.

All chip inputs and outputs are TTL- and CMOS-compatible, and operation is from either a single 5V (AS7C4098) or 3.3V (AS7C34098) supply. Both devices are available in the JEDEC standard 400-mL, 44-pin SOJ and TSOP II packages.

## Absolute maximum ratings

| Parameter | Device | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Voltage on $V_{CC}$ relative to GND | AS7C4098 | $V_{t1}$ | −0.50 | +7.0 | V |
| | AS7C34098 | $V_{t1}$ | −0.50 | +5.0 | V |
| Voltage on any pin relative to GND | | $V_{t2}$ | −0.50 | $V_{CC}$ +0.50 | V |
| Power dissipation | | $P_D$ | – | 1.5 | W |
| Storage temperature (plastic) | | $T_{stg}$ | −65 | +150 | °C |
| Ambient temperature with $V_{CC}$ applied | | $T_{bias}$ | −55 | +125 | °C |
| DC current into outputs (low) | | $I_{OUT}$ | – | ±20 | mA |

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{LB}$ | $\overline{UB}$ | I/O1–I/O8 | I/O9–I/O16 | Mode |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | High Z | Standby ($I_{SB}$, $I_{SB1}$) |
| L | H | H | X | X | High Z | High Z | Output disable ($I_{CC}$) |
| L | X | X | H | H | | | |
| L | H | L | L | H | $D_{OUT}$ | High Z | Read ($I_{CC}$) |
| | | | H | L | High Z | $D_{OUT}$ | |
| | | | L | L | $D_{OUT}$ | $D_{OUT}$ | |
| L | L | X | L | H | $D_{IN}$ | High Z | Write ($I_{CC}$) |
| | | | H | L | High Z | $D_{IN}$ | |
| | | | L | L | $D_{IN}$ | $D_{IN}$ | |

Key: X = Don't care, L = Low, H = High.

## Recommended operating conditions

| Parameter | | | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage | | AS7C4098 | $V_{CC}$ (10/12/15/20) | 4.5 | 5.0 | 5.5 | V |
| | | AS7C34098 | $V_{CC}$ (–10) | 3.15 | 3.3 | 3.6 | V |
| | | AS7C34098 | $V_{CC}$ (10/12/15/20) | 3.0 | 3.3 | 3.6 | V |
| Input voltage | | AS7C4098 | $V_{IH}$ | 2.2 | – | $V_{CC}$ + 0.5 | V |
| | | AS7C34098 | $V_{IH}$ | 2.0 | – | $V_{CC}$ + 0.5 | V |
| | | | $V_{IL}$ | –0.5* | – | 0.8 | V |
| Ambient operating temperature | commercial | | $T_A$ | 0 | – | 70 | °C |
| | industrial | | $T_A$ | –40 | – | 85 | °C |

* $V_{IL}$ min = –3.0V for pulse width less than $t_{RC}/2$.

## DC operating characteristics (over the operating range)[1]

| Parameter | Symbol | Test conditions | | –10 | | –12 | | –15 | | –20 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Input leakage current | $\lvert I_{LI} \rvert$ | $V_{CC}$ = Max<br>$V_{IN}$ = GND to $V_{CC}$ | | – | 1 | – | 1 | – | 1 | – | 1 | µA |
| Output leakage current | $\lvert I_{LO} \rvert$ | $V_{CC}$ = Max<br>$\overline{CE}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$<br>or $\overline{WE}$ = $V_{IL}$<br>$V_{I/O}$ = GND to $V_{CC}$ | | – | 1 | – | 1 | – | 1 | – | 1 | µA |
| Operating power supply current | $I_{CC}$ | $V_{CC}$ = Max<br>Min cycle, 100% duty<br>$\overline{CE}$ = $V_{IL}$, $I_{OUT}$ = 0mA | AS7C4098 | – | – | – | 250 | – | 220 | – | 180 | mA |
| | | | AS7C34098 | – | 160 | – | 130 | – | 110 | – | 100 | mA |
| Standby power supply current | $I_{SB}$ | $V_{CC}$ = Max<br>$\overline{CE}$ = $V_{IH}$, f = Max | AS7C4098 | – | – | – | 60 | – | 60 | – | 60 | mA |
| | | | AS7C34098 | – | 60 | – | 60 | – | 60 | – | 60 | mA |
| | $I_{SB1}$ | $V_{CC}$ = Max<br>$\overline{CE}$ ≥ $V_{CC}$ – 0.2V, $V_{IN}$ ≥ $V_{CC}$ – 0.2V or $V_{IN}$ ≤ 0.2V, f = 0 | AS7C4098 | – | – | – | 20 | – | 20 | – | 20 | mA |
| | | | AS7C34098 | – | 20 | – | 20 | – | 20 | – | 20 | mA |
| Output voltage | $V_{OL}$ | $I_{OL}$ = 8 mA, $V_{CC}$ = Min | | – | 0.4 | – | 0.4 | – | 0.4 | – | 0.4 | V |
| | $V_{OH}$ | $I_{OH}$ = –4 mA, $V_{CC}$ = Min | | 2.4 | – | 2.4 | – | 2.4 | – | 2.4 | – | V |

## Capacitance (f = 1MHz, $T_a$ = 25° C, $V_{CC}$ = NOMINAL)[2]

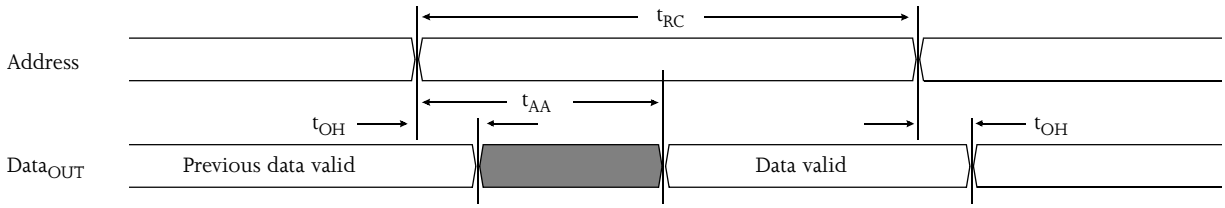
| Parameter | Symbol | Signals | Test conditions | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ | $V_{IN}$ = 0V | 6 | pF |
| I/O capacitance | $C_{I/O}$ | I/O | $V_{IN}$ = $V_{OUT}$ = 0V | 8 | pF |

## Read cycle (over the operating range)[3,9]

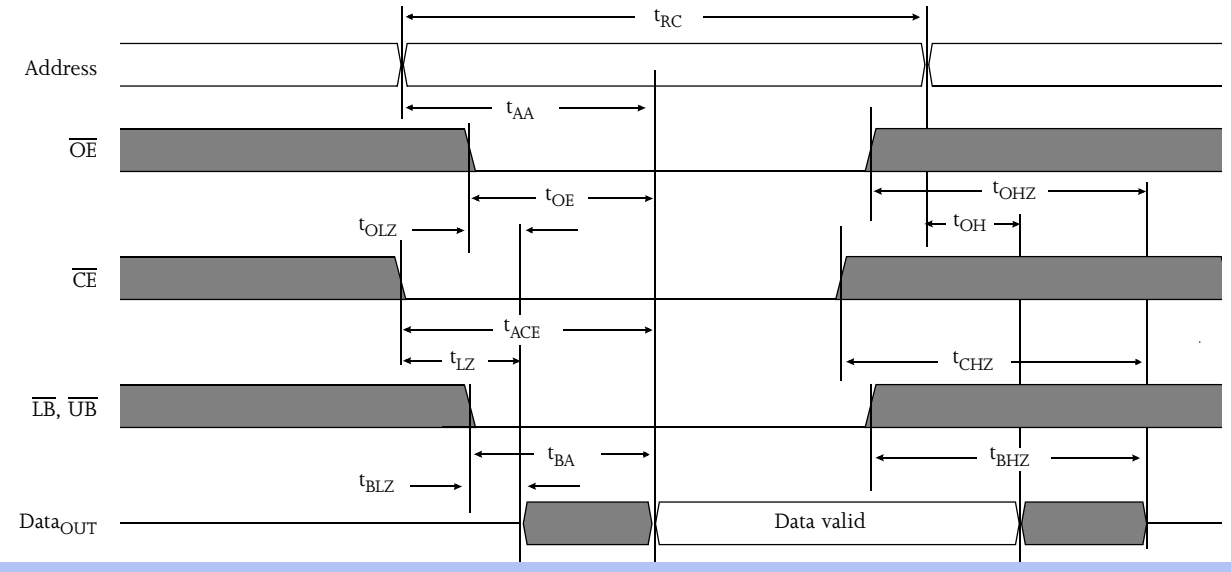
| Parameter | Symbol | −10 | | −12 | | −15 | | −20 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Read cycle time | $t_{RC}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Address access time | $t_{AA}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | |
| Chip enable ($\overline{CE}$) access time | $t_{ACE}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | |
| Output enable ($\overline{OE}$) access time | $t_{OE}$ | – | 5 | – | 6 | – | 7 | – | 8 | ns | |
| Output hold from address change | $t_{OH}$ | 3 | – | 3 | – | 3 | – | 3 | – | ns | 5 |
| $\overline{CE}$ Low to output in low Z | $t_{CLZ}$ | 0 | – | 3 | – | 0 | – | 0 | – | ns | 4, 5 |
| $\overline{CE}$ High to output in higfch Z | $t_{CHZ}$ | – | 5 | – | 6 | – | 7 | – | 9 | ns | 4, 5 |
| $\overline{OE}$ Low to output in low Z | $t_{OLZ}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 4, 5 |
| $\overline{OE}$ High to output in high Z | $t_{OHZ}$ | – | 5 | – | 6 | – | 7 | – | 9 | ns | 4, 5 |
| $\overline{LB}$, $\overline{UB}$ access time | $t_{BA}$ | – | 5 | – | 6 | – | 7 | – | 8 | ns | |
| $\overline{LB}$, $\overline{UB}$ Low to output in low Z | $t_{BLZ}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| $\overline{LB}$, $\overline{UB}$ High to output in high Z | $t_{BHZ}$ | – | 5 | – | 6 | – | 7 | – | 9 | ns | |
| Power up time | $t_{PU}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 5 |
| Power down time | $t_{PD}$ | – | 10 | – | 12 | – | 15 | – | 20 | ns | 5 |

## Key to switching waveforms


## Read waveform 1 (address controlled)[6,7,9]



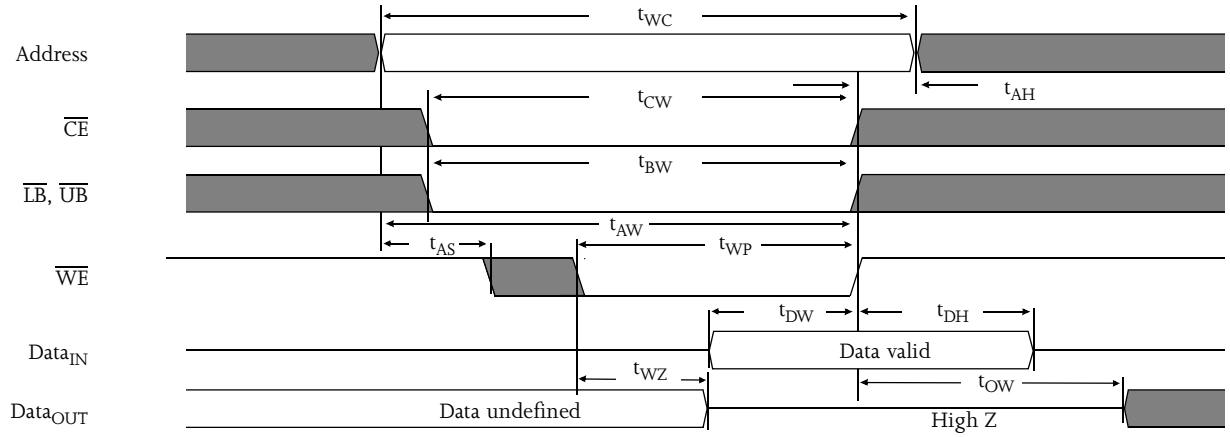

## Read waveform 2 ($\overline{CE}$, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ controlled)[6,8,9]



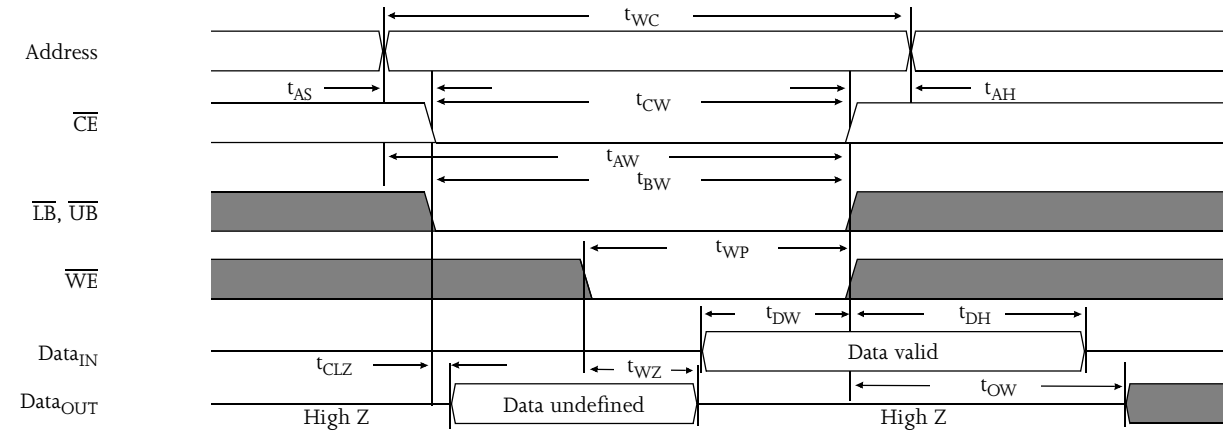
## Write cycle (over the operating range)[11]

| Parameter | Symbol | −10 | | −12 | | −15 | | −20 | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Write cycle time | $t_{WC}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Chip enable ($\overline{CE}$) to write end | $t_{CW}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | |
| Address setup to write end | $t_{AW}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | |
| Address setup time | $t_{AS}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Write pulse width ($\overline{OE}$ = High) | $t_{WP1}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | |
| Write pulse width ($\overline{OE}$ = Low) | $t_{WP2}$ | 10 | – | 12 | – | 15 | – | 20 | – | ns | |
| Address hold from end of write | $t_{AH}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| Data valid to write end | $t_{DW}$ | 5 | | 6 | | 7 | – | 9 | – | ns | |
| Data hold time | $t_{DH}$ | 0 | – | 0 | – | 0 | – | 0 | – | ns | 4, 5 |
| Write enable to output in High-Z | $t_{WZ}$ | 0 | 5 | 0 | 6 | 0 | 7 | 0 | 9 | ns | 4, 5 |
| Output active from write end | $t_{OW}$ | 3 | – | 3 | – | 3 | – | 3 | – | ns | 4, 5 |
| Byte enable Low to write end | $t_{BW}$ | 7 | – | 8 | – | 10 | – | 12 | – | ns | 4, 5 |

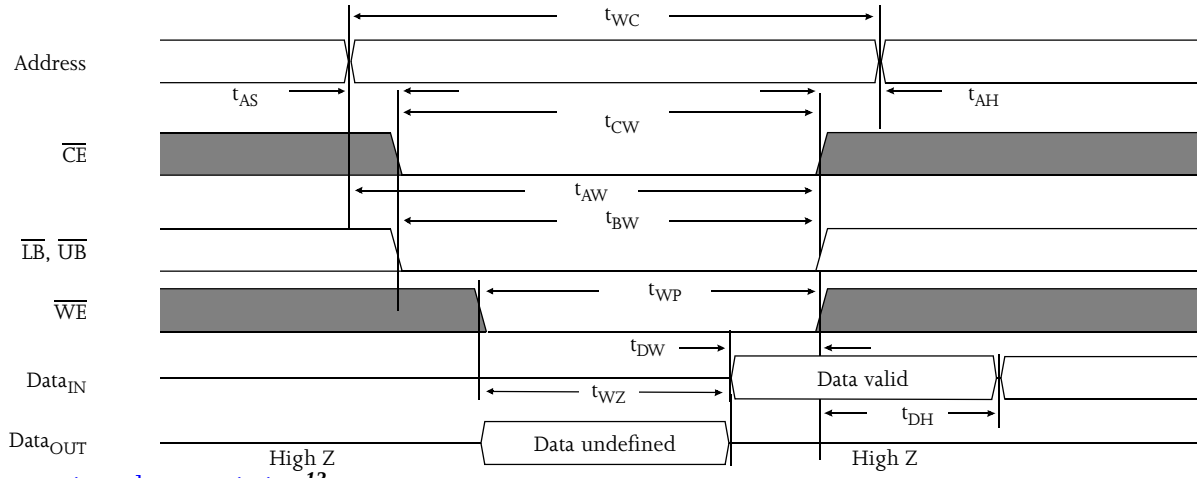
## Write waveform 1 ($\overline{WE}$ controlled)[10,11]




## Write waveform 2 ($\overline{CE}$ controlled)[10,11]



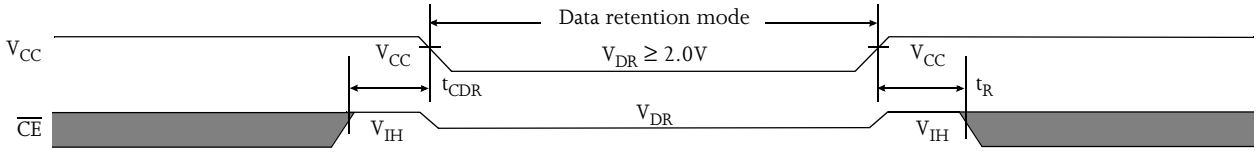
## Write waveform 3 [10,11]




## Data retention characteristics [13]

| Parameter | Symbol | Test conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ for data retention | $V_{DR}$ | $V_{CC}$ = 2.0V | 2.0 | – | V |
| Data retention current | $I_{CCDR}$ | $\overline{CE} \geq V_{CC} - 0.2V$ | – | 500 | µA |
| Chip deselect to data retention time | $t_{CDR}$ | $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | 0 | – | ns |
| Operation recovery time | $t_R$ | | $t_{RC}$ | – | ns |
| Input leakage current | $\lvert I_{LI} \rvert$ | | – | 1 | µA |

## Data retention waveform




## AC test conditions

- Output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

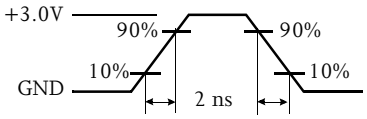



Figure A: Input pulse

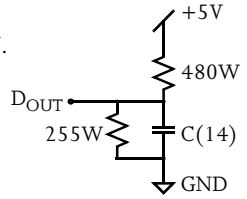



Figure B: 5V Output load

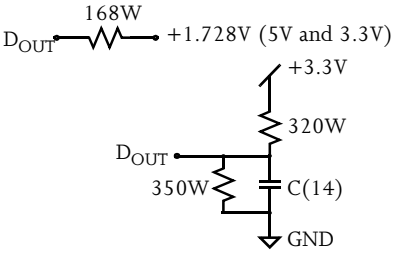


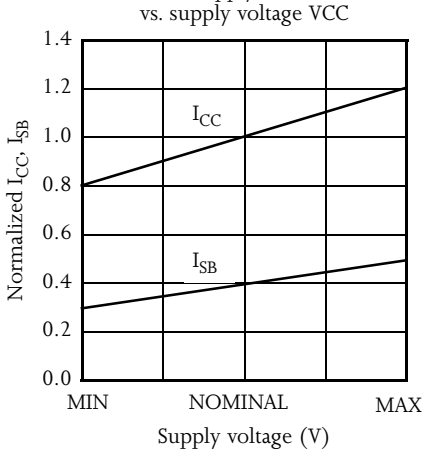

Figure C: 3.3V Output load

## Notes

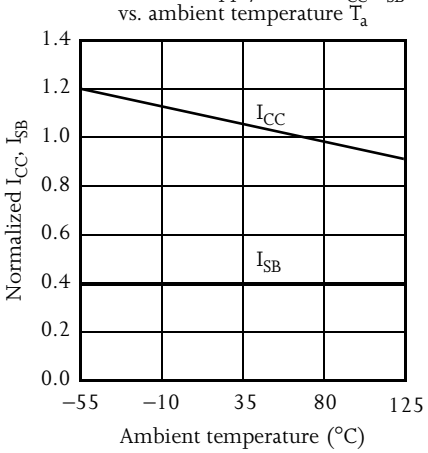
1 During $V_{CC}$ power-up, a pull-up resistor to $V_{CC}$ on $\overline{CE}$ is required to meet $I_{SB}$ specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 $t_{CLZ}$ and $t_{CHZ}$ are specified with $C_L$ = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be High during address transitions. Either $\overline{CE}$ or $\overline{WE}$ asserting high terminates a write cycle.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 Not applicable.
13 2V data retention applies to commercial temperature range operation only.
14 C = 30pF, except on High Z and Low Z parameters, where C = 5pF.

## Typical DC and AC characteristics[12]

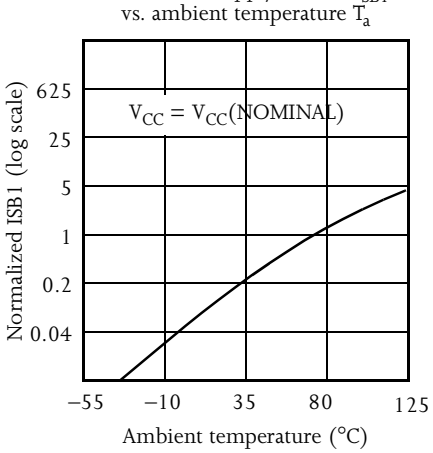
Normalized supply current ICC, ISB vs. supply voltage VCC



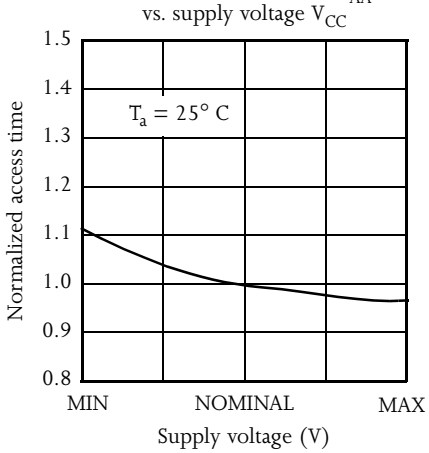

Normalized supply current $I_{CC}$, $I_{SB}$ vs. ambient temperature $T_a$



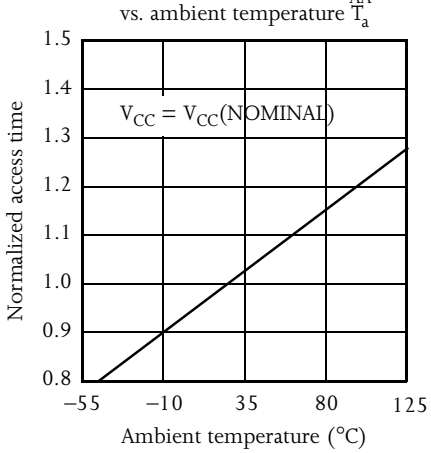

Normalized supply current $I_{SB1}$ vs. ambient temperature $T_a$



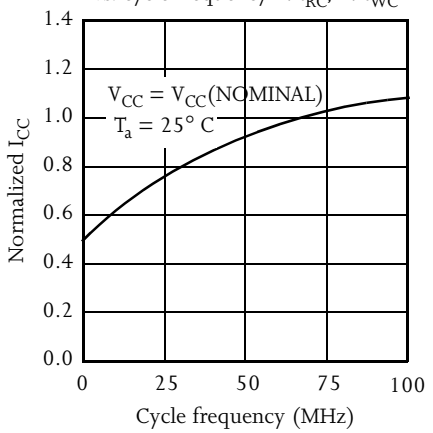

Normalized access time $t_{AA}$ vs. supply voltage $V_{CC}$



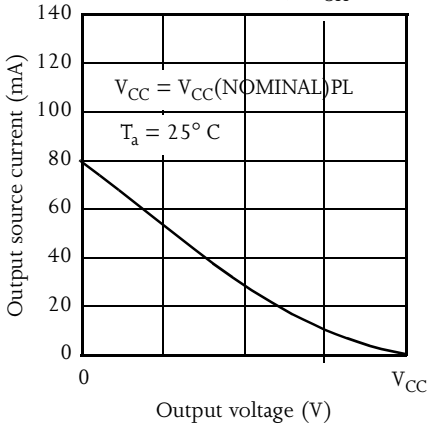

Normalized access time $t_{AA}$ vs. ambient temperature $T_a$



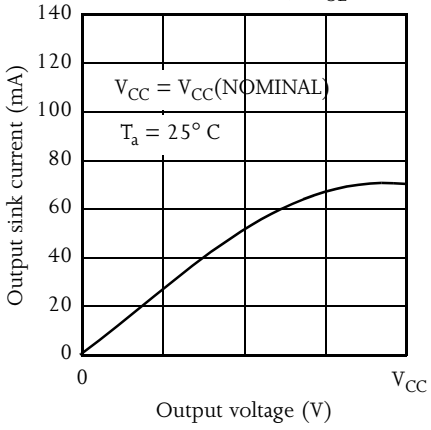

Normalized supply current $I_{CC}$ vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



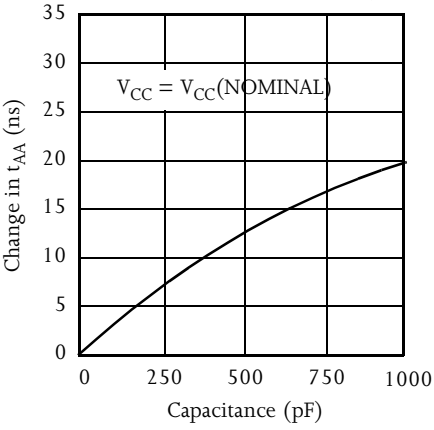

Output source current $I_{OH}$ vs. output voltage $V_{OH}$



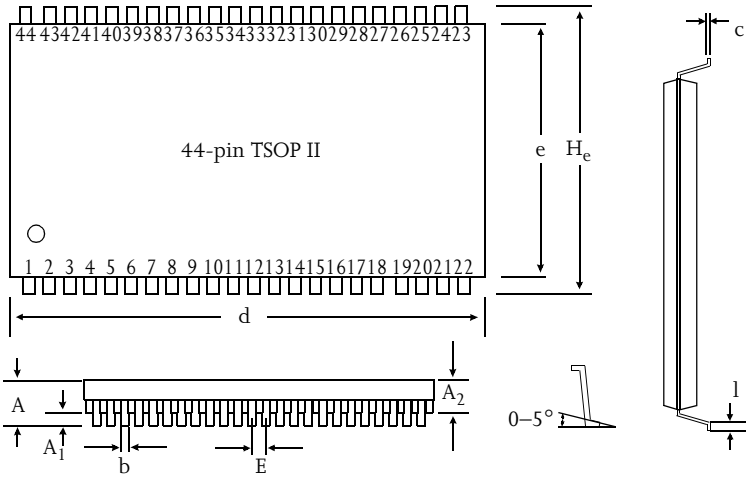

Output sink current $I_{OL}$ vs. output voltage $V_{OL}$



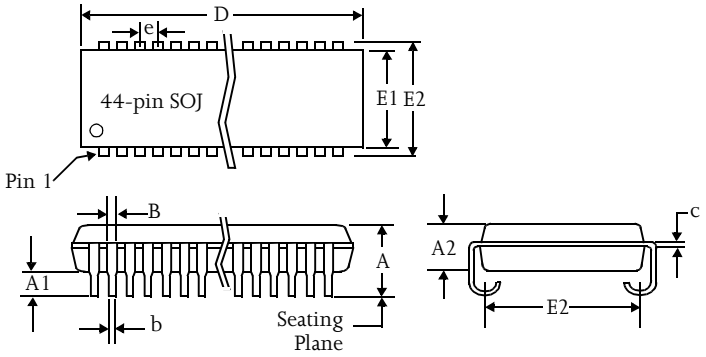

Typical access time change $\Delta t_{AA}$ vs. output capacitive loading



## Package dimensions




| | 44-pin TSOP II | |
|---|---|---|
| | Min (mm) | Max (mm) |
| A | | 1.2 |
| $A_1$ | 0.05 | |
| $A_2$ | 0.95 | 1.05 |
| b | 0.25 | 0.45 |
| c | 0.15 (typical) | |
| d | 18.28 | 18.54 |
| e | 10.06 | 10.26 |
| $H_e$ | 11.56 | 11.96 |
| E | 0.80 (typical) | |
| l | 0.40 | 0.60 |




| | 44-pin SOJ 400 mils | |
|---|---|---|
| | Min(mils) | Max(mils) |
| A | 0.128 | 0.148 |
| A1 | 0.025 | - |
| A2 | 1.105 | 1.115 |
| B | 0.026 | 0.032 |
| b | 0.015 | 0.020 |
| c | 0.007 | 0.013 |
| D | 1.120 | 1.130 |
| E | 0.370 NOM | |
| E1 | 0.395 | 0.405 |
| E2 | 0.435 | 0.445 |
| e | 0.050 NOM | |

## Ordering Codes

| Package | Version | 10 ns | 12 ns | 15 ns | 20 ns |
|---|---|---|---|---|---|
| SOJ | 5V commercial | NA | AS7C4098-12JC | AS7C4098-15JC | AS7C4098-20JC |
| | 5V industrial | NA | AS7C4098-12JI | AS7C4098-15JI | AS7C4098-20JI |
| | 3.3V commercial | AS7C34098-10JC | AS7C34098-12JC | AS7C34098-15JC | AS7C34098-20JC |
| | 3.3V industrial | NA | AS7C34098-12JI | AS7C34098-15JI | AS7C34098-20JI |
| TSOP II | 5V commercial | NA | AS7C4098-12TC | AS7C4098-15TC | AS7C4098-20TC |
| | 5V industrial | NA | AS7C4098-12TI | AS7C4098-15TI | AS7C4098-20TI |
| | 3.3V commercial | AS7C34098-10TC | AS7C34098-12TC | AS7C34098-15TC | AS7C34098-20TC |
| | 3.3V industrial | NA | AS7C34098-12TI | AS7C34098-15TI | AS7C34098-20TI |

NA: not available.

## Part numbering system

| AS7C | X | 4098 | –XX | J, T | X |
|---|---|---|---|---|---|
| SRAM prefix | Blank: 5V CMOS<br>3: 3.3V CMOS | Device number | Access time | Packages:<br>J: SOJ 400 mil<br>T: TSOP II 400 mil | Temperature ranges:<br>C: Commercial, 0°C to 70°C<br>I: Industrial, –40°C to 85°C |