

# 74ALVT16601

18-bit universal bus transceiver; 3-state

Rev. 03 — 5 July 2005

Product data sheet

## 1. General description

The 74ALVT16601 is a high-performance Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) product designed for  $V_{CC}$  operation at 2.5 V and 3.3 V with I/O compatibility up to 5 V. This device is an 18-bit universal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ), latch enable (LEAB and LEBA), and clock (CPAB and CPBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A-bus data is latched if CPAB is held at a HIGH or LOW level. If LEAB is LOW, the A-bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CPAB. When  $\overline{OEAB}$  is LOW, the outputs are active. When  $\overline{OEAB}$  is HIGH, the outputs are in the high-impedance state. The clocks can be controlled with the clock enable inputs ( $\overline{CEAB}$  and  $\overline{CEBA}$ ).

Data flow for B-to-A is similar to that of A-to-B but uses  $\overline{OEBA}$ , LEBA and CPBA.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## 2. Features

- 18-bit bidirectional bus interface
- 5 V I/O compatible
- 3-state buffers
- Output capability: +64 mA and –32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Positive-edge triggered clock inputs
- Latch-up protection:
  - ◆ JESD78: exceeds 500 mA
- ESD protection:
  - ◆ MIL STD 883, method 3015: exceeds 2000 V
  - ◆ Machine model: exceeds 200 V

**PHILIPS**

### 3. Quick reference data

**Table 1: Quick reference data**

$GND = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ .

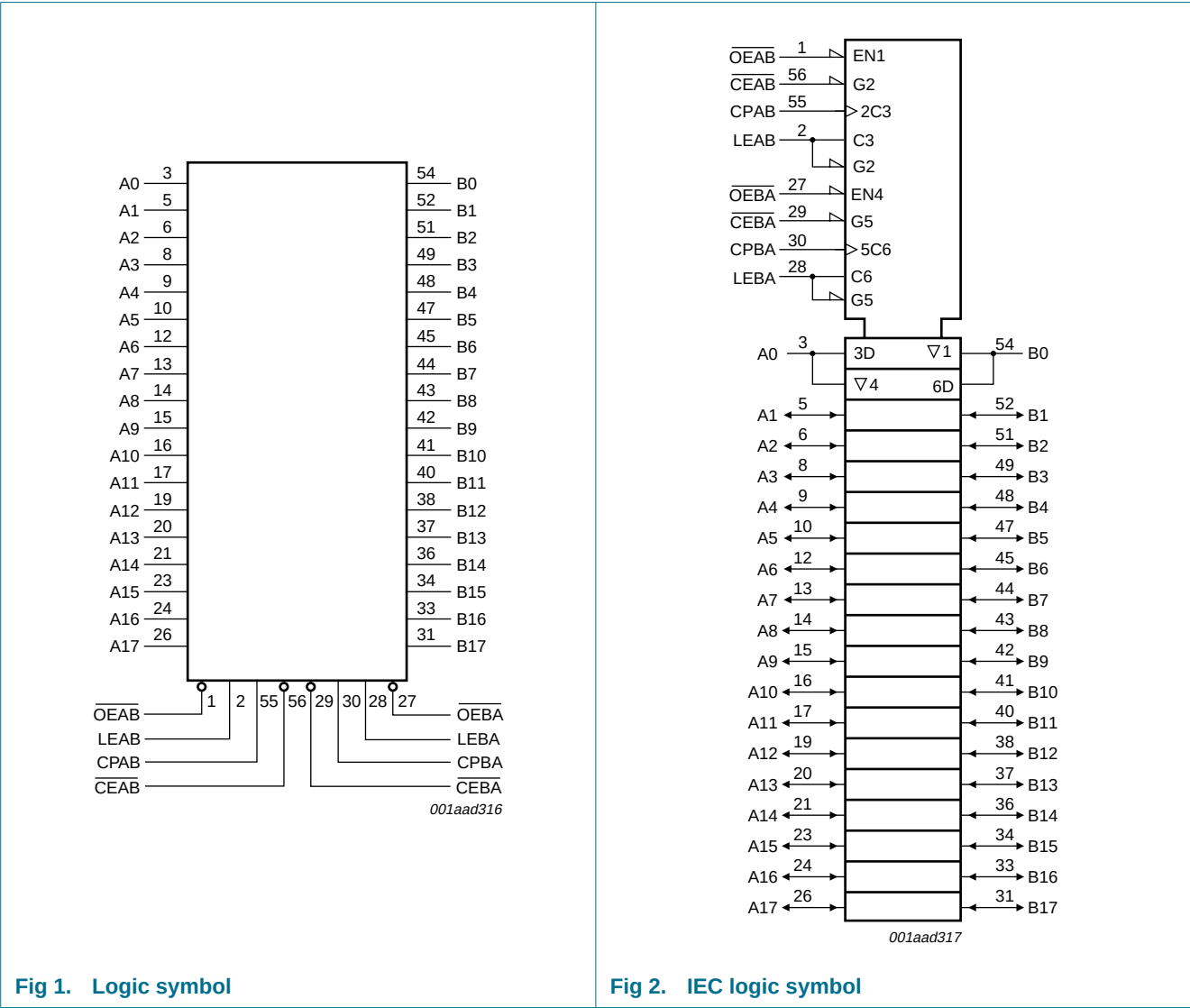
| Symbol                                    | Parameter                              | Conditions                                           | Min | Typ | Max | Unit          |
|-------------------------------------------|----------------------------------------|------------------------------------------------------|-----|-----|-----|---------------|
| <b><math>V_{CC} = 2.5\text{ V}</math></b> |                                        |                                                      |     |     |     |               |
| $t_{PLH}$                                 | propagation delay An to Bn or Bn to An | $C_L = 30\text{ pF}$                                 | -   | 1.8 | -   | ns            |
| $t_{PHL}$                                 | propagation delay An to Bn or Bn to An | $C_L = 30\text{ pF}$                                 | -   | 2.2 | -   | ns            |
| $C_i$                                     | input capacitance of control pins      | $V_I = 0\text{ V}$ or $V_{CC}$                       |     | 4   | -   | pF            |
| $C_{io}$                                  | input/output capacitance of I/O pins   | $V_{IO} = 0\text{ V}$ or $V_{CC}$ ; outputs disabled |     | 8   | -   | pF            |
| $I_{CC}$                                  | supply current                         | outputs disabled                                     | -   | 40  | -   | $\mu\text{A}$ |
| <b><math>V_{CC} = 3.3\text{ V}</math></b> |                                        |                                                      |     |     |     |               |
| $t_{PLH}$                                 | propagation delay An to Bn or Bn to An | $C_L = 50\text{ pF}$                                 | -   | 1.9 | -   | ns            |
| $t_{PHL}$                                 | propagation delay An to Bn or Bn to An | $C_L = 50\text{ pF}$                                 | -   | 2   | -   | ns            |
| $C_i$                                     | input capacitance of control pins      | $V_I = 0\text{ V}$ or $V_{CC}$                       |     | 4   | -   | pF            |
| $C_{io}$                                  | input/output capacitance of I/O pins   | $V_{IO} = 0\text{ V}$ or $V_{CC}$ ; outputs disabled |     | 8   | -   | pF            |
| $I_{CC}$                                  | supply current                         | outputs disabled                                     | -   | 60  | -   | $\mu\text{A}$ |

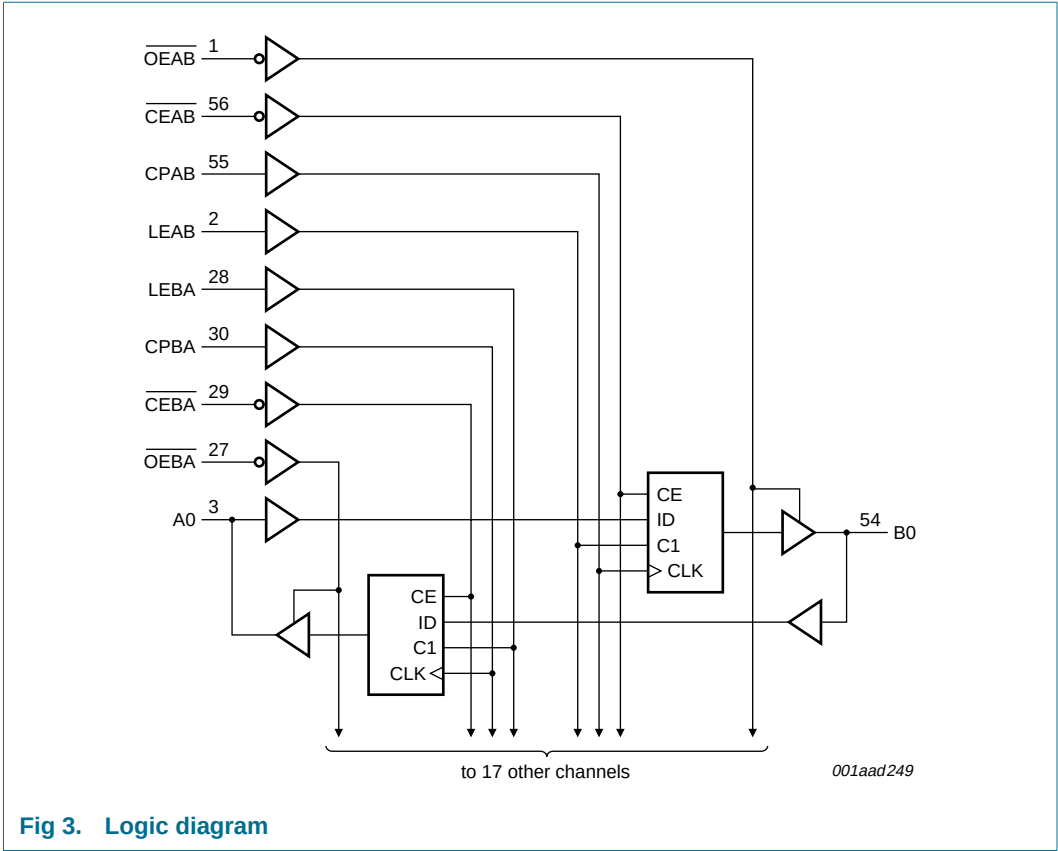
### 4. Ordering information

**Table 2: Ordering information**

| Type number    | Package           |         |                                                                        |          |
|----------------|-------------------|---------|------------------------------------------------------------------------|----------|
|                | Temperature range | Name    | Description                                                            | Version  |
| 74ALVT16601DL  | -40 °C to +85 °C  | SSOP56  | plastic shrink small outline package; 56 leads; body width 7.5 mm      | SOT371-1 |
| 74ALVT16601DGG | -40 °C to +85 °C  | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |

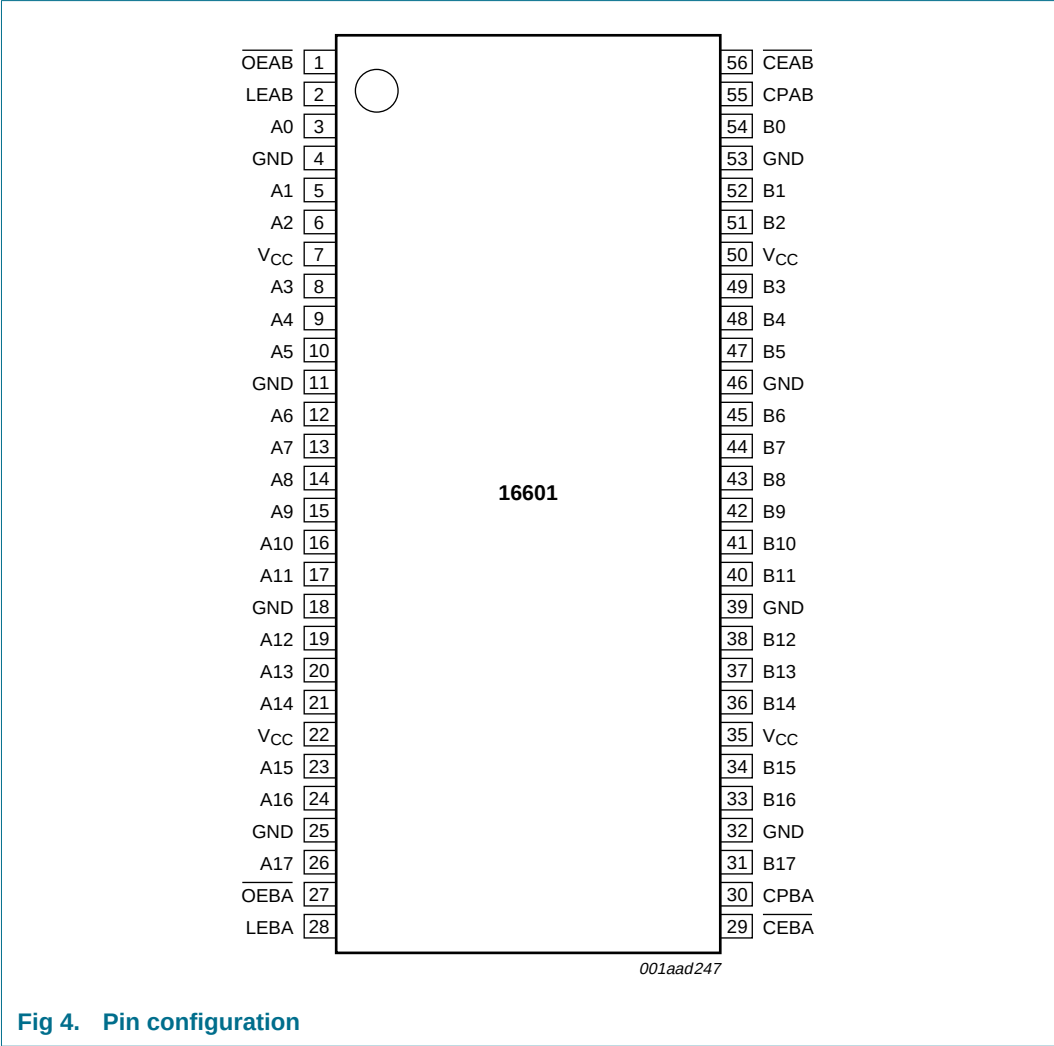
5. Functional diagram





6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3: Pin description

| Symbol          | Pin | Description                             |
|-----------------|-----|-----------------------------------------|
| OEAB            | 1   | A-to-B output enable input (active LOW) |
| LEAB            | 2   | A-to-B latch enable input               |
| A0              | 3   | data input or output (A side)           |
| GND             | 4   | ground (0 V)                            |
| A1              | 5   | data input or output (A side)           |
| A2              | 6   | data input or output (A side)           |
| V <sub>CC</sub> | 7   | voltage supply                          |
| A3              | 8   | data input or output (A side)           |

Table 3: Pin description ...continued

| Symbol          | Pin | Description                             |
|-----------------|-----|-----------------------------------------|
| A4              | 9   | data input or output (A side)           |
| A5              | 10  | data input or output (A side)           |
| GND             | 11  | ground (0 V)                            |
| A6              | 12  | data input or output (A side)           |
| A7              | 13  | data input or output (A side)           |
| A8              | 14  | data input or output (A side)           |
| A9              | 15  | data input or output (A side)           |
| A10             | 16  | data input or output (A side)           |
| A11             | 17  | data input or output (A side)           |
| GND             | 18  | ground (0 V)                            |
| A12             | 19  | data input or output (A side)           |
| A13             | 20  | data input or output (A side)           |
| A14             | 21  | data input or output (A side)           |
| V <sub>CC</sub> | 22  | voltage supply                          |
| A15             | 23  | data input or output (A side)           |
| A16             | 24  | data input or output (A side)           |
| GND             | 25  | ground (0 V)                            |
| A17             | 26  | data input or output (A side)           |
| OEBA            | 27  | B-to-A output enable input (active LOW) |
| LEBA            | 28  | B-to-A latch enable input               |
| CEBA            | 29  | B-to-A clock enable (active LOW)        |
| CPBA            | 30  | B-to-A clock input (active rising edge) |
| B17             | 31  | data input or output (B side)           |
| GND             | 32  | ground (0 V)                            |
| B16             | 33  | data input or output (B side)           |
| B15             | 34  | data input or output (B side)           |
| V <sub>CC</sub> | 35  | voltage supply                          |
| B14             | 36  | data input or output (B side)           |
| B13             | 37  | data input or output (B side)           |
| B12             | 38  | data input or output (B side)           |
| GND             | 39  | ground (0 V)                            |
| B11             | 40  | data input or output (B side)           |
| B10             | 41  | data input or output (B side)           |
| B9              | 42  | data input or output (B side)           |
| B8              | 43  | data input or output (B side)           |
| B7              | 44  | data input or output (B side)           |
| B6              | 45  | data input or output (B side)           |
| GND             | 46  | ground (0 V)                            |
| B5              | 47  | data input or output (B side)           |
| B4              | 48  | data input or output (B side)           |
| B3              | 49  | data input or output (B side)           |

Table 3: Pin description ...continued

| Symbol          | Pin | Description                             |
|-----------------|-----|-----------------------------------------|
| V <sub>CC</sub> | 50  | voltage supply                          |
| B2              | 51  | data input or output (B side)           |
| B1              | 52  | data input or output (B side)           |
| GND             | 53  | ground (0 V)                            |
| B0              | 54  | data input or output (B side)           |
| CPAB            | 55  | A-to-B clock input (active rising edge) |
| CEAB            | 56  | A-to-B clock enable (active LOW)        |

## 7. Functional description

### 7.1 Function table

Table 4: Function table [1]

| Control |      |      |      | Input          | Output         |
|---------|------|------|------|----------------|----------------|
| CEAB    | OEAB | LEAB | CPAB | A <sub>n</sub> | B <sub>n</sub> |
| CEBA    | OEBA | LEBA | CPBA | B <sub>n</sub> | A <sub>n</sub> |
| X       | H    | X    | X    | X              | Z              |
| X       | L    | H    | X    | L              | L              |
|         |      |      |      | H              | H              |
| L       | L    | L    | ↑    | L              | L              |
|         |      |      |      | H              | H              |
| L       | L    | L    | H    | X              | Y [2]          |
|         |      |      | L    | X              | Y [3]          |
| H       | L    | L    | X    | X              | Y [2]          |

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care;  
 Z = high-impedance OFF-state;  
 ↑ = LOW-to-HIGH clock transition

[2] Output level before the indicated steady-state input conditions were established.

[3] Output level before the indicated steady-state input conditions were established, provided that CPAB or CPBA was LOW before LEAB or LEBA went LOW.

## 8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol          | Parameter      | Conditions                        | Min      | Max  | Unit |
|-----------------|----------------|-----------------------------------|----------|------|------|
| V <sub>CC</sub> | supply voltage |                                   | -0.5     | +4.6 | V    |
| V <sub>I</sub>  | input voltage  |                                   | [1] -0.5 | +7.0 | V    |
| V <sub>O</sub>  | output voltage | output in OFF-state or HIGH-state | [1] -0.5 | +7.0 | V    |

**Table 5: Limiting values ...continued**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol    | Parameter            | Conditions           | Min   | Max  | Unit |
|-----------|----------------------|----------------------|-------|------|------|
| $I_{IK}$  | input diode current  | $V_I < 0$ V          | -     | -50  | mA   |
| $I_{OK}$  | output diode current | $V_O < 0$ V          | -     | -50  | mA   |
| $I_O$     | output current       | output in LOW-state  | -     | 128  | mA   |
|           |                      | output in HIGH-state | -     | -64  | mA   |
| $T_{stg}$ | storage temperature  |                      | -65   | +150 | °C   |
| $T_j$     | junction temperature |                      | [2] - | 150  | °C   |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

| Symbol                                                    | Parameter                          | Conditions                                        | Min | Typ | Max | Unit |
|-----------------------------------------------------------|------------------------------------|---------------------------------------------------|-----|-----|-----|------|
| <b><math>V_{CC} = 2.5</math> V <math>\pm</math> 0.2 V</b> |                                    |                                                   |     |     |     |      |
| $V_{CC}$                                                  | supply voltage                     |                                                   | 2.3 | -   | 2.7 | V    |
| $V_I$                                                     | input voltage                      |                                                   | 0   | -   | 5.5 | V    |
| $V_{IH}$                                                  | HIGH-level input voltage           |                                                   | 1.7 | -   | -   | V    |
| $V_{IL}$                                                  | LOW-level input voltage            |                                                   | -   | -   | 0.7 | V    |
| $I_{OH}$                                                  | HIGH-level output current          |                                                   | -   | -   | -8  | mA   |
| $I_{OL}$                                                  | LOW-level output current           | none                                              | -   | -   | 8   | mA   |
|                                                           |                                    | current duty cycle $\leq$ 50 %;<br>$f \geq$ 1 kHz | -   | -   | 24  | mA   |
| $\Delta t/\Delta V$                                       | input transition rise or fall rate | outputs enabled                                   | -   | -   | 10  | ns/V |
| $T_{amb}$                                                 | ambient temperature                |                                                   | -40 | -   | +85 | °C   |
| <b><math>V_{CC} = 3.3</math> V <math>\pm</math> 0.3 V</b> |                                    |                                                   |     |     |     |      |
| $V_{CC}$                                                  | supply voltage                     |                                                   | 3.0 | -   | 3.6 | V    |
| $V_I$                                                     | input voltage                      |                                                   | 0   | -   | 5.5 | V    |
| $V_{IH}$                                                  | HIGH-level input voltage           |                                                   | 2.0 | -   | -   | V    |
| $V_{IL}$                                                  | LOW-level input voltage            |                                                   | -   | -   | 0.8 | V    |
| $I_{OH}$                                                  | HIGH-level output current          |                                                   | -   | -   | -32 | mA   |
| $I_{OL}$                                                  | LOW-level output current           | none                                              | -   | -   | 32  | mA   |
|                                                           |                                    | current duty cycle $\leq$ 50 %;<br>$f \geq$ 1 kHz | -   | -   | 64  | mA   |
| $\Delta t/\Delta V$                                       | input transition rise or fall rate | outputs enabled                                   | -   | -   | 10  | ns/V |
| $T_{amb}$                                                 | ambient temperature                | in free air                                       | -40 | -   | +85 | °C   |



## 10. Static characteristics

**Table 7: Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

$T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

| Symbol                                                         | Parameter                               | Conditions                                                                                                                                                       | Min            | Typ      | Max       | Unit          |
|----------------------------------------------------------------|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------|-----------|---------------|
| <b><math>V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}</math> [1]</b> |                                         |                                                                                                                                                                  |                |          |           |               |
| $V_{IK}$                                                       | input diode voltage                     | $V_{CC} = 2.3\text{ V}$ ; $I_{IK} = -18\text{ mA}$                                                                                                               | -              | -0.85    | -1.2      | V             |
| $V_{OH}$                                                       | HIGH-level output voltage               | $V_{CC} = 2.3\text{ V}$ to $3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$                                                                                   | $V_{CC} - 0.2$ |          | -         | V             |
|                                                                |                                         | $V_{CC} = 2.3\text{ V}$ ; $I_{OH} = -8\text{ mA}$                                                                                                                | 1.8            |          | -         | V             |
| $V_{OL}$                                                       | LOW-level output voltage                | $V_{CC} = 2.3\text{ V}$ ; $I_{OL} = 100\text{ }\mu\text{A}$                                                                                                      | -              | 0.07     | 0.2       | V             |
|                                                                |                                         | $V_{CC} = 2.3\text{ V}$ ; $I_{OL} = 24\text{ mA}$                                                                                                                | -              | 0.3      | 0.5       | V             |
|                                                                |                                         | $V_{CC} = 2.3\text{ V}$ ; $I_{OL} = 8\text{ mA}$                                                                                                                 | -              | -        | 0.4       | V             |
| $V_{RST}$                                                      | power-up LOW-state output voltage       | $V_{CC} = 2.7\text{ V}$ ; $I_O = 1\text{ mA}$ ; $V_I = V_{CC}$ or GND                                                                                            | [2] -          | -        | 0.55      | V             |
| $I_{LI}$                                                       | input leakage current                   |                                                                                                                                                                  |                |          |           |               |
|                                                                | control pins                            | $V_{CC} = 2.7\text{ V}$ ; $V_I = V_{CC}$ or GND                                                                                                                  | -              | 0.1      | $\pm 1$   | $\mu\text{A}$ |
|                                                                |                                         | $V_{CC} = 0\text{ V}$ or $2.7\text{ V}$ ; $V_I = 5.5\text{ V}$                                                                                                   |                | 0.1      | 10        | $\mu\text{A}$ |
|                                                                | I/O data pins                           | $V_{CC} = 0\text{ V}$ or $2.7\text{ V}$ ; $V_I = 5.5\text{ V}$                                                                                                   | [3] -          | 0.1      | 20        | $\mu\text{A}$ |
|                                                                |                                         | $V_{CC} = 2.7\text{ V}$ ; $V_I = V_{CC}$                                                                                                                         | [3] -          | 0.1      | 10        | $\mu\text{A}$ |
|                                                                |                                         | $V_{CC} = 2.7\text{ V}$ ; $V_I = 0\text{ V}$                                                                                                                     | [3] -          | +0.1     | -5        | $\mu\text{A}$ |
| $I_{OFF}$                                                      | power-down leakage current              | $V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V}$ to $4.5\text{ V}$                                                                                            | -              | 0.1      | $\pm 100$ | $\mu\text{A}$ |
| $I_{HOLD}$                                                     | bus hold current data inputs            | $V_{CC} = 2.3\text{ V}$ ; $V_I = 0.7\text{ V}$                                                                                                                   | [4] -          | 90       | -         | $\mu\text{A}$ |
|                                                                |                                         | $V_{CC} = 2.3\text{ V}$ ; $V_I = 1.7\text{ V}$                                                                                                                   | [4] -          | -75      | -         | $\mu\text{A}$ |
| $I_{EX}$                                                       | external current into output            | output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5\text{ V}$ ; $V_{CC} = 2.3\text{ V}$                                                                        | -              | 10       | 125       | $\mu\text{A}$ |
| $I_{PU}, I_{PD}$                                               | power-up/down 3-state output current    | $V_{CC} \leq 1.2\text{ V}$ ; $V_O = 0.5\text{ V}$ to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $\overline{\text{OEAB}}$ or $\overline{\text{OEAB}}$ don't care | [5] -          | 1        | 100       | $\mu\text{A}$ |
| $I_{CC}$                                                       | supply current                          | $V_{CC} = 2.7\text{ V}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $I_O = 0\text{ A}$                                                                                    |                |          |           |               |
|                                                                | outputs HIGH-state                      |                                                                                                                                                                  | -              | 0.04     | 0.1       | mA            |
|                                                                | outputs LOW-state                       |                                                                                                                                                                  | -              | 2.5      | 4.5       | mA            |
|                                                                | outputs disabled                        |                                                                                                                                                                  | [6] -          | 0.04     | 0.1       | mA            |
| $\Delta I_{CC}$                                                | additional supply current per input pin | $V_{CC} = 2.3\text{ V}$ to $2.7\text{ V}$ ; one input at $V_{CC} - 0.6\text{ V}$ , other inputs at $V_{CC}$ or GND                                               | [7] -          | 0.01     | 0.4       | mA            |
| $C_i$                                                          | input capacitance of control pins       | $V_I = 0\text{ V}$ or $V_{CC}$                                                                                                                                   |                | 4        | -         | pF            |
| $C_{iO}$                                                       | input/output capacitance of I/O pins    | $V_{IO} = 0\text{ V}$ or $V_{CC}$ ; outputs disabled                                                                                                             |                | 8        | -         | pF            |
| <b><math>V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}</math> [8]</b> |                                         |                                                                                                                                                                  |                |          |           |               |
| $V_{IK}$                                                       | input diode voltage                     | $V_{CC} = 3.0\text{ V}$ ; $I_{IK} = -18\text{ mA}$                                                                                                               | -              | -0.85    | -1.2      | V             |
| $V_{OH}$                                                       | HIGH-level output voltage               | $V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$                                                                                   | $V_{CC} - 0.2$ | $V_{CC}$ | -         | V             |
|                                                                |                                         | $V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -32\text{ mA}$                                                                                                               | 2.0            | 2.3      | -         | V             |

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

 $T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

| Symbol           | Parameter                               | Conditions                                                                                                                                                    | Min           | Typ  | Max       | Unit          |
|------------------|-----------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|------|-----------|---------------|
| $V_{OL}$         | LOW-level output voltage                | $V_{CC} = 3.0\text{ V}; I_{OL} = 100\text{ }\mu\text{A}$                                                                                                      | -             | 0.07 | 0.2       | V             |
|                  |                                         | $V_{CC} = 3.0\text{ V}; I_{OL} = 16\text{ mA}$                                                                                                                | -             | 0.25 | 0.4       | V             |
|                  |                                         | $V_{CC} = 3.0\text{ V}; I_{OL} = 32\text{ mA}$                                                                                                                | -             | 0.3  | 0.5       | V             |
|                  |                                         | $V_{CC} = 3.0\text{ V}; I_{OL} = 64\text{ mA}$                                                                                                                | -             | 0.4  | 0.55      | V             |
| $V_{RST}$        | power-up LOW-state output voltage       | $V_{CC} = 2.7\text{ V}; I_O = 1\text{ mA}; V_I = V_{CC}$ or GND                                                                                               | [2] -         | -    | 0.55      | V             |
| $I_{LI}$         | input leakage current                   |                                                                                                                                                               |               |      |           |               |
|                  |                                         | control pins                                                                                                                                                  |               |      |           |               |
|                  |                                         | $V_{CC} = 3.6\text{ V}; V_I = V_{CC}$ or GND                                                                                                                  | -             | 0.1  | $\pm 1$   | $\mu\text{A}$ |
|                  |                                         | $V_{CC} = 0\text{ V}$ or $3.6\text{ V}; V_I = 5.5\text{ V}$                                                                                                   | -             | 0.1  | 10        | $\mu\text{A}$ |
|                  | I/O data pins                           | $V_{CC} = 3.6\text{ V}; V_I = 5.5\text{ V}$                                                                                                                   | [3] -         | 0.1  | 20        | $\mu\text{A}$ |
|                  |                                         | $V_{CC} = 3.6\text{ V}; V_I = V_{CC}$                                                                                                                         | [3] -         | 0.5  | 10        | $\mu\text{A}$ |
|                  |                                         | $V_{CC} = 3.6\text{ V}; V_I = 0\text{ V}$                                                                                                                     | [3] -         | +0.1 | -5        | $\mu\text{A}$ |
| $I_{OFF}$        | power-down leakage current              | $V_{CC} = 0\text{ V}; V_I$ or $V_O = 0\text{ V}$ to $4.5\text{ V}$                                                                                            | -             | 0.1  | $\pm 100$ | $\mu\text{A}$ |
| $I_{HOLD}$       | bus hold current data inputs            | $V_{CC} = 3\text{ V}; V_I = 0.8\text{ V}$                                                                                                                     | [9] 75        | 130  | -         | $\mu\text{A}$ |
|                  |                                         | $V_{CC} = 3\text{ V}; V_I = 2.0\text{ V}$                                                                                                                     | [9] -75       | -140 | -         | $\mu\text{A}$ |
|                  |                                         | $V_{CC} = 0\text{ V}$ to $3.6\text{ V}; V_{CC} = 3.6\text{ V}$                                                                                                | [9] $\pm 500$ | -    | -         | $\mu\text{A}$ |
| $I_{EX}$         | external current into output            | output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5\text{ V}; V_{CC} = 2.3\text{ V}$                                                                        | -             | 10   | 125       | $\mu\text{A}$ |
| $I_{PU}, I_{PD}$ | power-up/down 3-state output current    | $V_{CC} \leq 1.2\text{ V}; V_O = 0.5\text{ V}$ to $V_{CC}$ ; $V_I = \text{GND}$ or $V_{CC}$ ; $\overline{\text{OEAB}}$ or $\overline{\text{OEAB}}$ don't care | [10] -        | 1    | $\pm 100$ | $\mu\text{A}$ |
| $I_{CC}$         | supply current                          | $V_{CC} = 3.6\text{ V}; V_I = \text{GND}$ or $V_{CC}; I_O = 0\text{ A}$                                                                                       |               |      |           |               |
|                  |                                         | outputs HIGH-state                                                                                                                                            | -             | 0.06 | 0.1       | mA            |
|                  |                                         | outputs LOW-state                                                                                                                                             | -             | 3.5  | 5         | mA            |
|                  |                                         | outputs disabled                                                                                                                                              | [6] -         | 0.06 | 0.1       | mA            |
| $\Delta I_{CC}$  | additional supply current per input pin | $V_{CC} = 3\text{ V}$ to $3.6\text{ V}$ ; one input at $V_{CC} - 0.6\text{ V}$ , other inputs at $V_{CC}$ or GND                                              | [7] -         | 0.04 | 0.4       | mA            |
| $C_i$            | input capacitance of control pins       | $V_I = 0\text{ V}$ or $V_{CC}$                                                                                                                                |               | 4    | -         | pF            |
| $C_{iO}$         | input/output capacitance of I/O pins    | $V_{IO} = 0\text{ V}$ or $V_{CC}$ ; outputs disabled                                                                                                          |               | 8    | -         | pF            |

[1] All typical values are at  $V_{CC} = 2.5\text{ V}$  and  $T_{amb} = 25^{\circ}\text{C}$ .

[2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

[3] Unused pins at  $V_{CC}$  or GND.

[4] Not guaranteed.

[5] This parameter is valid for any  $V_{CC}$  between  $0\text{ V}$  and  $1.2\text{ V}$  with a transition time of up to  $10\text{ ms}$ . From  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  a transition time of  $100\text{ }\mu\text{s}$  is permitted. This parameter is valid for  $T_{amb} = 25^{\circ}\text{C}$  only.[6]  $I_{CC}$  is measured with outputs pulled up to  $V_{CC}$  or pulled down to ground.[7] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.[8] All typical values are at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25^{\circ}\text{C}$ .

[9] This is the bus hold overdrive current required to force the input to the opposite logic state.

[10] This parameter is valid for any  $V_{CC}$  between  $0\text{ V}$  and  $1.2\text{ V}$  with a transition time of up to  $10\text{ ms}$ . From  $V_{CC} = 1.2\text{ V}$  to  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  a transition time of  $100\text{ }\mu\text{s}$  is permitted. This parameter is valid for  $T_{amb} = 25^{\circ}\text{C}$  only.

## 11. Dynamic characteristics

**Table 8: Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 11](#).

$T_{amb} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

| Symbol                                                                                          | Parameter                                                            | Conditions                    | Min  | Typ  | Max | Unit |
|-------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|-------------------------------|------|------|-----|------|
| <b><math>V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}</math> [1]; <math>C_L = 30\text{ pF}</math></b> |                                                                      |                               |      |      |     |      |
| $t_{PHL}$                                                                                       | propagation delay                                                    |                               |      |      |     |      |
|                                                                                                 | An to Bn or Bn to An                                                 | see <a href="#">Figure 5</a>  | 1.4  | 2.2  | 3.5 | ns   |
|                                                                                                 | LEAB to Bn or LEBA to An                                             | see <a href="#">Figure 6</a>  | 1.5  | 2.5  | 4.0 | ns   |
|                                                                                                 | CPAB to Bn or CPBA to An                                             | see <a href="#">Figure 7</a>  | 1.9  | 3.2  | 5.2 | ns   |
| $t_{PLH}$                                                                                       | propagation delay                                                    |                               |      |      |     |      |
|                                                                                                 | An to Bn or Bn to An                                                 | see <a href="#">Figure 5</a>  | 1.0  | 1.8  | 3.0 | ns   |
|                                                                                                 | LEAB to Bn or LEBA to An                                             | see <a href="#">Figure 6</a>  | 1.5  | 2.5  | 4.0 | ns   |
|                                                                                                 | CPAB to Bn or CPBA to An                                             | see <a href="#">Figure 7</a>  | 2.2  | 3.5  | 5.0 | ns   |
| $t_{PHZ}$                                                                                       | output disable time from HIGH-level                                  | see <a href="#">Figure 9</a>  | 2.2  | 3.1  | 4.4 | ns   |
| $t_{PLZ}$                                                                                       | output disable time from LOW-level                                   | see <a href="#">Figure 10</a> | 1.6  | 2.3  | 3.4 | ns   |
| $t_{PZH}$                                                                                       | output enable time to HIGH-level                                     | see <a href="#">Figure 9</a>  | 2.3  | 3.6  | 4.8 | ns   |
| $t_{PZL}$                                                                                       | output enable time to LOW-level                                      | see <a href="#">Figure 10</a> | 1.9  | 2.9  | 4.4 | ns   |
| $t_{h(H)}$                                                                                      | hold time HIGH                                                       |                               |      |      |     |      |
|                                                                                                 | An to CPAB or Bn to CPBA                                             | see <a href="#">Figure 8</a>  | 0.0  | -1.1 | -   | ns   |
|                                                                                                 | An to LEAB or Bn to LEAB                                             | see <a href="#">Figure 8</a>  | 1.5  | 0.4  | -   | ns   |
|                                                                                                 | $\overline{\text{CEAB}}$ to CPAB or $\overline{\text{CEBA}}$ to CPBA | see <a href="#">Figure 8</a>  | 2.0  | 0.4  | -   | ns   |
| $t_{h(L)}$                                                                                      | hold time LOW                                                        |                               |      |      |     |      |
|                                                                                                 | An to CPAB or Bn to CPBA                                             | see <a href="#">Figure 8</a>  | 0.0  | -0.3 | -   | ns   |
|                                                                                                 | An to LEAB or Bn to LEAB                                             | see <a href="#">Figure 8</a>  | 1.9  | 1.0  | -   | ns   |
|                                                                                                 | $\overline{\text{CEAB}}$ to CPAB or $\overline{\text{CEBA}}$ to CPBA | see <a href="#">Figure 8</a>  | +0.8 | -0.1 | -   | ns   |
| $t_{su(H)}$                                                                                     | set-up time HIGH                                                     |                               |      |      |     |      |
|                                                                                                 | An to CPAB or Bn to CPBA                                             | see <a href="#">Figure 8</a>  | 2.0  | 0.4  | -   | ns   |
|                                                                                                 | An to LEAB or Bn to LEBA                                             | see <a href="#">Figure 8</a>  | 0.0  | -1.0 | -   | ns   |
|                                                                                                 | $\overline{\text{CEAB}}$ to CPAB or $\overline{\text{CEBA}}$ to CPBA | see <a href="#">Figure 8</a>  | 0.7  | 0.3  | -   | ns   |
| $t_{su(L)}$                                                                                     | set-up time LOW                                                      |                               |      |      |     |      |
|                                                                                                 | An to CPAB or Bn to CPBA                                             | see <a href="#">Figure 8</a>  | 2.0  | 1.2  | -   | ns   |
|                                                                                                 | An to LEAB or Bn to LEBA                                             | see <a href="#">Figure 8</a>  | 1.5  | 0.4  | -   | ns   |
|                                                                                                 | $\overline{\text{CEAB}}$ to CPAB or $\overline{\text{CEBA}}$ to CPBA | see <a href="#">Figure 8</a>  | +0.3 | -0.4 | -   | ns   |
| $t_{WH}$                                                                                        | pulse width HIGH                                                     |                               |      |      |     |      |
|                                                                                                 | CPAB or CPBA                                                         | see <a href="#">Figure 7</a>  | 3.0  | -    | -   | ns   |
|                                                                                                 | LEAB or LEBA                                                         | see <a href="#">Figure 6</a>  | 1.5  | -    | -   | ns   |
| $t_{WL}$                                                                                        | pulse width LOW                                                      |                               |      |      |     |      |
|                                                                                                 | CPAB or CPBA                                                         | see <a href="#">Figure 7</a>  | 3.0  | -    | -   | ns   |

**Table 8: Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 11](#).

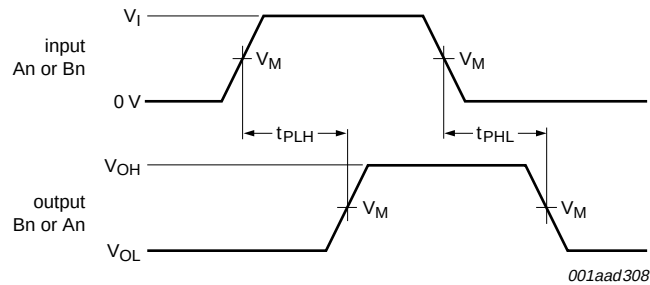
$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

| Symbol                                                                                          | Parameter                                              | Conditions                    | Min  | Typ  | Max | Unit |
|-------------------------------------------------------------------------------------------------|--------------------------------------------------------|-------------------------------|------|------|-----|------|
| <b><math>V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}</math> [2]; <math>C_L = 50\text{ pF}</math></b> |                                                        |                               |      |      |     |      |
| $t_{PHL}$                                                                                       | propagation delay                                      |                               |      |      |     |      |
|                                                                                                 | An to Bn or Bn to An                                   | see <a href="#">Figure 5</a>  | 1.1  | 2.0  | 2.8 | ns   |
|                                                                                                 | LEAB to Bn or LEBA to An                               | see <a href="#">Figure 6</a>  | 1.4  | 2.3  | 3.6 | ns   |
|                                                                                                 | CPAB to Bn or CPBA to An                               | see <a href="#">Figure 7</a>  | 1.7  | 2.7  | 4.1 | ns   |
| $t_{PLH}$                                                                                       | propagation delay                                      |                               |      |      |     |      |
|                                                                                                 | An to Bn or Bn to An                                   | see <a href="#">Figure 5</a>  | 1.2  | 1.9  | 2.9 | ns   |
|                                                                                                 | LEAB to Bn or LEBA to An                               | see <a href="#">Figure 6</a>  | 1.5  | 2.5  | 3.8 | ns   |
|                                                                                                 | CPAB to Bn or CPBA to An                               | see <a href="#">Figure 7</a>  | 2.1  | 3.1  | 4.5 | ns   |
| $t_{PHZ}$                                                                                       | output disable time from HIGH-level                    | see <a href="#">Figure 9</a>  | 2.7  | 3.6  | 4.9 | ns   |
| $t_{PLZ}$                                                                                       | output disable time from LOW-level                     | see <a href="#">Figure 10</a> | 2.1  | 2.8  | 4   | ns   |
| $t_{PZH}$                                                                                       | output enable time to HIGH-level                       | see <a href="#">Figure 9</a>  | 2.2  | 3.2  | 4.2 | ns   |
| $t_{PZL}$                                                                                       | output enable time to LOW-level                        | see <a href="#">Figure 10</a> | 1.6  | 2.5  | 3.8 | ns   |
| $t_{h(H)}$                                                                                      | hold time HIGH                                         |                               |      |      |     |      |
|                                                                                                 | An to CPAB or Bn to CPBA                               | see <a href="#">Figure 8</a>  | +1.0 | -0.5 | -   | ns   |
|                                                                                                 | An to LEAB or Bn to LEAB                               | see <a href="#">Figure 8</a>  | 1.5  | 0.1  | -   | ns   |
|                                                                                                 | $\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA | see <a href="#">Figure 8</a>  | 1.5  | 0.7  | -   | ns   |
| $t_{h(L)}$                                                                                      | hold time LOW                                          |                               |      |      |     |      |
|                                                                                                 | An to CPAB or Bn to CPBA                               | see <a href="#">Figure 8</a>  | +1.0 | -0.3 | -   | ns   |
|                                                                                                 | An to LEAB or Bn to LEAB                               | see <a href="#">Figure 8</a>  | 1.5  | 0.5  | -   | ns   |
|                                                                                                 | $\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA | see <a href="#">Figure 8</a>  | +1.0 | -0.3 | -   | ns   |
| $t_{su(H)}$                                                                                     | set-up time HIGH                                       |                               |      |      |     |      |
|                                                                                                 | An to CPAB or Bn to CPBA                               | see <a href="#">Figure 8</a>  | 1.5  | 0.4  | -   | ns   |
|                                                                                                 | An to LEAB or Bn to LEBA                               | see <a href="#">Figure 8</a>  | +1.0 | -0.5 | -   | ns   |
|                                                                                                 | $\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA | see <a href="#">Figure 8</a>  | 1.5  | 0.3  | -   | ns   |
| $t_{su(L)}$                                                                                     | set-up time LOW                                        |                               |      |      |     |      |
|                                                                                                 | An to CPAB or Bn to CPBA                               | see <a href="#">Figure 8</a>  | 1.5  | 0.6  | -   | ns   |
|                                                                                                 | An to LEAB or Bn to LEBA                               | see <a href="#">Figure 8</a>  | +1.0 | -0.1 | -   | ns   |
|                                                                                                 | $\overline{CEAB}$ to CPAB or $\overline{CEBA}$ to CPBA | see <a href="#">Figure 8</a>  | 1.0  | -0.4 | -   | ns   |
| $t_{WH}$                                                                                        | pulse width HIGH                                       |                               |      |      |     |      |
|                                                                                                 | CPAB or CPBA                                           | see <a href="#">Figure 7</a>  | 2.0  | -    | -   | ns   |
|                                                                                                 | LEAB or LEBA                                           | see <a href="#">Figure 6</a>  | 1.5  | -    | -   | ns   |
| $t_{WL}$                                                                                        | pulse width LOW                                        |                               |      |      |     |      |
|                                                                                                 | CPAB or CPBA                                           | see <a href="#">Figure 7</a>  | 2.0  | -    | -   | ns   |

[1] All typical values are measured at  $V_{CC} = 2.5\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] All typical values are measured at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

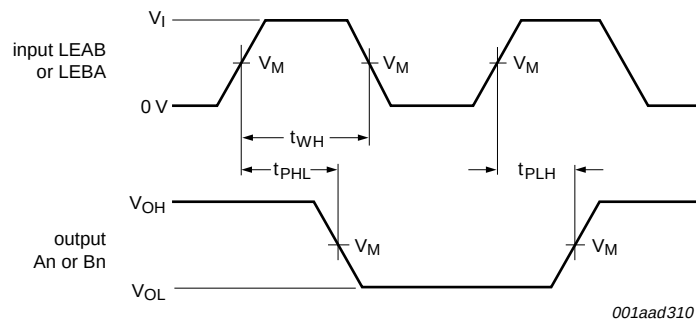
## 12. Waveforms



Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output drop that occur with the output load.

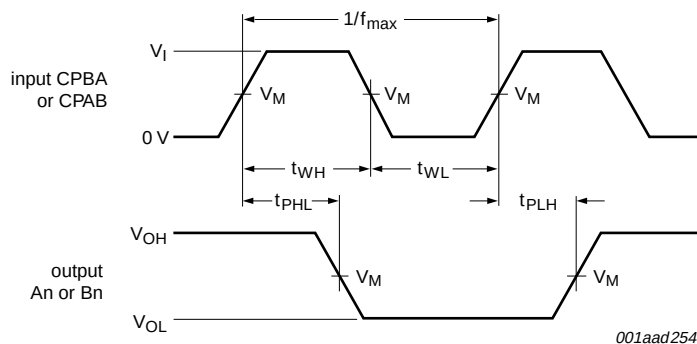
**Fig 5. Propagation delay input (An, Bn) to output (Bn, An) in transparent mode**



Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output drop that occur with the output load.

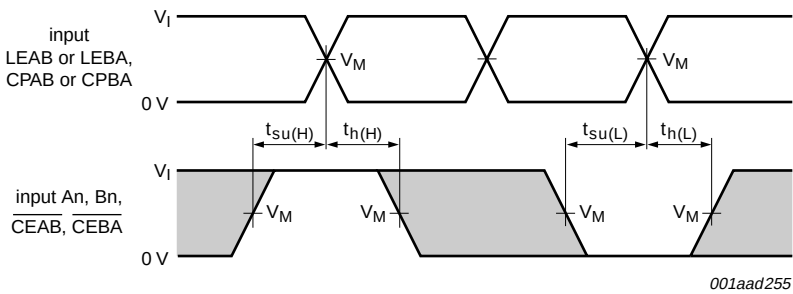
**Fig 6. Propagation delay latch enable (LEAB, LEBA) to output (An, Bn) and latch enable (LEAB, LEBA) pulse width**



Measurement points are given in [Table 9](#).

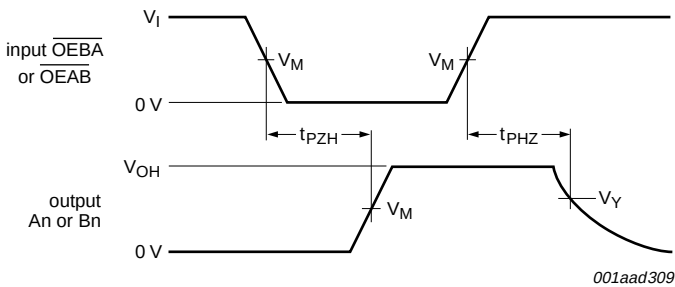
$V_{OL}$  and  $V_{OH}$  are typical voltage output drop that occur with the output load.

**Fig 7. Propagation delay clock input (CPAB, CPBA) to output (An, Bn), clock pulse width (CPAB, CPBA) and maximum clock frequency (CPAB, CPBA)**



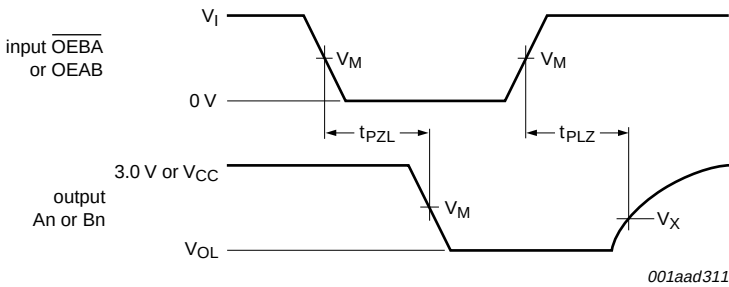
Measurement points are given in [Table 9](#).  
The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 8. Data set-up and hold times



Measurement points are given in [Table 9](#).  
 $V_{OH}$  is typical voltage output drop that occur with the output load.

Fig 9. 3-state output enable time to HIGH-level and output disable time from HIGH-level

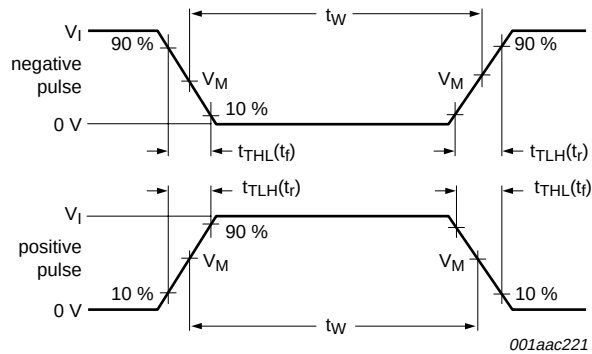


Measurement points are given in [Table 9](#).  
 $V_{OL}$  is typical voltage output drop that occur with the output load.

Fig 10. 3-state output enable time to LOW-level and output disable time from LOW-level

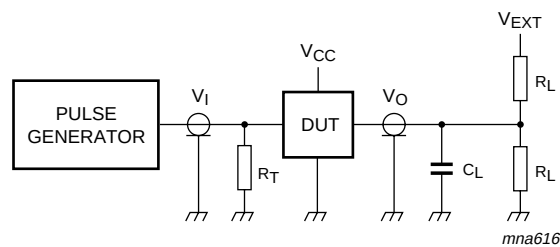
Table 9: Measurement points

| Supply voltage      | Input               | Output              |                          |                          |
|---------------------|---------------------|---------------------|--------------------------|--------------------------|
|                     | $V_M$               | $V_M$               | $V_X$                    | $V_Y$                    |
| $\geq 3\text{ V}$   | 1.5 V               | 1.5 V               | $V_{OL} + 0.3\text{ V}$  | $V_{OH} - 0.3\text{ V}$  |
| $\leq 2.7\text{ V}$ | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15\text{ V}$ | $V_{OH} - 0.15\text{ V}$ |



Measurement points are given in [Table 9](#).

a. Input pulse definition



Test data is given in [Table 10](#).

Definitions test circuit:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = Test voltage for switching times.

b. Test circuit

Fig 11. Load circuitry for switching times

Table 10: Test data

| Input                               |                      |        |                      | Load           |              | $V_{EXT}$                |                    |                    |  |
|-------------------------------------|----------------------|--------|----------------------|----------------|--------------|--------------------------|--------------------|--------------------|--|
| $V_I$                               | $f_i$                | $t_W$  | $t_r, t_f$           | $C_L$          | $R_L$        | $t_{PLZ}, t_{PZL}$       | $t_{PLH}, t_{PHL}$ | $t_{PHZ}, t_{PZH}$ |  |
| 3.0 V or $V_{CC}$ whichever is less | $\leq 10\text{ MHz}$ | 500 ns | $\leq 2.5\text{ ns}$ | 30 pF or 50 pF | 500 $\Omega$ | 6 V or $2 \times V_{CC}$ | open               | GND                |  |

13. Package outline

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm SOT371-1

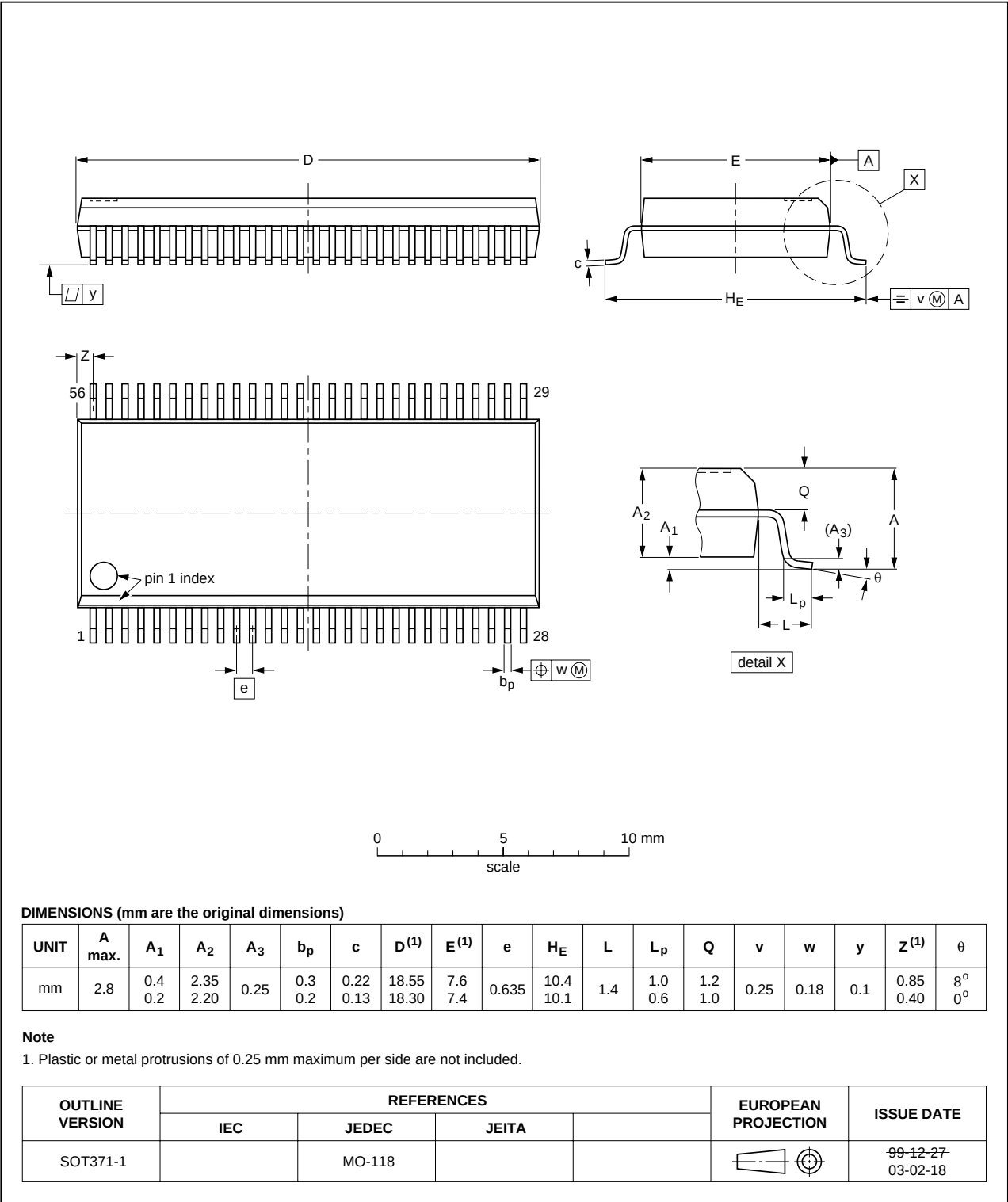


Fig 12. Package outline SOT371-1 (SSOP56)



TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

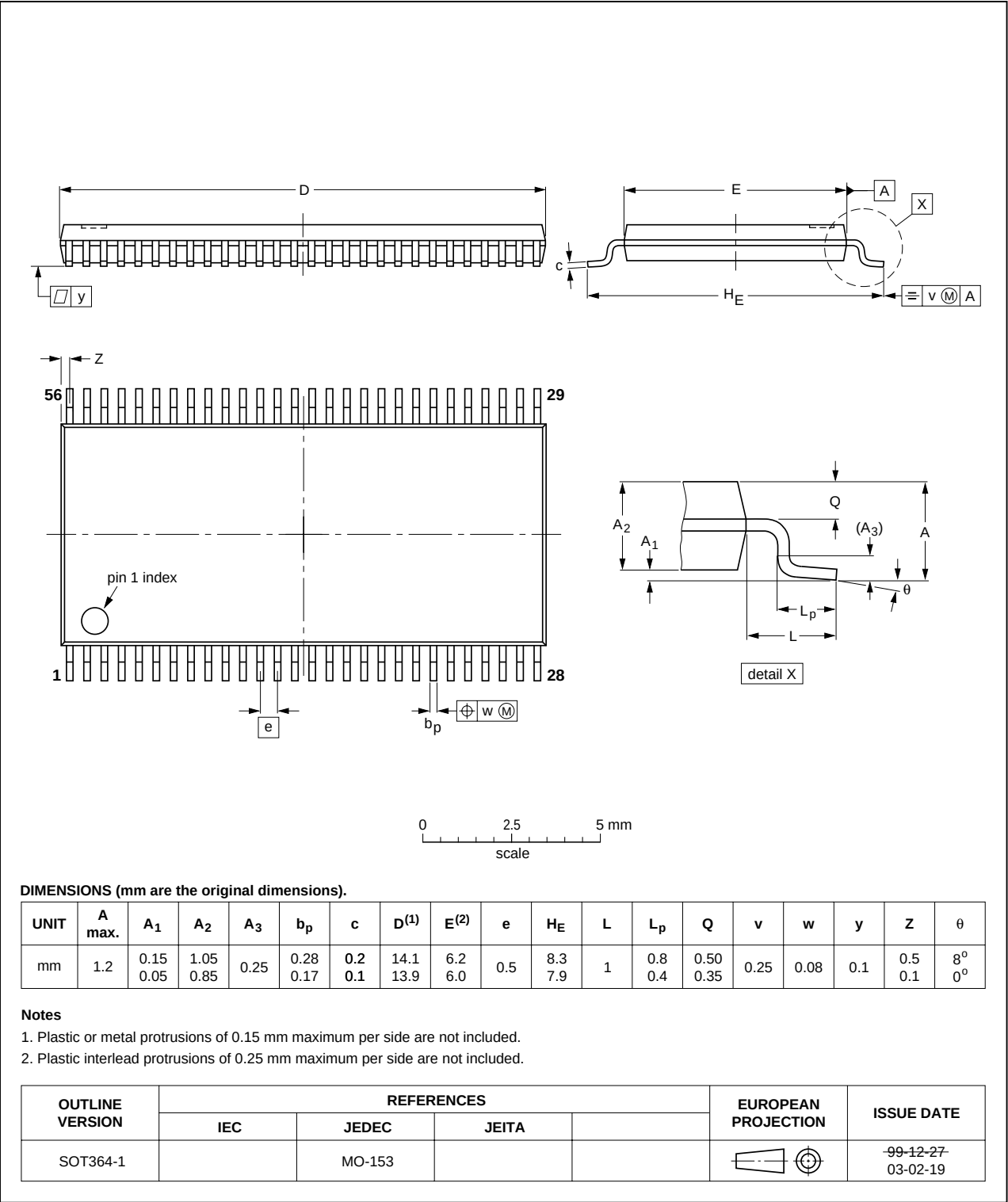


Fig 13. Package outline SOT364-1 (TSSOP56)

14. Revision history

Table 11: Revision history

| Document ID                                                                                                                                                                                                                                                                                                                                                                                                           | Release date | Data sheet status     | Change notice | Doc. number    | Supersedes    |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|-----------------------|---------------|----------------|---------------|
| 74ALVT16601_3                                                                                                                                                                                                                                                                                                                                                                                                         | 20050705     | Product data sheet    | -             | -              | 74ALVT16601_2 |
| Modifications:                                                                                                                                                                                                                                                                                                                                                                                                        |              |                       |               |                |               |
| <ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li><li><a href="#">Section 2 “Features”</a>: modified ‘JEDEC Std 17’ into ‘JESD78’.</li><li><a href="#">Table 8 “Dynamic characteristics”</a>: changed values of propagation delay, output enable and output disable time.</li></ul> |              |                       |               |                |               |
| 74ALVT16601_2                                                                                                                                                                                                                                                                                                                                                                                                         | 19980213     | Product specification | -             | 9397 750 03571 | 74ALVT16601_1 |
| 74ALVT16601_1                                                                                                                                                                                                                                                                                                                                                                                                         | -            | -                     | -             | -              | -             |

## 15. Data sheet status

| Level | Data sheet status <sup>[1]</sup> | Product status <sup>[2] [3]</sup> | Definition                                                                                                                                                                                                                                                                                     |
|-------|----------------------------------|-----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I     | Objective data                   | Development                       | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.                                                                                                    |
| II    | Preliminary data                 | Qualification                     | This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.             |
| III   | Product data                     | Production                        | This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). |

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## 16. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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