

SN74SSTL16837A 20-BIT SSTL_3 INTERFACE UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

SCBS675G – SEPTEMBER 1996 – REVISED SEPTEMBER 1998

- Member of the Texas Instruments *Widebus™* Family
- Supports SSTL_3 Signal Inputs and Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Meets SSTL_3 Class I and Class II Specifications
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Packaged in Plastic Thin Shrink Small-Outline Package

description

This 20-bit universal bus driver is designed for 3-V to 3.6-V V_{CC} operation and SSTL_3 or LVTTTL I/O levels.

Data flow from A to Y is controlled by the output-enable (\overline{OE}) input. The device operates in the transparent mode when latch enable (LE) is high. The A data is latched if LE is low and clock (CLK) is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74SSTL16837A is characterized for operation from 0°C to 70°C.

DGG PACKAGE
(TOP VIEW)

| | | | |
|-----------------|----|----|----------|
| Y1 | 1 | 64 | A1 |
| Y2 | 2 | 63 | A2 |
| GND | 3 | 62 | GND |
| Y3 | 4 | 61 | A3 |
| Y4 | 5 | 60 | A4 |
| V_{DDQ} | 6 | 59 | V_{CC} |
| Y5 | 7 | 58 | A5 |
| Y6 | 8 | 57 | A6 |
| GND | 9 | 56 | GND |
| Y7 | 10 | 55 | A7 |
| Y8 | 11 | 54 | A8 |
| V_{DDQ} | 12 | 53 | V_{CC} |
| Y9 | 13 | 52 | A9 |
| Y10 | 14 | 51 | A10 |
| GND | 15 | 50 | GND |
| \overline{OE} | 16 | 49 | CLK |
| V_{REF} | 17 | 48 | LE |
| GND | 18 | 47 | GND |
| Y11 | 19 | 46 | A11 |
| Y12 | 20 | 45 | A12 |
| V_{DDQ} | 21 | 44 | V_{CC} |
| Y13 | 22 | 43 | A13 |
| Y14 | 23 | 42 | A14 |
| GND | 24 | 41 | GND |
| Y15 | 25 | 40 | A15 |
| Y16 | 26 | 39 | A16 |
| V_{DDQ} | 27 | 38 | V_{CC} |
| Y17 | 28 | 37 | A17 |
| Y18 | 29 | 36 | A18 |
| GND | 30 | 35 | GND |
| Y19 | 31 | 34 | A19 |
| Y20 | 32 | 33 | A20 |



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| INPUTS | | | | OUTPUT Y |
|--------|----|-----|---|----------------|
| OE | LE | CLK | A | |
| L | H | X | H | H |
| L | H | X | L | L |
| L | L | ↑ | H | H |
| L | L | ↑ | L | L |
| L | L | H | X | Y_0^\dagger |
| L | L | L | X | Y_0^\ddagger |
| H | X | X | X | Z |

‡ Output level before the indicated steady-state input conditions were established

The diagram illustrates a single channel of a 20-channel 16-bit counter. The counter block has inputs \overline{OE} (16), CLK (49), LE (48), and A1 (64). The output Y1 (1) is shown. The counter is connected to 19 other channels via a bus structure.

| | |
|---|-----------------------------|
| Supply voltage range, V_{CC} or V_{DDQ} | −0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | −0.5 V to $V_{CC} + 0.5$ V |
| Output voltage range, V_O (see Notes 1 and 2) | −0.5 V to $V_{DDQ} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | −50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | −50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{DDQ}) | ±50 mA |
| Continuous current through each V_{CC} , V_{DDQ} , or GND | ±100 mA |
| Package thermal impedance, θ_{JA} (see Note 3) | 73°C/W |
| Storage temperature range, T_{sta} | −65°C to 150°C |

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{DDQ}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

| | | MIN | NOM | MAX | UNIT |
|------------------|---|------------------------|------------------|-------------------------|------|
| V _{CC} | Supply voltage | V _{DDQ} | | 3.6 | V |
| V _{DDQ} | Output supply voltage | 3 | | 3.6 | V |
| V _{REF} | Reference voltage (V _{REF} = 0.45 × V _{DDQ}) | 1.3 | 1.5 | 1.7 | V |
| V _{TT} | Termination voltage (V _{REF} = V _{TT} = 0.45 × V _{DDQ}) | V _{REF} –50mV | V _{REF} | V _{REF} +50mV | V |
| V _I | Input voltage | 0 | | V _{CC} | V |
| V _{IH} | AC high-level input voltage | All inputs | | V _{REF} +400mV | V |
| V _{IL} | AC low-level input voltage | All inputs | | V _{REF} –400mV | V |
| V _{IH} | DC high-level input voltage | All inputs | | V _{REF} +200mV | V |
| V _{IL} | DC low-level input voltage | All inputs | | V _{REF} –200mV | V |
| I _{OH} | High-level output current | | | –20 | mA |
| I _{OL} | Low-level output current | | | 20 | |
| T _A | Operating free-air temperature | 0 | | 70 | °C |

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | V _{CC} | MIN | TYP† | MAX | UNIT |
|-----------------|------------------------------|---------------------------------|-----------------------------------|-----------------|----------------------|------|------|------|
| V _{IK} | | I _I = −18 mA | | 3 V | | | −1.2 | V |
| V _{OH} | | I _{OH} = −100 μA | | 3 V to 3.6 V | V _{CC} −0.2 | | | V |
| | | I _{OH} = −16 mA | | 3 V | 2.2 | | | |
| | | I _{OH} = −20 mA | | | 2.1 | | | |
| V _{OL} | | I _{OL} = 100 μA | | 3 V to 3.6 V | | | 0.2 | V |
| | | I _{OL} = 16 mA | | 3 V | | | 0.5 | |
| | | I _{OL} = 20 mA | | | | | 0.55 | |
| I _I | LE | V _I = 2.1 V or 0.9 V | V _{REF} = 1.3 V or 1.7 V | 3.6 V | | | ±40 | μA |
| | | V _I = 3.6 V or 0 | | | | | ±1.2 | mA |
| | Data inputs, \overline{OE} | V _I = 2.1 V or 0.9 V | V _{REF} = 1.3 V or 1.7 V | 3.6 V | | | ±5 | μA |
| | | V _I = 3.6 V or 0 | | | | | ±5 | |
| | CLK | V _I = 2.1 V or 0.9 V | V _{REF} = 1.3 V or 1.7 V | 3.6 V | | | ±150 | mA |
| | | V _I = 3.6 V or 0 | | | | | ±4 | |
| | V _{REF} | | V _{REF} = 1.3 V or 1.7 V | | 3.6 V | | | ±150 |
| I _{OZ} | | V _O = 0.9 V or 2.1 V | | 3.6 V | | | ±10 | μA |
| | | V _O = 0 or 3.6 V | | | | | ±10 | |
| I _{CC} | | V _I = 2.1 V or 0.9 V | I _O = 0 | 3.6 V | | | 90 | mA |
| | | V _I = 3.6 V or 0 | | | | | 90 | |
| C _i | Control inputs | V _I = 2.1 V or 0.9 V | | 3.3 V | 2.5 | | | pF |
| | A port | | | | 2 | | | |
| C _O | Y port | V _O = 2.1 V or 0.9 V | | 3.3 V | 3 | | | pF |

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | UNIT |
|--------------------|-----------------|--------------------------|----------|---|-----|------|
| | | | | MIN | MAX | |
| f_{clock} | Clock frequency | | | 200 | | MHz |
| t_w | Pulse duration | LE high | | 2.5 | | ns |
| | | CLK high or low | | 2.5 | | |
| t_{su} | Setup time | A before CLK \uparrow | LE low | 1.5 | | ns |
| | | A before LE \downarrow | CLK high | 1.5 | | |
| | | | CLK low | 2 | | |
| t_h | Hold time | A after CLK \uparrow | LE low | 1 | | ns |
| | | A after LE \downarrow | | 1 | | |

switching characteristics over recommended operating free-air temperature range,
Class I, $V_{\text{REF}} = V_{\text{TT}} = V_{\text{DDQ}} \times 0.45$ and $C_L = 10\text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | UNIT |
|------------------|------------------------|----------------|---|-----|------|
| | | | MIN | MAX | |
| f_{max} | | | 200 | | MHz |
| t_{pd} | A | Y | 1.1 | 4 | ns |
| | LE | | 1.5 | 4.1 | |
| | CLK | | 1 | 3 | |
| t_{en} | $\overline{\text{OE}}$ | Y | 1.8 | 5.5 | ns |
| t_{dis} | $\overline{\text{OE}}$ | Y | 1.8 | 6 | ns |

switching characteristics over recommended operating free-air temperature range,
Class II, $V_{\text{REF}} = V_{\text{TT}} = V_{\text{DDQ}} \times 0.45$ and $C_L = 30\text{ pF}$ (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | UNIT |
|------------------|------------------------|----------------|---|-----|------|
| | | | MIN | MAX | |
| f_{max} | | | 200 | | MHz |
| t_{pd} | A | Y | 1.1 | 4.2 | ns |
| | LE | | 1.5 | 4.3 | |
| | CLK | | 1 | 3.2 | |
| t_{en} | $\overline{\text{OE}}$ | Y | 1.8 | 5.5 | ns |
| t_{dis} | $\overline{\text{OE}}$ | Y | 1.8 | 6 | ns |

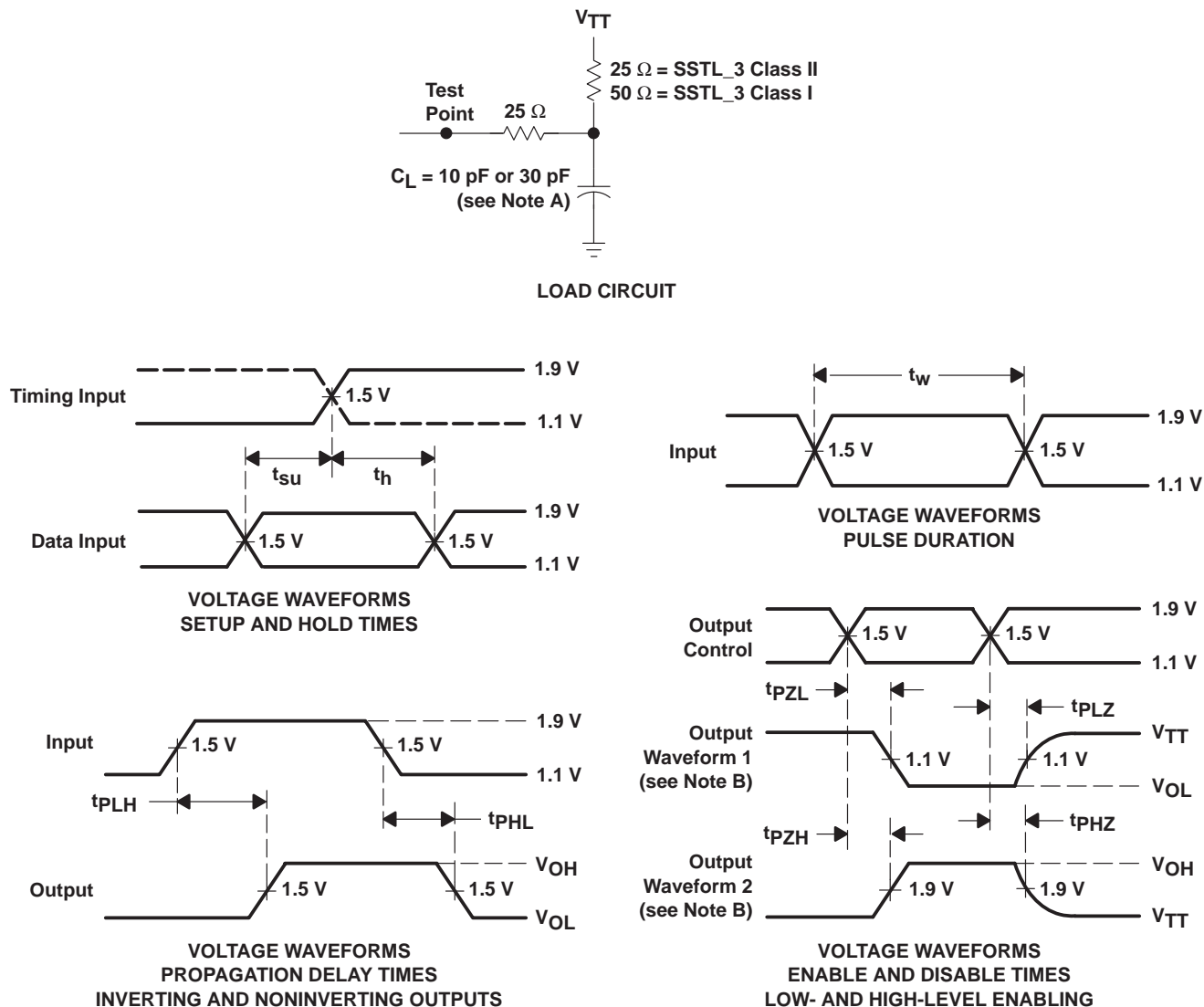
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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 1 \text{ ns}$, $t_f \leq 1 \text{ ns}$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. $V_{TT} = V_{REF} = V_{CC} \times 0.45$
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PHL} and t_{PLH} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

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