TwinDie™ DDR2 SDRAM

MT47H512M4 – 32 Meg x 4 x 8 Banks x 2 Ranks
MT47H256M8 – 16 Meg x 8 x 8 Banks x 2 Ranks

For the latest component data sheet, refer to Micron's Web site: www.micron.com

Functionality

The 2Gb (TwinDie™) DDR2 SDRAM uses Micron's 1Gb DDR2 monolithic die and, therefore, has similar functionality. This TwinDie data sheet is intended to provide a general description, package dimensions, and the ballout only. Refer to the Micron 1Gb DDR2 data sheet for complete information regarding individual die initialization, register definition, command descriptions, and die operation.

Features

- Uses 1Gb Micron die
- Two ranks (includes dual CS#, ODT, and CKE balls)
- Each rank has 8 internal banks for concurrent operation
- $V_{DD} = V_{DDQ} = +1.8V \pm 0.1V$
- JEDEC-standard 63-ball ballout
- Low-profile package size (1.2mm MAX thickness)

Options / Marking

Options	Marking
• Configuration	
– 32 Meg x 4 x 8 banks x 2 ranks	512M4
– 16 Meg x 8 x 8 banks x 2 ranks	256M8
• FBGA package (lead-free)	
– 63-ball FBGA (8mm x 10mm)	THN
• Timing – cycle time[1]	
– 2.5ns @ CL = 5 (DDR2-800)	-25E
– 3.0ns @ CL = 5 (DDR2-667)	-3
• Self refresh	
– Standard	None
• Operating temperature	
– Commercial ($0°C \le T_C \le 85°C$)	None
– Industrial ($-40°C \le T_C \le 95°C$; $-40°C \le T_A \le 85°C$)	IT
• Revision	:H

Notes: 1. CL = CAS (READ) latency

Table 1: Key Timing Parameters

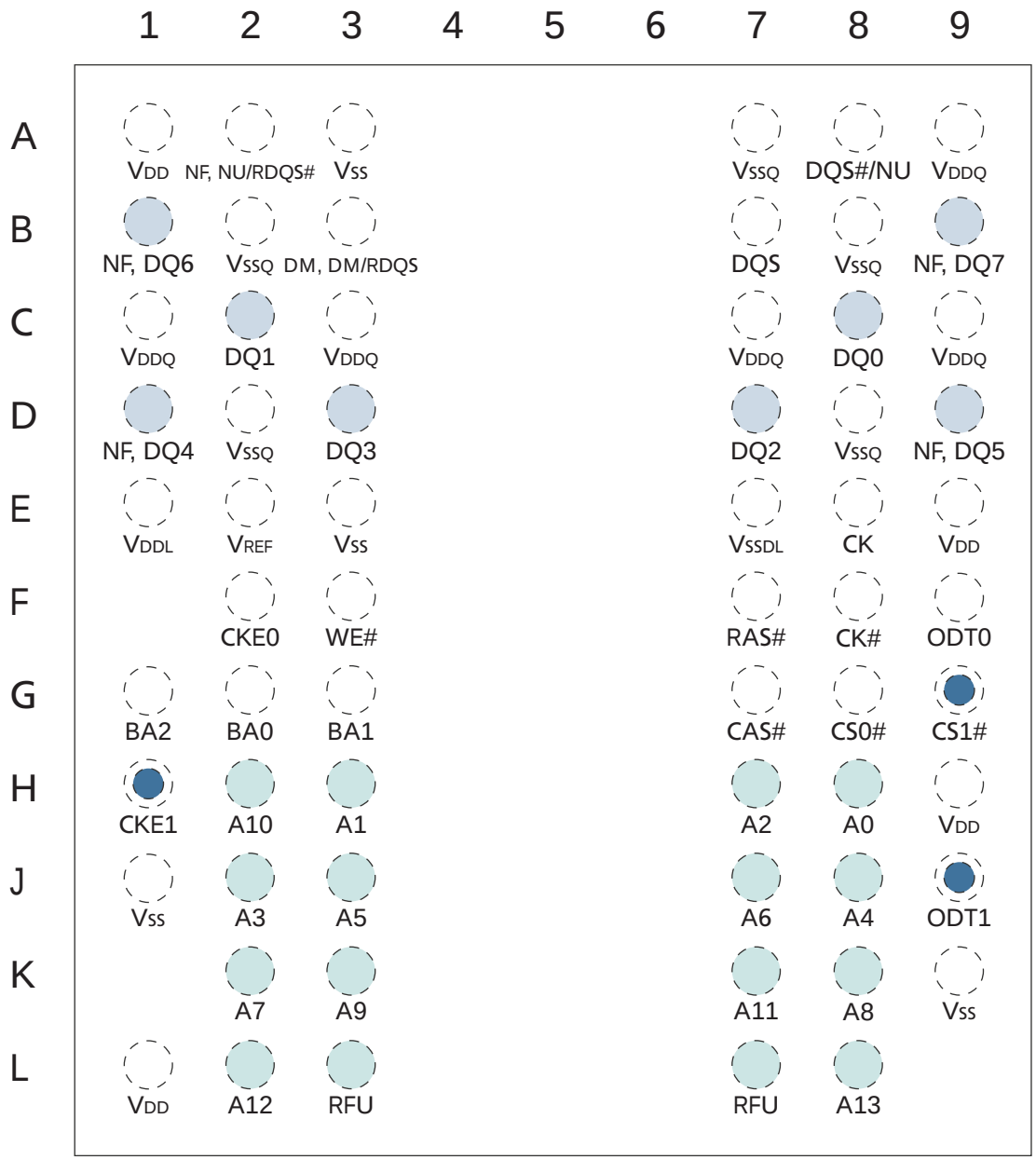
Speed Grade	Data Rate (MT/s)				^tRCD (ns)	^tRP (ns)	^tRC (ns)	^tRFC (ns)
	CL = 6	CL = 5	CL = 4	CL = 3				
-25E	–	800	533	–	12.5	12.5	55	127.5
-3	–	667	533	400	15	15	55	127.5

Table 2: Addressing

Parameter	256 Meg x 8	512 Meg x 4
Refresh count	8K	8K
Row address	16K A[13:0]	16K A[13:0]
Bank address	8 BA[2:0]	8 BA[2:0]
Configuration	16 Meg x 8 x 8 x 2	32 Meg x 4 x 8 x 2
Column address	1K A[9:0]	2K A[9:0], A11
Rank address	2 CS#[1:0]	2 CS#[1:0]

Ball Assignments and Descriptions

Figure 1: 63-Ball FBGA Assignments – x4, x8 (Top View)



Notes: 1. The three balls with dots designate balls that differ from the monolithic versions.

Table 3: 63-Ball FBGA Ball Descriptions – x4, x8

Symbol	Type	Description
A[13:0]	Input	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a precharge command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA[2:0]) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR, EMR1, EMR2, and EMR3) is loaded during the LOAD MODE command.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#.
CKE[1:0]	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) the internal circuitry and clocks on the DDR2 SDRAM.
DM	Input	**Input data mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with the input data, during a write access. DM is sampled on both edges of DQS. Although the DM balls are input-only, DM loading is designed to match that of the DQ and DQS balls.
ODT[1:0]	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR2 SDRAM. When enabled in normal operation, ODT is applied only to the following balls: DQ, DQS, DQS#, and DM. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered.
CS#[1:0]	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder.
DQ[3:0]	I/O	**Data input/output:** Bidirectional data bus for the x4 configuration.
DQ[7:0]	I/O	**Data input/output:** Bidirectional data bus for the x8 configuration.
DQS#, DQS	I/O	**Data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned with write data. DQS# is used only when differential data strobe mode is enabled via the LOAD MODE command.
RDQS, RDQS#	I/O	**Redundant data strobe:** For the x8 configuration only. RDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When RDQS is enabled, RDQS is output with read data only and is ignored during write data. When RDQS is disabled, B3 becomes data mask (see DM ball). RDQS# is only used when both RDQS and the differential data strobe mode are enabled.
V_{DD}	Supply	**Power supply:** 1.8V ±0.1V.
V_{DDL}	Supply	**DLL power supply:** 1.8V ±0.1V.
V_{DDQ}	Supply	**DQ power supply:** 1.8V ±0.1V. Isolated on the device for improved noise immunity.
V_{REF}	Supply	**Reference voltage:** $V_{DD}/2$.
V_{SS}	Supply	Ground.
V_{SSDL}	Supply	**DLL ground:** Isolated on the device from Vss and Vssq.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
NF	–	**No function:** These balls provide no functionality on the x4 configuration only.
NU	–	**Not used:** For the x8 configuration only. If EMR(E10) = 0, A2 is RDQS# and A8 is DQS#. If EMR(E10) = 1, then A2 and A8 are not used.
RFU	–	**Reserved for future use:** Row address bits A14 and A15.

Functional Description

The 2Gb (TwinDie) DDR2 SDRAM is a high-speed, CMOS dynamic random access memory device that contains 2,147,483,648 bits and is internally configured as two 8-bank 1Gb DDR2 SDRAM devices.

Although each die is tested individually within the dual-die package, some TwinDie test results may vary from a like die tested within a monolithic die package.

Each DDR2 SDRAM die uses a double data rate architecture to achieve high-speed operation. The DDR2 architecture is essentially a 4*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access consists of a single 4*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

Addressing of the TwinDie is identical to the monolithic device. Additionally, multiple chip selects select the desired rank.

This TwinDie data sheet is intended to provide a general description, package dimensions, and the ballout only. Refer to the Micron 1Gb DDR2 data sheet for complete information regarding individual die initialization, register definition, command descriptions, and die operation.

Functional Block Diagrams

Figure 2: Functional Block Diagram (32 Meg x 4 x 8 Banks x 2 Ranks)

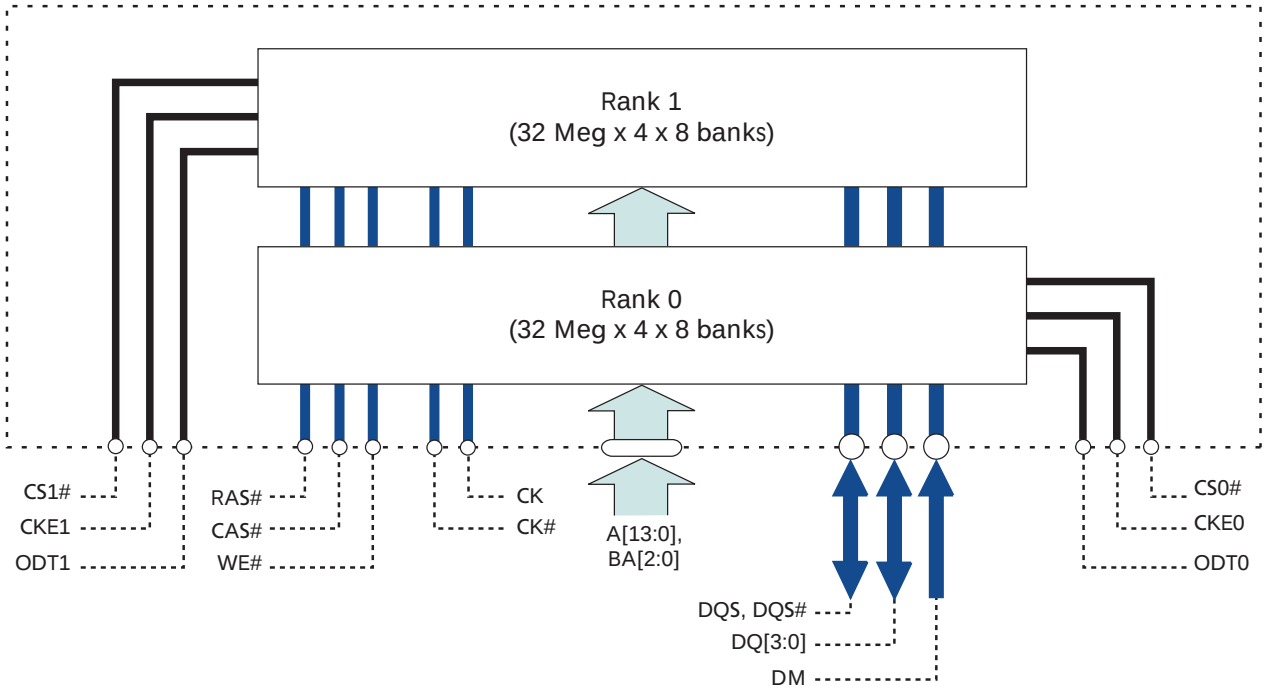
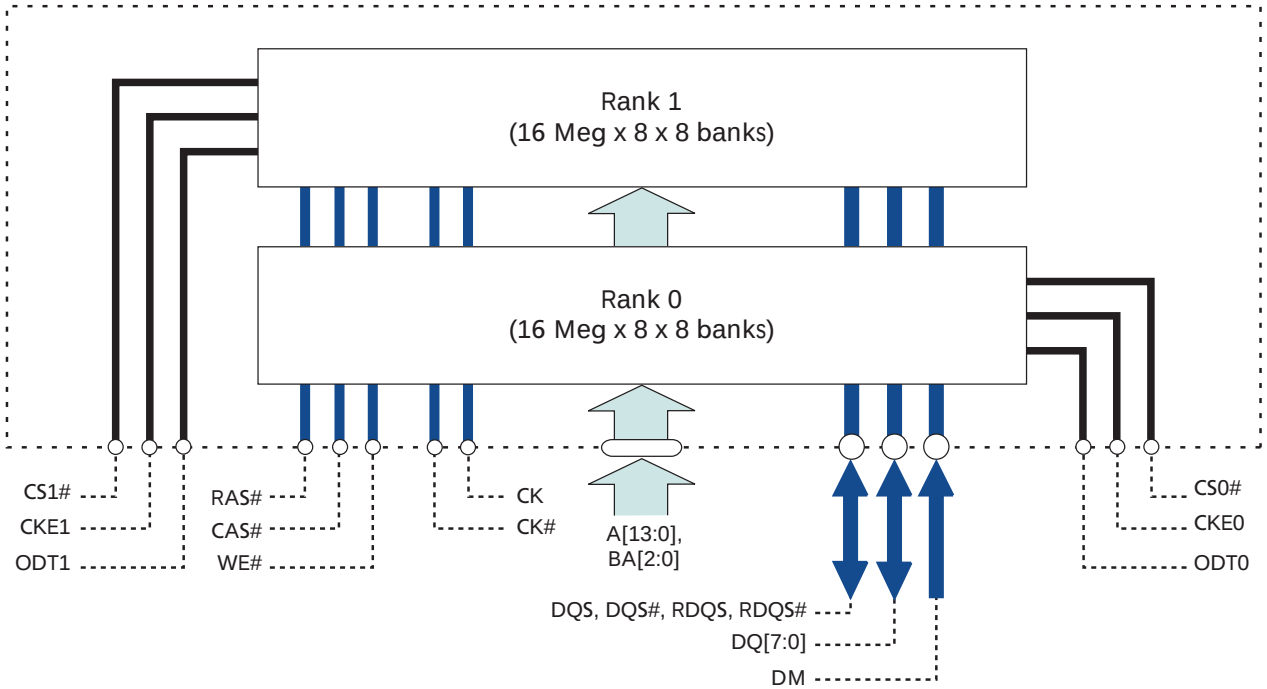


Figure 3: Functional Block Diagram (16 Meg x 8 x 8 Banks x 2 Ranks)



Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the devices at these or any other conditions outside those indicated in the device data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–1.0	+2.3	V	1
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SSQ}	–0.5	+2.3	V	1, 2
V_{DDL}	V_{DDL} supply voltage relative to V_{SSDL}	–0.5	+2.3	V	1
V_{IN}, V_{OUT}	Voltage on any ball relative to V_{SS}	–0.5	+2.3	V	3
I_I	Input leakage current; Any input $0V \le V_{IN} \le V_{DD}$ (All other balls not under test = 0V)	–10	+10	µA	
I_{OZ}	Output leakage current; $0V \le V_{OUT} \le V_{DDQ}$; DQ and ODT are disabled	–10	+10	µA	
I_{VREF}	V_{REF} leakage current; V_{REF} = valid V_{REF} level	–4	+4	µA	

Notes:
1. V_{DD}, V_{DDQ}, and V_{DDL} must be within 300mV of each other at all times.
2. $V_{REF} \le 0.6 \times V_{DDQ}$; however, V_{REF} may be $\ge V_{DDQ}$ provided that $V_{REF} \le 300mV$.
3. Voltage on any I/O may not exceed voltage on V_{DDQ}.

Temperature and Thermal Impedance

It is imperative that the DDR2 SDRAM device's temperature specifications, shown in Table 5 on page 7, be maintained to ensure the junction temperature is in the proper operating range to meet data sheet specifications. An important step in maintaining the proper junction temperature is using the device's thermal impedances correctly. Thermal impedances listed in Table 5 on page 7 apply to the current die revision and its packages.

Incorrectly using thermal impedances can produce significant errors. Read Micron technical note TN-00-08: "Thermal Applications" prior to using the thermal impedances in Table 6 on page 7. For designs that are expected to last several years and require the flexibility to use several DRAM die shrinks, consider using final target theta values (rather than existing values) to account for increased thermal impedances from the reduction in die size.

The DDR2 SDRAM device's safe junction temperature range can be maintained when the T_C specifications are not exceeded. In applications where the device's ambient temperature is too high, use of forced air and/or heat sinks may be required to satisfy the case temperature specifications.

Table 5: Temperature Limits

Symbol	Parameter	Min	Max	Units	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_C	Operating temperature – commercial	0	85	°C	2, 3

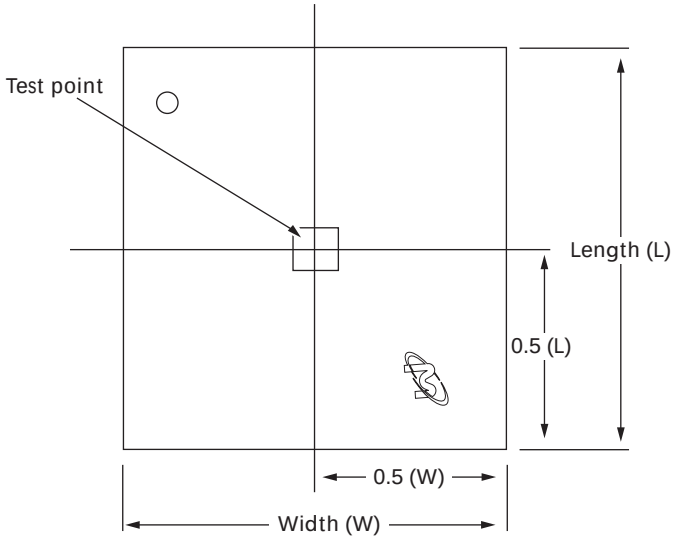
Notes:
1. Maximum storage case temperature; T_{STG} is measured in the center of the package, as shown in Figure 4. This case temperature limit is allowed to be exceeded briefly during package reflow, as noted in technical note TN-00-15: "Recommended Soldering Parameters," available on Micron's Web site.
2. Maximum operating case temperature; T_C is measured in the center of the package, as shown in Figure 4.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.

Table 6: Thermal Impedance

Die Rev	Package	Substrate	θ JA (°C/W) Airflow = 0m/s	θ JA (°C/W) Airflow = 1m/s	θ JA (°C/W) Airflow = 2m/s	θ JB (°C/W)	θ JC (°C/W)	Notes
H	63-ball	2-layer	71.8	54.3	48.3	35.3	5.5	1
		4-layer	54.1	44.8	41.3	34.9		

Notes:
1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Figure 4: Temperature Test Point Location



Lmm x Wmm FBGA

I_{CDD} Specifications and Conditions

Table 7: DDR2 I_{CDD} Specifications and Conditions

Notes: 1–8 apply to the entire document; notes appear on page 9

Parameter/Condition	Combined Symbol	Individual Die Status	-25E	-3	Units
Operating one bank active-precharge current: $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD0}	$I_{CDD0} = I_{DD0} + I_{DD2P}$	72	67	mA
Operating one bank active-read-precharge current: I_{OUT} = 0mA; Burst length (BL) = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRC = {}^tRC (I_{DD})$, $^tRAS = {}^tRAS$ MIN (I_{DD}), $^tRCD = {}^tRCD (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data pattern is the same as I_{DD4W} (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD1}	$I_{CDD1} = I_{DD1} + I_{DD2P}$	82	77	mA
Precharge power-down current: All banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	I_{CDD2P}	$I_{CDD2P} = I_{DD2P} + I_{DD2P}$	14	14	mA
Precharge quiet standby current: All banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	I_{CDD2Q}	$I_{CDD2Q} = I_{DD2Q} + I_{DD2P}$	31	31	mA
Precharge standby current: All banks idle; $^tCK = {}^tCK (I_{DD})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD2N}	$I_{CDD2N} = I_{DD2N} + I_{DD2P}$	35	31	mA
Active power-down current: All banks open; $^tCK = {}^tCK (I_{DD})$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating (individual die status: $I_{CDD3P} = I_{DD3P} + I_{DD2P}$)	I_{CDD3P}	Fast PDN exit MR[12] = 0	27	22	mA
		Slow PDN exit MR[12] = 1	17	17	mA
Active standby current: All banks open; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD3N}	$I_{CDD3N} = I_{DD3N} + I_{DD2P}$	40	37	mA
Operating burst write current: All banks open; Continuous burst writes; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD4W}	$I_{CDD4W} = I_{DD4W} + I_{DD2P}$	132	127	mA
Operating burst read current: All banks open; Continuous burst reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = 0; $^tCK = {}^tCK (I_{DD})$, $^tRAS = {}^tRAS$ MAX (I_{DD}), $^tRP = {}^tRP (I_{DD})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD4R}	$I_{CDD4R} = I_{DD4R} + I_{DD2P}$	122	117	mA
Burst refresh current: $^tCK = {}^tCK (I_{DD})$; REFRESH command at every $^tRFC (I_{DD})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD5}	$I_{CDD5} = I_{DD5} + I_{DD2P}$	152	147	mA

Table 7: DDR2 I_{CDD} Specifications and Conditions (continued)

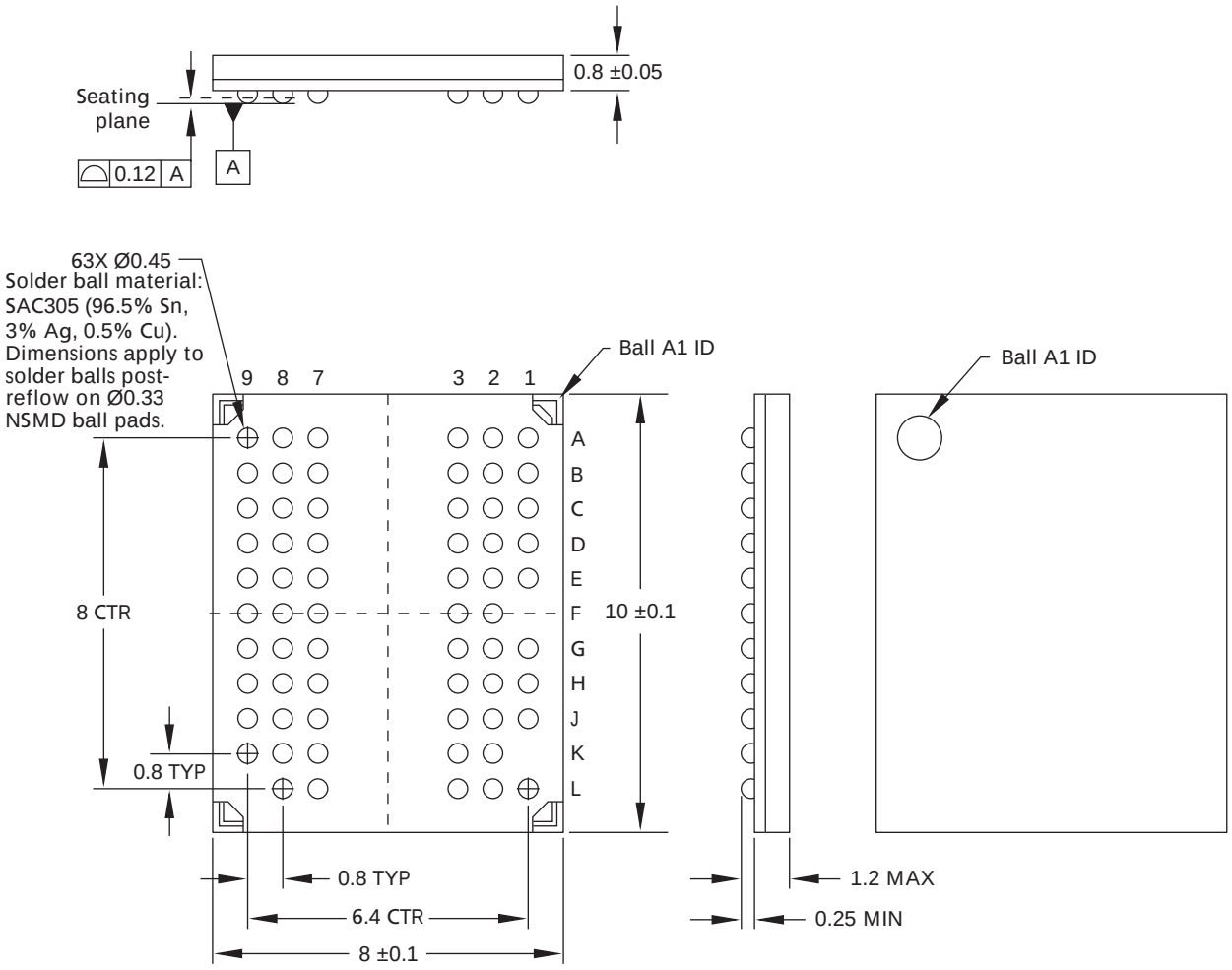
Notes: 1–8 apply to the entire document; notes appear on page 9

Parameter/Condition	Combined Symbol	Individual Die Status	-25E	-3	Units
Self refresh current: CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are floating; Data bus inputs are floating	I_{CDD6}	I_{CDD6} = I_{DD6} + I_{DD6}	14	14	mA
Operating bank interleave read current: All banks interleaving reads; I_{OUT} = 0mA; BL = 4, CL = CL (I_{DD}), AL = ^{t}RCD (I_{DD}) - 1 × ^{t}CK (I_{DD}); ^{t}CK = ^{t}CK (I_{DD}), ^{t}RC = ^{t}RC (I_{DD}), ^{t}RRD = ^{t}RRD (I_{DD}), ^{t}RCD = ^{t}RCD (I_{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching (inactive die is in I_{DD2P} condition, but with inputs switching)	I_{CDD7}	I_{CDD7} = I_{DD7} + I_{DD2P}	217	192	mA

Notes:
1. I_{CDD}/I_{DD} specifications are tested after the device is properly initialized. 0°C ≤ T_C ≤ +85°C. V_{DD} = V_{DDQ} = +1.8V ±0.1V; V_{DDL} = +1.8V ±0.1V; V_{REF} = V_{DDQ}/2.
2. I_{CDD}/I_{DD} parameters are specified with ODT disabled.
3. Data bus consists of DQ, DM, DQS, DQS#, RDQS, and RDQS#.
4. I_{CDD}/I_{DD} values must be met with all combinations of EMR bits 10 and 11.
5. Definitions for Icdd/Idd conditions:
   - 5a. LOW: $V_{IN} \leq V_{IL(AC)max}$
   - 5b. HIGH: $V_{IN} \geq V_{IH(AC)min}$
   - 5c. Stable: Inputs stable at a HIGH or LOW level
   - 5d. Floating: Inputs at V_{REF} = V_{DDQ}/2
   - 5e. Switching: Inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals
   - 5f. Switching: Inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, not including masks or strobes
6. I_{DD1}, I_{DD4R}, and I_{DD7} require EMR1, A12 to be enabled during testing.
7. I_{CDD}/I_{DD} values reflect the combined current of both individual die. I_{DDX} represents individual die values.
8. The following I_{DD} values must be derated (I_{DD} limits increase) on IT-option devices when operated outside of the range 0°C ≤ T_C ≤ 85°C:
   - 8a. When T_C ≤ 0°C
     I_{DD2P} and $I_{DD3P(SLOW)}$ must be derated by 4%; I_{DD4R} and I_{DD5W} must be derated by 2%; and I_{DD6} and I_{DD7} must be derated by 7%
   - 8b. When T_C ≥ 85°C
     I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2Q}, I_{DD3N}, $I_{DD3P(FAST)}$, I_{DD4R}, I_{DD4W}, and I_{DD5W} must be derated by 2%; I_{DD2P} must be derated by 20%; $I_{DD3P(SLOW)}$ must be derated by 30%; and I_{DD6} must be derated by 80% (I_{DD6} will increase by this amount if T_C < 85°C and the 2X refresh option is still enabled)

Package Dimensions

Figure 5: 63-Ball FBGA Package Dimensions (Part Rev. H)



Notes: 1. All dimensions are in millimeters.