MX25L1602

16M-BIT [16M x 1] CMOS SERIAL FLASH EEPROM

FEATURES

GENERAL

- 16,777,216 x 1 bit structure
- 256 Equal Sectors with 8K-byte each
  - Any sector can be erased
- 4096 Equal Segments with 512-byte each
  - Provides sequential output within any segment
- Single Power Supply Operation
  - 3.0 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Low Vcc write inhibit is equal to or less than 2.5V

PERFORMANCE

- High Performance
  - Fast access time: 20MHz serial clock (50pF + 1TTL Load)
  - Fast program time: 5ms/page (typical, 128-byte per page)
  - Fast erase time: 300ms/sector (typical, 8K-byte per sector)
- Low Power Consumption
  - Low active read current: 10mA (typical) at 17MHz
  - Low active programming current: 10mA (typical)
  - Low active erase current: 10mA (typical)
  - Low standby current: 30uA (typical, CMOS)
- Minimum 100,000 erase/program cycle

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code, 3-byte address, 1-byte byte address
- 512-byte Sequential Read Operation
- Built in 9-bit (A0 to A8) pre-settable address counter to support the 512-byte sequential read operation
- Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algroithm that automatically times the program pulse widths (Any page to be programed should have page in the erased state first)
- Status Register Feature
  - Provides detection of program and erase operation completion.
  - Provides auto erase/ program error report

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI Input
  - Serial Data Input
- SO Output
  - Serial Data Output
- PACKAGE
  - 28-pin SOP (330mil)

GENERAL DESCRIPTION

The MX25L1602 is a CMOS 16,777,216 bit serial Flash EEPROM, which is configured as 2,097,152 x 8 internally. The MX25L1602 features a serial peripheral interface and software protocol allowing operation on a simple 3- wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by $\overline{CS}$ input.

The MX25L1602 provide sequential read operation on whole chip. The sequential read operation is executed on a segment (512 byte) basis. User may start to read from any byte of the segment. While the end of the segment is reached, the device will wrap around to the beginning of the segment and continuously outputs data until $\overline{CS}$ goes high.

After program/erase command is issued, auto program/ erase algorithms which program/erase and verify the specified page locations will be executed. Program command is executed on a page (128 bytes) basis, and erase command is executed on both chip and sector (8K bytes) basis.

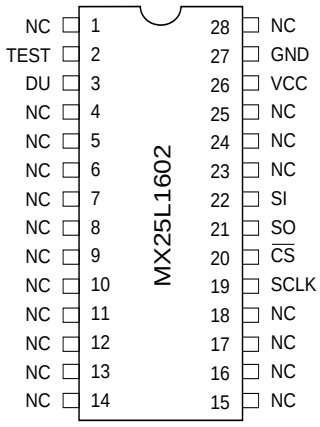
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion and error flag status of a program or erase operation.

When the device is not in operation and $\overline{CS}$ is high, it is put in standby mode and draws less than 30uA DC current.

The MX25L1602 utilizes MXIC's proprietary memory cell which reliably stores memory contents even after 100,000 program and erase cycles.

PIN CONFIGURATIONS

28-PIN SOP (330 mil)



PIN DESCRIPTION

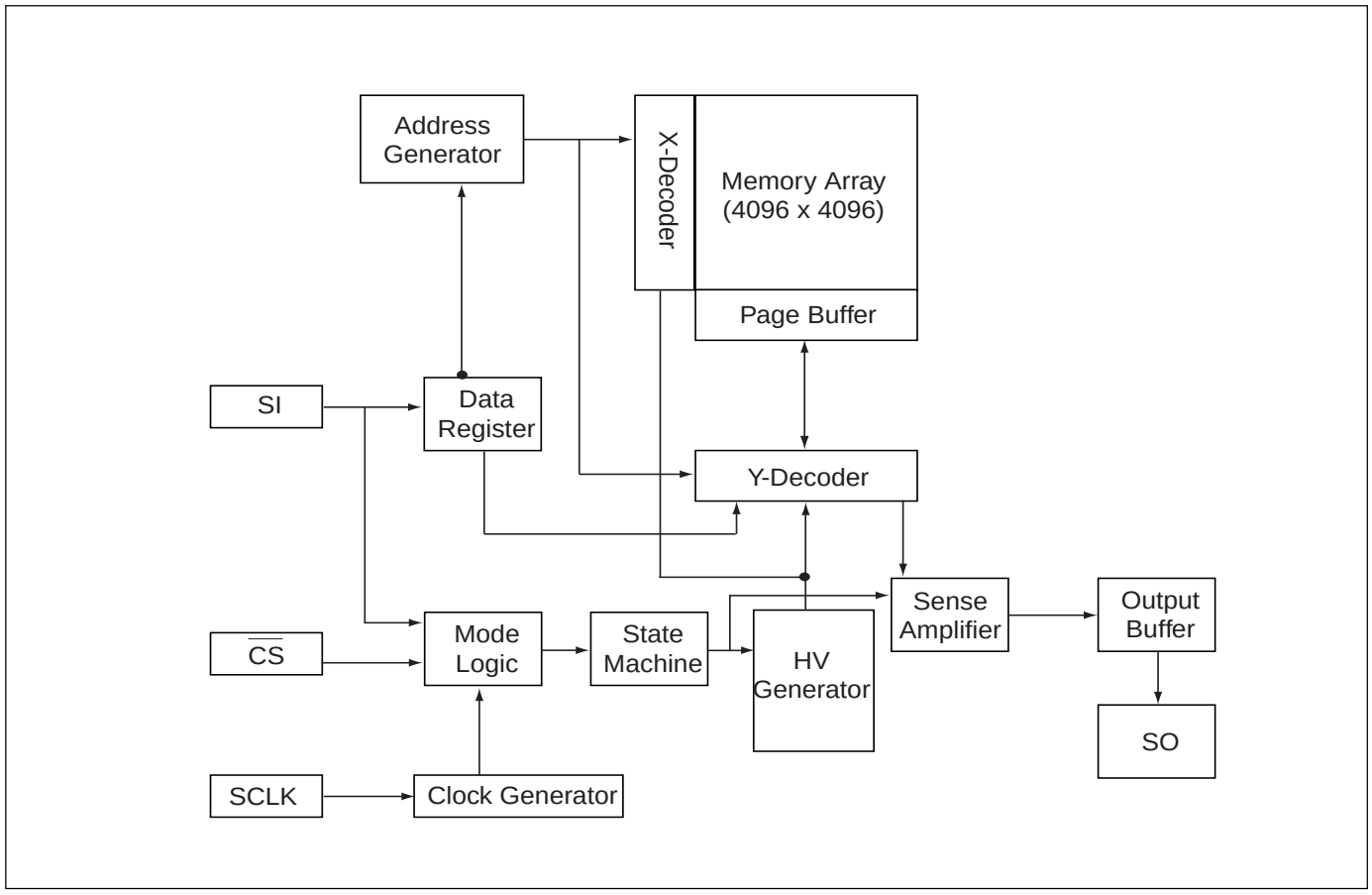
SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select
TEST(1)	Test Mode Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
VCC	+ 3.3V Power Supply
GND	Ground
DU(2)	Do Not Use(for Test Mode only)
NC	No Internal Connection

Note:

1. TEST input is used for in-house testing and must be tied to ground during normal user operation.

2. DU pin is used for in-house testing and can be tied to VCC, GND or open for normal operation.

BLOCK DIAGRAM



COMMAND DEFINITION

Com-mand (byte)	Read Array	Status Read	Clear Status	Read ID	Sector Erase	Chip Erase	Page Program
1st	52H	83H	89H	85H	F1H	F4H	F2H
2nd	AD1	X		X	AD1	X	AD1
3rd	AD2				AD2	X	AD2
4th	AD3						AD3
5th	BA						BA
6th	X						
7th	X						
8th	X						
9th	X						
Action	n bytes read out until $\overline{CS}$ goes high	Output status byte until $\overline{CS}$ goes high	Clear status byte	Output vendor code until $\overline{CS}$ goes high	Start to erase at $\overline{CS}$ rising edge	Start to erase at $\overline{CS}$ rising edge	Load n bytes data to buffer until $\overline{CS}$ goes high & start to program

Note:
1.X is dummy cycle and is necessary
2.AD1 to AD3 are address input data
3.BA is byte address

1-byte command code								
	Bit7(MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3-byte address(0 to 0FFFH)								
AD1:	X	X	X	X	A20	A19	A18	A17
AD2:	A16	A15	A14	A13	A12	A11	A10	A9
AD3:	X	X	X	X	X	X	A8	A7
1-byte byte address(0 to 7FH)								
BA:	X	A6	A5	A4	A3	A2	A1	A0

Note:
A20 to A13=Sector address
A20 to A9=Segment address

DEVICE OPERATION

1.Before a command is issued, status register should be checked to ensure device is ready for the intended operation.
2.When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS falling edge. In standby mode, SO pin of this LSI should be High-Z.
3.When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CSB rising edge.

COMMAND DESCRIPTION

(1) Read Array

This command is sent with the 4-byte address (command included), and the byte address, followed by four dummy bytes sent to give the device time to stabilize. The device will then send out data starting at the byte address until CS goes high. The clock to clock out the data is supplied by the master SPI. The read operation is executed on a segment (512 bytes) basis. If the end of the segment is reached then the device will wrap around to the beginning of the segment.

(2) Read Status Register

When this command is sent, the device will continuously send out the status register contents starting at bit7. The clock to clock out the data is supplied by the master SPI.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
program/erase completion	NA	NA	erase error	program error	NA	NA	ready/busy
Note1			1=error	1=error			1=ready 0=busy

Bit 6,5,2,1 = Reserve for future use.
Bit 4 = "1" -----> There is an error occurred in last erase operation.
= "0" -----> There is no error occurred in last erase operation.
Bit 3 = "1" -----> There is an error occurred in last program operation.
= "0" -----> There is no error occurred in last program operation.
Bit 0 ="1" -----> Device is in ready mode.
="0" -----> Device is in busy mode.

Note 1:The initial value of Bit7 is "1". Bit7 will have "1" to "0" transit only after program/erase operation is completed. Bit7 will shift from "0" to "1" only after issued program/erase/Clear status register command.

(3) Clear Status Register

This command only resets erase error bit (bit 4) and program error bit (bit 3) . These two bits are set by on-chip state machine during program/erase operation, and can only be reset by issuing a clear status register command or by powering down VCC .

If status register indicates that error occurred in the last program/erase operation, any further program/erase operation will be prohibited until status register is cleared.

(4) Read ID

This command is sent with an extra dummy byte(a 2-byte command). The device will clock out manufacturer code (C2H) and device code (01H) when this command is issued. The clock to clock out the data is supplied by the master SPI.

(5) Sector/Chip Erase

This command is sent with the sector address(A20~A13) when operating Sector Erase. The device will start the erase sequence after $\overline{CS}$ goes high without any further input. A sector should be erased in a typical of 300ms. The average current is less than 10mA. The chip erase operation does not require the sector address input but two extra dummy bytes are necessary. During this operation, customer can also access Read Status & Read ID operations.

(6) Page Program

This command is sent with the page number(A20~A7), and byte address(A6~A0), followed by programming data. One to 128 bytes of data can be loaded into the buffer of the device until $\overline{CS}$ goes high. If the end of the page is reached, then the device will wrap around to the beginning of the page. The device will program the specified page with buffered data(Until $\overline{CS}$ goes high) without any further input. The typical page program time is 5ms. The average current is less than 10mA. During this operation, customer can also access Read Status & Read ID operations.

(7) Standby Mode

When $\overline{CS}$ is high and there is no operation in progress, the device is put in standby mode. Typical standby current is less than 30uA.

POWER-ON STATE

After power-up, the device is placed in the standby state with following status:

The status register is reset with following status :

Bit 7 = "1" -----> Refer to page 5 for detail.
Bit 6,5,2,1 = Reserve for future use.
Bit 4 = "0" -----> Erase error flag is reset.
Bit 3 = "0" -----> Program error flag is reset.
Bit 0="1" -----> Device is in ready state.

DATA SEQUENCE

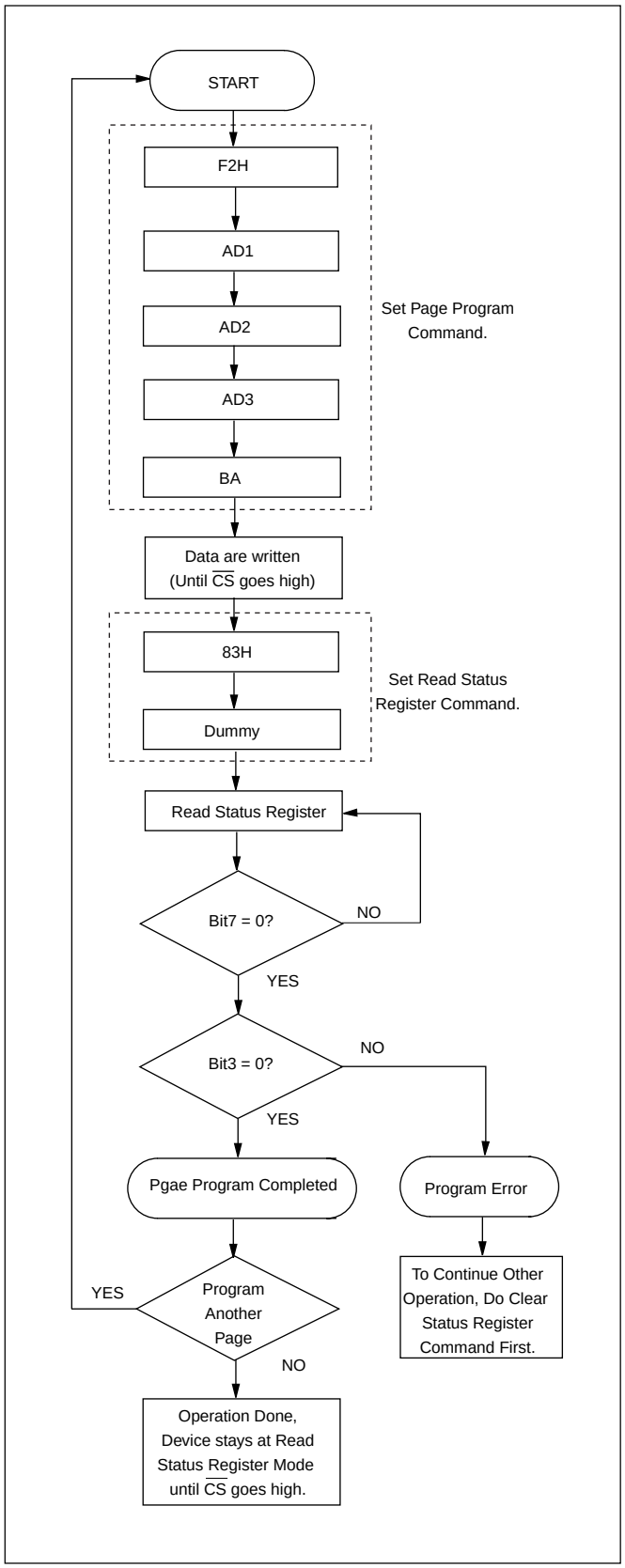
Output data is serially sent out through SO pin, synchronized with the rising edge of SCLK, whereas input data is serially read in through SI pin, synchronized with the rising edge of SCLK. The bit sequence for both input and output data is bit 7 (MSB) first, then bit 6, bit 5, ..., and bit 0.(LSB)

ADDRESS SEQUENCE

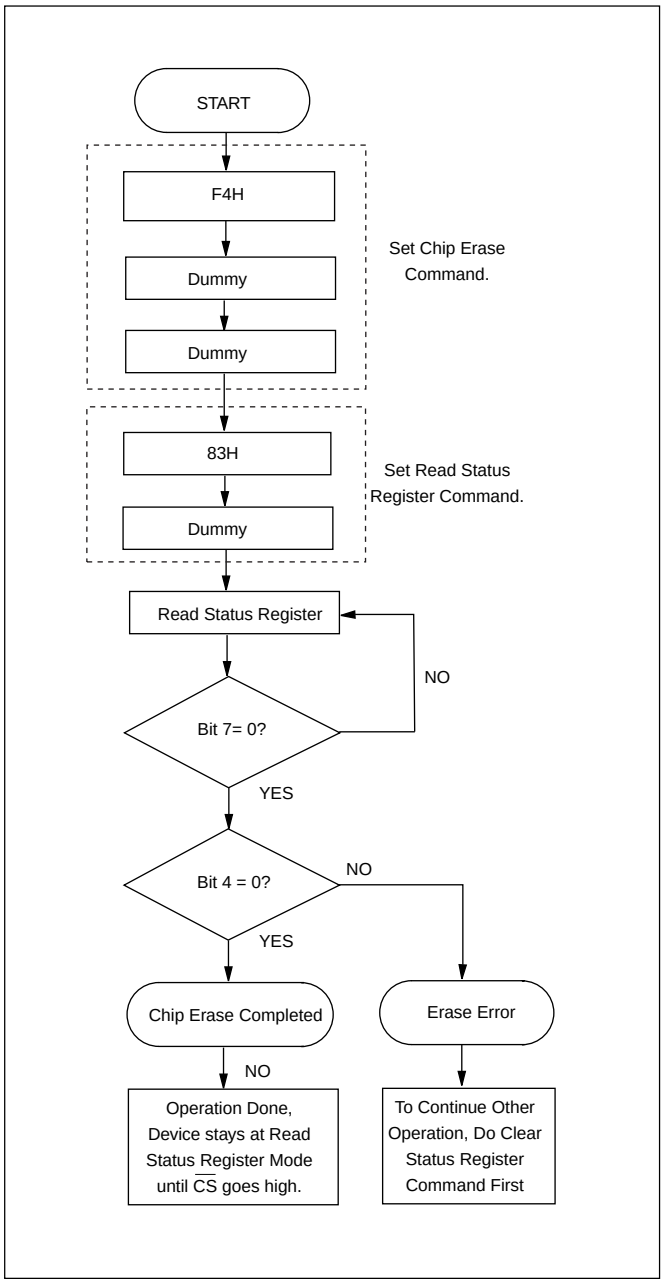
The address assignment is described as follows :

BA: Byte address Bit sequence:	X	A6	A5	A4	A3	A2	A1	A0
AD1:First Address Bit sequence:	X	X	X	X	A20	A19	A18	A17
AD2:Second Address Bit sequence:	A16	A15	A14	A13	A12	A11	A10	A9
AD3:Thrid Address Bit sequence:	X	X	X	X	X	X	A8	A7

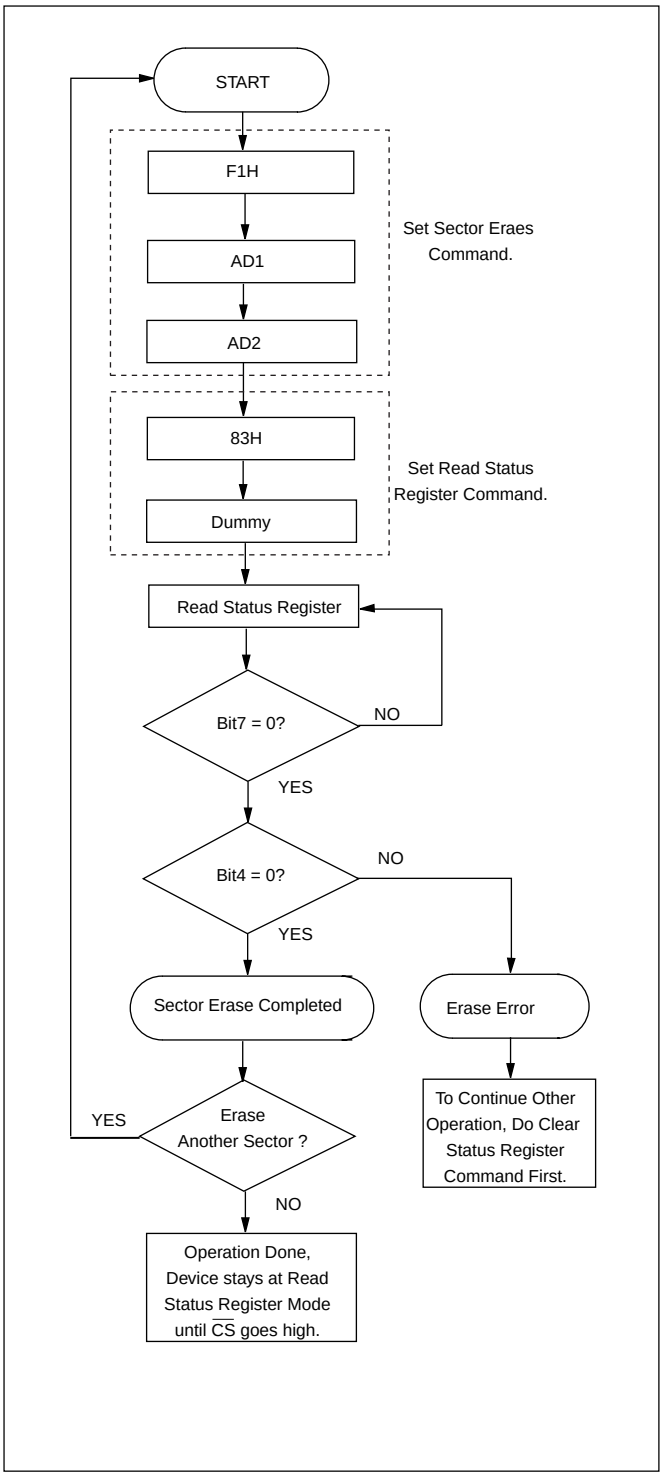
Auto Page Program Flow Chart



Auto Chip Erase Flow Chart



Auto Sector Erase Flow Chart



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0℃ to 70℃
Storage Temperature	-55℃ to 125℃
Applied Input Voltage	-0.5V to 4.6V
Applied Output Voltage	-0.5V to 4.6V
VCC to Ground Potential	-0.5V to 4.6V

NOTICE:

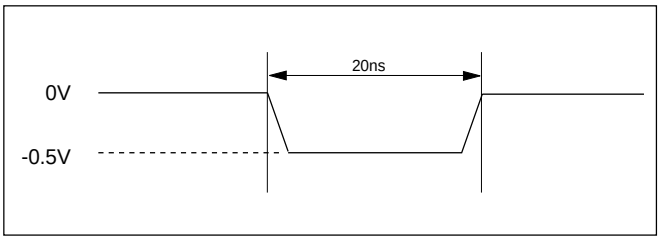
1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

2.Specifications contained within the following tables are subject to change.

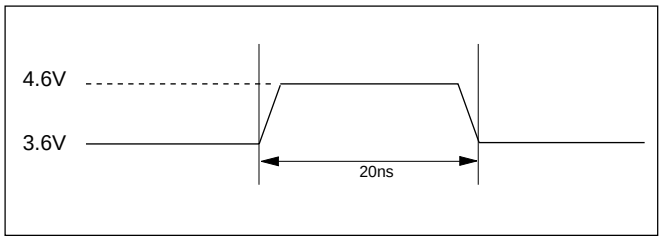
3.During voltage transitions, all pins may overshoot to 4.6V or -0.5V for period up to 20ns.

4.All input and output pins may overshoot to VCC+0.5V while VCC+0.5V is smaller than or equal to 4.6V.

Maximum Negative Overshoot Waveform



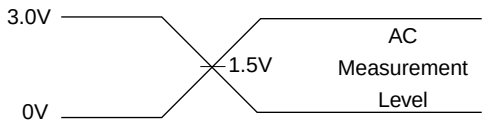
Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25°C, f = 1.0 MHz

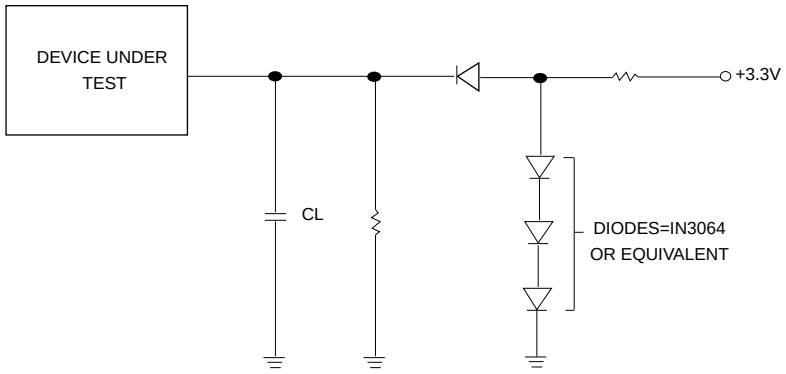
SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			10	pF	VIN = 0V
COUT	Output Capacitance			10	pF	VOUT = 0V

INPUT TEST WAVEFORMS AND MEASURESMENT LEVEL



Note:Input pulse rise and fall time are < 10ns

OUTPUT LOADING



CL=50pF Including jig capacitance

DC CHARACTERISTICS (Temperature = 0℃ to 70℃, VCC = 3.0V ~ 3.6V)

SYMBOL	PARAMETER	NOTES	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
IIL	Input Load Current	1			±10	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current	1			±10	uA	VCC = VCC Max VIN = VCC or GND
ISB1	VCC Standby Current(CMOS)	1		30	60	uA	VCC = VCC Max $\overline{CS}$ = VCC ± 0.2V
ISB2	VCC Standby Current(TTL)			1	3	mA	VCC = VCC Max $\overline{CS}$ = VIH
ICC1	VCC Read	1		10	30	mA	f=20MHz
ICC2	VCC Program Current	1		10	30	mA	Program in Progress
ICC3	VCC Erase Current	1		10	30	mA	Erase in Progress
VIL	Input Low Voltage		-0.5		0.8	V	
VIH	Input High Voltage		2.0		VCC+0.5	V	
VOL	Output Low Voltage				0.4	V	IOL = 500uA
VOH	Output High Voltage		2.4			V	IOH = -100uA

NOTES:

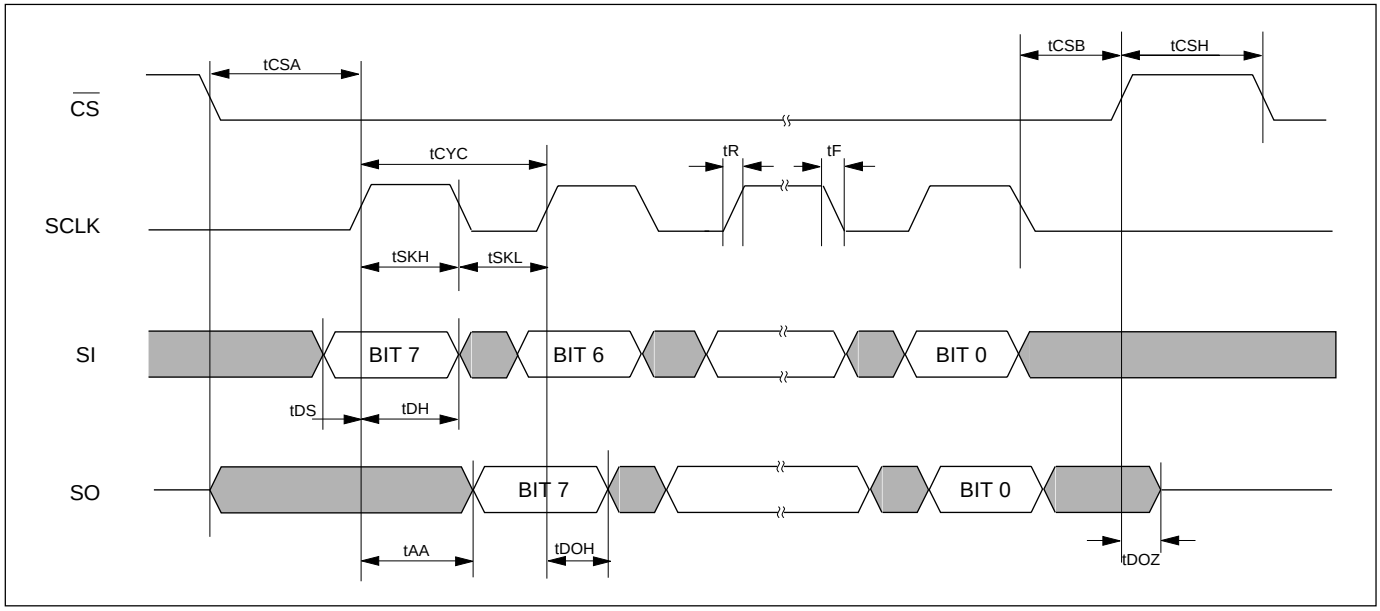
1. All currents are in RMS unless otherwise noted. Typical values at VCC = 3.3V, T = 25℃. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

AC CHARACTERISTICS (Temperature = 0℃ to 70℃, VCC = 3.0V ~ 3.6V)

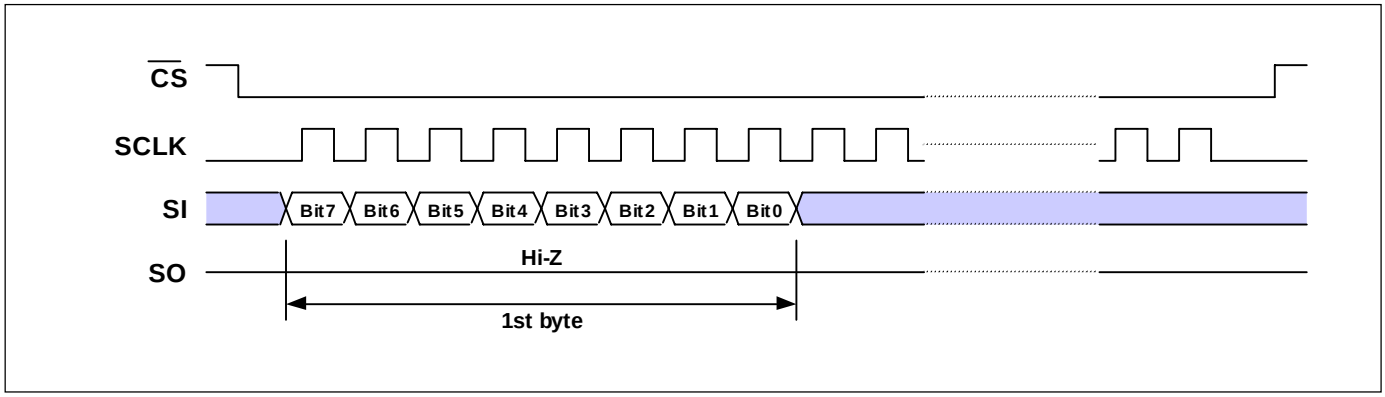
SYMBOL	PARAMETER	Min.	Typ.	Max.	Units	Conditions
fSCLK	Clock Frequency			20	MHz	
tCYC	Clock Cycle Time	50			ns	
tSKH	Clock High Time	25			ns	
tSKL	Clock Low Time	25			ns	
tR	Clock Rise Time			6	ns	
tF	Clock Fall Time			6	ns	
tCSA	$\overline{CS}$ Lead Clock Time	50			ns	
tCSB	$\overline{CS}$ Lag Clock Time	50			ns	
tCSH	$\overline{CS}$ High Time	100			ns	
tDS	SI Setup Time	5			ns	
tDH	SI Hold Time	25			ns	
tAA	Access Time			30	ns	
tDOH	SO Hold Time	5			ns	
tDOZ	SO Floating Time	0		20	ns	
tECY	Erase Cycle Time		300	1600	ms	
tPCY	Program Cycle Time		5	15	ms	

NOTES:
1. Typical value is calculated by simulation.

SERIAL DATA INPUT/OUTPUT TIMING

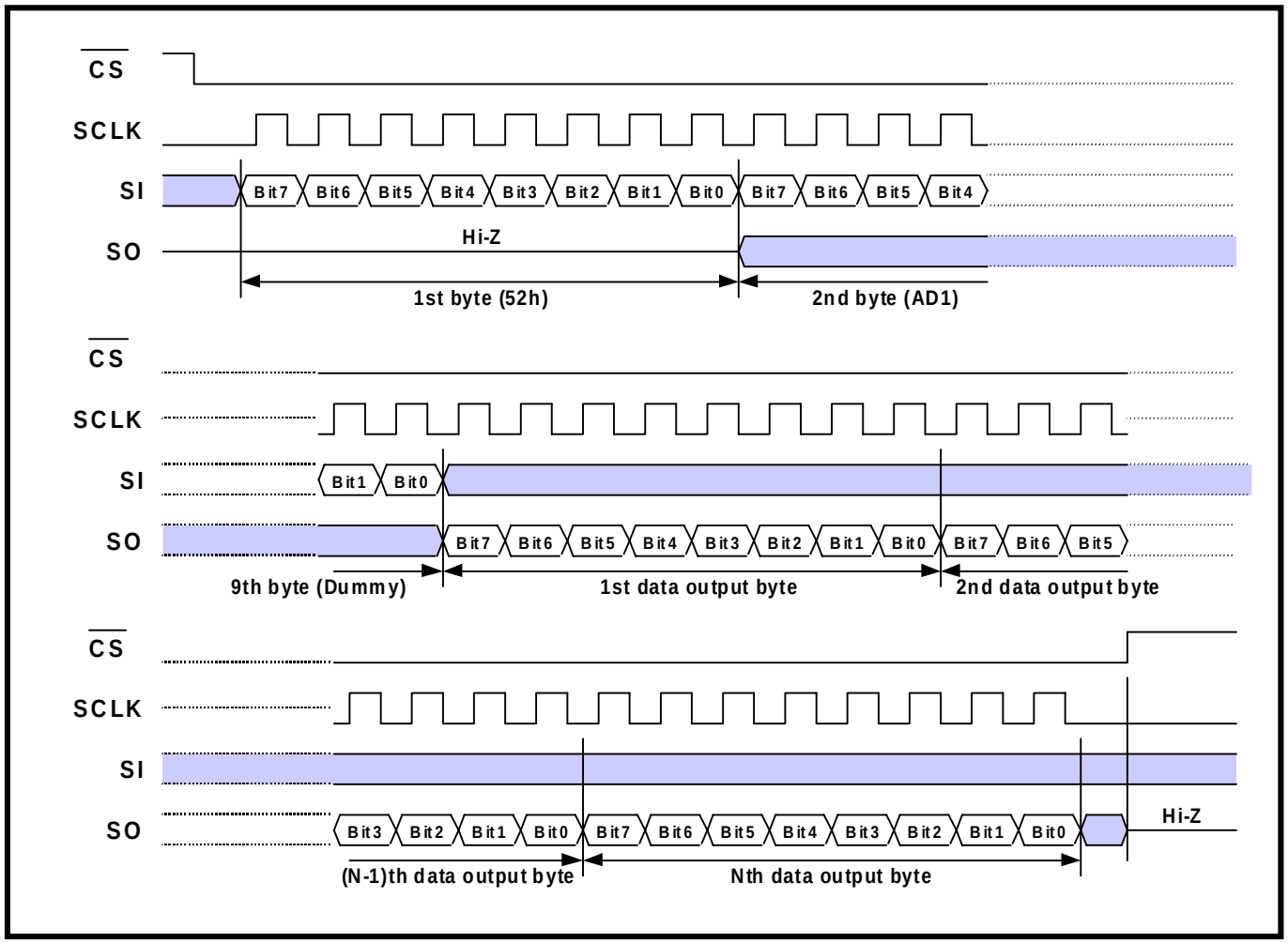


STANDBY TIMING WAVEFORM



When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next $\overline{CS}$ falling edge. In standby mode, SO pin of this LSI should be High-Z. While $\overline{CS}$=VIH, current=standby current, while $\overline{CS}$=VIL and commands are issuing, or commands are invalid, current=5mA(typ.) to 15mA(max.).

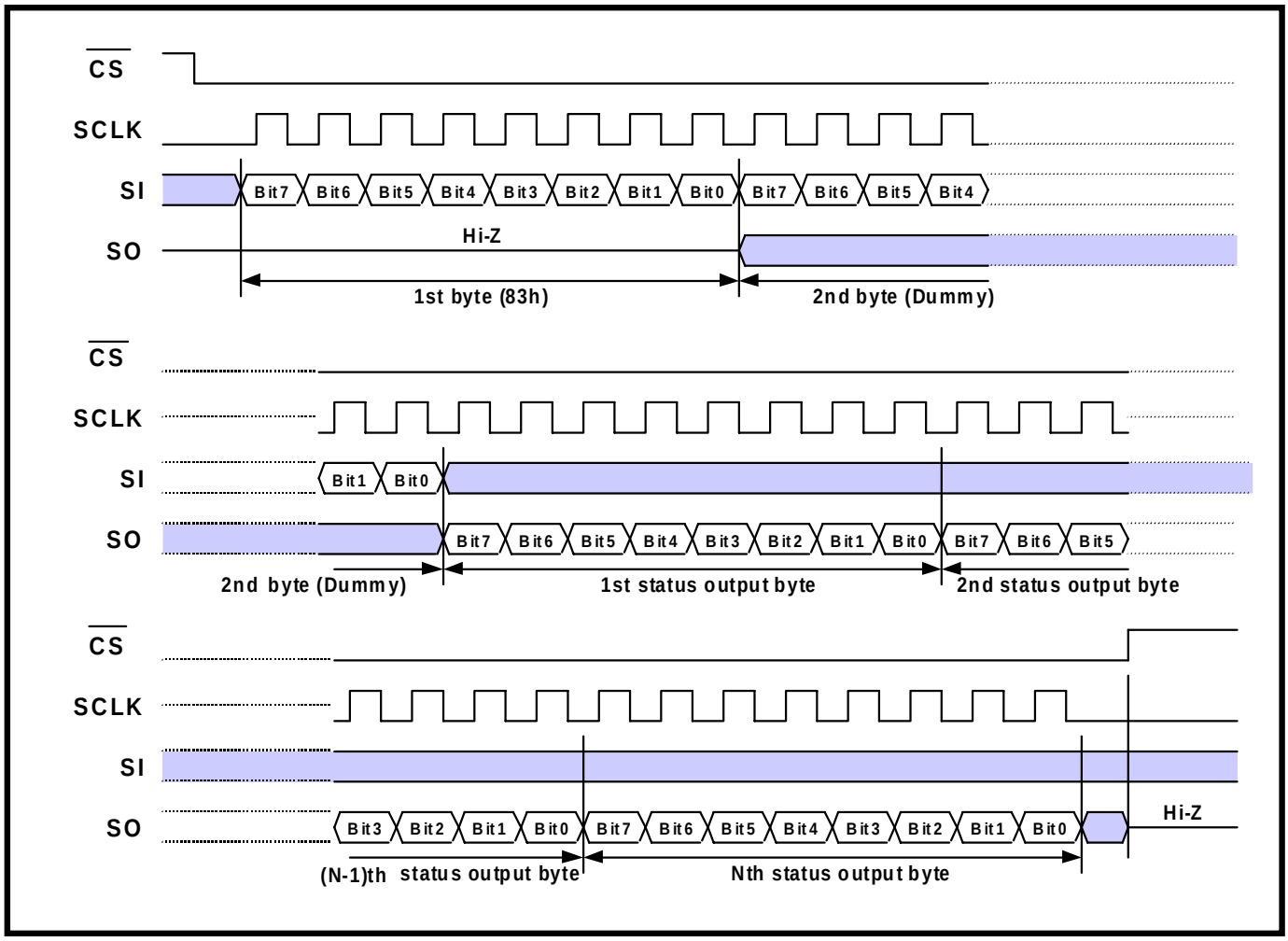
READ ARRAY TIMING WAVEFORM



NOTES:

1. 1st Byte='52h'
2. 2nd Byte=Address 1(AD1), A17=BIT 0, A18=BIT1, A19=BIT2, A20=BIT3.
3. 3rd Byte=Address 2(AD2), A9=BIT0, A10=BIT1,.....A16=BIT7
4. 4th Byte=Address 3(AD3), A7=BIT0, A8=BIT1
5. 5th Byte=Byte Address(BA), A0=BIT0, A1=BIT1,.....A6=BIT6
6. 6th-9th Bytes for SI ==> Dummy Bytes (Don't care)
7. From Byte 10, SO Would Output Array Data

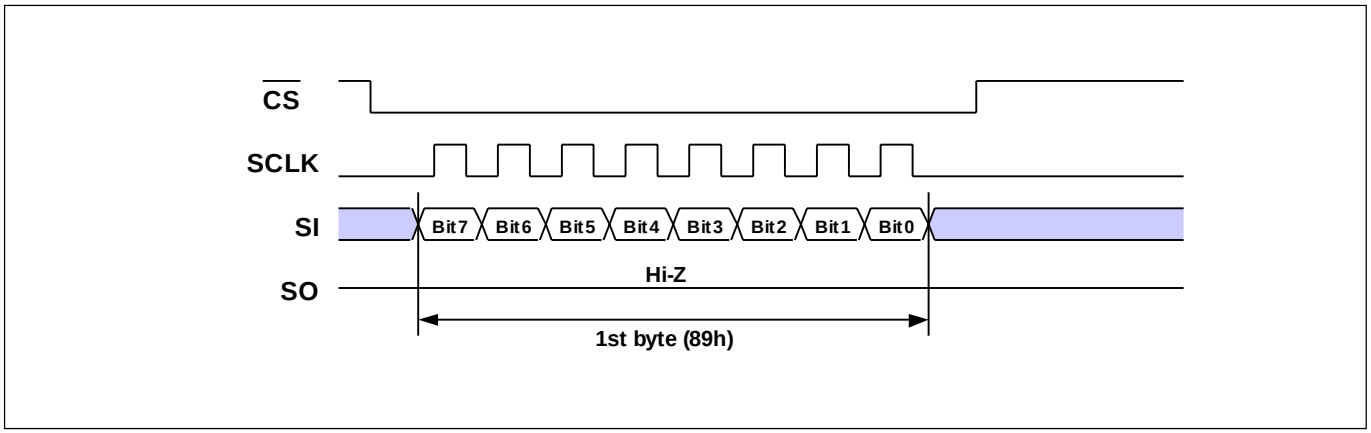
READ STATUS REGISTER TIMING WAVEFORM



NOTES:

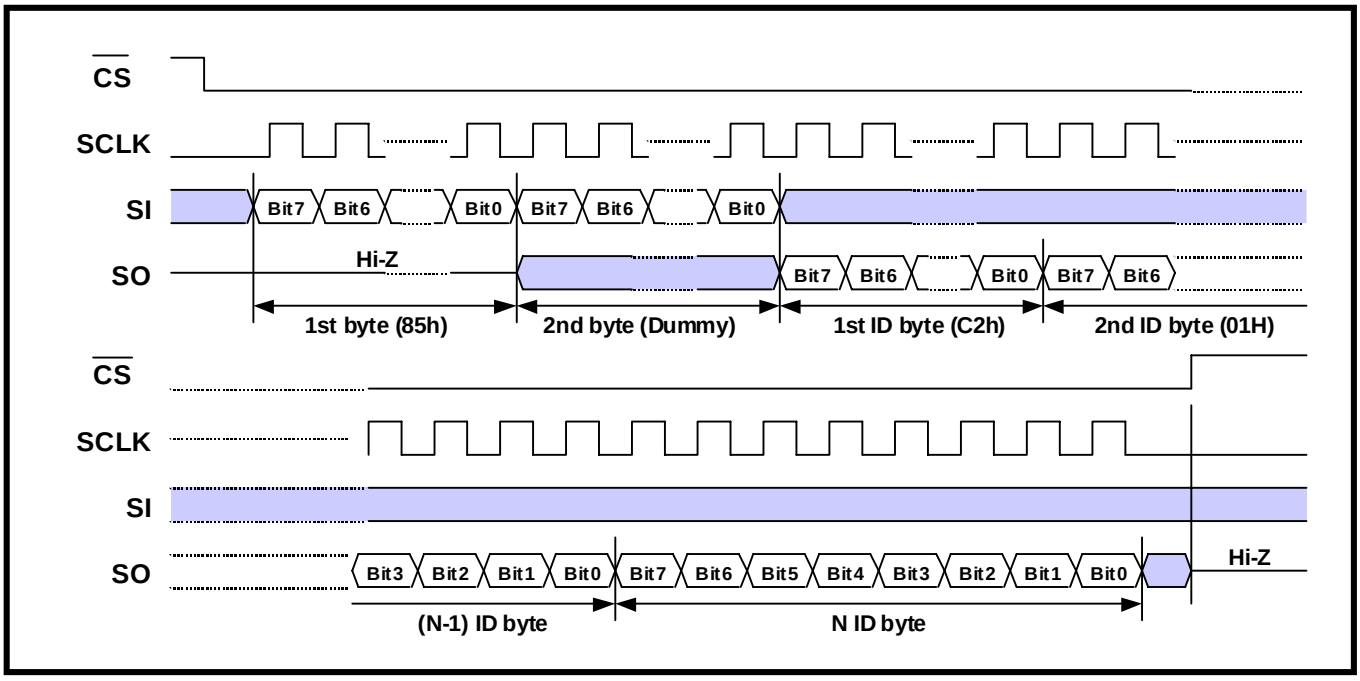
1. BIT 7=0 ==> Program/Erase completed
2. BIT 4=1 ==>Erase Error
3. BIT 3=1 ==>Program Error
4. BIT 1,2,5,6 ==> Reserve for future use
5. Bit 0=1 ==> Device is in ready state

CLEAR STATUS REGISTER TIMING WAVEFORM



NOTES:
1. 1st Byte='89h' ==> CLEAR STATUS REGISTER
2. SO at Hi-Z state

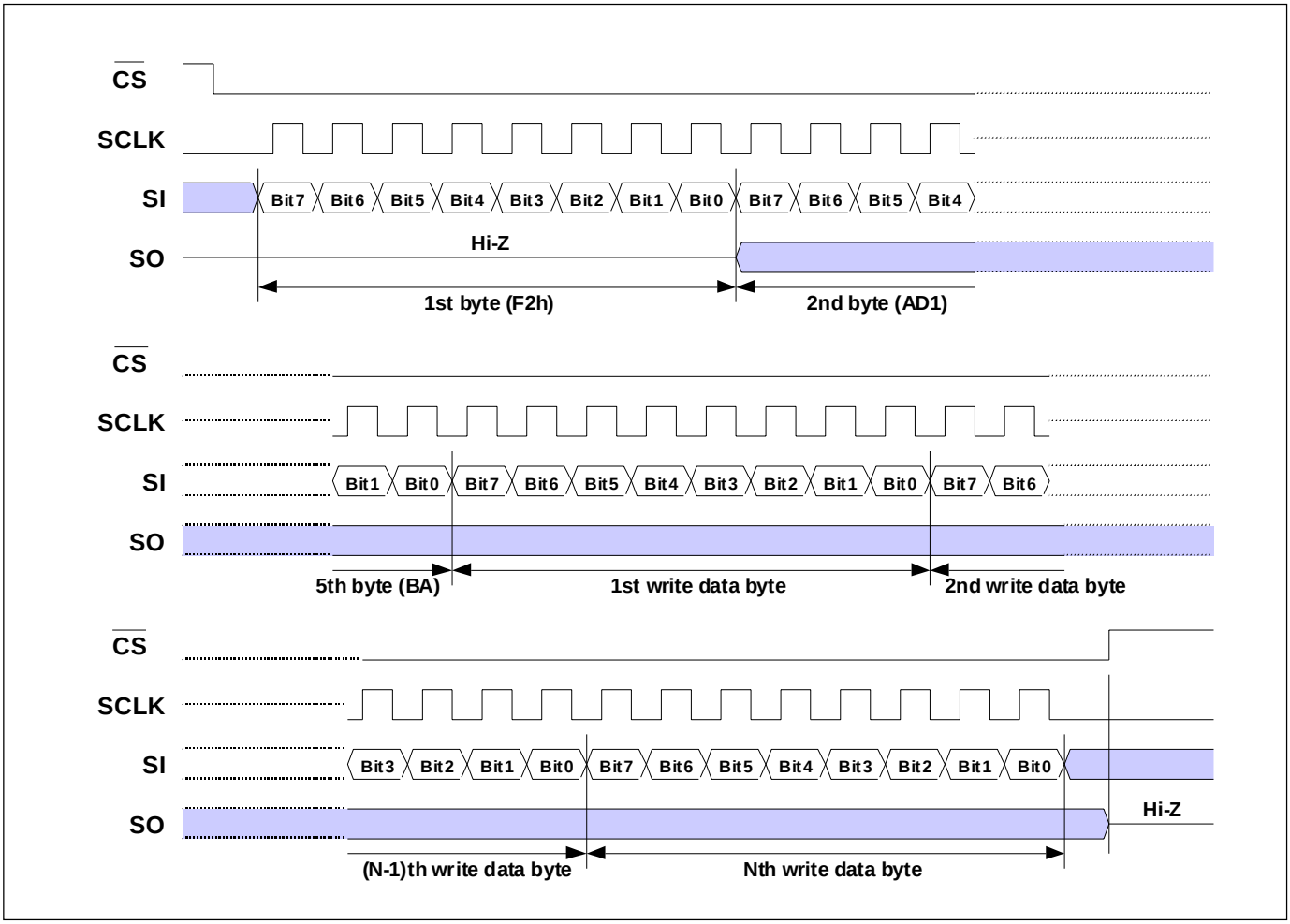
READ ID TIMING WAVEFORM



NOTES:

1. 1st Byte:85h.
2. 2nd Byte:Dummy Byte.
3. 3rd Byte:Output Manufacture Code(C2h).
4. 4th Byte:Output Device Code(01H).
5. The 2 bytes ID output will be wrap around.

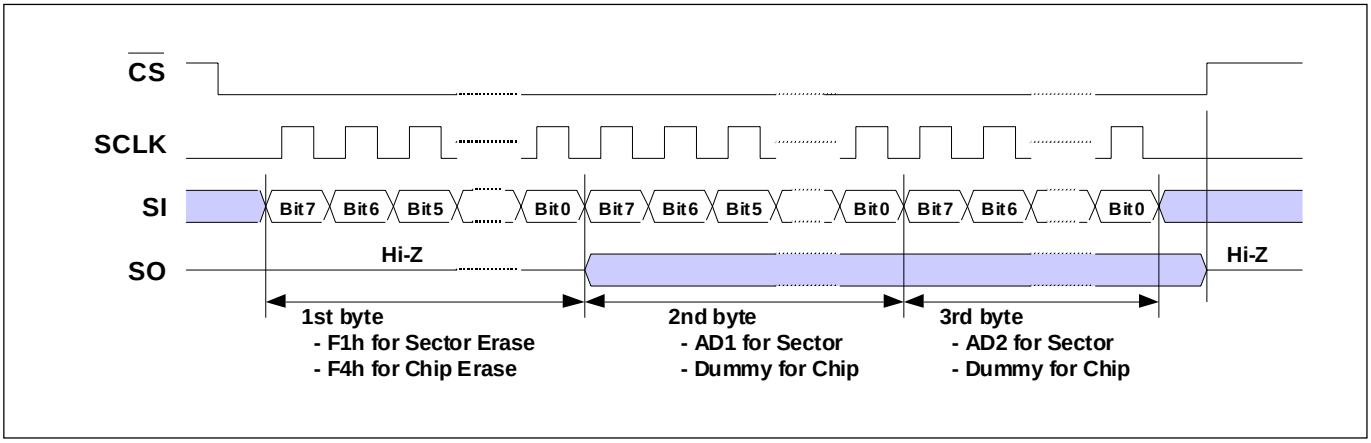
AUTO PAGE PROGRAM TIMING WAVEFORM



NOTES:

1. 1st Byte:F2h.
2. 2nd Byte:Address AD1.
3. 3rd Byte:Address AD2
4. 4th Byte:Address AD3
5. 5th Byte:Address BA.
6. 6th byte:1st write data byte.
7. When the last byte of the page will be written, the Byte Address will be wrap around to the first byte of the Page.

AUTO SECTOR/CHIP ERASE TIMING WAVEFORM



NOTES:

1. 1st byte:F1h for Sector Erase, F4h for Chip Erase.
2. 2nd byte:Address AD1 for Sector Erase, Dummy byte for Chip erase.
3. 3rd byte:Address AD2 for Sector Erase, Dummy byte for Chip erase.

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	TYP.(1)	Max.(2)	UNIT	Comments
Sector/Chip Erase Time	300	1,600	ms	
Page Programming Time	5	15	ms	Excludes system level
Chip Programming Time	48	240	s	overhead(3)

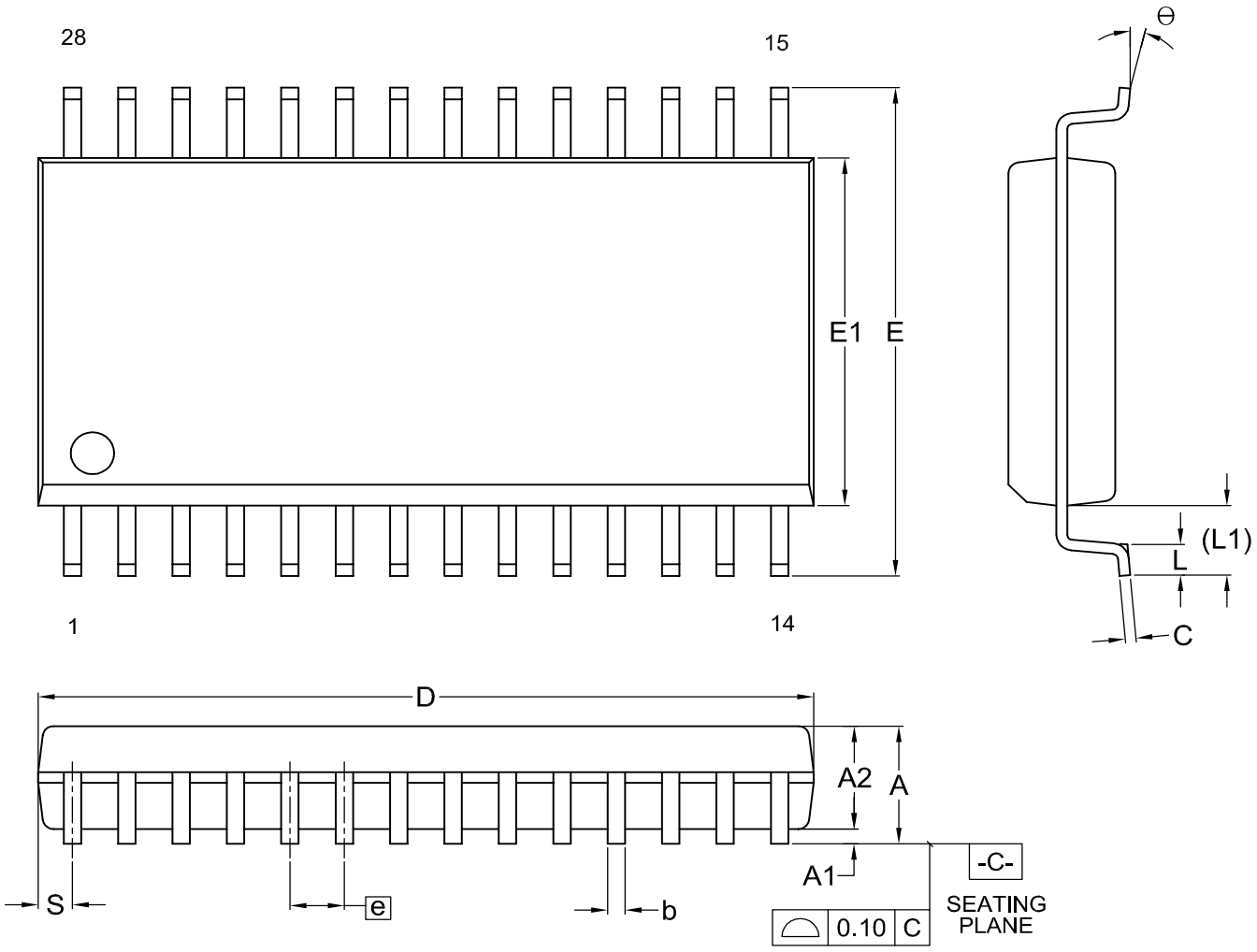
Note:
1.Typical program and erase time assumes the following conditions: 25℃,3.3V, and checker board pattern.
2.Under worst conditions of 0℃ and 3.0V.
3.System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4.The maximum chip programming time is evaluated under the worst conditions of 0℃, VCC=3.0V, and 100K cycle with 90% confidence level.

ORDERING INFORMATION

PART NO.	ACCESS TIME	OPERATING CURRENT	STANDBY CURRENT	PACKAGE
MX25L1602MC-50	20MHz	10mA	30uA	28 pin SOP (330 mil)

PACKAGE IMFORMATION

Title: Package Outline for SOP 28L (330MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	Min.	---	0.10	2.39	0.36	0.20	17.98	11.61	8.28		0.56	1.51	0.67	0
	Nom.	---	0.15	2.49	0.41	0.25	18.11	11.81	8.40	1.27	0.76	1.71	0.80	5
	Max.	2.84	0.25	2.59	0.51	0.30	18.24	12.02	8.53		0.96	1.91	0.92	8
Inch	Min.	---	0.004	0.094	0.014	0.008	0.708	0.457	0.326		0.022	0.059	0.026	0
	Nom.	---	0.006	0.098	0.016	0.010	0.713	0.465	0.331	0.050	0.030	0.067	0.031	5
	Max.	0.112	0.010	0.102	0.020	0.012	0.718	0.473	0.336		0.038	0.075	0.036	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1403	7	MO-059			09-24-'02

REVISION HISTORY

Revision No.	Description	Page	Date
0.1	Remove "256 Equal sectors with 8K-byte each"	P1	AUG/09/2001
	Change 25MHz to 20MHz	P1	
	Revise 100,000 erase/program cycle to 10,000	P1	
	Change Pin 2:NC to TEST ; Pin 3:TEST to DU ; Pin 4:DU to NC ; Pin 27:NC to GND ; Pin 26:NC to VCC ; Pin 23:VCC to NC	P2	
	Remove "Sector" in General Description	P2	
	Remove "A20 tp A13=Sector address"	P4	
	Remove "sector erase typical 300ms"	P6	
	Revise "100K cycle" to "10K cycle"	P20	
	Change fSCLK max 25 to 20 MHz	P12	
	Change fCYC min 40 to 50 MHz	P12	
	Change fSKH min 20 to 25 MHz	P12	
	Change fSKY min 20 to 25 MHz	P12	
	Delete BIT5=1-->Sleep mode	P15	
0.2	Delete "Segment read"	P1	AUG/10/2001
	Delete "A19 to A9=Segment Address"	P4	
	Delete "Segment read"	P5	
	Delete note 8	P14	
0.3	Add 100K program/erase cycles	P1,20	NOV/21/2001
	Add sector erase function	P1,4,5,19,20	
	Wording changed:automatically programming -- (any page to be programmed should have the page in erase state first)	P1	
0.4	Tighten the page programming time:90ms(max.)-->15ms(max.)	P13,21	DEC/04/2001
	Add ordering information	P21	
	Correct mis-typing: remove "Sleep/Wake up" Waveform	P20	
0.5	Change typical page programming time:3ms(typ)-->5ms(typ)	P1,6,13,21	MAY/10/2002
	Add "Segment read"	P1,2,4,5	
0.6	1. To modify Package Information	P22	NOV/21/2002

MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-348-8385
FAX:+65-348-8096

TAIPEI OFFICE:
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.

TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com