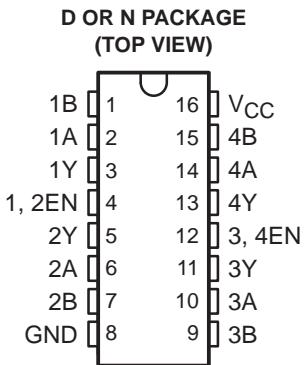


- Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27
- Designed to Operate Up To 20 Mbaud
- $-7\text{ V}$  to  $7\text{ V}$  Common-Mode Input Voltage Range With 300-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . .  $12\text{ k}\Omega$  Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement 35 mA Max
- Improved Speed and Power Consumption Compared to MC3486



### description

The SN75ALS199 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specification of ITU Recommendations V.10, V.11, X.26, and X.27.

The SN75ALS199 features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of  $\pm 300\text{ mV}$  over a common-mode input voltage range of  $\pm 7\text{ V}$ . It also features an active-high enable function for each of two receiver pairs. The SN75ALS199 is designed for optimum performance when used with the SN75ALS194 quadruple, differential line driver.

The SN75ALS199 is characterized for operation from  $0^\circ\text{C}$  to  $70^\circ\text{C}$ .

FUNCTION TABLE  
(each receiver)

DIFFERENTIAL INPUTS A-B	EN	OUTPUT Y
$V_{ID} \geq 0.3\text{ V}$	H	H
$-0.3\text{ V} < V_{ID} < 0.3\text{ V}$	H	?
$V_{ID} \leq -0.3\text{ V}$	H	L
X	L	Z
Open	H	H

H = high level, L = low level, X = irrelevant,  
? = indeterminate, Z = high impedance (off)

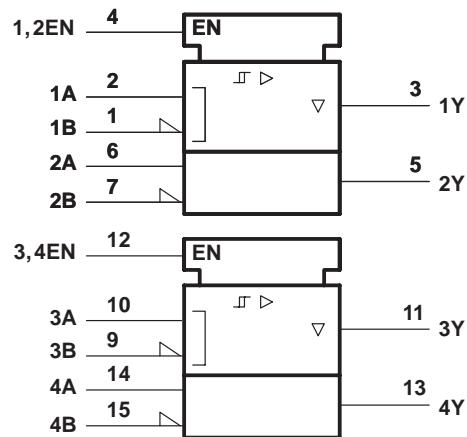


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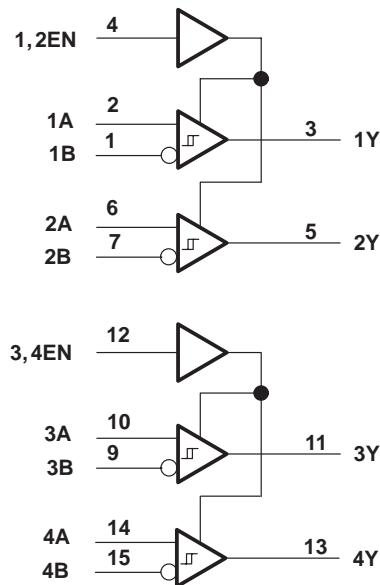
# SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS046C – JANUARY 1989 – REVISED MAY 1995

## logic symbol†

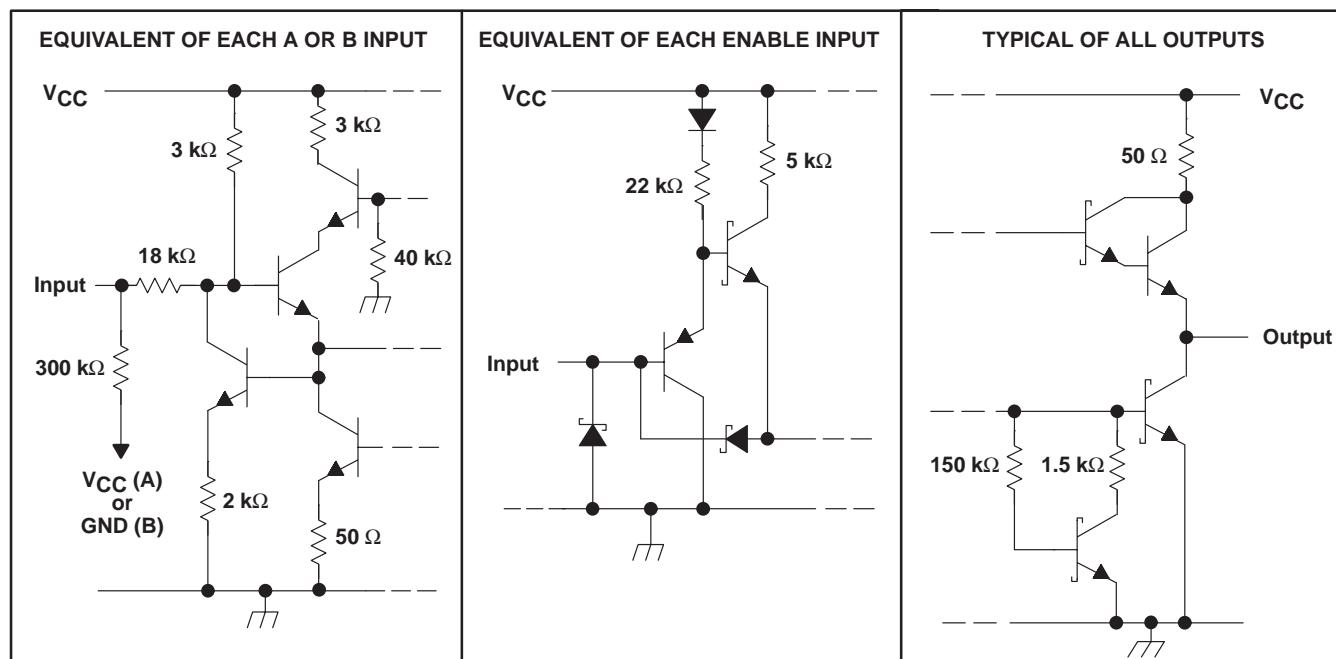


## logic diagram



† This symbol is in accordance with ANSI/IEEE Std 91-1984  
and IEC Publication 617-12.

## schematics of inputs and outputs



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$ (A or B inputs)	$\pm 15$ V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm 15$ V
Enable input voltage, $V_I$	7 V
Low-level output current, $I_{OL}$	50 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.

2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

**recommended operating conditions**

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
Common-mode input voltage, $V_{IC}$			$\pm 7$	V
Differential input voltage, $V_{ID}$			$\pm 12$	V
High-level input voltage, $V_{IH}$		2		V
Low-level input voltage, $V_{IL}$			0.8	V
High-level output current, $I_{OH}$			–400	$\mu\text{A}$
Low-level output current, $I_{OL}$			16	mA
Operating free-air temperature, $T_A$	0		70	$^\circ\text{C}$

# SN75ALS199

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

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### electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
$V_{IT+}$	Positive-going input threshold voltage			300	mV	
$V_{IT-}$	Negative-going input threshold voltage			-300‡	mV	
$V_{hys}$	Hysteresis voltage ( $V_{IT+} - V_{IT-}$ )			120	mV	
$V_{IK}$	Enable-input clamp voltage	$I_I = -18 \text{ mA}$		-1.5	V	
$V_{OH}$	High-level output voltage	$V_{ID} = 300 \text{ mV}$ , $I_{OH} = -400 \mu\text{A}$	2.7	3.6	V	
$V_{OL}$	$V_{OL}$ Low-level output voltage	$V_{ID} = -300 \text{ mV}$	$I_{OL} = 8 \text{ mA}$	0.45	V	
			$I_{OL} = 16 \text{ mA}$	0.5		
$I_{OZ}$	High-impedance-state output current	$V_{IL} = 0.8 \text{ V}$ , $V_{ID} = -3 \text{ V}$ , $V_O = 2.7 \text{ V}$		20	$\mu\text{A}$	
		$V_{IL} = 0.8 \text{ V}$ , $V_{IO} = 3 \text{ V}$ , $V_O = 0.5 \text{ V}$		-20		
$I_I$	Line input current	Other input at 0 V, See Note 3	$V_I = 15 \text{ V}$	0.7	mA	
			$V_I = -15 \text{ V}$	-1		
$I_{IH}$	High-level enable-input current		$V_{IH} = 2.7 \text{ V}$	20	$\mu\text{A}$	
			$V_{IH} = 5.25 \text{ V}$	100		
$I_{IL}$	Low-level enable-input current	$V_{IL} = 0.4 \text{ V}$		-100	$\mu\text{A}$	
Input resistance				12	$\text{k}\Omega$	
$I_{OS}$	Short-circuit output current§	$V_{ID} = 3 \text{ V}$ , $V_O = 0$	-15	-78	-130	mA
$I_{CC}$	Supply current	Outputs disabled		22	35	mA

† All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: Refer to ITU Recommendations V.10 and V.11 for exact conditions.

### switching characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	$V_{ID} = 0 \text{ V}$ to $3 \text{ V}$ , $C_L = 15 \text{ pF}$ , See Figure 2		15	22	ns
$t_{PHL}$			15	22	
$t_{PZH}$	$C_L = 15 \text{ pF}$ , See Figure 3		13	25	ns
$t_{PZL}$			11	25	
$t_{PHZ}$	$C_L = 15 \text{ pF}$ , See Figure 3		13	25	ns
$t_{PLZ}$			15	22	

PARAMETER MEASUREMENT INFORMATION

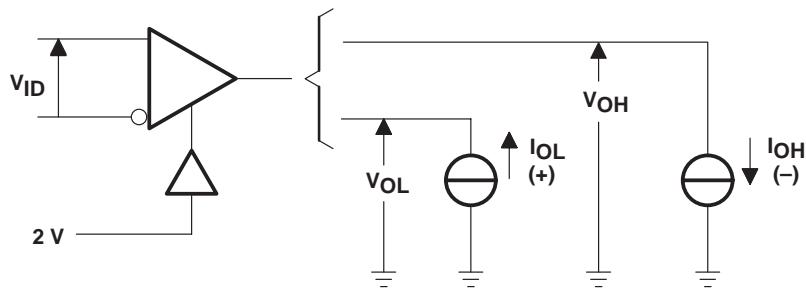
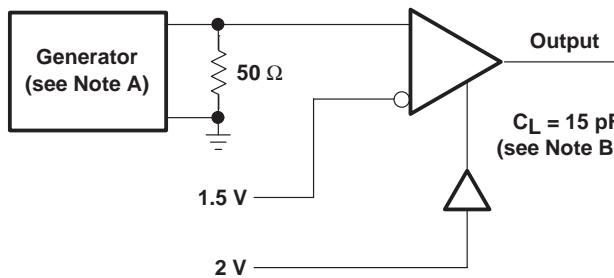
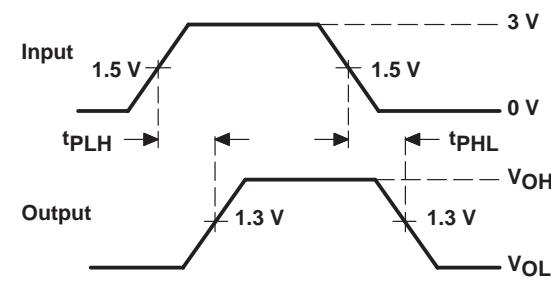


Figure 1.  $V_{OH}$  and  $V_{OL}$  Test Circuit



TEST CIRCUIT

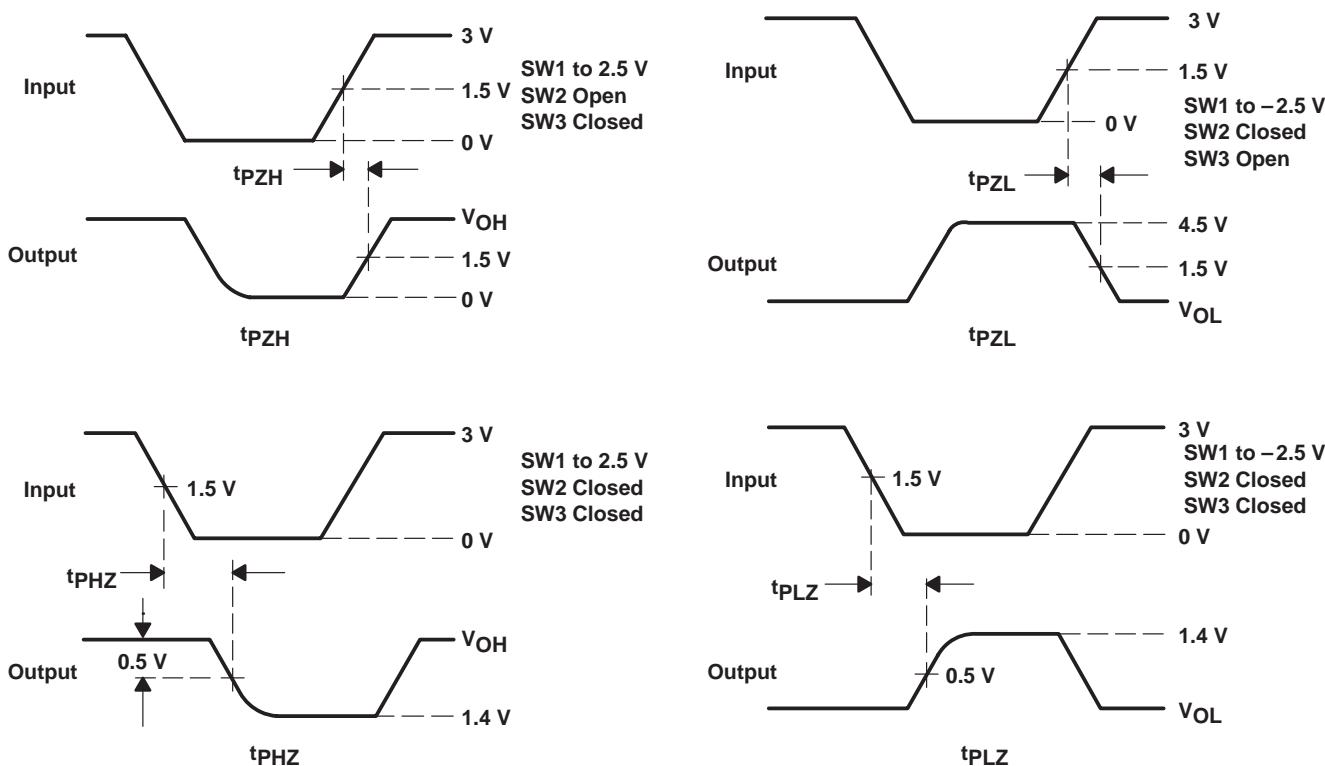
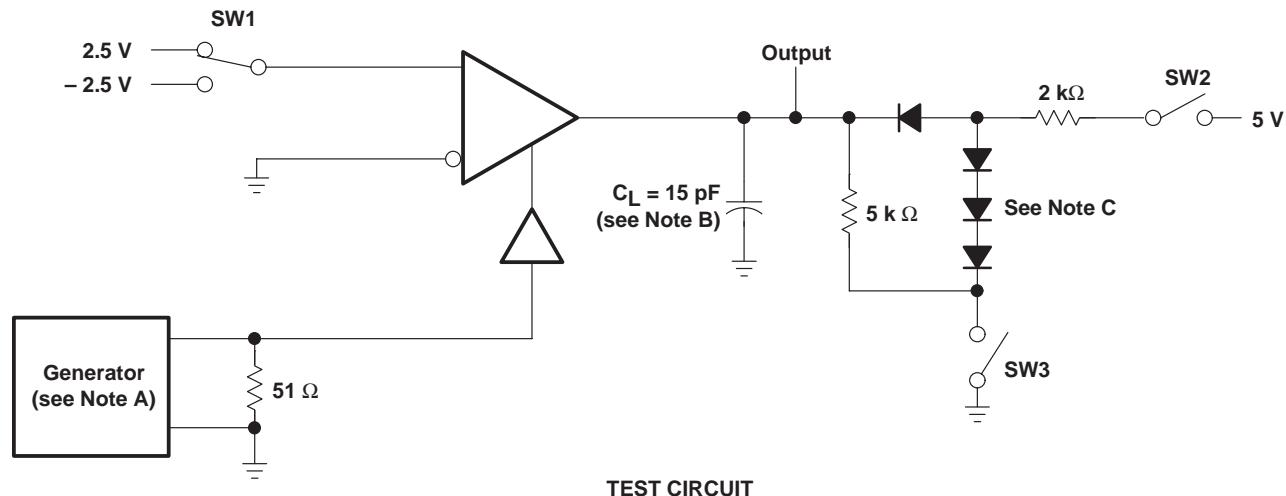


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle  $\leq$  50%,  $Z_O = 50 \Omega$ ,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns.  
 B.  $C_L$  includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

## PARAMETER MEASUREMENT INFORMATION

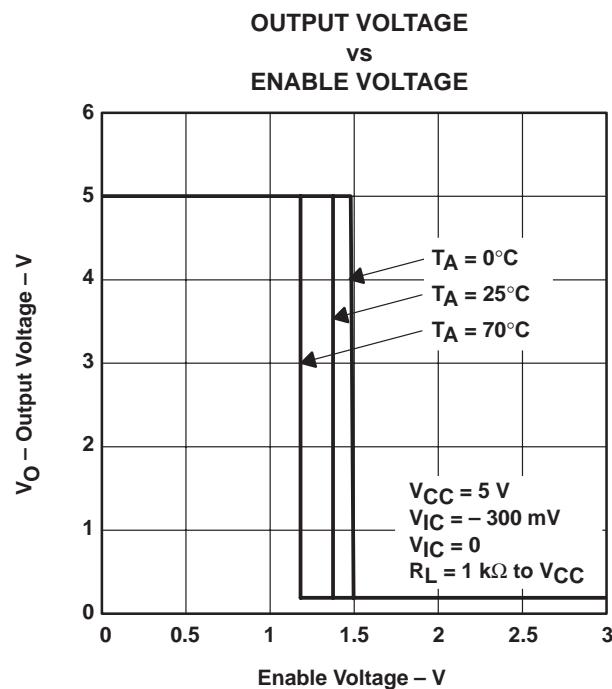
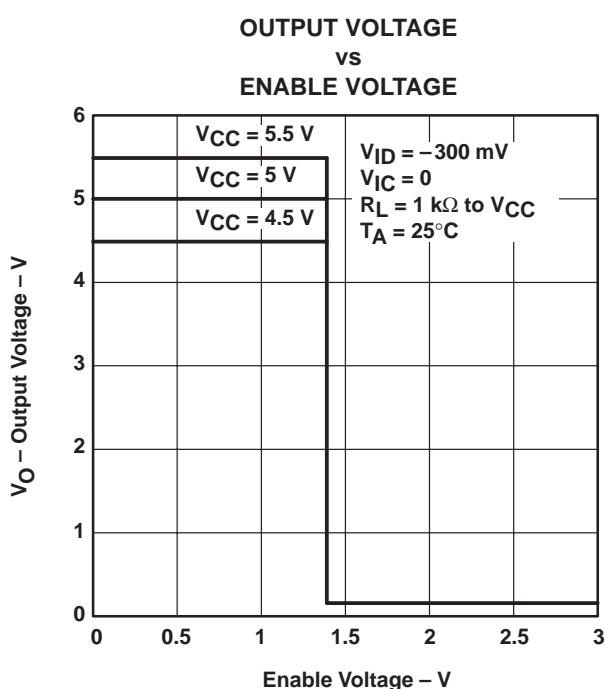
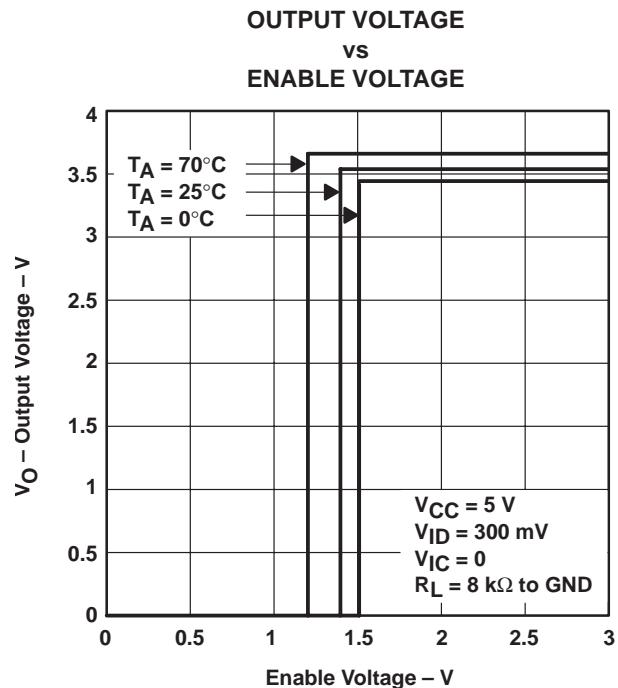
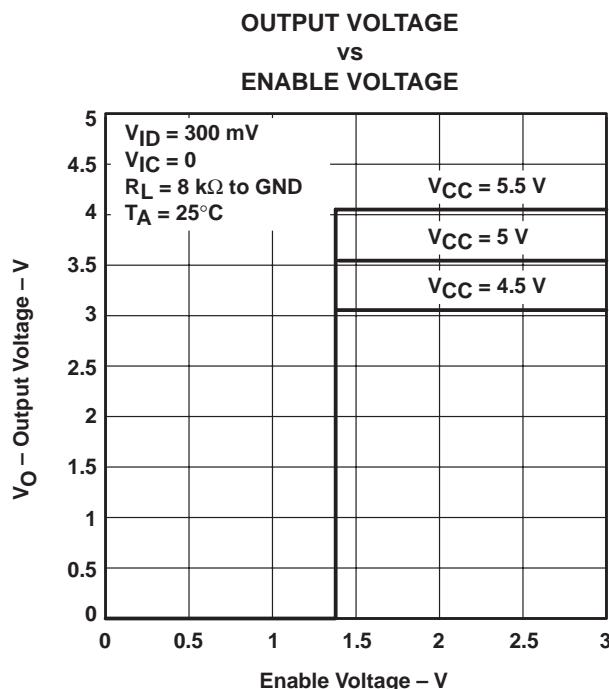


NOTES:

- The input pulse is supplied by a generator having the following characteristics: PRR  $\leq$  1 MHz, duty cycle  $\leq$  50%,  $Z_O = 50 \Omega$ ,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns.
- $C_L$  includes probe and jig capacitance.
- All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



# SN75ALS199

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

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### TYPICAL CHARACTERISTICS

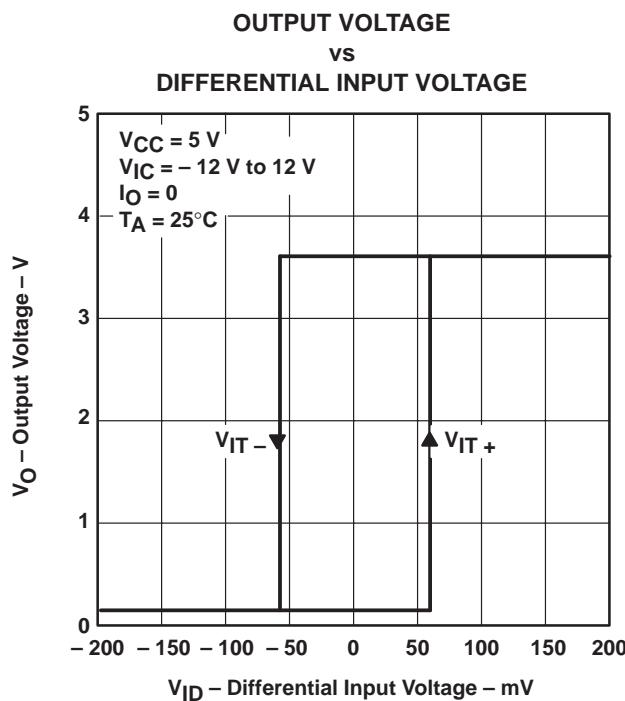


Figure 8

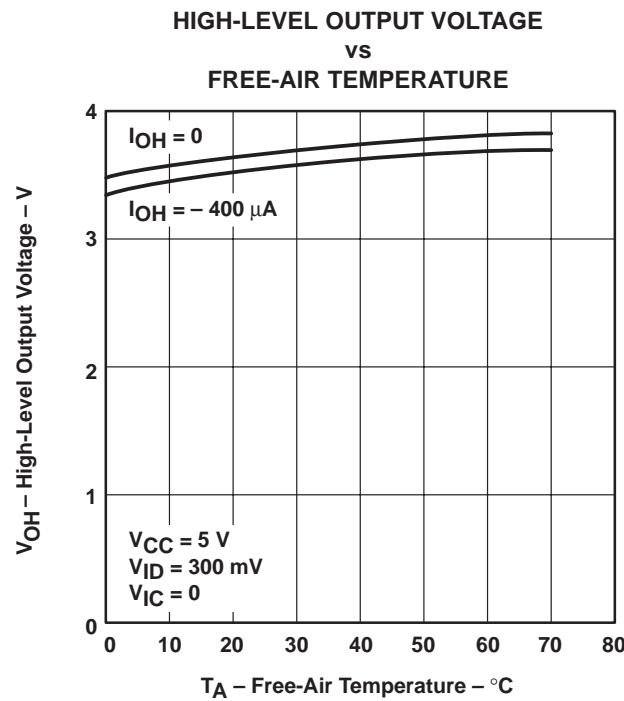


Figure 9

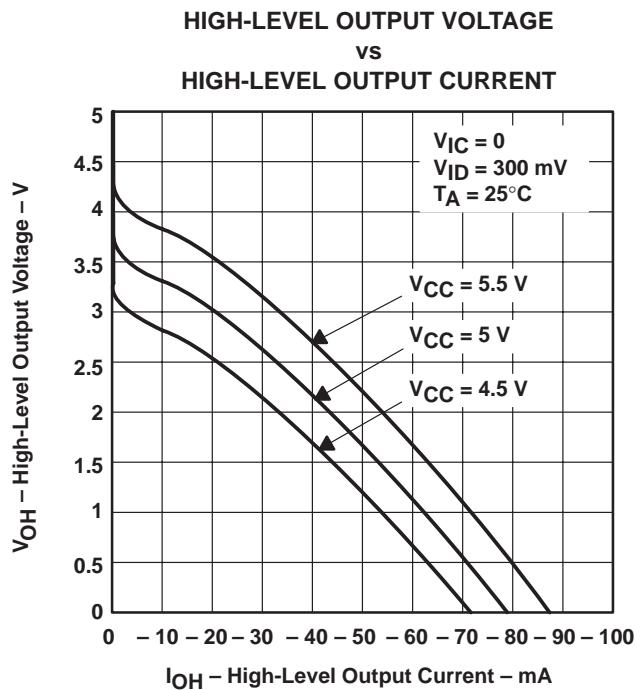


Figure 10

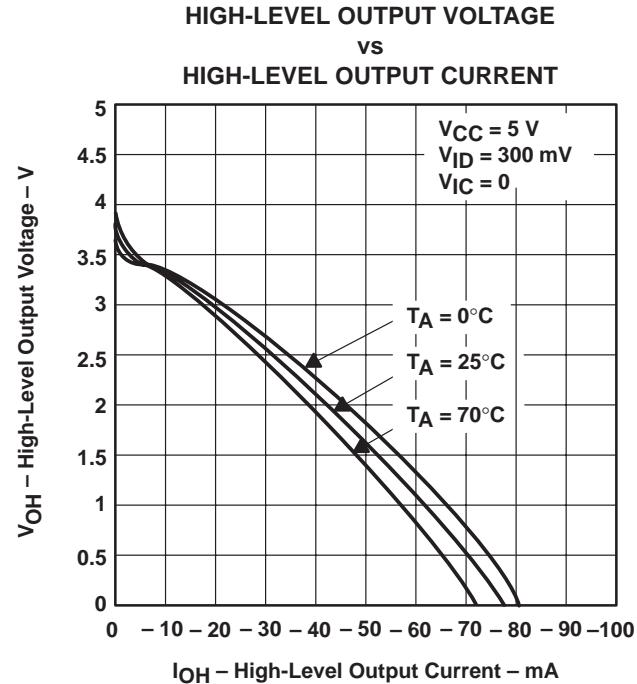


Figure 11

TYPICAL CHARACTERISTICS

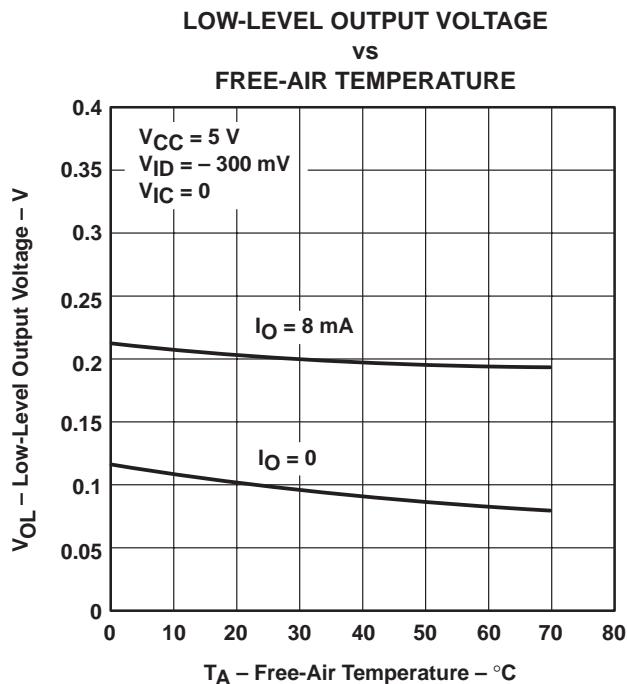


Figure 12

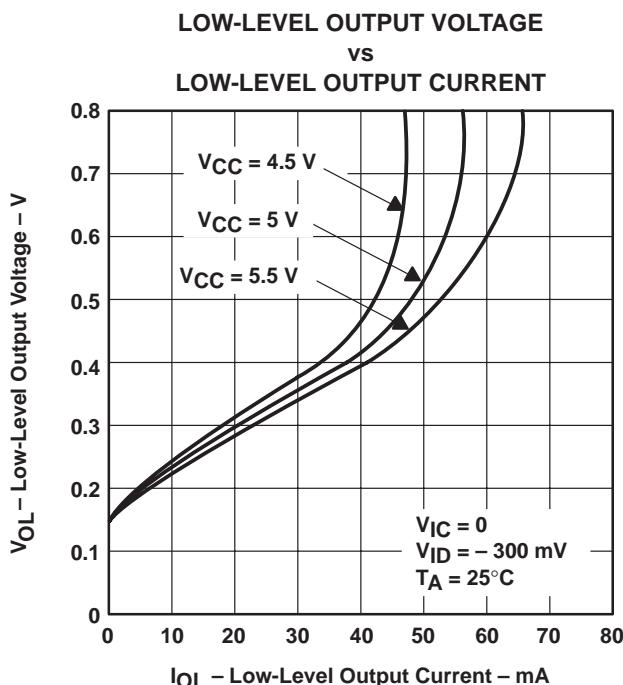


Figure 13

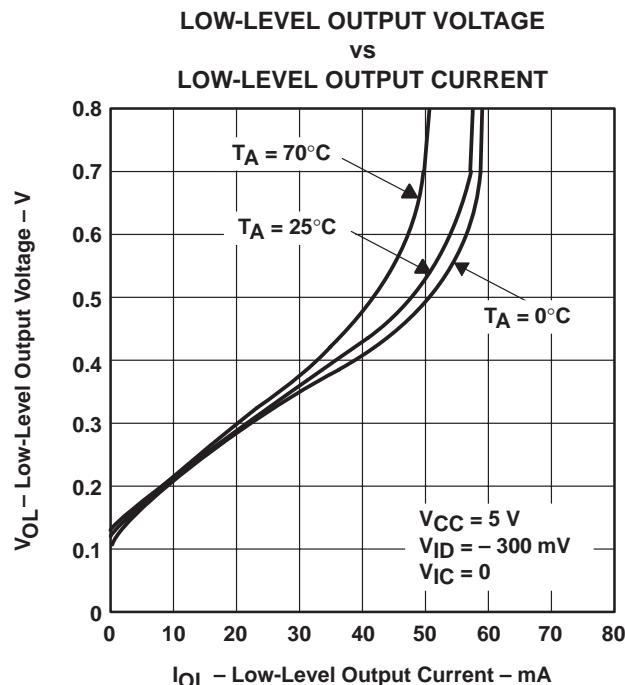


Figure 14

# SN75ALS199

## QUADRUPLE DIFFERENTIAL LINE RECEIVER

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### TYPICAL CHARACTERISTICS

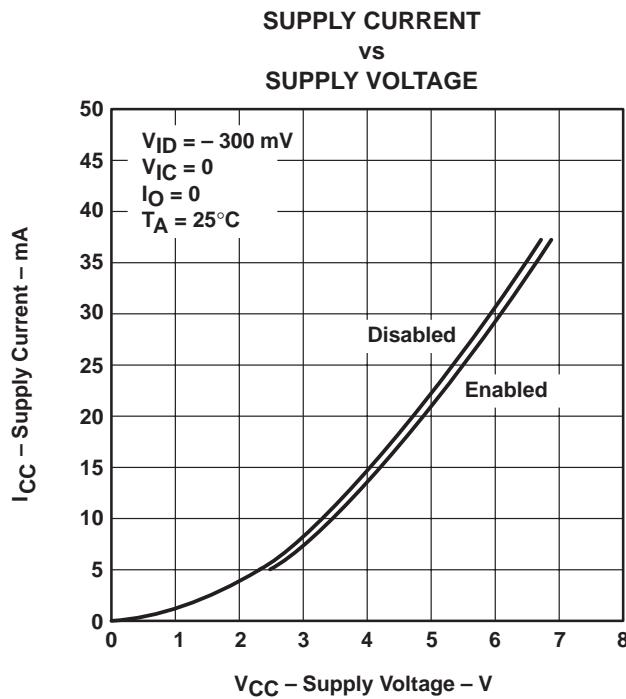


Figure 15

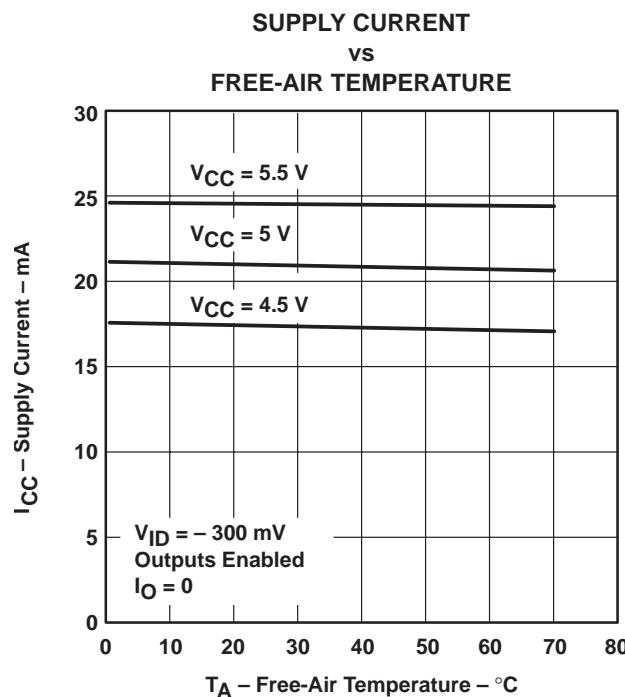


Figure 16

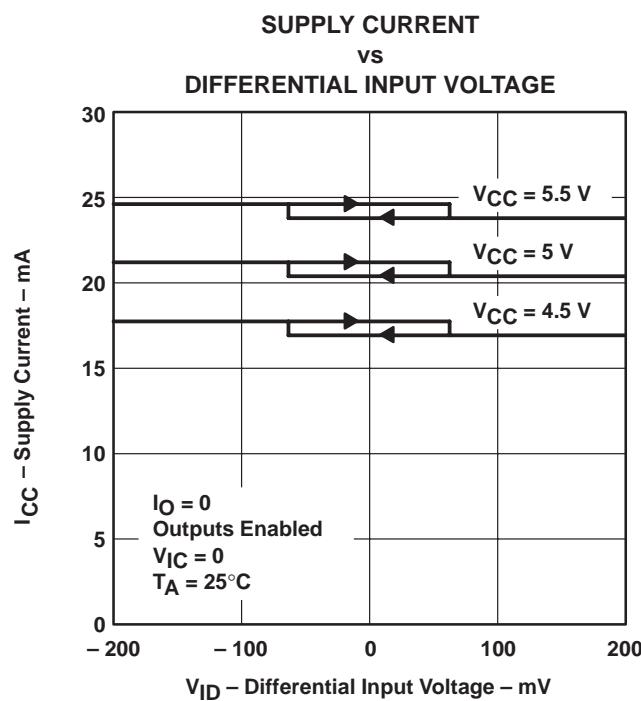


Figure 17

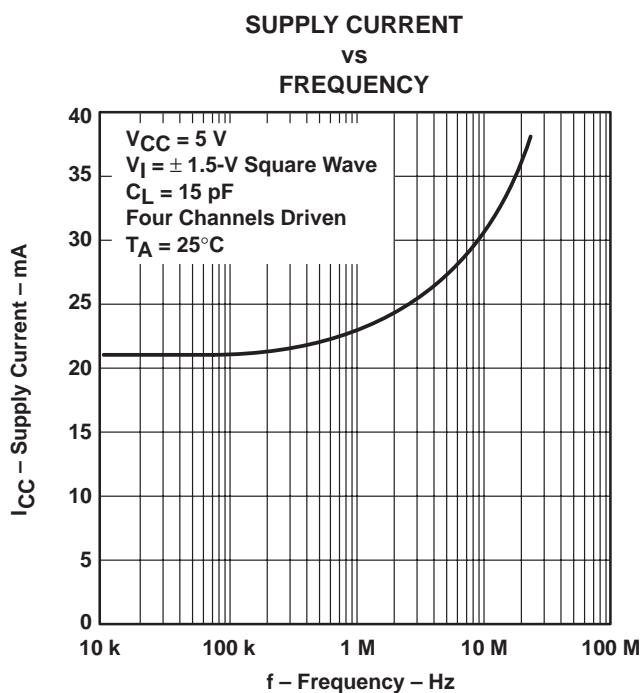


Figure 18

TYPICAL CHARACTERISTICS

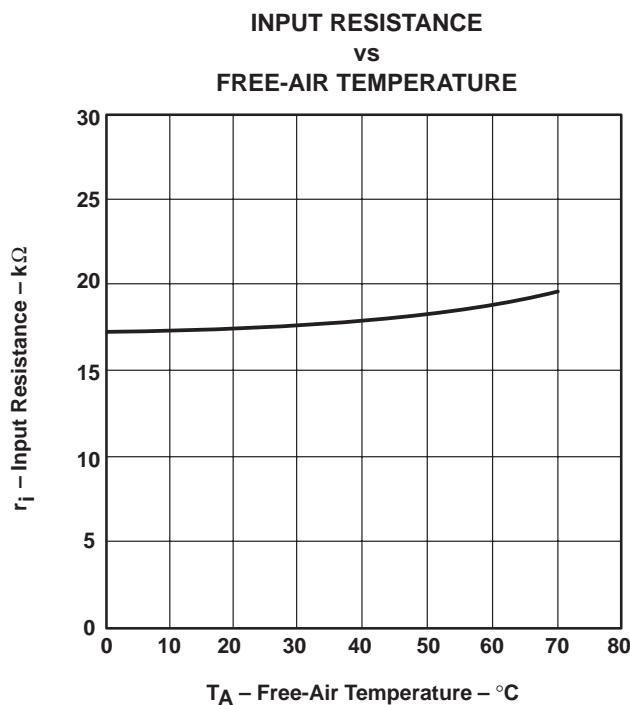


Figure 19

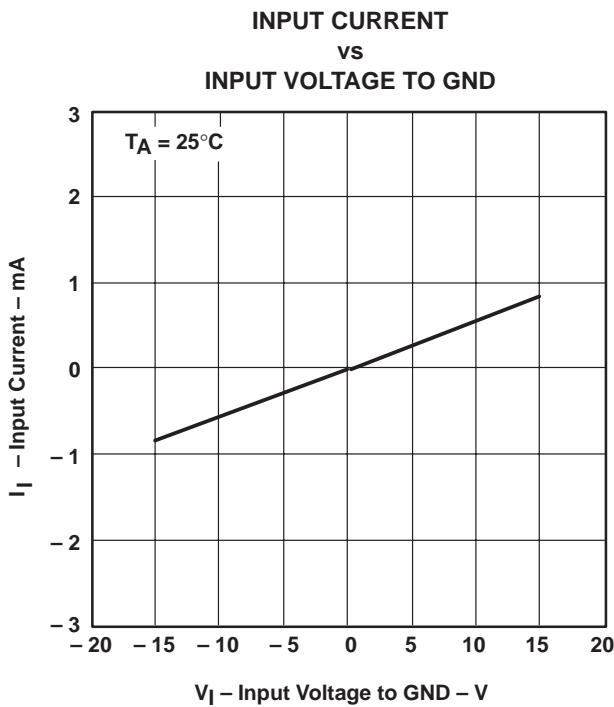


Figure 20

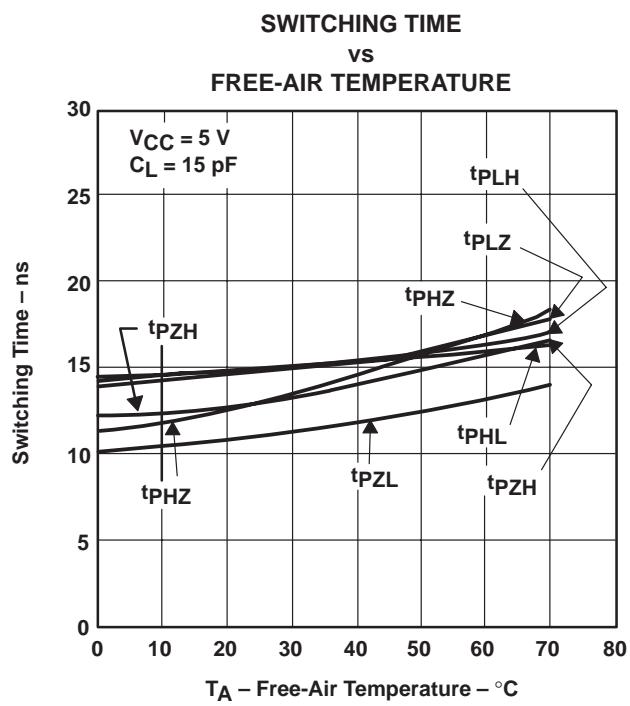


Figure 21

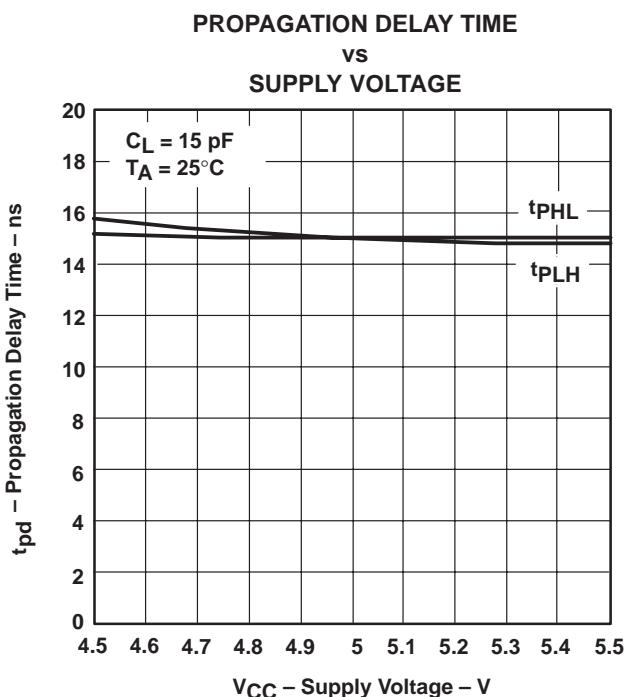


Figure 22

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Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75ALS199D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS199DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS199DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS199DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS199DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS199DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS199N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75ALS199NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

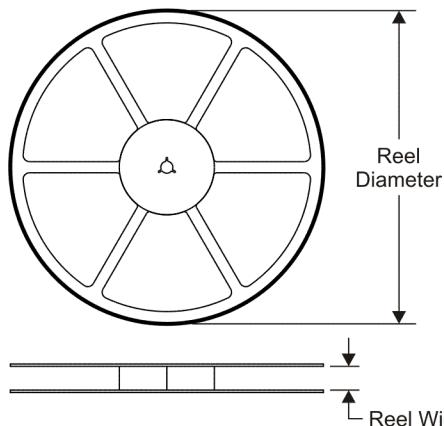
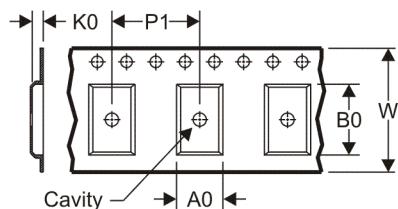
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

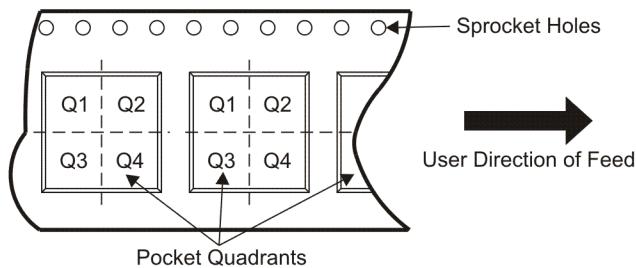
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


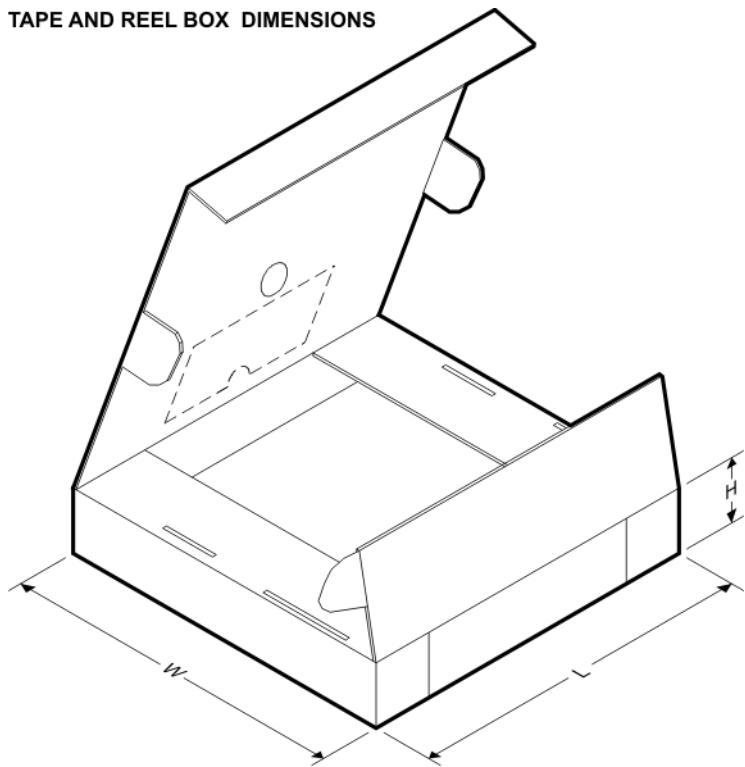
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS199DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

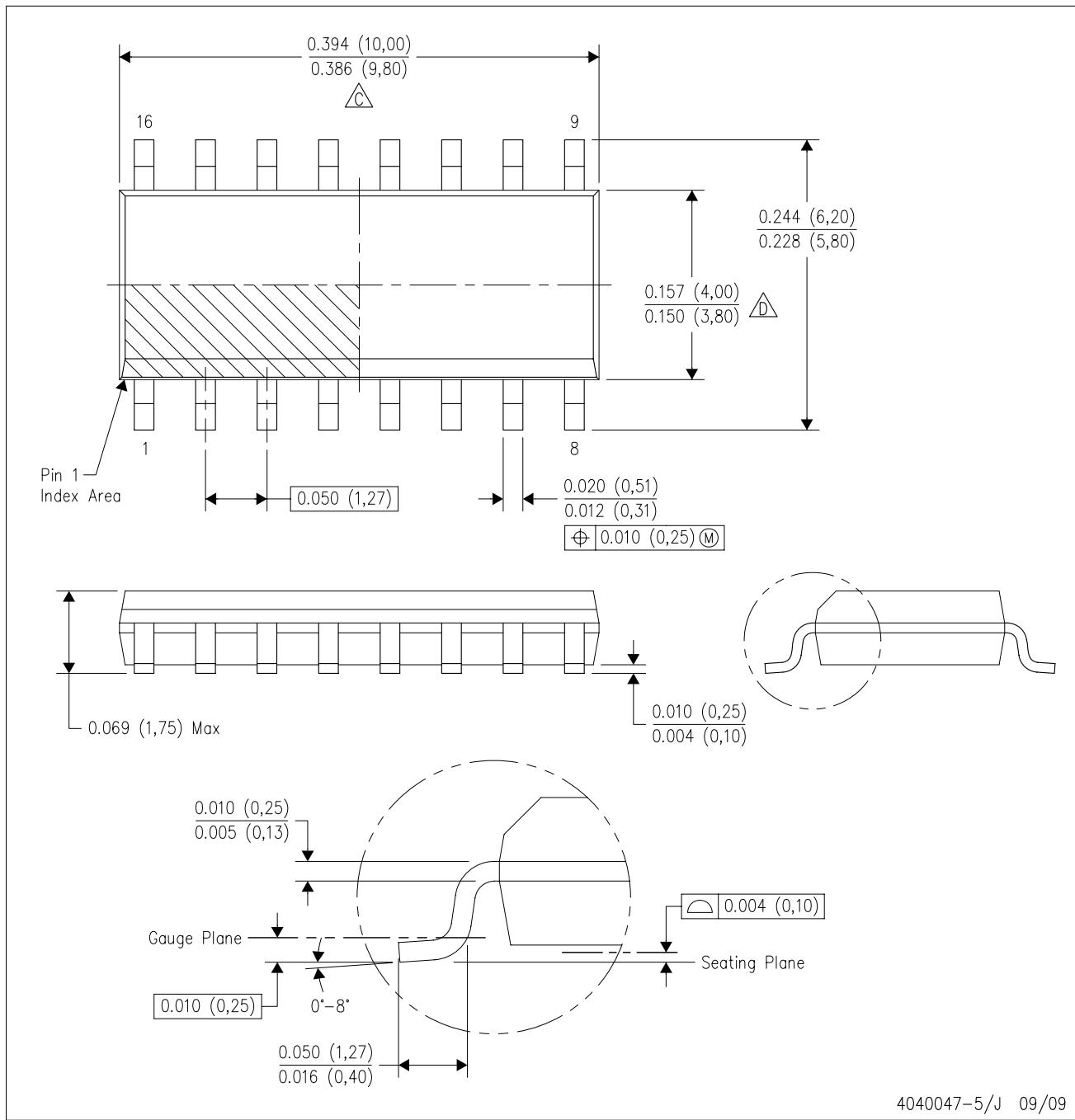


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS199DR	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

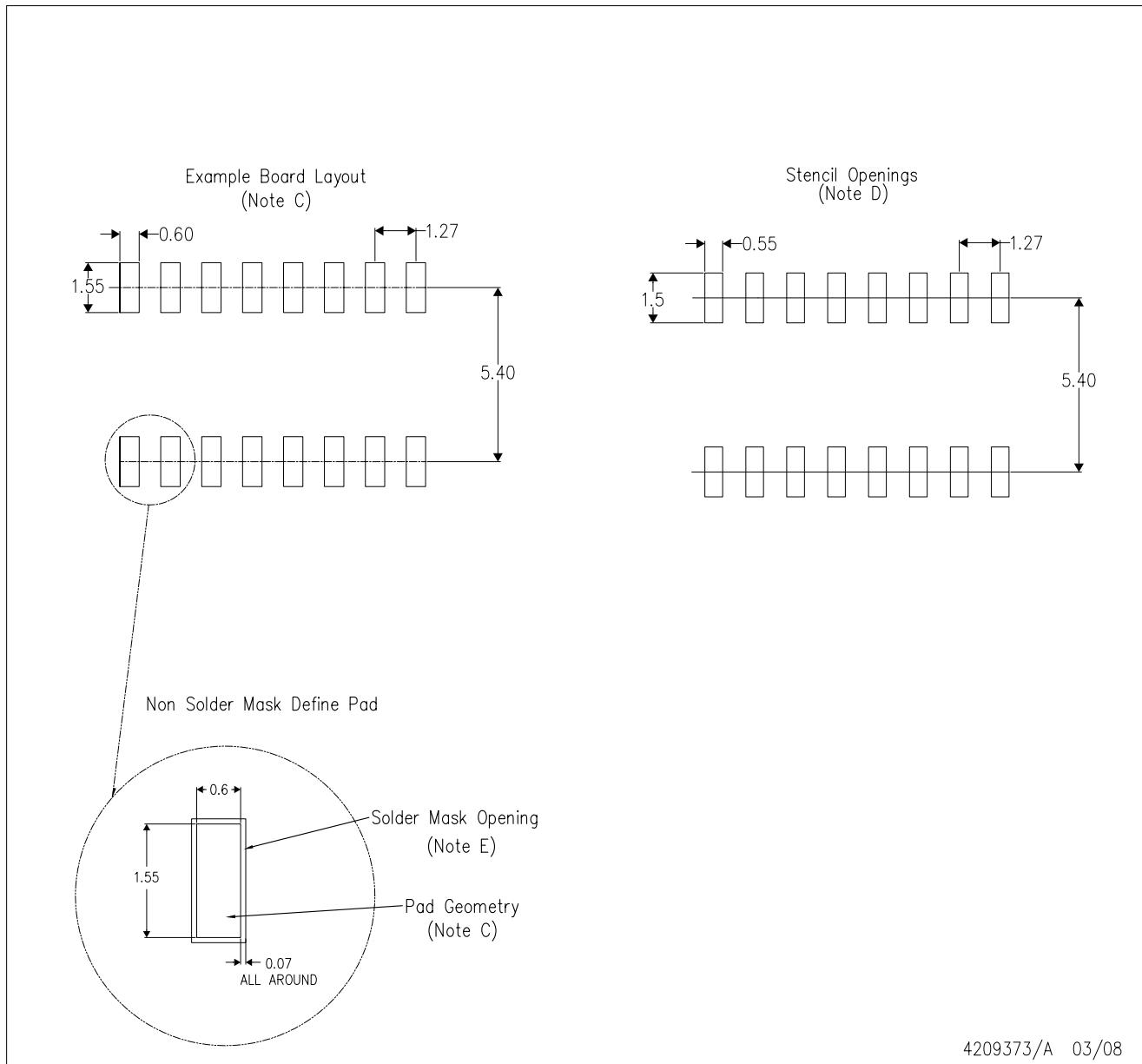
B. This drawing is subject to change without notice.

△C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

△D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



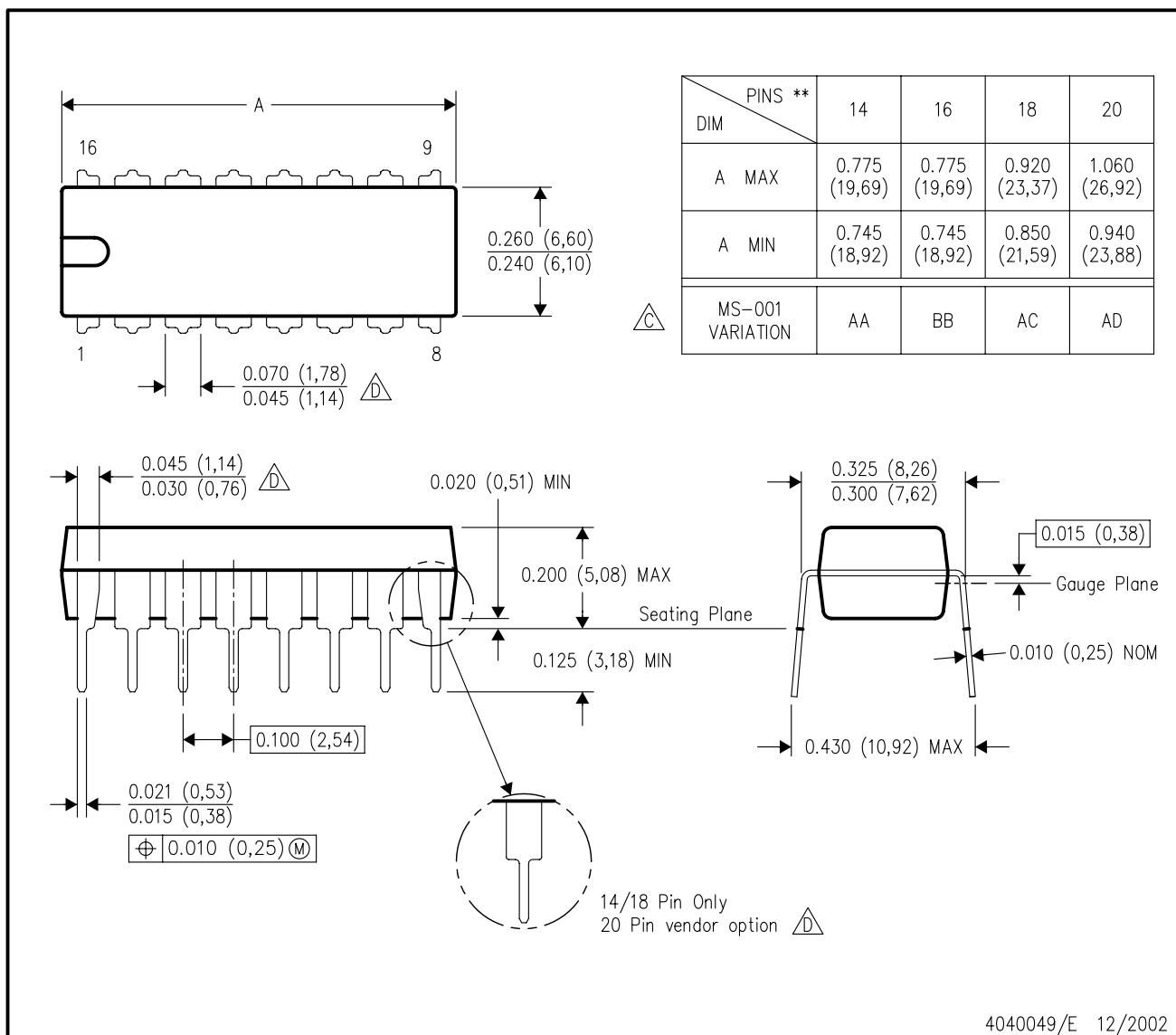
NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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