# Evaluation Board For PulSAR 48 Lead ADCs

Preliminary Technical Data

# EVAL-AD76XXEDZ

## FEATURES

**Converter and Evaluation Development (EVAL-CED1Z) compatibility**
**Versatile analog signal conditioning circuitry**
**On-board reference, clock oscillator and buffers**
**Buffered 14, 16 (or 18) bit parallel outputs**
**Buffered serial port interface**
**Ideal for DSP and data acquisition card interfaces**
**Analog and digital prototyping area**
**PC software for control and data analysis**

## GENERAL DESCRIPTION

The EVAL-AD76XXEDZ is an evaluation board for the 48 lead AD761X, AD762X, AD763X, AD764X, AD765X, AD766X, AD767X and AD795X 14-bit, 16-bit and 18- bit PulSAR® analog to digital converter (ADC) family. These low power, successive approximation register (SAR) architecture ADCs (see ordering guide for product list ) offer very high performance with 100kSPS to 3MSPS throughput rate range with a flexible parallel or serial interface. The evaluation board is designed to demonstrate the ADC's performance and to provide an easy to understand interface for a variety of system applications. A full description of the ADCs for this board are available at www.Analog.com/PulSAR and should be consulted when utilizing this evaluation board.

The evaluation board is ideal for use with Analog Devices USB based Converter and Evaluation Development EVAL-CED1Z, (CED) or as a stand-alone system. These boards are also compatible for use with the EVAL-CONTROL BRDxZ capture board and software for using this board is available on the website. Since many newer PC's do not offer a parallel port along with overcomplicated BIOS port settings, the CED board is strongly recommended.

The design offers the flexibility of applying external control signals and is capable of generating conversion results on parallel 14-bit, 16-bit or 18-bit wide buffered outputs. On-board components include a high precision band gap reference, (AD780, ADR431, or ADR435), reference buffers, a signal conditioning circuit with two op-amps and digital logic.

The EVAL-AD76XXEDZ interfaces to the CED capture board with a 96-pin DIN connector. A 40-pin IDC connector is used for parallel output, and test points are provided for the serial port. SMB connectors are provided for the low noise analog signal source, and for an externally generated $\overline{\text{CNVST}}$ (convert start input.

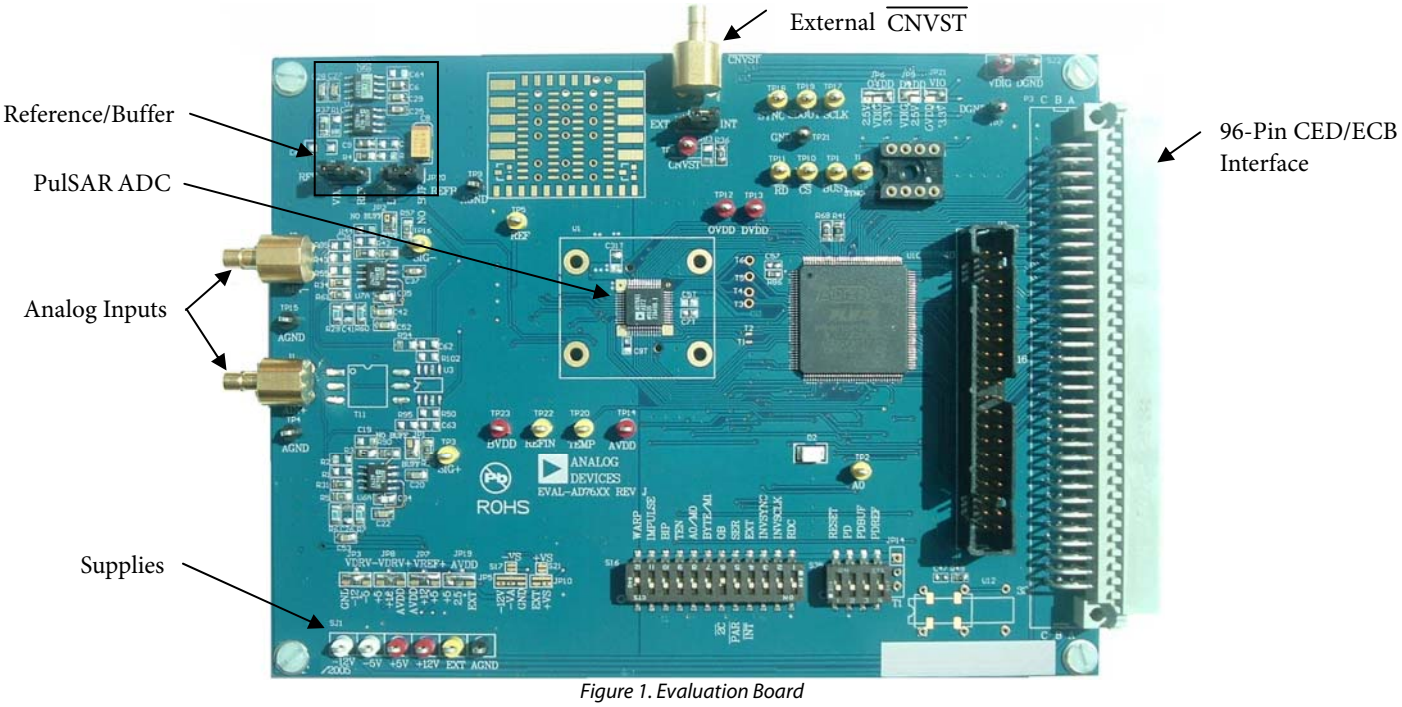


*Figure 1. Evaluation Board*

**Rev. PrB**

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## OVERVIEW

Figure 1 shows the EVAL-AD76XXEDZ evaluation board. When used in stand-alone mode or in conjunction with the EVAL-CED1Z, the gate array, U10, provides the necessary control signals for conversion and buffers the ADC data. The evaluation board is a flexible design that enables the user to choose among many different board configurations, analog signal conditioning, reference, and different modes of conversion data.

## CONVERSION CONTROL/MASTER CLOCK

Conversion start ($\overline{\text{CNVST}}$) controls the sample rate of the ADC and is the only input needed for conversion; all SAR timing is generated internally. $\overline{\text{CNVST}}$ is generated either by the gate array or externally via J3 (SMB) and setting JP22 in the external (EXT) position. The evaluation board is factory configured for the $\overline{\text{CNVST}}$ range shown in Table 1**.** Externally generated $\overline{\text{CNVST}}$ should have very low jitter and sharp edges for the maximum dynamic performance of the part. Since $\overline{\text{CNVST}}$ jitter usually results in poor SNR performance, it is recommended to use the on-board $\overline{\text{CNVST}}$ generation whenever possible.

The master clock (MCLK) source for the gate array is generated from the CED capture board or from U12, the 40MHz local oscillator selectable when using the accompanying software. The range for $\overline{\text{CNVST}}$ in

Table 1is a ratio generated from this master clock. In stand-alone mode, other clock frequencies can be used to change the gate array generated $\overline{\text{CNVST}}$ by this ratio. However, other timings will be affected – namely the slave serial clock (SCLK) interface. In serial slave mode, SCLK = MCLK.

While the ADC is converting, activity on the BUSY pin turns on the LED, D2. Additionally, the BUSY signal can be monitored test point TP1. Buffered conversion data (BD) is available at U10 on the output bus BD[0:15] on the 40-pin IDC connector P2, and on the 96-pin connector P3. When operating with the CED, data is transferred using a 16 bit bus and corresponding word and byte modes selectable with the software. For the 18 bit converters two consecutive 16 bit words are read, however, the ADC data is still read into the gate array as 18 bits. Additionally, BD is updated on the falling edge of BBUSY on P3-C17, and on the rising edge of $\overline{\text{DBUSY}}$ on P2-33. When either parallel or serial reading mode of the ADC is used, data is available on this parallel bus.

When using Serial Mode, serial data is available at T3, T4, T5, and T6 (SDOUT, SCLK, SYNC and RDERROR) and buffered serial data is output on TP17, TP18, and TP19 (SCLK, SYNC, and SDOUT). When using Slave Serial Mode, the external serial clock SCLK applied to the ADC is the MCLK, U12, frequency (40MHz). Refer to the device specific datasheet for full details of the interface modes.

## ANALOG INPUTS

The analog inputs amplifier circuitry (U6, U7 and discretes) allows configuration changes such as positive or negative gain, input range scaling, filtering, addition of a DC component, use of different op-amp and supplies depending on the ADC. The analog input amplifiers are set as unity gain buffers at the factory. The supplies are selectable with solder pads and are set for the ±12V range.

Table 1 shows the analog input range for the available evaluation boards.

The default configuration for the single ended (SE) unipolar ADCs sets U6 at mid-scale from the voltage divider ($V_{CM}$ * R6/(R6+R7)) and U7 at mid-scale from the voltage divider ($V_{CM}$ * R29(R29+R60)) for the differential unipolar ADCs.

For the bipolar devices (AD7663, AD665, AD7671), the buffer output is centered at 0V (mid-scale) as these boards are configured for the +/-5V input range. Note the input impedance is 1k ohm (R6, R29 =1k ohm to GND). To use another input range, the solder pads S[7:1] need to be reconfigured.

These input configurations allows a transition noise test (histogram) without any other equipment. In some applications, it is desired to use a bipolar or wider analog input range, for instance, ± 10V, ± 5V, ± 2.5V, or 0 to -5V. For ADCs which do not use these input ranges directly, simple modifications of the input driver circuitry can be made without any performance degradation. Refer to the datasheet under the *Application Hints* section for component values or to application note AN594 on the product web page for other input ranges.

Note that the AD7663, AD7665, and AD7671 evaluation boards are factory configured for the +/-5V range. For different ranges, the board needs appropriate solder pad configurations.

For dynamic performance, an FFT test can be done by applying a very low distortion AC source.

## POWER SUPPLIES AND GROUNDING

The evaluation board ground plane is separated into two sections: a plane for the digital interface circuitry and an analog plane for the analog input and external reference circuitry. To attain high resolution performance, the board was designed to ensure that all digital ground return paths do not cross the analog ground return paths by connecting the planes together directly under the converter. Power is supplied to the board through P3 when using with the EVAL-CED1Z

## USING THE EVAL-AD762X/AD765X/AD766X/ AD767XEDZ AS STAND-ALONE

Using the evaluation board as stand-alone does not require the CED nor does it require use of the accompanied software. When the CONTROL input to the gate array is LOW, which is pulled down by default, the gate array provides the necessary signals for conversion and buffers the conversion data.

In stand-alone mode, the gate arrays flexible logic buffers the ADC data according to the read data mode configuration (word or byte). In parallel reading mode the board is configured for continuous reading since $\overline{CS}$ and $\overline{RD}$ are always driven LOW by the gate array. Thus, the digital bus is not tri-stated in this mode of operation and BD[0:15] will continuously be updated after a new conversion. BD[0:15] is available on P2 after BUSY goes HIGH. Note that with the 18 bit devices the full 18 bits of data BD[-2:15] are output directly on P2 since the evaluation board is not limited to 16 bit wide transfers in stand-alone operation. When either parallel or serial reading mode, the data is available on this parallel bus. Refer to Figure 9 to obtain the data output pins on P2.

### *Configuration Switches*

The evaluation board is configurable for the different operating modes with 16 positions on the configuration select switches, S16 and S35. A description of each switch setting and jumper position is listed in Figure 9 and the available test points are listed in Table 5. Note that the switches in the ON position define a logic HIGH level (pulled up with 10kΩ,) and that the switches are active only in stand-alone mode.

For all interface modes, S16 and S35 allows the selection of:
Warp, Normal or Impulse mode conversions (where applicable)
Binary or 2s complement data output
Reading during or after conversion
Resetting the ADC
ADC power-down
Internal Reference and Buffer power-down (where applicable)

In parallel reading mode, s16 allows the selection of:
Byte swapping for 8 bit interfacing (LSByte with MSByte)
18-bit, 16-bit and 8-bit interfacing (for 18-bit converters)

In serial reading mode, the default settings are Master Read during Conversion Mode using the internal ADC serial clock. Serial data is available at T3, T4, T5 and T6 for SDOUT, SCLK, SYNC and RDERROR respectively. Buffered serial data is output on the three test points TP17, TP18 and TP19 for SCLK, SYNC, and SDOUT respectively.

For serial reading mode, S16 allows the selection of:
Choice of inverting SCLK and SYNC
Choice of using internal or external (slave mode) SCLK

## SCHEMATICS/PCB LAYOUT

The EVAL-AD76XXEDZ is a 4-layer board carefully laid out and tested to demonstrate the specific high accuracy performance of the PulSAR ADC. Figure 8 to Figure 10 show the schematics of the evaluation board. The printed circuit layouts of the board are given in Figure 11 - Figure 16. Note these layouts are not to scale.

Top side silk-screen - Figure 11
Top side layer - Figure 12
Ground layer - Figure 13
Shield layer - Figure 14
Bottom side layer - Figure 15
Bottom side silk-screen - Figure 16

## SUPPLYING POWER FOR STAND-ALONE USE

Power needs to be supplied through the two power supply blocks SJ1 and SJ2. Linear supplies are recommended. SJ1 is the analog supply for the ADC (AVDD), front end op amps and reference circuitry. SJ2 is the digital supply for the ADC (DVDD, OVDD) and gate array. The supplies to the device are configurable through the power supply jumpers shown in . In most applications four supplies are required; ±12V and +5V for analog, and +5V for digital. On board regulators, where applicable, are used to reduce the operating voltages to the correct levels. The analog and digital supplies can be from the same source however, R27 (typically 20Ω) is required from AVDD to DVDD. In this configuration, JP9, DVDD selection, should be left open. Furthermore, the OVDD (ADC digital output supply) may need to be brought up after the analog +5V supply. See datasheet for details.

## EVALUATION BOARD SETTING FOR BIPOLAR ADC INPUT CONFIGURATIONS

The AD7610, AD7612, AD7631, AD7634, AD7663, AD7665, AD7671, AD7951 and AD7952 can use both unipolar and bipolar ranges. The available options are +/-10V, +/-5V, +/-2.5V, 0 to 10V, 0 to 5V and 0 to 2.5V (depending on the ADC).

For the AD7663, AD7665 and AD7671 the evaluation board is set for the ±5V bipolar input range since these ADCs input ranges are hardware pin strapped. Simple modifications to these evaluation boards can be made to accommodate the different input ranges by changing the INA-IND inputs with the available solder pads.

### *iCMOS ADCs*

For the AD7610, AD7612, AD7631 AD7634 and AD7951, the evaluation board can use all input ranges since the input range is controlled by software (or S16 DIP switches in stand-alone mode).

For operating in unipolar mode for any of the bipolar evaluation boards it is recommended to use the voltage divider consisting of ($V_{CM}$ * R6/(R6+R7)) and ($V_{CM}$ * R29/(R29+R60)). This allows a transition noise test without any additional equipment.

## HARDWARE SETUP

### *Using EVAL-CED1Z Capture Board*

- EVAL-AD76XXEDZ PulSAR ADC evaluation board
- EVAL-CED1Z
- Enclosed World compatible 7V DC supply
- Enclosed USB to mini USB cable
- DC source (low noise for checking different input ranges)
- AC source (low distortion)
- Band pass filter suitable for 16 or 18 bit testing (value based on signal frequency)

- PC operating Windows XP.

Proceed to the Software Installation section to install the software. **Note: The EVAL-CED1Z board must not be connected to the PC's USB port until the Software is installed.** The 7V DC supply can be connected however to check the board has power (green LED lit).

## SOFTWARE INSTALLATION

It is recommended to close all Windows' applications prior to installing the software.

### *System Requirements*

- PC operating Windows XP.
- USB 2.0 (for CED board)
- Administrator privileges

***CD-ROM*** –Navigate to Software\CED Version x.x, double click on *setup.exe* and follow the instructions on the screen. If another version of Analog Devices PulSAR Evaluation Software is present, it may be necessary to remove this. To remove, click on the Windows "Start" button, select "Control Panel" and "Add or Remove Programs". When the list populates, navigate to Analog Devices High Resolution sampling ADC's Evaluation Software or PulSAR Evaluation Software and select Remove.

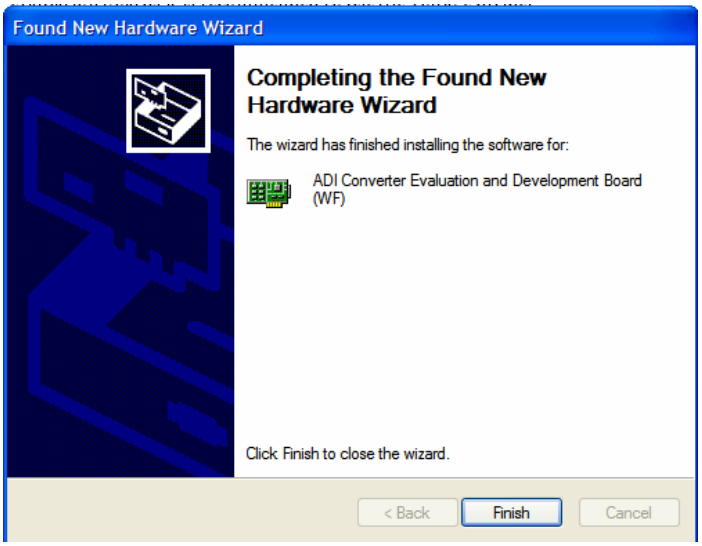
### *Website Download*

The software versions are also available from the Analog Devices PulSAR Analog to Digital Converter Evaluation Kit page. After downloading the software, it is recommended to use the WinZip "Extract" function to extract all of the necessary components as opposed to just clicking on *setup.exe* in the zipped file. After extracting, click on *seteup.exe* in the folder created during the extraction and follow the instructions on the screen. If another version exists, it may be necessary to remove as detailed in the above CD-ROM section.

### *USB Drivers*

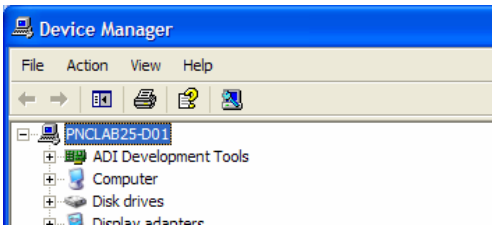
The software will also install the necessary USB drivers. After installing the software, power up the CED board and connect to the PC USB 2.0 port. The Windows "Found New Hardware" Wizard will display. Click on Next to install the drivers automatically.

When installed properly, Windows displays the following.



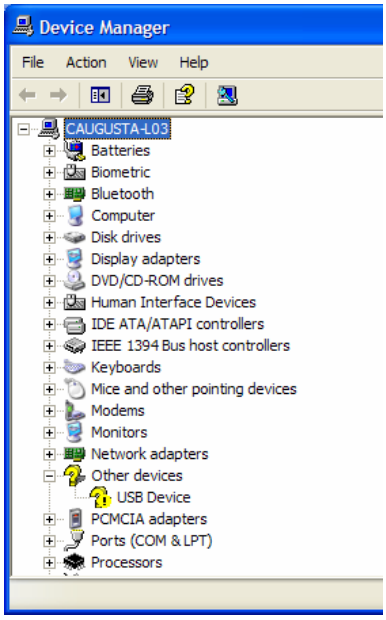

On some PCs, the Found New hardware Wizard may show up again and if so follow the same procedure to install it properly.

The "Device Manager" can be used to verify that the driver was installed successfully.

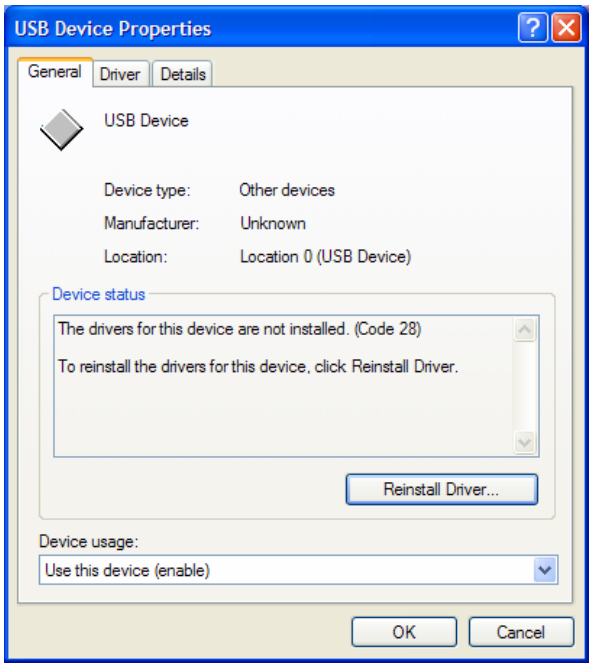



### *Troubleshooting the Install*

If the driver was not installed successfully the device manager will display a question mark for "Other devices" as Windows does not recognize the CED1Z board.




The "USB Device" can be opened to view it's uninstalled properties.




This is usually the case if the software and drivers were installed by a user without administrator privileges. If so, log on as an administrator with full privileges and reinstall the software.

## RUNNING THE EVALUATION SOFTWARE

The evaluation board includes software for analyzing the AD7682, AD7689, AD7699 and AD7949. The EVAL-CED1Z is required when using the software. The software is used to perform the following tests:

- Histogram for determining code transition noise (DC)
- Fast Fourier transforms (FFT) for signal to noise ratio (SNR), SNR and distortion (SINAD), total harmonic distortion (THD) and spurious free dynamic range (SFDR)

The software is located at *C:\Program Files\Analog Devices\PulSAR ADC Evaluation Software\Eval PulSAR CED.exe*.

A shortcut is also added to the Windows "Start" menu under *"Analog Devices PulSAR ADC Evaluation Software", "Eval PulSAR CED"*. To run the software, select the program from either location.

## SETUP SCREEN

Figure 2 is the setup screen where ADC device selection, test type, input voltage range, sample rate and number of samples are selected.

## DC TESTING - HISTOGRAM

Figure 4 shows a screen shot for the histogram screen. This tests the ADC for the code distribution for DC input and computes the mean and standard deviation, or transition noise of the converter and displays the results. Raw data is captured and passed to the PC for statistical computations. To perform a histogram test, select "Histogram" from the test selection window and click on the "Start" radio button. Note: a histogram test can be performed without an external source since the evaluation board has a buffered $V_{REF}/2$ source at the ADC input for unipolar parts and at 0V for bipolar devices. To test other DC values, apply a source to the J1/J2 inputs. It is advised to filter the signal to make the DC source noise compatible with that of the ADC. C26/C41 provide this filtering.

## AC TESTING

Figure 6 is a screen shot of the fast Fourier transform, FFT. This tests the traditional AC characteristics of the converter and displays an FFT of the result. As in the histogram test, raw data is captured and passed to the PC where the FFT is performed thus displaying SNR, SINAD, THD and SFDR. The data can also be displayed in the time domain. To perform an AC test, apply a sinusoidal signal to the evaluation board at the SMB inputs J1 for IN+ and J2 for IN-. Low distortion, better than 100dB, is required to allow true evaluation of the part. One possibility is to filter the input signal from the AC source. There is no suggested bandpass filter but consideration should be taken in the choice. Furthermore, if using a low frequency bandpass filter when the full-scale input range is more than a few Vpp, it is recommended to use the on board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

**Table 1. $\overline{\text{CNVST}}$ Generation, Analog Input Range**

| Part | Resolution (bits) | Sample Rate | Analog Input Range | Analog Input Type |
|---|---|---|---|---|
| AD7621 | 16 | 3 MSPS | 0 to 2.5V | Diff, Unipolar |
| AD7622 | 16 | 2 MSPS | 0 to 2.5V | Diff, Unipolar |
| AD7623 | 16 | 1.33 MSPS | 0 to 2.5V | Diff, Unipolar |
| AD7641 | 18 | 2 MSPS | 0 to 2.5V | Diff, Unipolar |
| AD7643 | 18 | 1.25 MSPS | 0 to 2.5V | Diff, Unipolar |
| AD7650 | 16 | 100 kSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7651 | 16 | 100 kSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7652 | 16 | 500 kSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7653 | 16 | 1 MSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7660 | 16 | 100 kSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7661 | 16 | 100 kSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7663 | 16 | 250 kSPS | -5V to +5V[1] | Single Ended, Bipolar |
| AD7664 | 16 | 570 kSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7665 | 16 | 570 kSPS | -5V to +5V | Single Ended, Bipolar |
| AD7666 | 16 | 500 kSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7667 | 16 | 1 MSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7671 | 16 | 1 MSPS | -5V to +5V | Single Ended, Bipolar |
| AD7674 | 18 | 800KSPS | 0 to 5V | Diff, Unipolar |
| AD7675 | 16 | 100 kSpS | 0 to 2.5V | Single Ended, Unipolar |
| AD7676 | 16 | 500 kSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7677 | 16 | 1 MSPS | 0 to 2.5V | Single Ended, Unipolar |
| AD7678 | 18 | 100KSPS | 0 to 5V | Diff, Unipolar |
| AD7679 | 18 | 571KSPS | 0 to 5V | Diff, Unipolar |

[1] Available Input Ranges are 0 to 2.5V, 0 to 5V, 0 to 10V, +/- 2.5V, +/-5V, and +/- 10V. however the board is factory configured for the +/-5V input range. Modify S1 to S7 accordingly (see schematics and datasheets) for different input range configuration.

**Table 2. Jumper Description**

| Jumper | Name | Default Position | Function |
|---|---|---|---|
| JP1, JP2 | BUFF | BUFF | Buffer amplifier: BUFF = use op amps to buffer analog input. NO BUFF = direct input from J1, J2 (SMB). |
| JP3 | VDRV- | -12V | Buffer amplifier negative supply: Selection of -12V, -5V or GND when using EVAL-CED1Z or voltages on SJ1 in stand alone mode. |
| JP4 | REFS | REF | Reference selection: REF = use on board reference output for ADC reference. VDD = use analog supply (AVDD) for ADC reference. |
| JP6 | OVDD | 3.3V | ADC digital output supply voltage: Selection of 2.5V, 3.3V and VDIG. VDIG = +5V when using EVAL-CED1Z or voltage on SJ2 in stand-alone mode. |
| JP7 | VREF+ | +12V | Reference circuit positive supply: Selection of +12V, +5V or AVDD when using EVAL-CED1Z or voltages on SJ1 in stand alone mode. |
| JP8 | VDRV+ | +12V | Buffer amplifier positive supply: Selection of +12V, +5V or AVDD when using EVAL-CED1Z or voltages on SJ1 in stand alone mode. |
| JP9 | DVDD | VDIG/2.5[1] | ADC digital supply voltage: Selection of +2.5V or VDIG (+5V) when using EVAL-CED1Z or voltage on SJ2 in stand-alone mode. |
| JP19 | AVDD | +5V/2.5[1] | ADC analog supply voltage: Selection of +2.5V, +5V or EXT when using EVAL-CED1Z |
| JP20 | REFB | BUF | Reference buffer: BUFF = use U2 to buffer or amplify reference source. NO BUFF = use reference directly into ADC. |
| JP21 | VIO | 3.3V | Gate array I/O voltage: Selection of 3.3V or OVDD. Note: gate array will be damaged if >3.3V (ie. when using OVDD = VDIG). |
| JP22 | $\overline{\text{CNVST}}$ | INT | $\overline{\text{CNVST}}$ source: INT = use gate array to generate $\overline{\text{CNVST}}$. EXT = use external source into J3, SMB for $\overline{\text{CNVST}}$. |

[1] For AD7621/22/23//25/41/43 these are set to +2.5V. Note that setting these to +5V will permanently destruct the ADC.

**Table 3. S16 - Configuration Select Switch Description**

Note: (OFF = LOW, ON = HIGH)

| Position | Name | Default Position | Function |
|---|---|---|---|
| 1 | WARP | LOW | Conversion mode selection: Used in conjunction with IMPULSE. When HIGH with IMPULSE= LOW, the fastest (Warp) mode is used for maximum throughput. When LOW and IMPULSE = LOW, Normal mode is used. |
| 2 | IMPULSE | LOW | Conversion mode selection: Used in conjunction with WARP. When HIGH with WARP = LOW, a reduced power mode is used in which the power consumption is proportional to the throughput rate. |
| 3 | BIP | LOW | For future use. |
| 4 | TEN | LOW | For future use. |
| 5 | A0/M0 | LOW | A0, input Mux selection: Used for AD7654/AD7655 (refer to datasheet).<br>M0, data output interface selection: Used along with M1 for 18-bit ADCs. |
| 6 | BYTE/M1 | LOW | BYTESWAP, used for 8-bit interface mode on 16-bit ADCs: MSByte is swapped with LSByte on 8 data lines.<br>M1, data output interface selection: Used along with M0 for 18-bit ADCs. |
| 7 | OB/$\overline{\text{2C}}$ | HIGH | Data output select: LOW = Use 2's complement output. HIGH = Straight binary output. |
| 8 | SER/$\overline{\text{PAR}}$ | LOW | Data output interface select: LOW = Parallel interface. HIGH = Serial interface. |
| 9 | EXT/$\overline{\text{INT}}$ | LOW | Serial clock source select: LOW = Use ADC internal serial clock, SCLK is an output. HIGH= Use external clock, which is MCLK (40 MHz) and SCLK is an input. Not used in parallel reading mode. |
| 10 | INVSYNC | LOW | Serial sync (SYNC) active state: LOW = SYNC is active HIGH. HIGH = SYNC is active LOW. Used only for Master mode (internal SCLK). Not used in parallel reading mode. |
| 11 | INVSCLK | LOW | Serial clock (SCLK) active edge: LOW = Use SCLK falling edge. HIGH = Use SCLK rising edge. Active in all serial modes. Not used in parallel reading mode. |
| 12 | RDC | LOW | Read during convert: LOW = Read data after conversion (BUSY = LOW). HIGH = Read data during conversions (BUSY = HIGH). Used in both parallel and serial interface modes. |

**Table 4. S35 - Configuration Select Switch Description**

Note: (OFF = LOW, ON = HIGH)

| Position | Name | Default Position | Function |
|---|---|---|---|
| 1 | RESET | LOW | Reset ADC: LOW = Enables the converter. HIGH = Abort conversion (if any). |
| 2 | PD | LOW | Power down: LOW = Enables the converter . HIGH = Powers down the converter. Power consumption is reduced to a minimum after the current conversion. |
| 3 | PDBUF | LOW | Internal reference buffer power down: LOW = Enable on chip buffer. HIGH = Power down internal buffer. |
| 4 | PDREF | LOW | Internal reference power down: LOW = Enable on chip reference. HIGH = Power down internal reference. Note that when using the on chip reference, the buffer also needs to be enabled (PDREF = PDBUF = HIGH). |

**Table 5.Test Points**

| Test Point | Available Signal | Type | Description |
|---|---|---|---|
| TP1 | BUSY | Output | BUSY signal. |
| TP2 | A0/M0 | Input | Same as S16, position 5 |
| TP3 | SIG+ | Input | Analog +input. |
| TP4 | AGND | GND | Analog ground close to SIG+. |
| TP5 | REF | Input/Output | Reference input. Output for devices with on-chip reference. |
| TP7 | DGND | GND | Digital ground near SJ2. |
| TP8 | $\overline{\text{CNVST}}$ | Input | $\overline{\text{CNVST}}$ signal. |
| TP9 | AGND | GND | Analog ground close to REF. |
| TP10 | $\overline{\text{CS}}$ | Input | $\overline{\text{CS}}$, chip select signal. |
| TP11 | $\overline{\text{RD}}$ | Input | $\overline{\text{RD}}$, read signal. |
| TP12 | OVDD | Power | Digital output supply. |
| TP13 | DVDD | Power | Digital core supply. |
| TP14 | AVDD | Power | Analog supply. |
| TP15 | AGND | GND | Analog ground close to SIG-. |
| TP16 | SIG- | Input | Analog –input for differential parts. |
| TP17 | SCLK | Input/Output | Buffered serial clock. |
| TP18 | SYNC | Output | Buffered serial sync. |
| TP19 | SDOUT | Output | Buffered serial data. |
| TP20 | TEMP | Output | TEMP, for ADC with internal reference. Outputs temperature dependant voltage (approx. 300mV with $T_A$ = 25°C). |
| TP22 | REFIN | Input/Output | For ADCs with internal reference, REFBUFIN can be used to connect external reference into the reference buffer input when PDBUF = LOW and PDREF = HIGH. With the internal reference (and buffer) enabled, this pin will produce the internal bandgap reference voltage. |
| TP23 | BVDD | Output | Internal reference bandgap supply. Connected to AVDD via s19. |
| T3 | SDOUT | Output | Direct ADC serial data. |
| T4 | SCLK | Input/Output | Direct ADC serial clock. |
| T5 | SYNC | Output | Direct ADC serial SYNC. |
| T6 | RDERROR | Output | Direct ADC serial read error. |

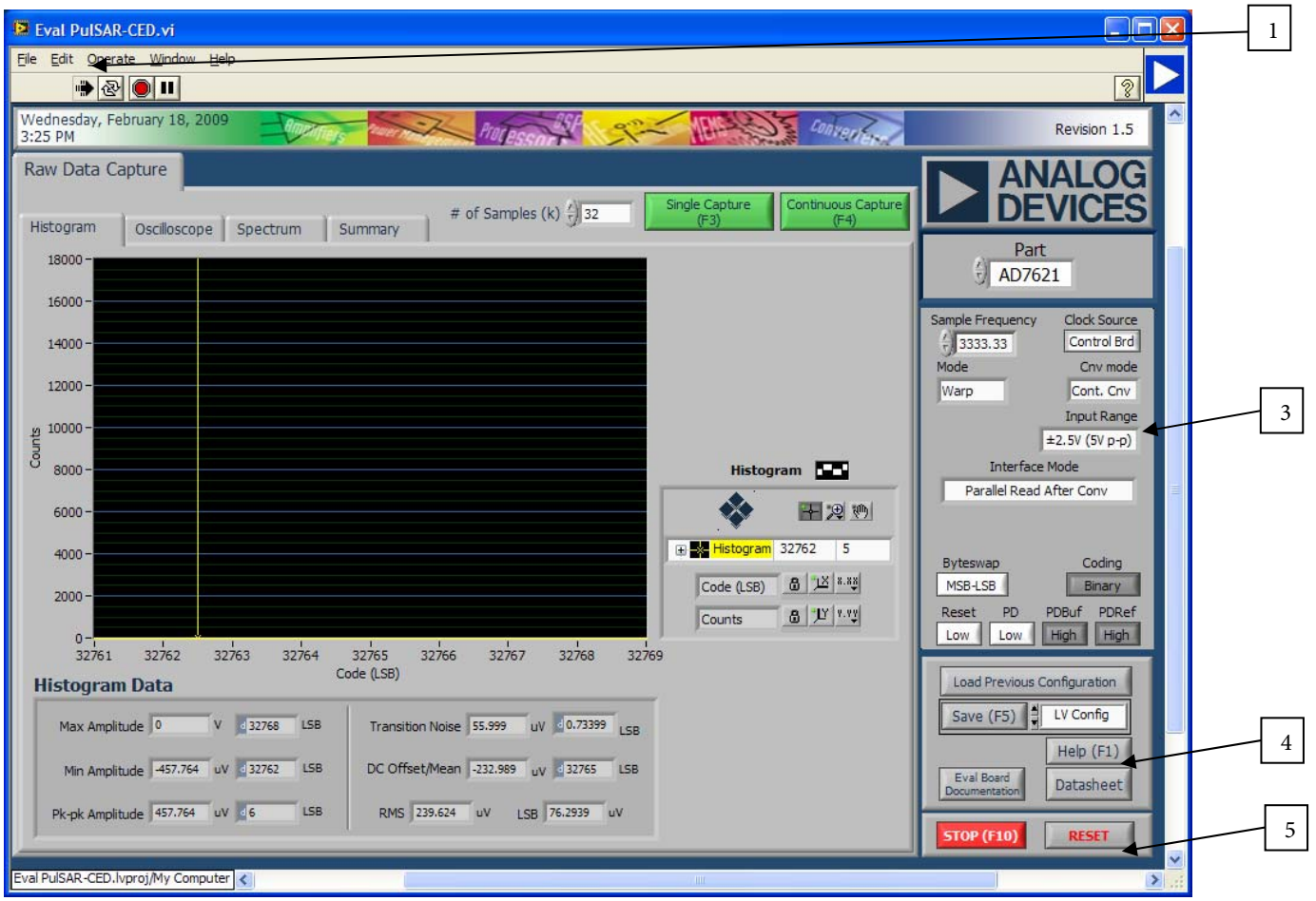



*Figure 2. Setup Screen*

**1.** The arrow is used to start the software. When running is displayed.

**2.** The part to be evaluated is selected here.

**3.** The controls are used to set:

***Sample Frequency*** – Enter in kHz Units can be used such as 3k (case sensitive) for 3,000,000 Hz or 3MSPS.

***Clock Source*** - Selections between control (capture) board or evaluation board.

***Mode*** – This selects the conversion mode of operation. Some ADCs have different modes Warp, Normal, and Impulse.

***Cnv Mode*** – Conversion mode; this selects between continuous (Cont.) or Burst conversion modes. In continuous mode, the ADC is continuously converting. In Burst mode, the ADC is not converting (sample clock held in inactive state) and the conversions begin once the "*Single Capture*" or "*Continuous Capture*" buttons have been selected.

***Interface mode*** – This selects the digital interface to the on-board FPGA.

***Byteswap*** – A subset of the digital interface mode, this is used to demonstrate byte-wide transfers to the FPGA.

***Coding*** – Another subset to the digital interface mode, this can be used to select straight binary or 2's complement output. Note the time domain chart and data output (F5) plots and saves data in straight binary.

***Reset*** – Resets the ADC.

***PD, PDREF, PDBUF*** – These can be used to power down the ADC, internal reference and internal reference buffer.

**4**. These controls are used for saving, printing, help, etc. and are also accessed in the File menu.

Save (F5): type – LabView config, allows the current configuration to be saved to a *filename.dat* file. Useful when changing many of the default controls. To load the saved configuration, use the Load Previous Configuration.

Type – Html, saves the current screen shot to an Html file.

Type – Spreadsheet, saves the current data displayed in the chart in a tab delimited spreadsheet. Raw ADC Data is time domain in Codes, FFT or Decimated is in dB.

**5**. Stop (F10) is used to stops the software. The can also be used to stop the software. RESET is used to reset the CED or ECB capture boards.

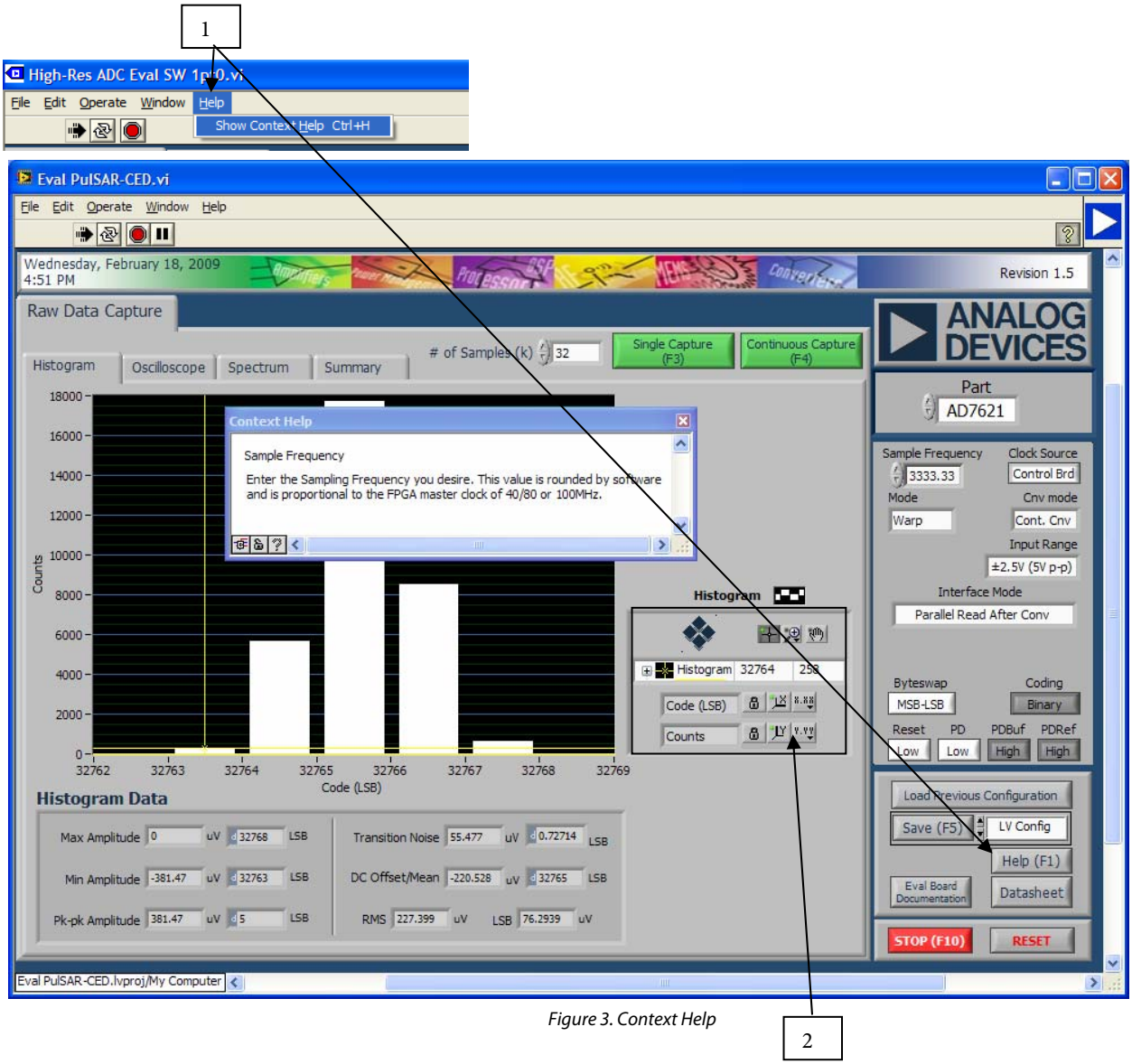



*Figure 3. Context Help*

**1.** To use the on-screen help. Select Help, Show Context Help or click the Help (F1). An example of the Context Help is shown above for the Sample Frequency. Placing the curser on most screen items displays useful help for the particular control or displayed unit.

**2.** These controls are used for axes and zooming panning.

Locks the graph axis to automatically fit the data.

Uses last axis set by user. , rescale the axes to the automatic values.

, are used to set axes properties such as format, precision, color, etc. Right mouse click to change to Hexadecimal, number of digits, etc.

Displays the cursor.

Is used For zooming in and out.

Is used for panning.

Is used to set various graph properties such as graph type, colors, lines, etc.

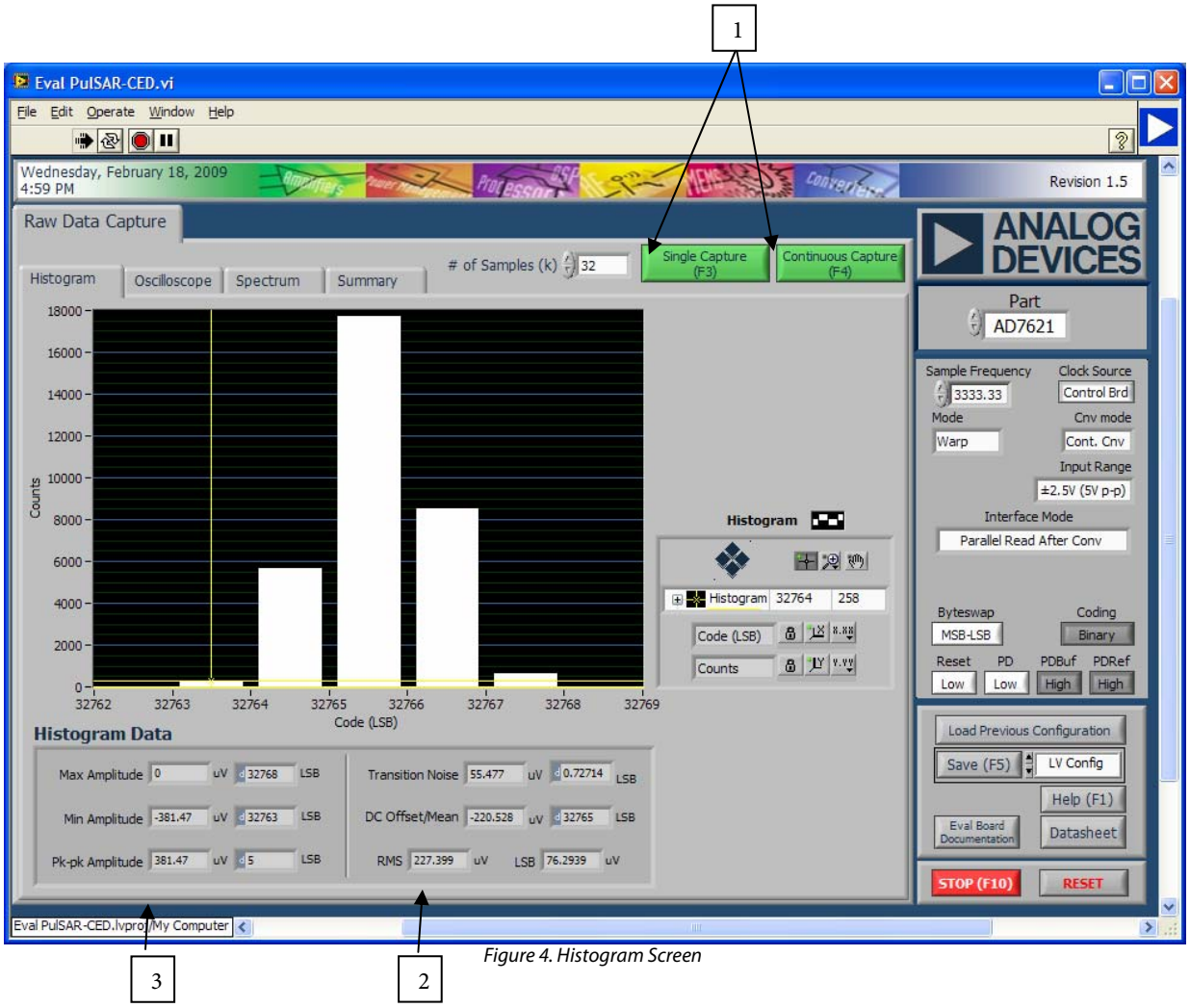
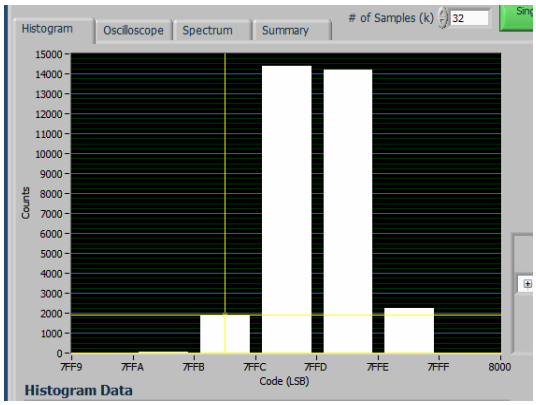
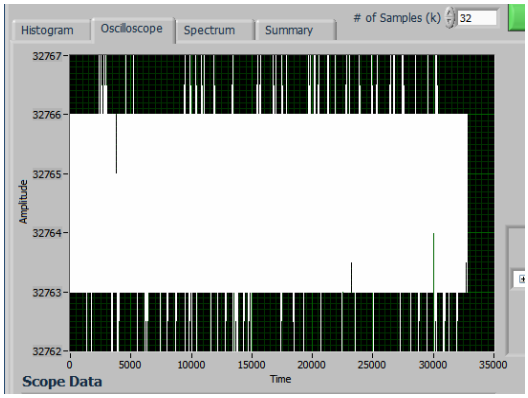



*Figure 4. Histogram Screen*

**1.** These radio buttons are used to perform a Single Capture or Continuous Capture of data set in the *# of Samples* field. The results are displayed in the chart. Note that the results can be displayed as:




A Histogram




Or an Oscilloscope (time domain)

**2., 3.**These display the statistics for the X and Y-axes, respectively.

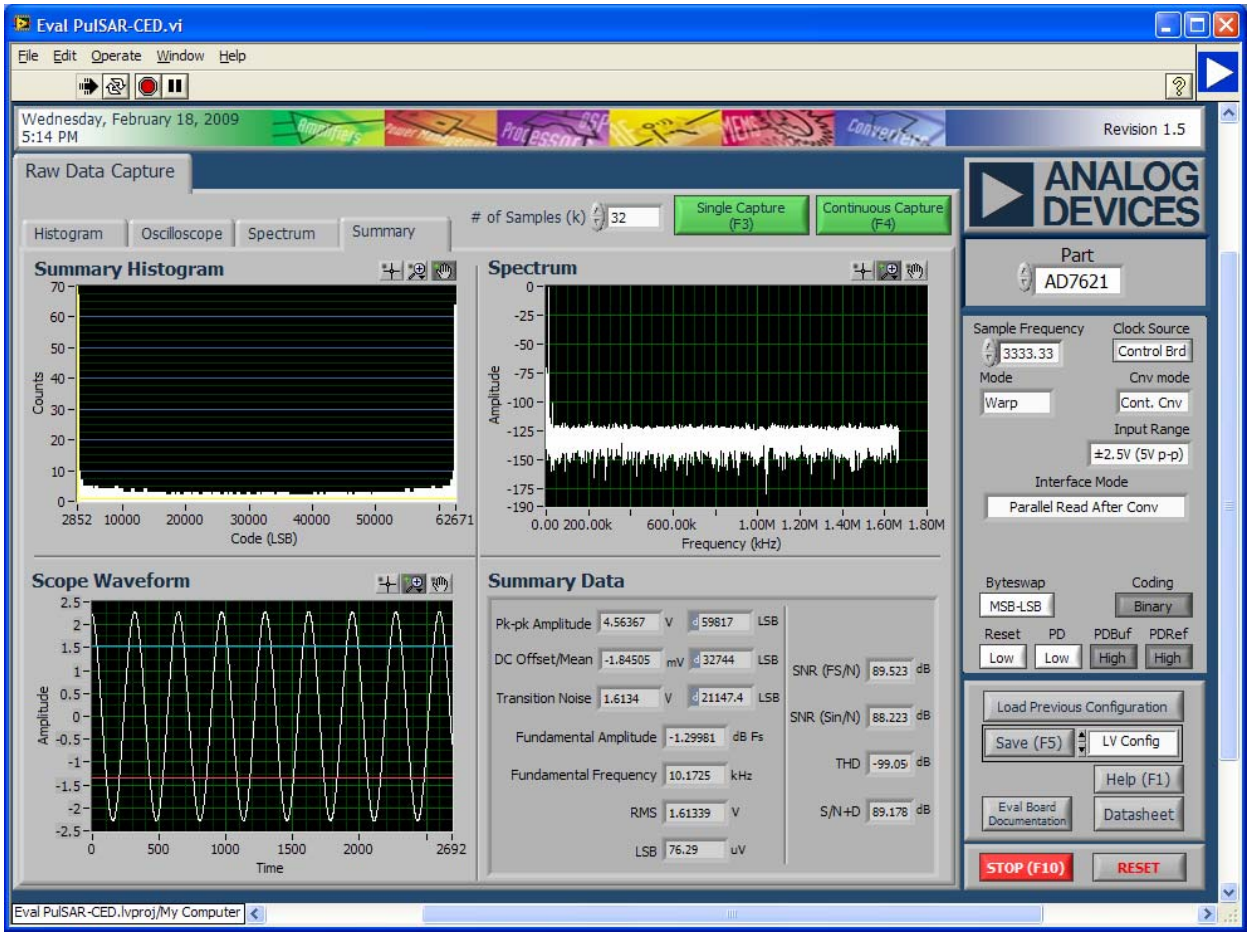
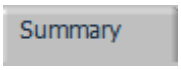



*Figure 5. Summary*

The charts can be displayed together when the  tab is selected.

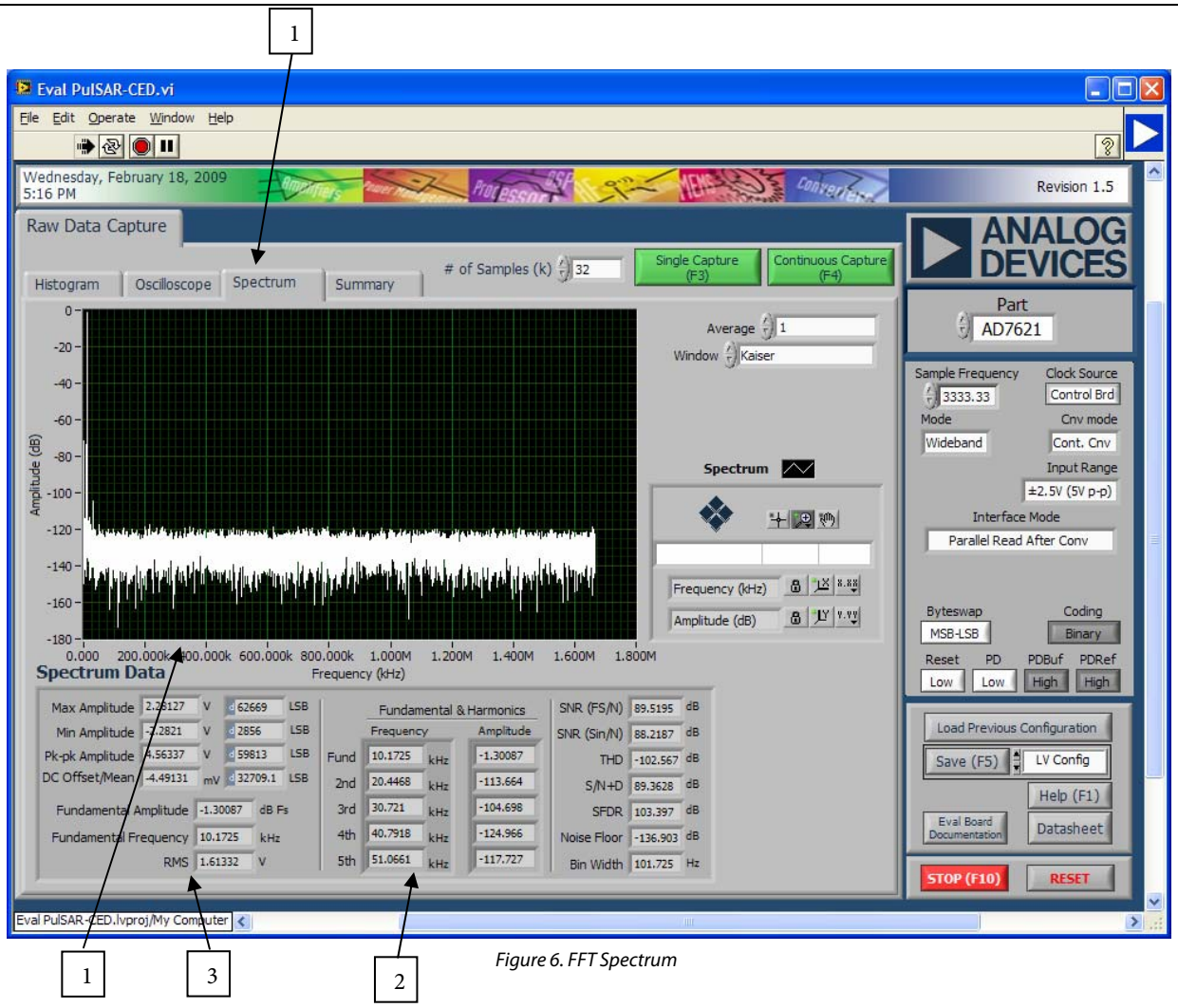



*Figure 6. FFT Spectrum*

**1.** Displays the FFT when the Spectrum chart is selected

**2., 3.** Display the data for the X and Y-axes, respectively.

.

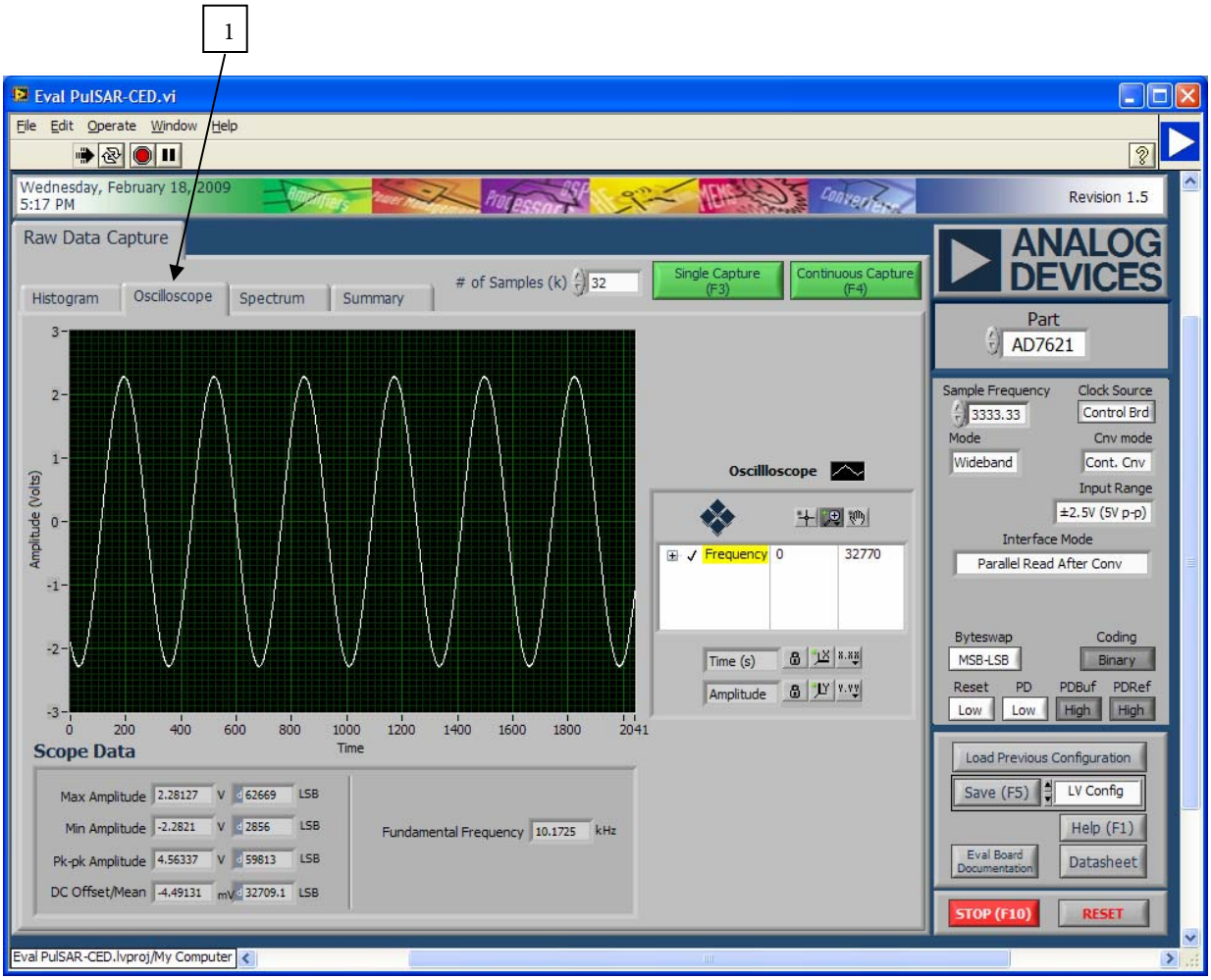



*Figure 7. Oscilloscope*

**1**. Time domain data can be viewed with the oscilloscope also.

## EVALUATION BOARD SCHEMATICS AND ARTWORK

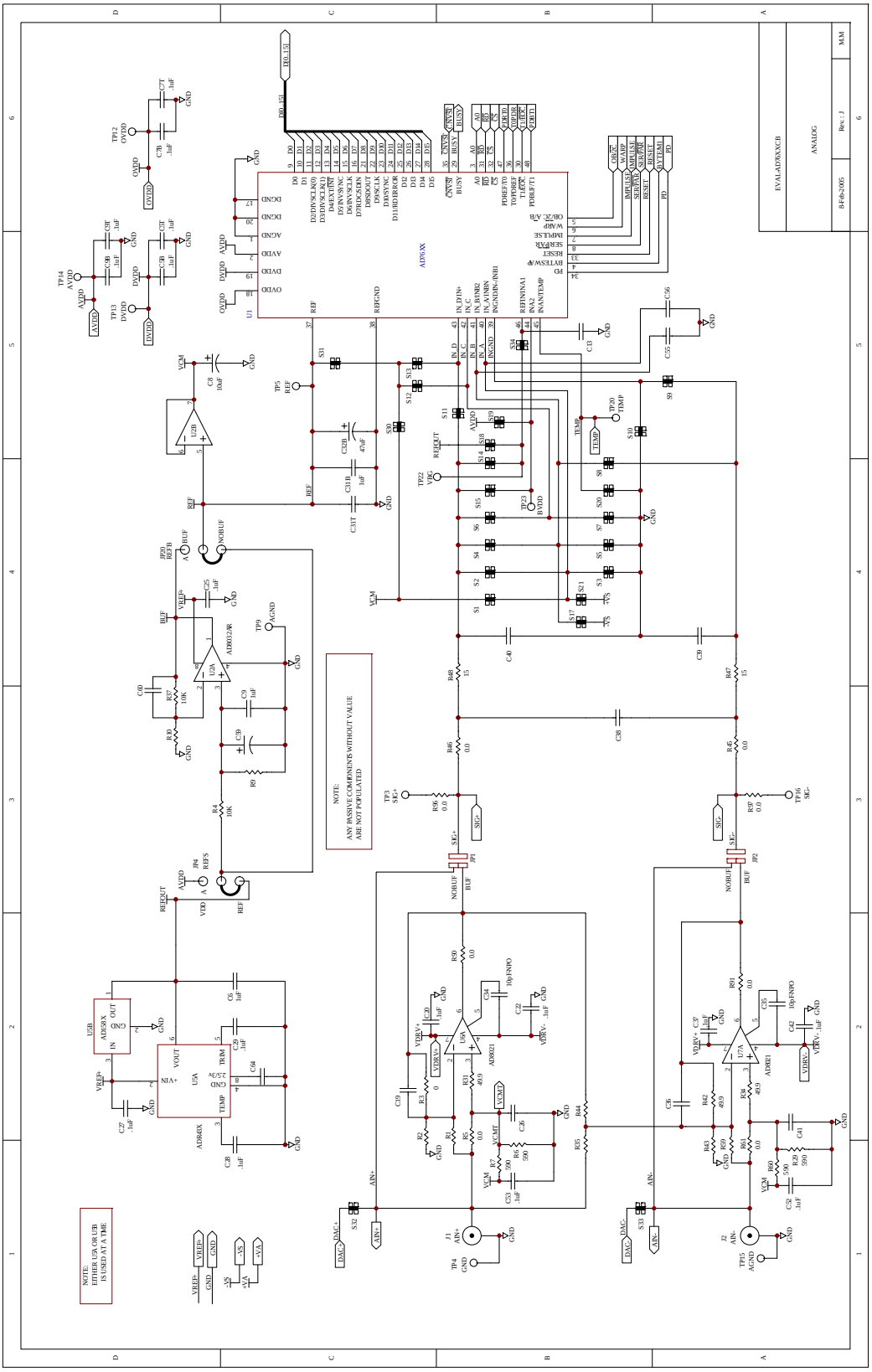


*Figure 8. Schematic, Analog*

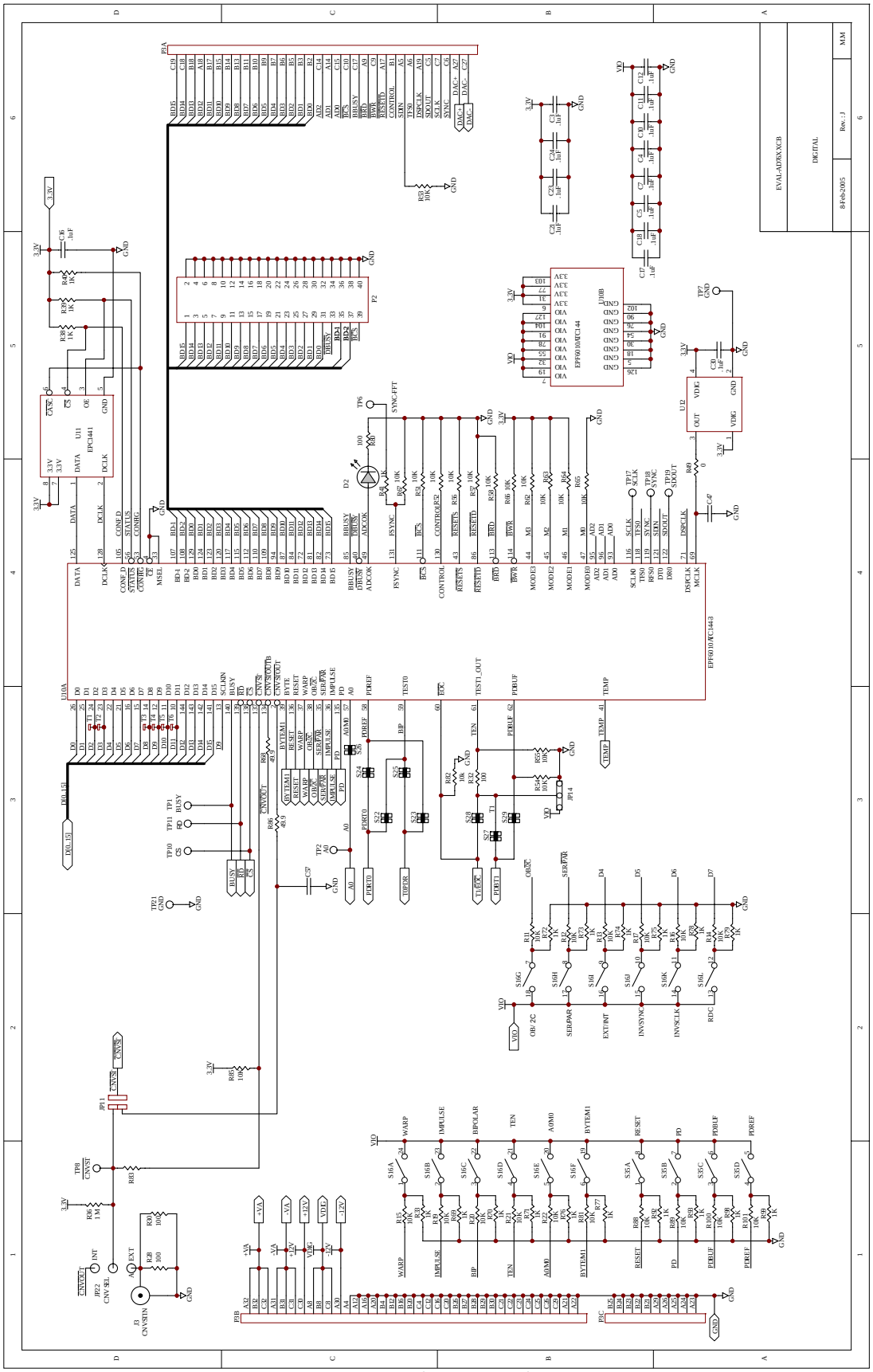


*Figure 9. Schematic, Digital*

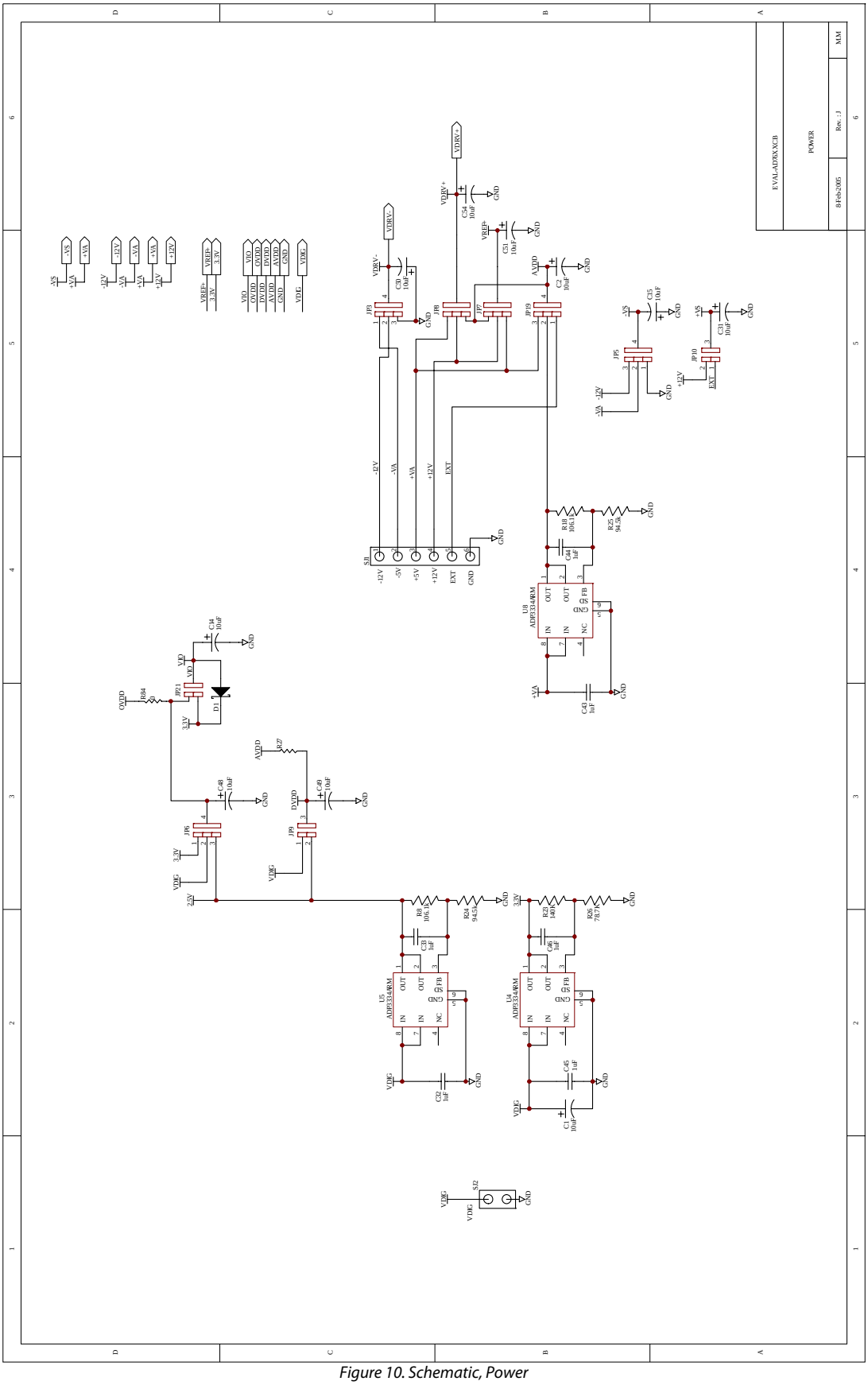



*Figure 10. Schematic, Power*

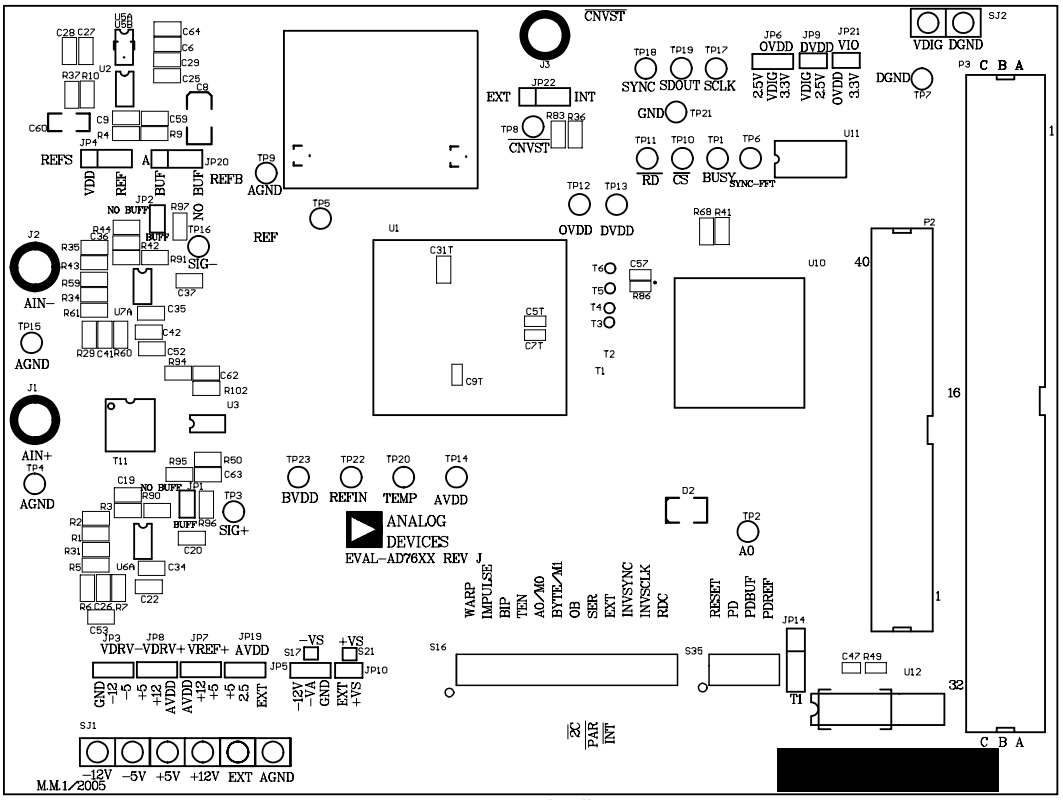



*Figure 11. Top Side Silk-Screen*

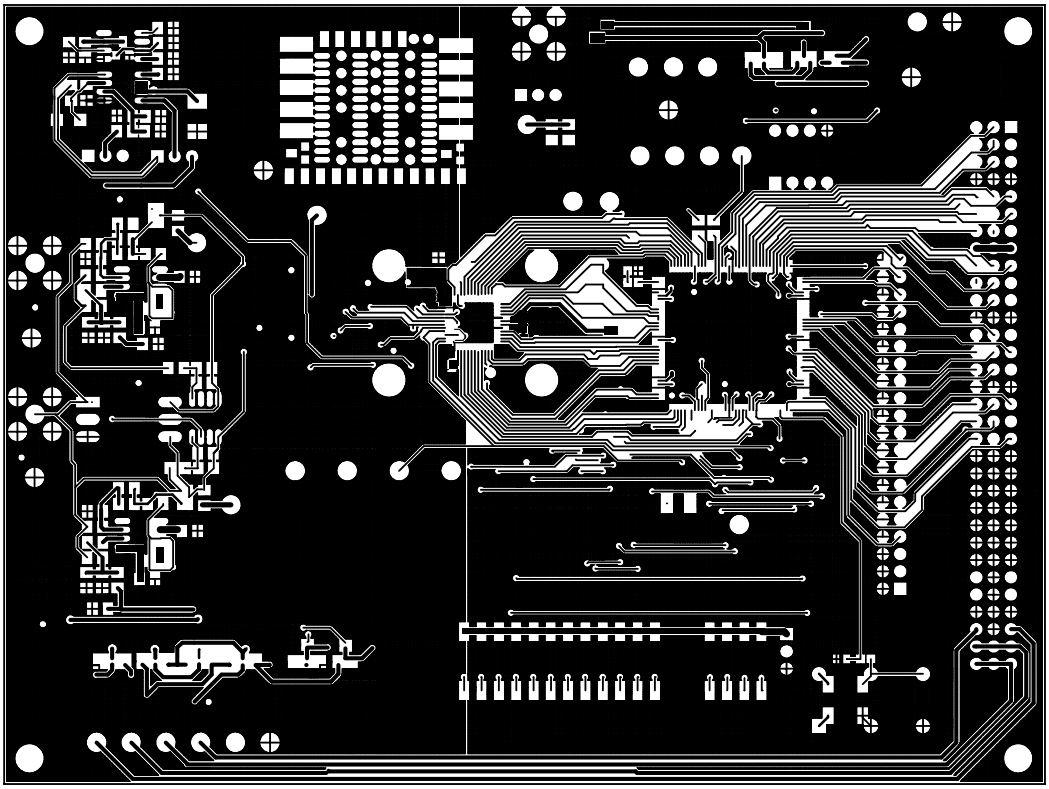


*Figure 12. Top Layer*

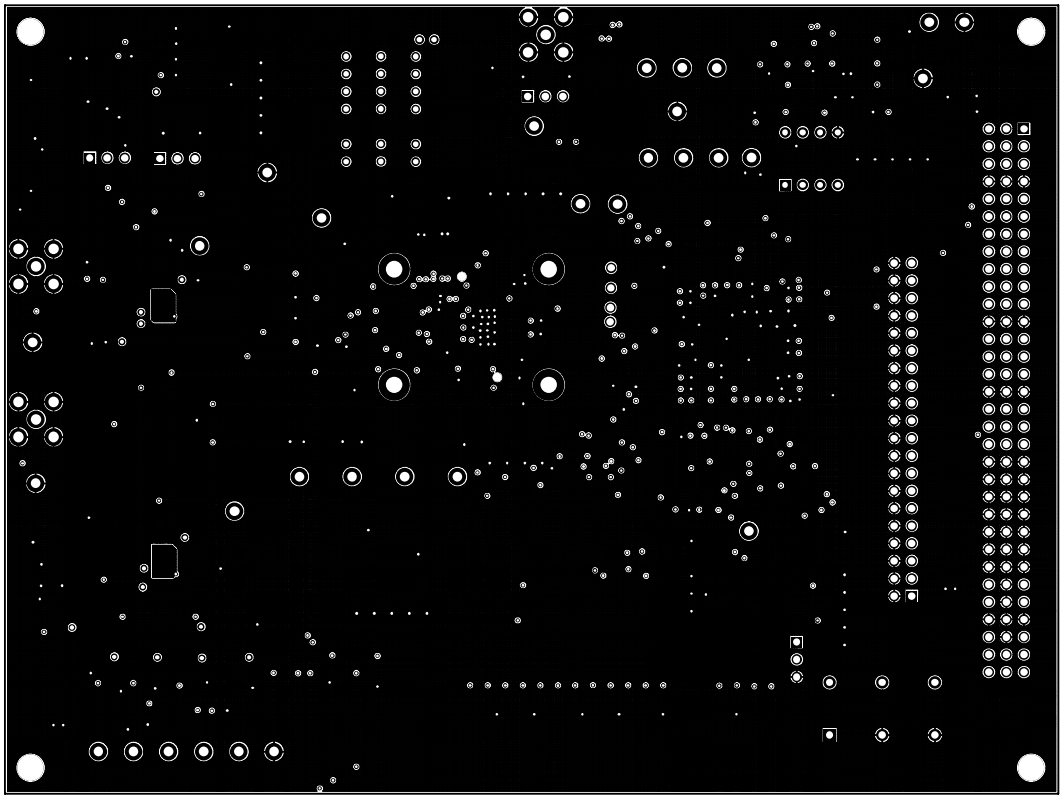


*Figure 13. Ground Layer*

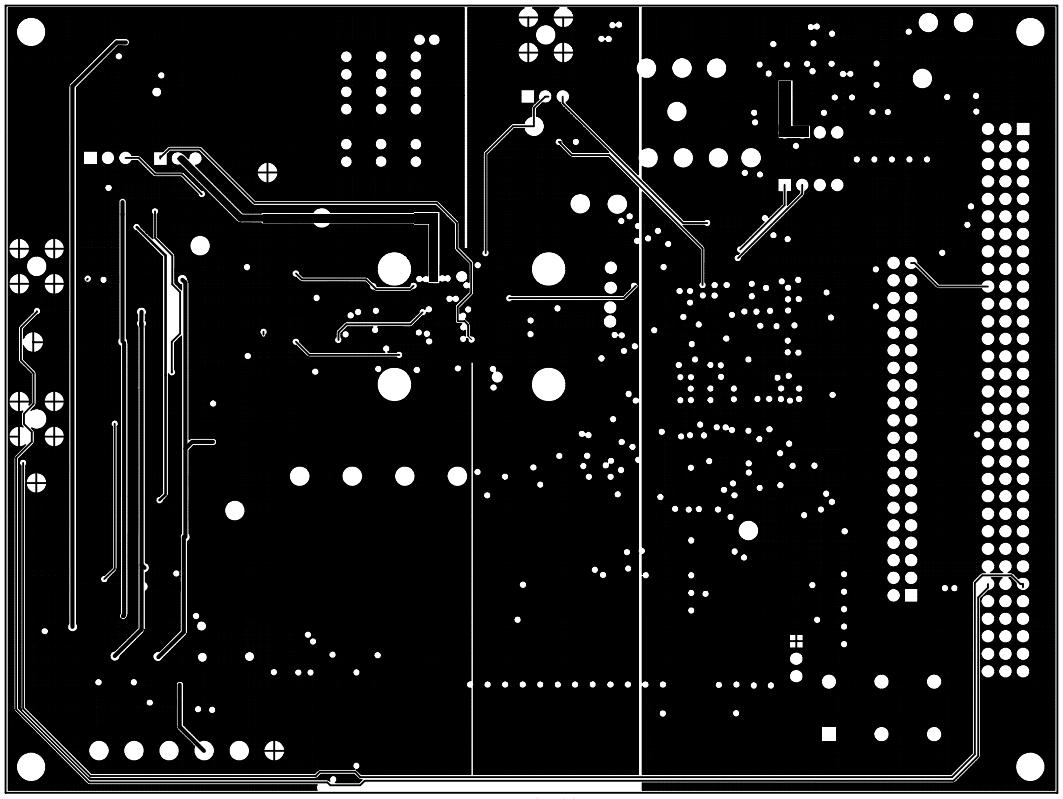


*Figure 14. Shield Layer*

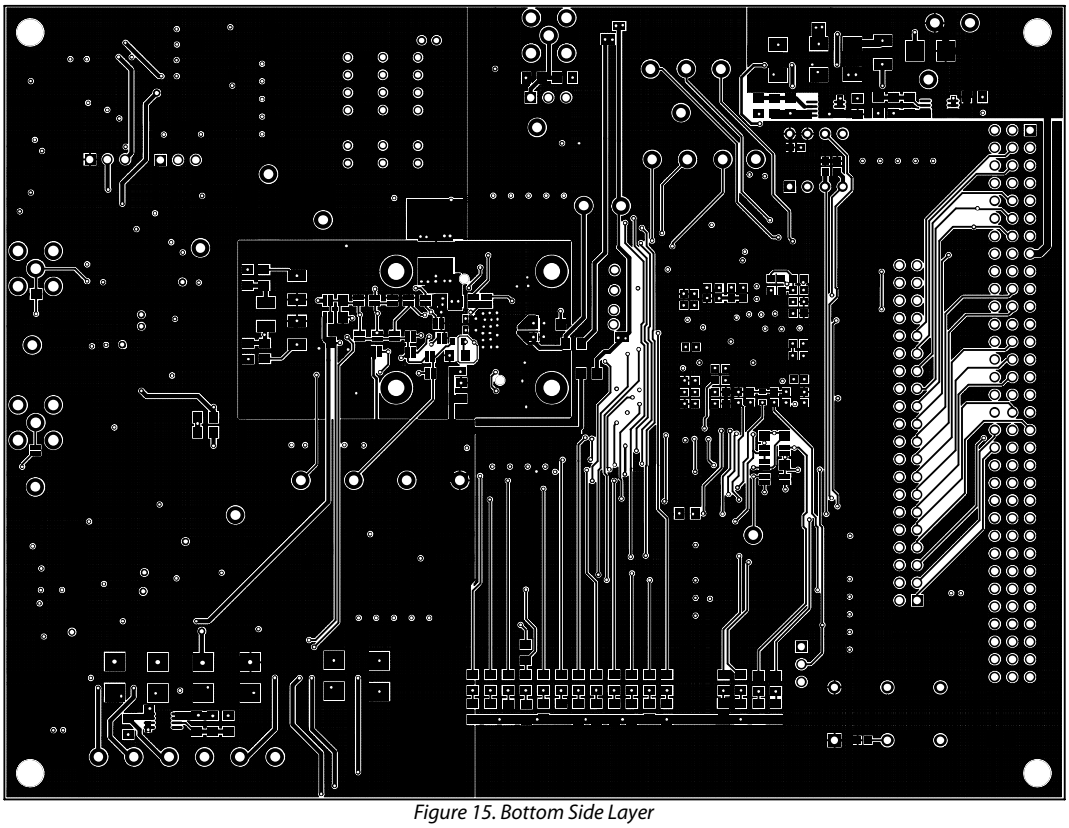


*Figure 15. Bottom Side Layer*

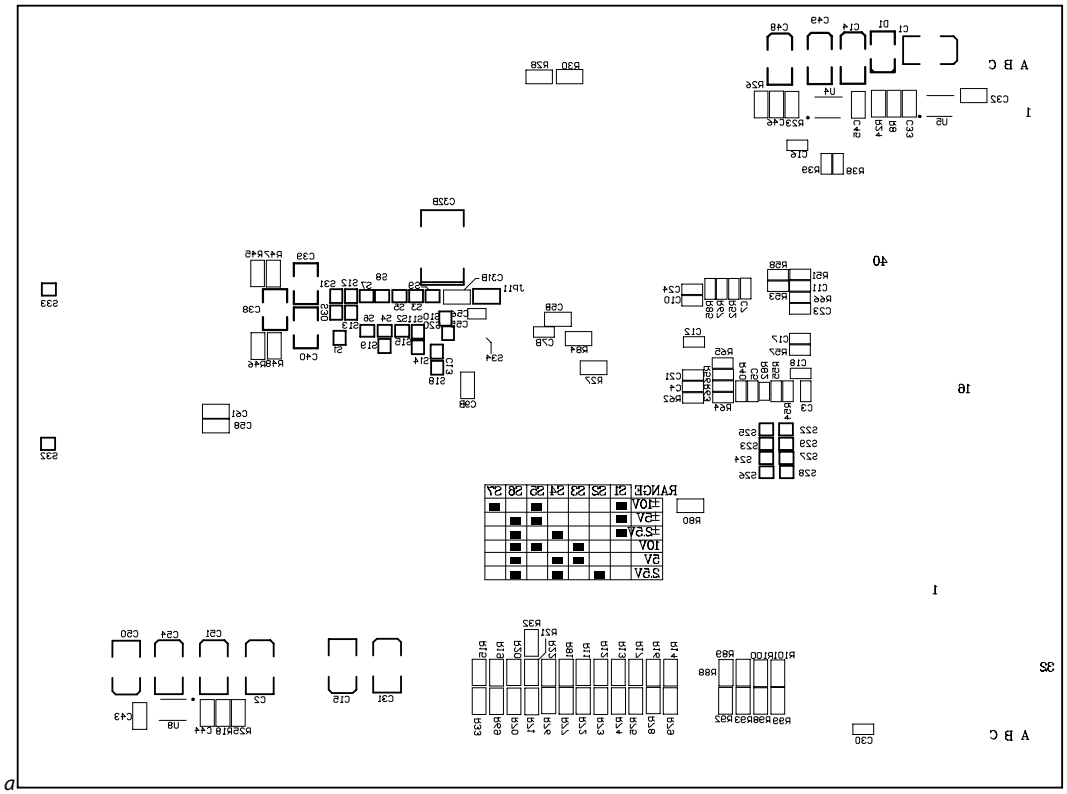


*Figure 16. Bottom Side Silk-Screen*

**Table 6. Bill of Materials for the Connectors**

| Ref Des | Connector Type | Manf. | Part No. |
|---|---|---|---|
| J1 – J3 | RT Angle SMB Male | Pasternack | PE4177 |
| P2 | 0.100 X 0.100 straight IDC header 2X20 | 3M | 2540-6002UB |
| P3 | 32X3 RT PC MOUNT CONNECTOR | ERNI | 533402 |

## ORDERING GUIDE

These evaluation boards are compatible with both EVAL-CED1Z and EVAL-CONTROL BRDxZ. For simplicity, this document was made especially for EVAL-CED1Z usage. Refer to Analog Devices PulSAR Evaluation Kit product page for the user's guide specific to EVAL-CONTROL BRDxZ usage.

| Evaluation Board Model | Product |
|---|---|
| EVAL-AD7621CBZ | AD7621ASTZ/ACPZ |
| EVAL-AD7622CBZ | AD7622BSTZ/BCPZ |
| EVAL-AD7623CBZ | AD7623ASTZ/ACPZ |
| EVAL-AD7641CBZ | AD7641BSTZ/BCPZ |
| EVAL-AD7643CBZ | AD7643BSTZ/BCPZ |
| EVAL-AD7650CBZ | AD7650ASTZ/ACPZ |
| EVAL-AD7651CBZ | AD7651ASTZ/ACPZ |
| EVAL-AD7652CBZ | AD7652ASTZ/ACPZ |
| EVAL-AD7653CBZ | AD7653ASTZ/ACPZ |
| EVAL-AD7660CBZ | AD7660ASTZ/ACPZ |
| EVAL-AD7661CBZ | AD7661ASTZ/ACPZ |
| EVAL-AD7663CBZ | AD7663ASTZ/ACPZ |
| EVAL-AD7664CBZ | AD7664ASTZ/ACPZ |
| EVAL-AD7665CBZ | AD7665ASTZ/ACPZ |
| EVAL-AD7666CBZ | AD7666ASTZ/ACPZ |
| EVAL-AD7667CBZ | AD7667ASTZ/ACPZ |
| EVAL-AD7671CBZ | AD7671ASTZ/ACPZ |
| EVAL-AD7674CBZ | AD7674ASTZ/ACPZ |
| EVAL-AD7675CBZ | AD7675ASTZ/ACPZ |
| EVAL-AD7676CBZ | AD7676ASTZ/ACPZ |
| EVAL-AD7677CBZ | AD7677ASTZ/ACPZ |
| EVAL-AD7678CBZ | AD7678ASTZ/ACPZ |
| EVAL-AD7679CBZ | AD7679ASTZ/ACPZ |
| EVAL-CED1Z | USB Capture Board |

## NOTES

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