

# Power system basis chip with high speed CAN and LIN transceivers

The 33907/33908 SMARTMOS devices are multi-output, power supply, integrated circuit, including HSCAN and/or LIN transceivers, dedicated to the automotive market.

Multiple switching and linear voltage regulators, including low-power mode (32  $\mu$ A) are available with various wake-up capabilities. An advanced power management scheme is implemented to maintain high efficiency over wide input voltages (down to 2.7 V) and wide output current ranges (up to 1.5 A).

The 33907/33908 include enhanced safety features, with multiple fail-safe outputs, becoming a full part of a safety oriented system partitioning, to reach a high integrity safety level (up to ASIL D).

The built-in enhanced high-speed CAN interface fulfills the ISO11898-2 and -5 standards. The LIN interface fulfills LIN protocol specifications 1.3, 2.0, 2.1, 2.2, and SAEJ2602-2

## Features

- Battery voltage sensing & MUX output pin
- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- Switching mode power supply (SMPS) dedicated to MCU core supply, from 1.2 V to 3.3 V delivering up to 1.5 A
- Multiple wake-up sources in low-power mode: CAN, LIN, and/or IOs
- Six configurable I/Os
- Linear voltage regulator dedicated to auxiliary functions, or to a sensor supply ( $V_{CCA}$  tracker or independent), 5.0 V or 3.3 V
- Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply ( $V_{CCA}$ ), 5.0 V or 3.3 V

**33907**  
**33908**

## POWER SYSTEM BASIS CHIP



**AE SUFFIX (PB-FREE)**  
**98ASA00173D**  
**48-PIN LQFP-EP**

## Applications

- Electrical power steering
- Engine management
- Battery management
- Active suspension
- Gear box
- Transmission
- Electrical vehicle (EV), hybrid electrical vehicle (HEV), and inverter
- Advanced driver assistance systems

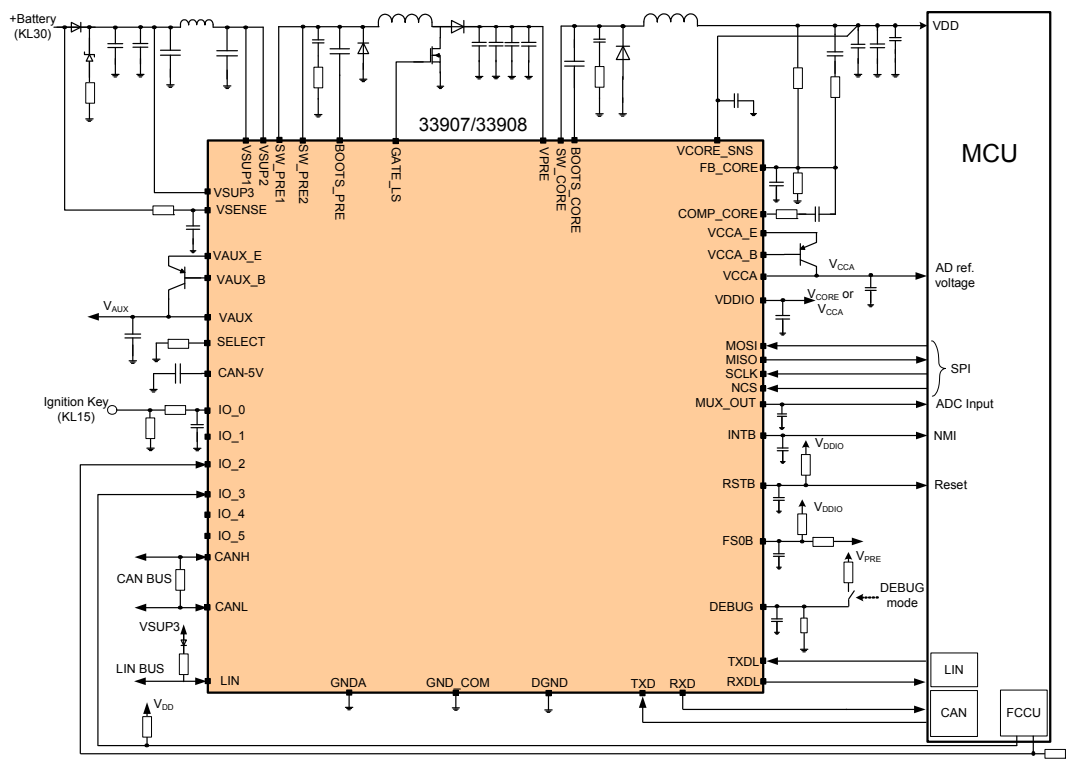
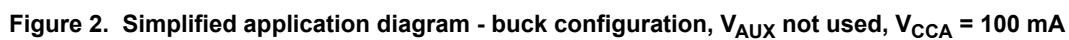


Figure 1. 33907/33908 simplified application diagram - buck boost configuration

\* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.



# 1 Orderable parts

Table 1. Orderable part variations

| Part number | Temperature (T <sub>A</sub> ) | Package                 | CAN | LIN | V <sub>CORE</sub> | Notes |
|-------------|-------------------------------|-------------------------|-----|-----|-------------------|-------|
| MC33907NAE  | -40 to 125 °C                 | 48-pin LQFP exposed pad | 1   | 0   | 0.8 A             | (1)   |
| MC33908NAE  |                               |                         |     | 0   | 1.5 A             |       |
| MC33907LAE  |                               |                         |     | 1   | 0.8 A             |       |
| MC33908LAE  |                               |                         |     | 1   | 1.5 A             |       |

Notes

1. To order parts in Tape & Reel, add the R2 suffix to the part number.

## 2 Internal Block Diagram

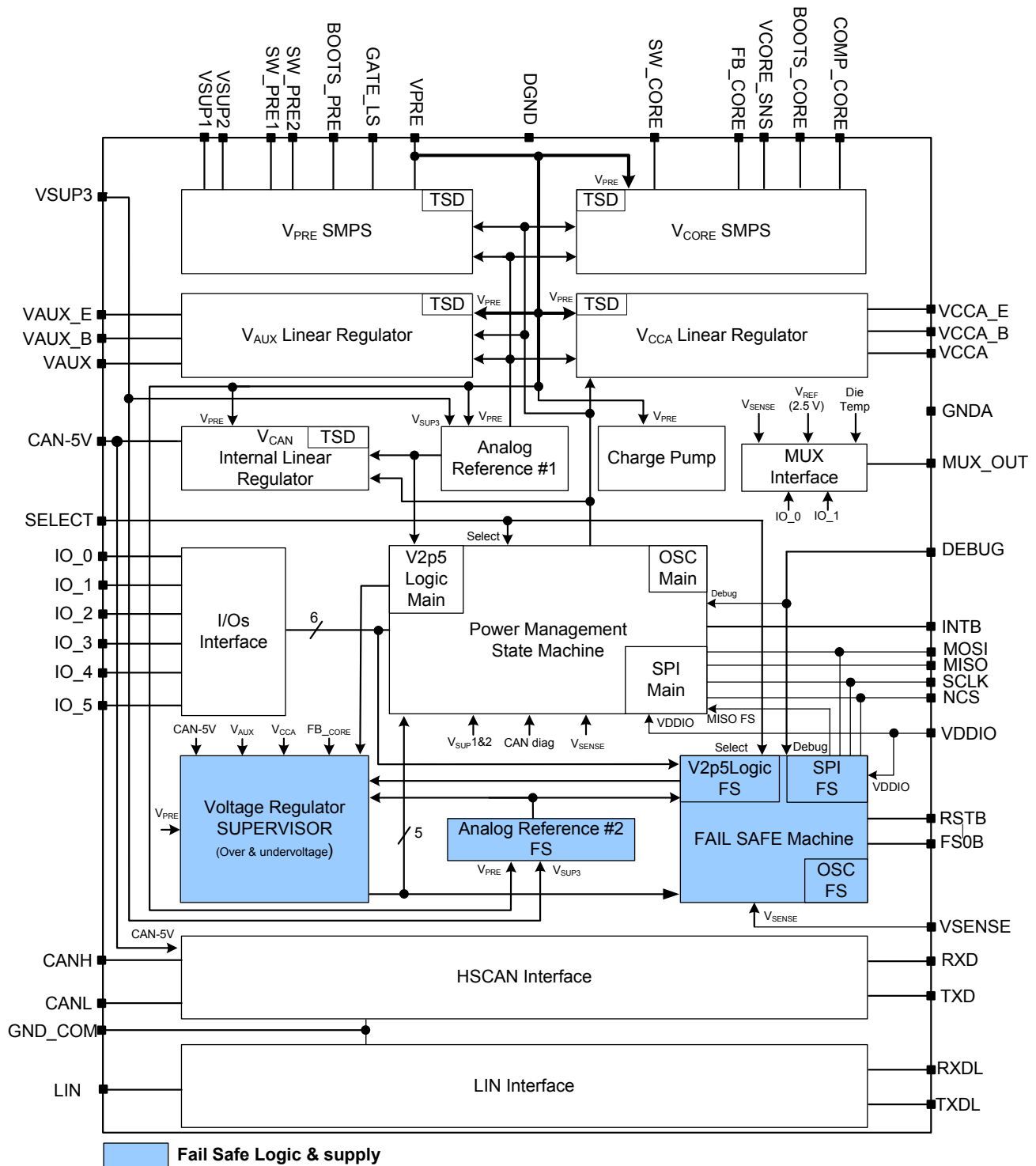


Figure 3. 33907L/33908L with CAN and LIN simplified internal block diagram

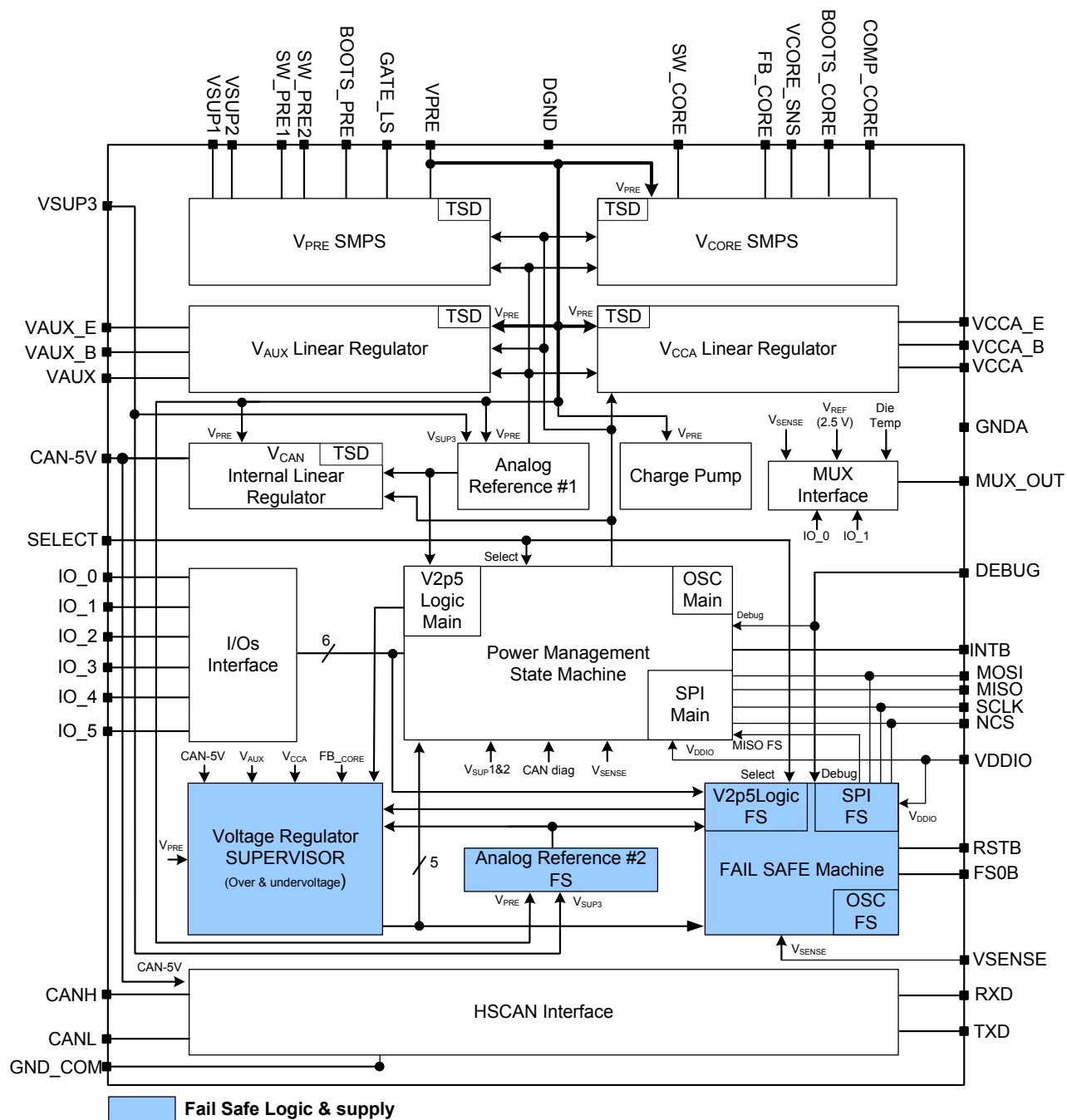


Figure 4. 33907N/33908N with CAN only simplified internal block diagram

## 3 Pin connections

### 3.1 Pinout diagram for 33907/33908

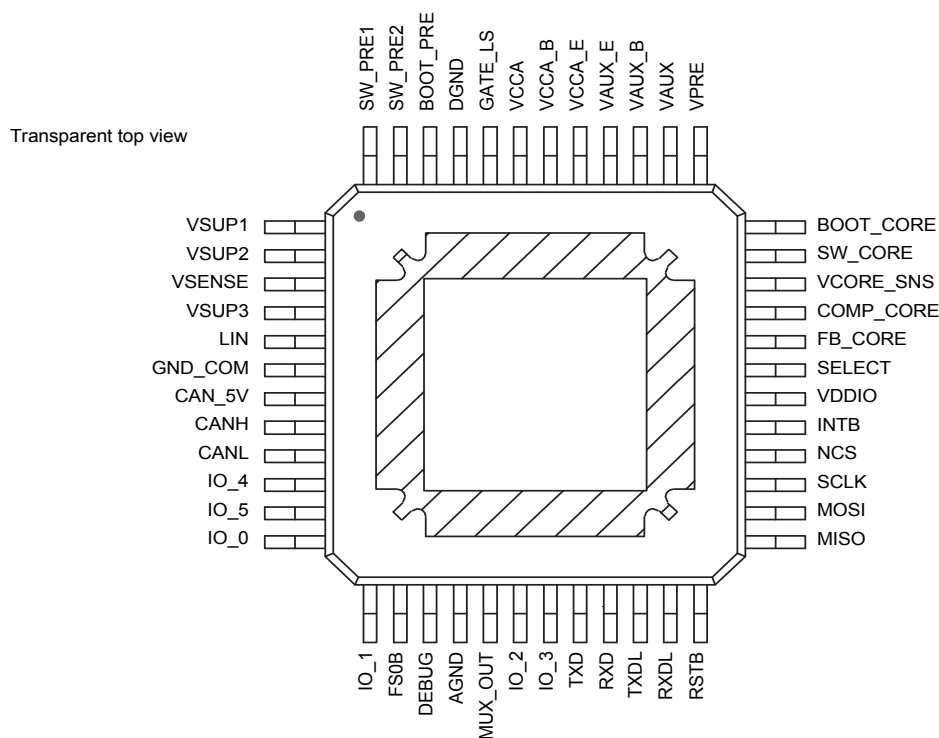


Figure 5. 33907L/33908L pinout with CAN and LIN

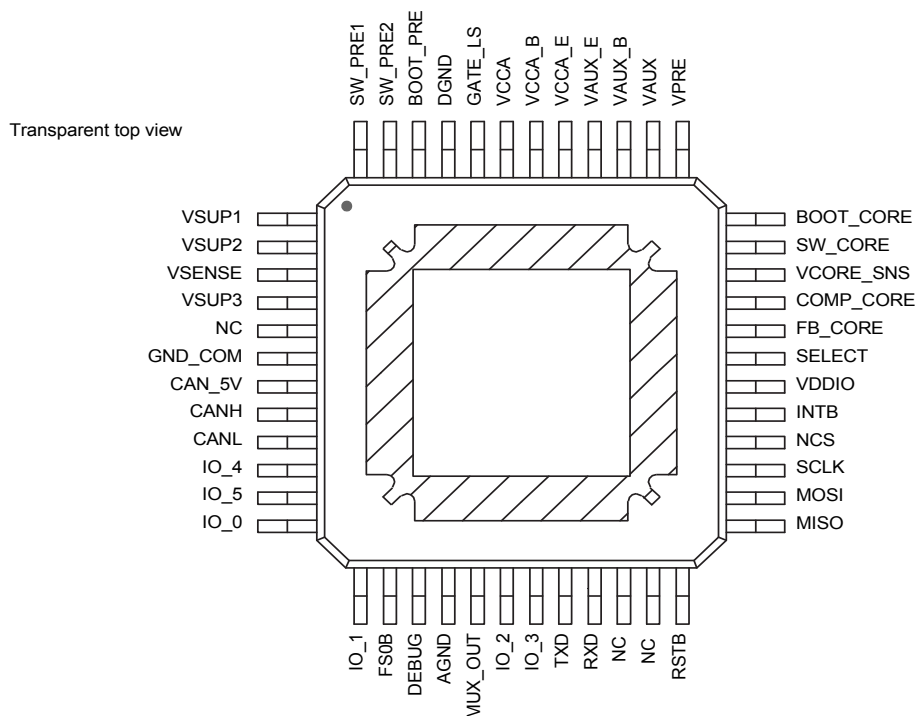


Figure 6. 33907N/33908N pinout with CAN only

## 3.2 Pin definitions

A functional description of each pin can be found in the functional pin description section beginning on [page 26](#).

**Table 2. 33907/33908 pin definition**

| 33907L/<br>33908L<br>pin number | 33907N/<br>33908N<br>pin number | Pin name | Type          | Definition  |
|---------------------------------|---------------------------------|----------|---------------|---|
| 1                               | 1                               | VSUP1    | A_IN          | Power supply of the device. An external reverse battery protection diode in series is mandatory   |
| 2                               | 2                               | VSUP2    | A_IN          | Second power supply. Protected by the external reverse battery protection diode used for VSUP1. VSUP1 and VSUP2 must be connected together externally.  |
| 3                               | 3                               | VSENSE   | A_IN          | Sensing of the battery voltage. Must be connected prior to the reverse battery protection diode.  |
| 4                               | 4                               | VSUP3    | A_IN          | Third power supply dedicated to the device supply. Protected by the external reverse battery protection diode used for VSUP1. Must be connected between the reverse protection diode and the input PI filter.   |
| 5                               | NC                              | LIN      | A_IN/OUT      | LIN single-wire bus transmitter and receiver. NC: pin must be left open for 33907N/33908N version   |
| 6                               | 6                               | GND_COM  | GND           | Dedicated ground for CAN  |
| 7                               | 7                               | CAN_5V   | A_OUT         | Output voltage for the embedded CAN interface   |
| 8                               | 8                               | CANH     | A_IN/OUT      | HSCAN output High   |
| 9                               | 9                               | CANL     | A_IN/OUT      | HSCAN output Low  |
| 10<br>11                        | 10<br>11                        | IO_4:5   | D_IN<br>A_OUT | Can be used as digital input (load dump proof) with wake-up capability or as an output gate driver<br><b>Digital input:</b> Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes.<br><b>Wake-up capability:</b> Can be selectable to wake-up on a rising or falling edge, or on a transition<br><b>Output gate driver:</b> Can drive a logic level low-side NMOS transistor. Controlled by the SPI.   |
| 12<br>13                        | 12<br>13                        | IO_0:1   | A_IN<br>D_IN  | Can be used as analog or digital input (load dump proof) with wake-up capability (selectable)<br><b>Analog input:</b> Pin status can be read through the MUX output pin<br><b>Digital input:</b> Pin status can be read through the SPI. Can be used to monitor error signals from another IC for safety purposes<br><b>Wake-up capability:</b> Can be selectable to wake-up on a rising or falling edge, or on a transition<br><b>Rk:</b> For safety purposes, IO_1 can also be used to monitor the middle point of a redundant resistor bridge connected on Vcore (in parallel to the one used to set the Vcore voltage). |
| 14                              | 14                              | FS0B     | D_OUT         | Output of the safety block (active low). The pin is asserted low at start-up and when a fault condition is detected. Open drain structure.  |
| 15                              | 15                              | DEBUG    | D_IN          | Debug mode entry input  |
| 16                              | 16                              | AGND     | GROUND        | Analog ground connection  |
| 17                              | 17                              | MUX_OUT  | A_OUT         | Multiplexed output to be connected to an MCU ADC input. Selection of the analog parameter is available at MUX-OUT through the SPI.  |
| 18<br>19                        | 18<br>19                        | IO_2:3   | D_IN          | Digital input pin with wake-up capability (logic level compatible)<br><b>Digital INPUT:</b> Pin status can be read through the SPI. Can be used to monitor error signals from MCU for safety purposes.<br><b>Wake-up capability:</b> Can be selectable to wake-up on a rising or falling edge, or on a transition.  |
| 20                              | 20                              | TXD      | D_IN          | Transceiver input from the MCU which controls the state of the HSCAN bus. Internal pull-up to VDDIO. Internal pull-up to VDDIO.   |
| 21                              | 21                              | RXD      | D_OUT         | Receiver output which reports the state of the HSCAN bus to the MCU   |
| 22                              | NC                              | TXDL     | D_IN          | Transceiver input from the MCU which controls the state of the LIN bus. Internal pull-up to VDDIO. NC: pin must be left open for 33907N/33908N version  |

**Table 2. 33907/33908 pin definition (continued)**

| 33907L/<br>33908L<br>pin number | 33907N/<br>33908N<br>pin number | Pin name  | Type     | Definition   |
|---------------------------------|---------------------------------|-----------|----------|--|
| 23                              | NC                              | RXDL      | D_OUT    | Receiver output which reports the state of the LIN bus to the MCU. NC: pin must be left open for 33907N/33908N version   |
| 24                              | 24                              | RSTB      | D_OUT    | This output is asserted low when the safety block reports a failure. The main function is to reset the MCU. Reset input voltage is also monitored in order to detect external reset and fault condition. Open drain structure. |
| 25                              | 25                              | MISO      | D_OUT    | SPI bus. Master Input Slave Output   |
| 26                              | 26                              | MOSI      | D_IN     | SPI bus. Master Output Slave Input   |
| 27                              | 27                              | SCLK      | D_IN     | SPI Bus. Serial clock  |
| 28                              | 28                              | NCS       | D_IN     | No Chip Select (Active low)  |
| 29                              | 29                              | INTB      | D_OUT    | This output pin generates a low pulse when an Interrupt condition occurs. Pulse duration is configurable. Internal pull-up to VDDIO.   |
| 30                              | 30                              | VDDIO     | A_IN     | Input voltage for MISO output buffer. Allows voltage compatibility with MCU I/Os.  |
| 31                              | 31                              | SELECT    | D_IN     | Hardware selection pin for VAUX and VCCA output voltages   |
| 32                              | 32                              | FB_CORE   | A_IN     | VCORE voltage feedback. Input of the error amplifier.  |
| 33                              | 33                              | COMP_CORE | A_IN     | Compensation network. Output of the error amplifier.   |
| 34                              | 34                              | VCORE_SNS | A_IN     | VCORE output voltage sense   |
| 35                              | 35                              | SW_CORE   | A_IN     | VCORE switching point  |
| 36                              | 36                              | BOOT_CORE | A_IN/OUT | Bootstrap capacitor for VCORE internal NMOS gate drive   |
| 37                              | 37                              | VPRE      | A_OUT    | VPRE output voltage  |
| 38                              | 38                              | VAUX      | A_OUT    | VAUX output voltage. External PNP ballast transistor. Collector connection   |
| 39                              | 39                              | VAUX_B    | A_OUT    | VAUX voltage regulator. External PNP ballast transistor. Base connection   |
| 40                              | 40                              | VAUX_E    | A_OUT    | VAUX voltage regulator. External PNP ballast transistor. Emitter connection  |
| 41                              | 41                              | VCCA_E    | A_OUT    | VCCA voltage regulator. External PNP ballast transistor. Emitter connection  |
| 42                              | 42                              | VCCA_B    | A_OUT    | VCCA voltage regulator. External PNP ballast transistor. Base connection   |
| 43                              | 43                              | VCCA      | A_OUT    | VCCA output voltage. External PNP ballast transistor. Collector connection   |
| 44                              | 44                              | GATE_LS   | A_OUT    | Low-side MOSFET gate drive for “Non-inverting Buck-boost” configuration  |
| 45                              | 45                              | DGND      | GROUND   | Digital ground connection  |
| 46                              | 46                              | BOOT_PRE  | A_IN/OUT | Bootstrap capacitor for the VPRE internal NMOS gate drive  |
| 47                              | 47                              | SW_PRE2   | A_IN     | Second pre-regulator switching point   |
| 48                              | 48                              | SW_PRE1   | A_IN     | First pre-regulator switching point  |



## 4 General product characteristics

### 4.1 Maximum ratings

**Table 3. Maximum ratings**

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol                     | Ratings  | Value                          | Unit | Notes |
|----------------------------|--|--------------------------------|------|-------|
| <b>Electrical ratings</b>  |  |                                |      |       |
| V <sub>SUP1/2/3</sub>      | DC Voltage at Power Supply Pins  | -1.0 to 40                     | V    | (2)   |
| V <sub>SENSE</sub>         | DC Voltage at Battery Sense Pin  | -14 to 40                      | V    |       |
| V <sub>SW1,2</sub>         | DC Voltage at SW_PRE1 and SW_PRE2 Pins   | -1.0 to 40                     | V    |       |
| V <sub>PRE</sub>           | DC Voltage at VPRE Pin   | -0.3 to 8                      | V    |       |
| V <sub>GATE_LS</sub>       | DC Voltage at Gate_LS pin  | -0.3 to 8                      | V    |       |
| V <sub>BOOT_PRE</sub>      | DC Voltage at BOOT_PRE pin   | -1.0 to 50                     | V    |       |
| V <sub>SW_CORE</sub>       | DC Voltage at SW_CORE pin  | -1.0 to 8.0                    | V    |       |
| V <sub>CORE_SNS</sub>      | DC Voltage at V <sub>CORE_SNS</sub> pin  | 0.0 to 8.0                     | V    |       |
| V <sub>BOOT_CORE</sub>     | DC Voltage at BOOT_CORE pin  | 0.0 to 15                      | V    |       |
| V <sub>FB_CORE</sub>       | DC Voltage at FB_CORE pin  | -0.3 to 2.5                    | V    |       |
| V <sub>COMP_CORE</sub>     | DC Voltage at COMP_CORE pin  | -0.3 to 2.5                    | V    |       |
| V <sub>AUX_E,B</sub>       | DC Voltage at VAUX_E, VAUX_B pin   | -0.3 to 40                     | V    |       |
| V <sub>AUX</sub>           | DC Voltage at VAUX pin   | -2.0 to 40                     | V    |       |
| V <sub>CCA_B,E</sub>       | DC Voltage at VCCA_B, VCCA_E pin   | -0.3 to 8.0                    | V    |       |
| V <sub>CCA</sub>           | DC Voltage at VCCA pin   | -0.3 to 8.0                    | V    |       |
| V <sub>DDIO</sub>          | DC Voltage at VDDIO  | -0.3 to 8.0                    | V    |       |
| V <sub>FS0</sub>           | DC Voltage at FS0B (with ext R mandatory)  | -0.3 to 40                     | V    |       |
| V <sub>DEBUG</sub>         | DC Voltage at DEBUG  | -0.3 to 40                     | V    |       |
| V <sub>IO_0,1,4,5</sub>    | DC Voltage at IO_0:1; 4:5 (with ext R = 5.1 kΩ in series mandatory)                        | -0.3 to 40                     | V    |       |
| V <sub>DIG</sub>           | DC Voltage at INTB, RSTB, MISO, MOSI, NCS, SCLK, MUX_OUT, RXD, TXD, RXDL, TXDL, IO_2, IO_3 | -0.3 to V <sub>DDIO</sub> +0.3 | V    |       |
| V <sub>SELECT</sub>        | DC Voltage at SELECT   | -0.3 to 8.0                    | V    |       |
| V <sub>BUS_CAN</sub>       | DC Voltage on CANL, CANH   | -27 to 40                      | V    |       |
| V <sub>BUS_LIN</sub>       | DC Voltage on LIN  | -18 to 40V                     | V    |       |
| V <sub>CAN_5V</sub>        | DC Voltage on CAN_5 V  | -0.3 to 8.0                    | V    |       |
| I <sub>IO_0, 1, 4, 5</sub> | IOs Maximum Current Capability(IO_0, IO_1, IO_4, IO_5)                                     | -5.0 to 5.0                    | mA   |       |

**Notes**

- All Vsups (V<sub>SUP1/2/3</sub>) shall be connected to the same supply ([Figure 58](#))

**Table 3. Maximum ratings (continued)**

All voltages are with respect to ground, unless otherwise specified. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol                 | Ratings  | Value | Unit | Notes |
|------------------------|--|-------|------|-------|
|                        | ESD Voltage  |       |      |       |
|                        | Human Body Model (JESD22/A114) - 100 pF, 1.5 k $\Omega$                        |       |      |       |
| V <sub>ESD-HBM1</sub>  | • All pins   | ±2.0  | kV   |       |
| V <sub>ESD-HBM2</sub>  | • VSUP1, VSUP2, VSUP3, VSENSE, VAUX, IO_0:1, IO_4:5, FS0B, DEBUG               | ±4.0  | kV   |       |
| V <sub>ESD-HBM3</sub>  | • CANH, CANL   | ±6.0  | kV   |       |
| V <sub>ESD-HBM4</sub>  | • LIN  | ±8.0  | kV   |       |
|                        | Charge Device Model (JESD22/C101):   |       |      |       |
| V <sub>ESD-CDM1</sub>  | • All Pins   | ±500  | V    |       |
| V <sub>ESD-CDM2</sub>  | • Corner Pins  | ±750  | V    |       |
|                        | System level ESD (Gun Test)  |       |      |       |
|                        | • VSUP1, VSUP2, VSUP3, VSENSE, VAUX, IO_0:1, IO_4:5, FS0B                      |       |      |       |
| V <sub>ESD-GUN1</sub>  | 330 $\Omega$ / 150 pF Unpowered According to IEC61000-4-2:                     | ±8.0  | kV   |       |
| V <sub>ESD-GUN2</sub>  | 330 $\Omega$ / 150 pF Unpowered According to OEM LIN, CAN, FLEXray Conformance | ±8.0  | kV   | (3)   |
| V <sub>ESD-GUN3</sub>  | 2.0 k $\Omega$ / 150 pF Unpowered According to ISO10605.2008                   | ±8.0  | kV   |       |
| V <sub>ESD-GUN4</sub>  | 2.0 k $\Omega$ / 330 pF Powered According to ISO10605.2008                     | ±8.0  | kV   |       |
|                        | • CANH, CANL   |       |      |       |
| V <sub>ESD-GUN5</sub>  | 330 $\Omega$ / 150 pF Unpowered According to IEC61000-4-2:                     | ±15.0 | kV   |       |
| V <sub>ESD-GUN6</sub>  | 330 $\Omega$ / 150 pF Unpowered According to OEM LIN, CAN, FLEXray Conformance | ±12.0 | kV   |       |
| V <sub>ESD-GUN7</sub>  | 2.0 k $\Omega$ / 150 pF Unpowered According to ISO10605.2008                   | ±15.0 | kV   |       |
| V <sub>ESD-GUN8</sub>  | 2.0 k $\Omega$ / 330 pF Powered According to ISO10605.2008                     | ±15.0 | kV   |       |
|                        | • LIN  |       |      |       |
| V <sub>ESD-GUN9</sub>  | 330 $\Omega$ / 150 pF Unpowered According to IEC61000-4-2:                     | ±15.0 | kV   |       |
| V <sub>ESD-GUN10</sub> | 330 $\Omega$ / 150 pF Unpowered According to OEM LIN, CAN, FLEXray Conformance | ±15.0 | kV   |       |
| V <sub>ESD-GUN11</sub> | 2.0 k $\Omega$ / 150 pF Unpowered According to ISO10605.2008                   | ±12.0 | kV   |       |
| V <sub>ESD-GUN12</sub> | 2.0 k $\Omega$ / 330 pF Powered According to ISO10605.2008                     | ±15.0 | kV   |       |

**Thermal ratings**

|                  |                      |            |    |  |
|------------------|----------------------|------------|----|--|
| T <sub>A</sub>   | Ambient Temperature  | -40 to 125 | °C |  |
| T <sub>J</sub>   | Junction Temperature | -40 to 150 | °C |  |
| T <sub>STG</sub> | Storage Temperature  | -55 to 150 | °C |  |

**Thermal resistance**

|                        |  |      |      |     |
|------------------------|--|------|------|-----|
| R <sub>θJA</sub>       | Thermal Resistance Junction to Ambient     | 30   | °C/W | (4) |
| R <sub>θJCTOP</sub>    | Thermal Resistance Junction to Case Top    | 24.2 | °C/W | (5) |
| R <sub>θJCBOTTOM</sub> | Thermal Resistance Junction to Case Bottom | 0.9  | °C/W | (6) |

**Notes**

3. Compared to AGND.
4. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC - 883 Method 1012.1).
6. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.

## 4.2 Static electrical characteristics

**Table 4. Operating range**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered ([Figure 25](#)).

| Symbol              | Parameter   | Min. | Typ. | Max. | Unit          | Notes |
|---------------------|---|------|------|------|---------------|-------|
| <b>Power supply</b> |   |      |      |      |               |       |
| $I_{SUP123}$        | Power Supply Current in Normal Mode ( $V_{SUP} > V_{SUP\_UV\_7}$ )                              | 2.0  | —    | 13.0 | mA            |       |
| $I_{SUP3}$          | Power Supply Current for VSUP3 in Normal Mode ( $V_{SUP} > V_{SUP\_UV\_7}$ )                    | —    | 3.5  | 5.0  | mA            |       |
| $I_{SUP\_LPOFF1}$   | Power Supply Current in LPOFF ( $V_{SUP} = 14\text{ V}$ at $T_A = 25\text{ }^{\circ}\text{C}$ ) | —    | 32   | —    | $\mu\text{A}$ |       |
| $I_{SUP\_LPOFF2}$   | Power Supply Current in LPOFF ( $V_{SUP} = 18\text{ V}$ at $T_A = 80\text{ }^{\circ}\text{C}$ ) | —    | 42   | 60   | $\mu\text{A}$ |       |
| $V_{SNS\_UV}$       | Power Supply Undervoltage Warning   | —    | 8.5  | —    | V             |       |
| $V_{SNS\_UV\_HYST}$ | Power Supply Undervoltage Warning Hysteresis  | 0.1  | —    | —    | V             |       |
| $V_{SUP\_UV\_7}$    | Power Supply Undervoltage Lockout (power-up)  | 7.0  | —    | 8.0  | V             |       |
| $V_{SUP\_UV\_5}$    | Power Supply Undervoltage Lockout (power-up)  | —    | —    | 5.6  | V             |       |
| $V_{SUP\_UV\_L}$    | Power Supply Undervoltage Lockout (falling - Boost config.)                                     | —    | —    | 2.7  | V             |       |
| $V_{SUP\_UV\_L\_B}$ | Power Supply Undervoltage Lockout (falling - Buck config.)                                      | —    | —    | 4.6  | V             | (7)   |
| $V_{SUP\_UV\_HYST}$ | Power Supply Undervoltage Lockout Hysteresis  | —    | 0.1  | —    | V             | (8)   |

### $V_{PRE}$ voltage pre-regulator

|                  |  |                                   |  |                       |   |     |
|------------------|--|-----------------------------------|--|-----------------------|---|-----|
| $V_{PRE}$        | $V_{PRE}$ Output Voltage <ul style="list-style-type: none"> <li>Buck mode (<math>V_{SUP} &gt; V_{SUP\_UV\_7}</math>)</li> <li>Buck mode (<math>V_{SUP\_UV\_7} \geq V_{SUP} \geq 4.6\text{ V}</math>)</li> <li>Boost mode (<math>V_{SUP} \geq 2.7\text{ V}</math>)</li> </ul>   | 6.25<br>$V_{PRE\_UV\_4P3}$<br>6.0 | —<br>$V_{SUP} - R_{DS(on)_{PRE}} \cdot I_{PRE}$<br>— | 6.75<br>—<br>7.0      | V |     |
| $I_{PRE}$        | $V_{PRE}$ Maximum Output Current Capability <ul style="list-style-type: none"> <li>Buck or Boost with <math>V_{SUP} &gt; V_{SUP\_UV\_7}</math></li> <li>Buck with <math>V_{SUP\_UV\_7} \geq V_{SUP} \geq 4.6\text{ V}</math></li> <li>Boost with <math>V_{SUP\_UV\_7} \geq V_{SUP} \geq 6.0\text{ V}</math></li> <li>Boost with <math>6.0\text{ V} \geq V_{SUP} \geq 4.0\text{ V}</math></li> <li>Boost with <math>4.0\text{ V} \geq V_{SUP} \geq 2.7\text{ V}</math></li> </ul> | 2.0<br>0.5<br>2.0<br>1.0<br>0.3   | —<br>2.0<br>—<br>—<br>—                              | —<br>—<br>—<br>—<br>— | A | (8) |
| $I_{PRE\_LPOFF}$ | $V_{PRE}$ Maximum Output Current Capability in LPOFF at low $V_{SUP}$ voltage <ul style="list-style-type: none"> <li>Buck with <math>V_{SUP\_UV\_7} \geq V_{SUP} \geq 4.6\text{ V}</math></li> <li>Boost with <math>V_{SUP\_UV\_7} \geq V_{SUP} \geq 6.0\text{ V}</math></li> <li>Boost with <math>6.0\text{ V} \geq V_{SUP} \geq 4.0\text{ V}</math></li> <li>Boost with <math>4.0\text{ V} \geq V_{SUP} \geq 2.7\text{ V}</math></li> </ul>                                    | 0.05<br>2.0<br>1.0<br>0.3         | —<br>—<br>—<br>—                                     | —<br>—<br>—<br>—      | A | (8) |
| $I_{PRE\_LIM}$   | $V_{PRE}$ Output Current Limitation with $V_{SUP} \leq 28\text{ V}$  | 3.5                               | —  | —                     | A |     |
| $I_{PRE\_OC}$    | $V_{PRE}$ Overcurrent Detection Threshold (in buck mode only) with $V_{SUP} \leq 28\text{ V}$  | 5.0                               | —  | —                     | A |     |
| $V_{PRE\_UV}$    | $V_{PRE}$ Undervoltage Detection Threshold (Falling)   | 5.5                               | —  | 6.0                   | V |     |

### Notes

- $V_{SUP\_UV\_L\_B} = V_{PRE\_UV\_4P3} + R_{DS(on)_{PRE}} \cdot I_{PRE}$
- Guaranteed by design

**Table 4. Operating range (continued)**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol   | Parameter   | Min.           | Typ.       | Max.      | Unit               | Notes |
|--|---|----------------|------------|-----------|--------------------|-------|
| <b>V<sub>PRE</sub> voltage pre-regulator (continued)</b> |   |                |            |           |                    |       |
| $V_{PRE\_UV\_HYST}$                                      | $V_{PRE}$ Undervoltage Hysteresis   | 0.05           | –          | 0.15      | V                  | (9)   |
| $V_{PRE\_UV\_4P3}$                                       | $V_{PRE}$ Shut-off Threshold (Falling - buck and buck/boost)  | 4.2            | –          | 4.5       | V                  |       |
| $V_{PRE\_UV\_4P3\_HYST}$                                 | $V_{PRE}$ Shut-off Hysteresis   | 0.05           | –          | 0.15      | V                  | (9)   |
| $R_{DS(on)\_PRE}$  | $V_{PRE}$ Pass Transistor On Resistance with $V_{SUP} \leq 28\text{ V}$   | –              | –          | 200       | m $\Omega$         |       |
| $L_{IR\_VPRE}$   | $V_{PRE}$ Line Regulation   | –              | 20         | –         | mV                 | (9)   |
| $LOR_{VPRE\_BUCK}$                                       | $V_{PRE}$ Load Regulation for $C_{OUT} = 57\text{ }\mu\text{F}$<br>• $I_{PRE}$ from 50 mA to 2.0 A - Buck mode  | –              | 100        | –         | mV                 | (9)   |
| $LOR_{VPRE\_BOOST}$                                      | $V_{PRE}$ Load Regulation for $C_{OUT} = 57\text{ }\mu\text{F}$<br>• $I_{PRE}$ from 50 mA to 2.0 A - Boost mode | –              | 500        | –         | mV                 | (9)   |
| $V_{PRE\_LL\_H}$<br>$V_{PRE\_LL\_L}$                     | $V_{PRE}$ Pulse Skipping Thresholds   | –<br>–         | 200<br>180 | –<br>–    | mV                 |       |
| $T_{WARN\_PRE}$  | $V_{PRE}$ Thermal Warning Threshold   | –              | 125        | –         | $^{\circ}\text{C}$ |       |
| $T_{SD\_PRE}$  | $V_{PRE}$ Thermal Shutdown Threshold  | 160            | –          | –         | $^{\circ}\text{C}$ |       |
| $T_{SD\_PRE\_HYST}$                                      | $V_{PRE}$ Thermal Shutdown Hysteresis   | –              | 10         | –         | $^{\circ}\text{C}$ | (9)   |
| $V_{SUP\_IPFF}$  | $I_{PFF}$ Input Voltage Detection   | 18             | –          | 24        | V                  |       |
| $V_{SUP\_IPFF\_HYST}$                                    | $I_{PFF}$ Input Voltage Hysteresis  | 0.2            | –          | –         | V                  |       |
| $I_{PRE\_IPFF\_PK}$                                      | $I_{PFF}$ High-side Peak Current Detection with $V_{SUP} \leq 28\text{ V}$                                      | 1.7            | –          | –         | A                  |       |
| $V_{G\_LS\_OH}$  | LS Gate Driver High Output Voltage ( $I_{OUT} = 50\text{ mA}$ )   | $V_{PRE}^{-1}$ | –          | $V_{PRE}$ | V                  |       |
| $V_{G\_LS\_OL}$  | LS Gate driver Low Level ( $I_{OUT} = 50\text{ mA}$ )   | –              | –          | 0.5       | V                  |       |

**V<sub>CORE</sub> voltage regulator**

|                    |   |                      |                  |                          |            |  |
|--------------------|---|----------------------|------------------|--------------------------|------------|--|
| $V_{CORE\_FB}$     | $V_{CORE}$ Feedback Input Voltage   | 0.784                | 0.8              | 0.816                    | V          |  |
| $I_{CORE}$         | $V_{CORE}$ Output Current Capability in Normal Mode<br>• 33907N<br>• 33908N<br>• 33907L<br>• 33908L | –<br>–<br>–<br>–     | –<br>–<br>–<br>– | 0.8<br>1.5<br>0.8<br>1.5 | A          |  |
| $I_{CORE\_LIM}$    | $V_{CORE}$ Output Current Limitation<br>• 33907N<br>• 33908N<br>• 33907L<br>• 33908L                | 1<br>1.8<br>1<br>1.8 | –<br>–<br>–<br>– | 2<br>3.5<br>2<br>3.5     | A          |  |
| $R_{DS(on)\_CORE}$ | $V_{CORE}$ Pass Transistor On Resistance  | –                    | –                | 200                      | m $\Omega$ |  |

Notes

9. Guaranteed by design

**Table 4. Operating range (continued)**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|--------|-----------|------|------|------|------|-------|
|--------|-----------|------|------|------|------|-------|

**V<sub>CORE</sub> voltage regulator (continued)**

|  |   |        |            |        |    |            |
|--|---|--------|------------|--------|----|------------|
| LOR <sub>V<sub>CORE</sub>_1.2</sub>              | V <sub>CORE</sub> Transient Load regulation - 1.2 V range | -60    | —          | 60     | mV | (10), (11) |
| LOR <sub>V<sub>CORE</sub>_3.3</sub>              | V <sub>CORE</sub> Transient Load regulation - 3.3 V range | -100   | —          | 100    | mV | (10), (11) |
| V <sub>CORE_LL_H</sub><br>V <sub>CORE_LL_L</sub> | V <sub>CORE</sub> Pulse Skipping Thresholds               | —<br>— | 180<br>160 | —<br>— | mV |            |
| T <sub>WARN_CORE</sub>                           | V <sub>CORE</sub> Thermal Warning Threshold               | —      | 125        | —      | °C |            |
| T <sub>SD_CORE</sub>                             | V <sub>CORE</sub> Thermal Shutdown Threshold              | 160    | —          | —      | °C |            |
| T <sub>SD_CORE_HYST</sub>                        | V <sub>CORE</sub> Thermal Shutdown Hysteresis             | —      | 10         | —      | °C | (10)       |

**V<sub>CCA</sub> voltage regulator**

|  |  |   |  |   |    |      |
|--|--|---|--|---|----|------|
| V <sub>CCA</sub>                                     | V <sub>CCA</sub> Output Voltage<br><ul style="list-style-type: none"> <li>5.0 V config. with Internal ballast at 100 mA</li> <li>5.0 V config with external ballast at 200 mA</li> <li>5.0 V config with external ballast at 300 mA</li> <li>3.3 V config with Internal ballast at 100 mA</li> <li>3.3 V config with external ballast at 200 mA</li> <li>3.3 V config with external ballast at 300 mA</li> </ul> | 4.95<br>4.9<br>4.85<br>3.2505<br>3.234<br>3.201 | 5.0<br>5.0<br>5.0<br>3.3<br>3.3<br>3.3 | 5.05<br>5.1<br>5.15<br>3.3495<br>3.366<br>3.399 | V  | (12) |
| I <sub>CCA_IN</sub>                                  | V <sub>CCA</sub> Output Current (int. MOSFET)  | —   | —                                      | 100   | mA |      |
| I <sub>CCA_OUT</sub>                                 | V <sub>CCA</sub> Output Current (external PNP)   | —   | —                                      | 300   | mA |      |
| I <sub>CCA_LIM_INT</sub>                             | V <sub>CCA</sub> Output Current Limitation (int. MOSFET)   | 100   | —                                      | 675   | mA |      |
| I <sub>CCA_LIM_OUT</sub>                             | V <sub>CCA</sub> Output Current Limitation (external PNP)  | 300   | —                                      | 675   | mA |      |
| I <sub>CCA_LIM_FB</sub>                              | V <sub>CCA</sub> Output Current Limitation Foldback  | 80  | —                                      | 200   | mA |      |
| V <sub>CCA_LIM_FB</sub>                              | V <sub>CCA</sub> Output Voltage Foldback Threshold   | 0.5   | —                                      | 1.1   | V  |      |
| V <sub>CCA_LIM_HYST</sub>                            | V <sub>CCA</sub> Output Voltage Foldback Hysteresis  | 0.03  | —                                      | 0.3   | V  |      |
| I <sub>CCA_BASE_SC</sub><br>I <sub>CCA_BASE_SK</sub> | V <sub>CCA</sub> Base Current Capability   | —<br>20   | —<br>—                                 | 30<br>—   | mA |      |
| T <sub>WARN_CCA</sub>                                | V <sub>CCA</sub> Thermal Warning Threshold (int. MOSFET only)  | —   | 125                                    | —   | °C |      |
| T <sub>SD_CCA</sub>                                  | V <sub>CCA</sub> Thermal Shutdown Threshold (int. MOSFET only)   | 160   | —                                      | —   | °C |      |
| T <sub>SD_CCA_HYST</sub>                             | V <sub>CCA</sub> Thermal Shutdown Hysteresis   | —   | 10                                     | —   | °C | (13) |
| LORT <sub>V<sub>CCA</sub></sub>                      | V <sub>CCA</sub> Transient Load Regulation<br><ul style="list-style-type: none"> <li>I<sub>CCA</sub> = 10 mA to 100 mA (internal MOSFET)</li> <li>I<sub>CCA</sub> = 10 mA to 300 mA (external ballast)</li> </ul>  | —   | —                                      | 1.0   | %  | (13) |

**Notes**

10. Guaranteed by design.
11. C<sub>OUT</sub> = 40 μF, I<sub>CORE</sub> = 10 mA to 1.5 A, dI<sub>CORE</sub>/dt ≤ 2.0 A/μs
12. External PNP gain within 150 to 450
13. Guaranteed by design.

**Table 4. Operating range (continued)**

$T_{CASE}$  = -40 °C to 125 °C, unless otherwise specified.  $V_{SUP}$  =  $V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V <  $V_{SUP}$  < 40 V, thermal dissipation must be considered ([Figure 25](#)).

| Symbol                                     | Parameter   | Min.     | Typ.   | Max.      | Unit | Notes |
|--|---|----------|--------|-----------|------|-------|
| <b>Vaux voltage regulator</b>              |   |          |        |           |      |       |
| $V_{AUX\_5}$                               | $V_{AUX}$ Output Voltage (5.0 V configuration)                            | 4.85     | 5.0    | 5.15      | V    |       |
| $V_{AUX\_33}$                              | $V_{AUX}$ Output Voltage (3.3 V configuration)                            | 3.2      | 3.3    | 3.4       | V    |       |
| $V_{AUX\_TRK}$                             | $V_{AUX}$ Tracking Error ( $V_{AUX\_5}$ and $V_{AUX\_33}$ )               | -15      | –      | +15       | mV   |       |
| $I_{AUX\_OUT}$                             | $V_{AUX}$ Output Current  | –        | –      | 300       | mA   |       |
| $I_{AUX\_LIM}$                             | $V_{AUX}$ Output Current Limitation                                       | 300      | –      | 700       | mA   |       |
| $I_{AUX\_LIM\_FB}$                         | $V_{AUX}$ Output Current Limitation Foldback                              | 100      | –      | 530       | mA   |       |
| $V_{AUX\_LIM\_FB}$                         | $V_{AUX}$ Output Voltage Foldback Threshold                               | 0.5      | –      | 1.1       | V    |       |
| $V_{AUX\_LIM\_HYST}$                       | $V_{AUX}$ Output Voltage Foldback Hysteresis                              | 0.03     | –      | 0.3       | V    |       |
| $I_{AUX\_BASE\_SC}$<br>$I_{AUX\_BASE\_SK}$ | $V_{AUX}$ Base Current Capability   | –<br>7.0 | –<br>– | -7.0<br>– | mA   |       |
| $TSD_{AUX}$                                | $V_{AUX}$ Thermal Shutdown Threshold                                      | 160      | –      | –         | °C   |       |
| $TSD_{AUX\_HYST}$                          | $V_{AUX}$ Thermal Shutdown Hysteresis                                     | –        | 10     | –         | °C   | (14)  |
| $LOR_{VAUX}$                               | $V_{AUX}$ Static Load Regulation ( $I_{AUX\_OUT}$ = 10 mA to 300 mA)      | –        | 15     | –         | mV   | (14)  |
| $LORT_{VAUX}$                              | $V_{AUX}$ Transient Load Regulation<br>• $I_{AUX\_OUT}$ = 10 mA to 300 mA | –        | –      | 1.0       | %    | (14)  |

**CAN\_5V voltage regulator**

|                     |  |      |     |      |    |      |
|---------------------|--|------|-----|------|----|------|
| $V_{CAN}$           | $V_{CAN}$ Output Voltage<br>$V_{SUP}$ > 6.0 V in Buck mode<br>$V_{SUP}$ > $V_{SUP\_UV\_L}$ in Boost mode | 4.8  | 5.0 | 5.2  | V  |      |
| $I_{CAN\_OUT}$      | $V_{CAN}$ Output Current   | –    | –   | 100  | mA |      |
| $I_{CAN\_LIM}$      | $V_{CAN}$ Output Current Limitation  | 100  | –   | 250  | mA |      |
| $TSD_{CAN}$         | $V_{CAN}$ Thermal Shutdown Threshold   | 160  | –   | –    | °C |      |
| $TSD_{CAN\_HYST}$   | $V_{CAN}$ Thermal Shutdown Hysteresis  | –    | 10  | –    | °C | (14) |
| $V_{CAN\_UV}$       | $V_{CAN}$ Undervoltage Detection Threshold   | 4.25 | –   | 4.8  | V  |      |
| $V_{CAN\_UV\_HYST}$ | $V_{CAN}$ Undervoltage Hysteresis  | 0.07 | –   | 0.22 | V  |      |
| $V_{CAN\_OV}$       | $V_{CAN}$ Overvoltage Detection Threshold  | 5.2  | –   | 5.55 | V  |      |
| $V_{CAN\_OV\_HYST}$ | $V_{CAN}$ Overvoltage Hysteresis   | 0.07 | –   | 0.22 | V  |      |
| $LOR_{VCAN}$        | $V_{CAN}$ Load Regulation (from 0 to 50 mA)  | –    | 100 | –    | mV | (14) |

Notes

14. Guaranteed by design.

**Table 4. Operating range (continued)**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol                                      | Parameter   | Min. | Typ. | Max.  | Unit     | Notes |
|---|---|------|------|-------|----------|-------|
| <b>Fail-safe machine voltage supervisor</b> |   |      |      |       |          |       |
| $V_{PRE\_OV}$                               | $V_{PRE}$ Overvoltage Detection Threshold                                 | 7.2  | –    | 8.0   | V        |       |
| $V_{PRE\_OV\_HYST}$                         | $V_{PRE}$ Overvoltage Hysteresis  | –    | 0.1  | –     | V        | (15)  |
| $V_{CORE\_FB\_UV}$                          | $V_{CORE}$ FB Undervoltage Detection Threshold                            | 0.67 | –    | 0.773 | V        |       |
| $V_{CORE\_FB\_UV\_D}$                       | $V_{CORE}$ FB Undervoltage Detection Threshold - Degraded mode            | 0.45 | –    | 0.58  | V        |       |
| $V_{CORE\_FB\_UV\_HYST}$                    | $V_{CORE}$ FB Undervoltage Hysteresis                                     | 10   | –    | 27    | mV       | (15)  |
| $V_{CORE\_FB\_OV}$                          | $V_{CORE}$ FB Overvoltage Detection Threshold                             | 0.84 | –    | 0.905 | V        |       |
| $V_{CORE\_FB\_OV\_HYS\_T}$                  | $V_{CORE}$ FB Overvoltage Hysteresis                                      | 10   | –    | 30    | mV       | (15)  |
| $V_{CORE\_FB\_DRIFT}$                       | $V_{CORE\_FB}$ Drift versus $IO\_1$                                       | 50   | 100  | 150   | mV       |       |
| $I_{PD\_CORE}$                              | $V_{CORE}$ Internal Pull-down Current (active when $V_{CORE}$ is enabled) | 5.0  | 12   | 25    | mA       |       |
| $V_{CCA\_UV\_5}$                            | $V_{CCA}$ Undervoltage Detection Threshold (5.0 V config)                 | 4.5  | –    | 4.75  | V        |       |
| $V_{CCA\_UV\_5D}$                           | $V_{CCA}$ Undervoltage Detection Threshold (Degraded 5.0 V)               | 3.0  | –    | 3.2   | V        |       |
| $V_{CCA\_UV\_33}$                           | $V_{CCA}$ Undervoltage Detection Threshold (3.3 V config)                 | 3.0  | –    | 3.2   | V        |       |
| $V_{CCA\_UV\_HYST}$                         | $V_{CCA}$ Undervoltage Hysteresis   | –    | 0.07 | –     | V        | (15)  |
| $V_{CCA\_OV\_5}$                            | $V_{CCA}$ Overvoltage Detection Threshold (5.0 V config)                  | 5.25 | –    | 5.5   | V        |       |
| $V_{CCA\_OV\_33}$                           | $V_{CCA}$ Overvoltage Detection Threshold (3.3 V config)                  | 3.4  | –    | 3.6   | V        |       |
| $V_{CCA\_OV\_HYST}$                         | $V_{CCA}$ Overvoltage Hysteresis  | –    | 0.15 | –     | V        | (15)  |
| $R_{PD\_CCA}$                               | $V_{CCA}$ Internal Pull-down Resistor (active when $V_{CCA}$ is disabled) | 50   | –    | 160   | $\Omega$ |       |
| $V_{AUX\_UV\_5}$                            | $V_{AUX}$ Undervoltage Detection Threshold (5.0 V config)                 | 4.5  | –    | 4.75  | V        |       |
| $V_{AUX\_UV\_5D}$                           | $V_{AUX}$ Undervoltage Detection Threshold (Degraded 5.0 V)               | 3.0  | –    | 3.2   | V        |       |
| $V_{AUX\_UV\_33}$                           | $V_{AUX}$ Undervoltage Detection Threshold (3.3 V config)                 | 3.0  | –    | 3.2   | V        |       |
| $V_{AUX\_UV\_HYST}$                         | $V_{AUX}$ Undervoltage Hysteresis   | –    | 0.07 | –     | V        | (15)  |
| $V_{AUX\_OV\_5}$                            | $V_{AUX}$ Overvoltage Detection Threshold (5.0 V config)                  | 5.25 | –    | 5.5   | V        |       |
| $V_{AUX\_OV\_33}$                           | $V_{AUX}$ Overvoltage Detection Threshold (3.3 V config)                  | 3.4  | –    | 3.6   | V        |       |
| $V_{AUX\_OV\_HYST}$                         | $V_{AUX}$ Overvoltage Hysteresis  | –    | 0.07 | –     | V        | (15)  |
| $R_{PD\_AUX}$                               | $V_{AUX}$ Internal Pull-down Resistor (active when $V_{AUX}$ is disabled) | 50   | –    | 170   | $\Omega$ |       |

Notes

15. Guaranteed by design.

**Table 4. Operating range (continued)**

$T_{CASE}$  = -40 °C to 125 °C, unless otherwise specified.  $V_{SUP}$  =  $V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol                   | Parameter  | Min. | Typ. | Max. | Unit | Notes |
|--------------------------|--|------|------|------|------|-------|
| <b>Fail-safe outputs</b> |  |      |      |      |      |       |
| $V_{RSTB\_OL}$           | Reset Low Output Level ( $I_{RSTB} = 2.0\text{ mA}$ and $2.0\text{ V} < V_{SUP} < 40\text{ V}$ ) | –    | –    | 0.5  | V    | (16)  |
| $I_{RSTB\_LIM}$          | Reset Output Current Limitation  | 12   | –    | 25   | mA   |       |
| $V_{RSTB\_IL}$           | External Reset Detection Threshold (falling)   | 1.0  | –    | –    | V    |       |
| $V_{RSTB\_IH}$           | External Reset Detection Threshold (rising)  | –    | –    | 2.0  | V    |       |
| $V_{RSTB\_IN\_HYST}$     | External Reset Input Hysteresis  | 0.2  | –    | –    | V    |       |
| $V_{FS0B\_OL}$           | FS0B Low Output Level ( $I_{FS0B} = 2.0\text{ mA}$ )   | –    | –    | 0.5  | V    |       |
| $I_{FS0B\_LK}$           | FS0B Input Current Leakage ( $V_{FS0B} = 28\text{ V}$ )  | –    | –    | 1.0  | μA   |       |
| $I_{FS0B\_LIM}$          | FS0B Output Current Limitation   | 6.0  | –    | 12   | mA   |       |

**Analog input - multi-purpose IOs**

|                   |  |     |   |     |    |  |
|-------------------|--|-----|---|-----|----|--|
| $V_{IO\_ANA\_WD}$ | Measurable Input Voltage (wide range)  | 3.0 | – | 19  | V  |  |
| $V_{IO\_ANA\_TG}$ | Measurable Input Voltage (tight range) | 3.0 | – | 9.0 | V  |  |
| $I_{IO\_IN\_ANA}$ | Input Current                          | –   | – | 100 | μA |  |

**Digital input**

|                     |   |      |     |     |    |      |
|---------------------|---|------|-----|-----|----|------|
| $V_{IO\_IH}$        | Digital High Input voltage level (IO_0:1, IO_4:5)<br>• Min Limit = 2.7 V at $V_{SUP} = 40\text{ V}$ | 2.6  | –   | –   | V  |      |
| $V_{IO23\_IH}$      | Digital High Input voltage level (IO_2, IO_3)   | 2.0  | –   | –   | V  |      |
| $V_{IO\_IL}$        | Digital Low Input voltage Level (IO_0:1; IO_4:5)  | –    | –   | 2.1 | V  |      |
| $V_{IO\_HYST}$      | Input Voltage Hysteresis (IO_0:1, IO_4:5)   | 50   | 120 | 500 | mV | (17) |
| $V_{IO23\_IL}$      | Digital Low Input voltage Level (IO_2, IO_3)  | –    | –   | 0.9 | V  |      |
| $V_{IO23\_HYST}$    | Input Voltage Hysteresis (IO_2, IO_3)   | 200  | 450 | 700 | mV | (17) |
| $I_{IO\_IN\_0:1}$   | Input Current for IO_0:1  | -5.0 | –   | 100 | μA |      |
| $I_{IO\_IN\_1}$     | Input Current for IO_1 when used for FB_Core monitoring   | -1.0 | –   | 1.0 | μA |      |
| $I_{IO\_IN\_2:5}$   | Input Current for IO_2:5  | -5.0 | –   | 5.0 | μA |      |
| $I_{IO\_IN\_LPOFF}$ | Input Current for IO_0:5 in LPOFF   | -1.0 | –   | 1.0 | μA |      |

**Output gate driver**

|  |   |                 |        |           |    |  |
|--|---|-----------------|--------|-----------|----|--|
| $V_{IO\_OH}$                           | High Output Level at $I_{IO\_OUT} = -2.5\text{ mA}$ | $V_{PRE} - 1.5$ | –      | $V_{PRE}$ | V  |  |
| $V_{IO\_OL}$                           | Low Output Level at $I_{IO\_OUT} = +2.5\text{ mA}$  | 0.0             | –      | 1.0       | V  |  |
| $V_{IO\_OUT\_SK}$<br>$V_{IO\_OUT\_SC}$ | Output Current Capability                           | 2.5<br>–        | –<br>– | –<br>-2.5 | mA |  |

**Notes**

16. For  $V_{SUP} < 2.0\text{ V}$ , all supplies are already off and external pull-up on RSTB (e.g  $V_{CORE}$  or  $V_{CCA}$ ) pulls the line down.

17. Guaranteed by design.



**Table 4. Operating range (continued)**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|--------|-----------|------|------|------|------|-------|
|--------|-----------|------|------|------|------|-------|

**Analog multiplexer**

|                     |   |       |      |       |                        |      |
|---------------------|---|-------|------|-------|------------------------|------|
| $V_{AMUX\_ACC}$     | Voltage Sense Accuracy ( $V_{SNS}$ , $IO\_0$ , $IO\_1$ ) using 5.1 k $\Omega$ resistor    | -5.0  | –    | 5.0   | %                      | (18) |
| $V_{AMUX\_WD\_5}$   | Divider Ratio (wide input voltage range) at $V_{DDIO} = 5.0\text{ V}$                     | –     | 5.0  | –     |                        |      |
| $V_{AMUX\_WD\_3P3}$ | Divider Ratio (wide input voltage range) at $V_{DDIO} = 3.3\text{ V}$                     | –     | 7.0  | –     |                        |      |
| $V_{AMUX\_TG\_5}$   | Divider Ratio (tight input voltage range) at $V_{DDIO} = 5.0\text{ V}$                    | –     | 2.0  | –     |                        |      |
| $V_{AMUX\_TG\_3P3}$ | Divider Ratio (tight input voltage range) at $V_{DDIO} = 3.3\text{ V}$                    | –     | 3.0  | –     |                        |      |
| $V_{AMUX\_REF1}$    | Internal Voltage Reference with $6.0\text{ V} < V_{SUP} < 19\text{ V}$                    | 2.475 | 2.5  | 2.525 | V                      |      |
| $V_{AMUX\_REF2}$    | Internal Voltage Reference with $V_{SUP} \leq 6.0\text{ V}$ or $V_{SUP} \geq 19\text{ V}$ | 2.468 | 2.5  | 2.532 | V                      |      |
| $V_{AMUX\_TP\_CO}$  | Internal Temperature sensor coefficient   | –     | 9.9  | –     | mV/ $^{\circ}\text{C}$ | (19) |
| $V_{AMUX\_TP}$      | Temperature Sensor MUX_OUT output voltage (at $T_J = 165^{\circ}\text{C}$ )               | 2.08  | 2.15 | 2.22  | V                      |      |

**Interrupt**

|                |  |   |    |     |               |  |
|----------------|--|---|----|-----|---------------|--|
| $V_{INTB\_OL}$ | Low Output Level ( $I_{INT} = 2.5\text{ mA}$ )       | – | –  | 0.5 | V             |  |
| $R_{PU\_INT}$  | Internal Pull-up Resistor (connected to $V_{DDIO}$ ) | – | 10 | –   | K $\Omega$    |  |
| $I_{INT\_LK}$  | Input Leakage Current                                | – | –  | 1   | $\mu\text{A}$ |  |

**CAN transceiver****CAN logic input pin (TXD)**

|                  |   |                       |    |                       |               |  |
|------------------|---|-----------------------|----|-----------------------|---------------|--|
| $V_{TXD\_IH}$    | TXD High Input Threshold                        | $0.7 \times V_{DDIO}$ | –  | –                     | V             |  |
| $V_{TXD\_IL}$    | TXD Low Input Threshold                         | –                     | –  | $0.3 \times V_{DDIO}$ | V             |  |
| $TXD_{PULL\_UP}$ | TXD Main Device Pull-up                         | 20                    | 33 | 50                    | K $\Omega$    |  |
| $TXD_{LK}$       | TXD Input Leakage Current, $V_{TXD} = V_{DDIO}$ | -1.0                  | –  | 1.0                   | $\mu\text{A}$ |  |

**CAN logic output pin (RXD)**

|                 |   |                           |   |     |   |  |
|-----------------|---|---------------------------|---|-----|---|--|
| $V_{RXD\_OL1}$  | Low Level Output Voltage ( $I_{RXD} = 250\text{ }\mu\text{A}$ )   | –                         | – | 0.4 | V |  |
| $V_{RXD\_OL2}$  | Low Level Output Voltage ( $I_{RXD} = 1.5\text{ mA}$ )  | –                         | – | 0.9 | V |  |
| $V_{OUT\_HIGH}$ | High Level Output Voltage ( $I_{RXD} = -250\text{ }\mu\text{A}$ , $V_{DDIO} = 3.0\text{ V}$ to $5.5\text{ V}$ ) | $V_{DDIO} - 0.4\text{ V}$ | – | –   | V |  |

**Notes**

18. If a higher resistor value than recommended is used, the accuracy degrades.  
 19. Guaranteed by design

**Table 4. Operating range (continued)**

$T_{CASE}$  = -40 °C to 125 °C, unless otherwise specified.  $V_{SUP}$  =  $V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol                              | Parameter  | Min.        | Typ.       | Max.        | Unit                           | Notes |
|-------------------------------------|--|-------------|------------|-------------|--------------------------------|-------|
| <b>CAN output pins (CANH, CANL)</b> |  |             |            |             |                                |       |
| $V_{DIFF\_COM\_MODE}$               | Differential Input Comparator Common Mode Range  | -12         | –          | 12          | V                              |       |
| $V_{IN\_DIFF\_SLEEP}$               | Differential Input Voltage Threshold in Sleep Mode   | 0.5         | –          | 0.9         | V                              |       |
| $V_{IN\_HYST}$                      | Differential Input Hysteresis (in TX, RX mode)   | 50          | –          | –           | mV                             |       |
| $R_{IN\_CHCL}$                      | CANH, CANL Input Resistance  | 5.0         | –          | 50          | k $\Omega$                     |       |
| $R_{IN\_DIFF}$                      | CAN Differential Input Resistance  | 10          | –          | 100         | k $\Omega$                     |       |
| $R_{IN\_MATCH}$                     | Input Resistance Matching  | -3.0        | –          | 3.0         | %                              |       |
| $V_{CANH}$                          | CANH Output Voltage ( $45\ \Omega < R_{BUS} < 65\ \Omega$ )<br>• TX dominant state<br>• TX recessive state   | 2.75<br>2.0 | –<br>2.5   | 4.5<br>3.0  | V                              |       |
| $V_{CANL}$                          | CANL Output Voltage ( $45\ \Omega < R_{BUS} < 65\ \Omega$ )<br>• TX dominant state<br>• TX recessive state   | 0.5<br>2.0  | –<br>2.5   | 2.25<br>3.0 | V                              |       |
| $V_{CAN\_SYM}$                      | CAN dominant voltage symmetry ( $V_{CANL} + V_{CANH}$ )  | 4.5         | 5          | 5.5         | V                              |       |
| $V_{OH}-V_{OL}$                     | Differential Output Voltage<br>• TX dominant state ( $45\ \Omega < R_{BUS} < 65\ \Omega$ )<br>• TX recessive state   | 1.5<br>-50  | 2.0<br>0.0 | 3.0<br>50   | V<br>mV                        |       |
| $I_{CANL-SK}$                       | CANL Sink Current Under Short-circuit Condition ( $V_{CANL} \leq 12\text{ V}$ , CANL driver ON, TXD low)   | 40          | –          | 100         | mA                             |       |
| $I_{CANH-SC}$                       | CANH Source Current Under Short-circuit Condition ( $V_{CANH} = -2.0\text{ V}$ , CANH driver ON, TXD low)  | -100        | –          | -40         | mA                             |       |
| $R_{INSLEEP}$                       | CANH, CANL Input Resistance Device Supplied and in CAN Sleep Mode  | 5.0         | –          | 50          | k $\Omega$                     |       |
| $V_{CANLP}$                         | CANL, CANH Output Voltage in Sleep Modes. No termination load.   | -0.1        | 0.0        | 0.1         | V                              |       |
| $I_{CAN}$                           | CANH, CANL Input Current, Device Unsupplied, ( $V_{CANH}, V_{CANL} = 5.0\text{V}$ )<br>• $V_{SUP}$ and $V_{CAN}$ connected to GND<br>• $V_{SUP}$ and $V_{CAN}$ connected to GND via 47k resistor | -10<br>-10  | –<br>–     | 10<br>10    | $\mu\text{A}$<br>$\mu\text{A}$ | (20)  |
| $T_{OT}$                            | Overtemperature Detection  | 160         | –          | –           | °C                             |       |
| $T_{HYST}$                          | Overtemperature Hysteresis   | –           | –          | 20          | °C                             |       |

**Digital interface**

|                |  |                  |     |     |               |  |
|----------------|--|------------------|-----|-----|---------------|--|
| $MISO_H$       | High Output Level on MISO ( $I_{MISO} = 1.5\text{ mA}$ ) | $V_{DDIO} - 0.4$ | –   | –   | V             |  |
| $MISO_L$       | Low Output Level on MISO ( $I_{MISO} = 2.0\text{ mA}$ )  | –                | –   | 0.4 | V             |  |
| $I_{MISO}$     | Tri-state Leakage Current ( $V_{DDIO} = 5.0\text{ V}$ )  | -5.0             | –   | 5.0 | $\mu\text{A}$ |  |
| $V_{DDIO}$     | Supply Voltage for MISO Output Buffer                    | 3.0              | –   | 5.5 | V             |  |
| $I_{V_{DDIO}}$ | Current consumption on VDDIO                             | –                | 1.0 | 3.0 | mA            |  |
| $SPI_{LK}$     | SCLK, NCS, MOSI Input Current                            | -1.0             | –   | 1.0 | $\mu\text{A}$ |  |
| $V_{SPI\_IH}$  | SCLK, NCS, MOSI High Input Threshold                     | 2.0              | –   | –   | V             |  |
| $R_{SPI}$      | NCS, MOSI Internal Pull-up (pull-up to VDDIO)            | 200              | 400 | 800 | K $\Omega$    |  |
| $V_{SPI\_IL}$  | SCLK, NCS, MOSI Low Input Threshold                      | –                | –   | 0.8 | V             |  |

**Table 4. Operating range (continued)**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol          | Parameter                    | Min. | Typ. | Max. | Unit          | Notes |
|-----------------|------------------------------|------|------|------|---------------|-------|
| <b>Debug</b>    |                              |      |      |      |               |       |
| $V_{DEBUG\_IL}$ | Low Input Voltage Threshold  | 2.1  | 2.35 | 2.6  | V             |       |
| $V_{DEBUG\_IH}$ | High Input Voltage Threshold | 4.35 | 4.6  | 4.97 | V             |       |
| $I_{DEBUG\_LK}$ | Input Leakage Current        | -10  | —    | 10   | $\mu\text{A}$ |       |

**LIN transceiver (when  $7.0\text{ V} < V_{SUP1,2,3} < 18\text{ V}$ , unless otherwise specified) (33907L/33908L)**

**LIN logic input pin (TXDL)**

|                  |   |      |    |     |               |  |
|------------------|---|------|----|-----|---------------|--|
| $V_{TXDL\_IH}$   | TXDL High Input Threshold                     | 2.0  | —  | —   | V             |  |
| $V_{TXDL\_IL}$   | TXDL Low Input Threshold                      | —    | —  | 0.8 | V             |  |
| $TXDL\_PULL\_UP$ | TXDL Internal Pull-up (to VDDIO)              | 20   | 33 | 50  | $k\Omega$     |  |
| $TXDL\_LK$       | TXD Input Leakage Current, $V_{TXDL} = VDDIO$ | -1.0 | —  | 1.0 | $\mu\text{A}$ |  |

**LIN logic input pin (RXDL)**

|                       |  |                        |   |     |   |  |
|-----------------------|--|------------------------|---|-----|---|--|
| $V_{RXDL\_OL1}$       | Low Level Output Voltage ( $I_{RXDL} = 250\text{ }\mu\text{A}$ )   | —                      | — | 0.4 | V |  |
| $V_{RXDL\_OL2}$       | Low Level Output Voltage ( $I_{RXDL} = 1.5\text{ mA}$ )  | —                      | — | 0.9 | V |  |
| $V_{RXDL\_OUT\_HIGH}$ | High Level Output Voltage ( $I_{RXDL} = -250\text{ }\mu\text{A}$ , $V_{DDIO} = 3.0\text{ V}$ to $5.5\text{ V}$ ) | $V_{DDIO}-0.4\text{V}$ | — | —   | V |  |

**LIN output pin**

|                     |  |               |     |                 |               |      |
|---------------------|--|---------------|-----|-----------------|---------------|------|
| $I_{BUS\_PAS\_DOM}$ | Input Leakage Current at the Receiver. Dominant State (Driver OFF, $V_{BAT} = 12\text{ V}$ , $V_{BUS} = 0\text{ V}$ )  | -1.0          | —   | —               | mA            | (21) |
| $I_{BUS\_PAS\_REC}$ | Input Leakage Current at the Receiver. Recessive State (Driver OFF, $8.0\text{ V} < V_{BAT} < 18\text{ V}$ , $8.0\text{ V} < V_{BUS} < 18\text{ V}$ , $V_{BUS} \geq V_{BAT}$ ) | —             | —   | 20              | $\mu\text{A}$ |      |
| $V_{DRIVER\_DOM}$   | Driver Dominant Voltage  | —             | —   | $0.251 V_{SUP}$ | V             |      |
| $V_{BUS\_DOM}$      | Receiver Dominant State  | —             | —   | $0.4 V_{SUP}$   | V             |      |
| $V_{BUS\_REC}$      | Receiver Recessive State   | $0.6 V_{SUP}$ | —   | —               | V             |      |
| $V_{BUS\_WU}$       | LIN Wake-up Detection Threshold ( $7.0\text{ V} < V_{SUP} < 18\text{ V}$ )   | $0.4 V_{SUP}$ | —   | $0.6 V_{SUP}$   | V             |      |
| $V_{LIN\_UV}$       | $V_{SUP}$ Undervoltage Threshold   | —             | —   | 7.0             | V             |      |
| $V_{SER\_DIODE}$    | Series Diode Voltage Drop ( $D_{SER\_MASTER}$ and $D_{SER\_INT}$ in pull-up path)  | 0.4           | 0.7 | 1.0             | V             |      |
| $I_{BUS\_LIM}$      | Current Limitation for Driver Dominant State ( $V_{BUS} = 18\text{ V}$ )   | 40            | —   | 200             | mA            | (22) |
| $R_{SLAVE}$         | LIN Pull-up Resistor   | 20            | —   | 60              | $k\Omega$     |      |
| $V_{SHIFT\_GND}$    | Ground Shift ( $V_{SHIFT\_GND} = V_{GND\_ECU} - V_{GND\_BATTERY}$ )  | 0.0           | —   | $11.5\%V_{BAT}$ | V             |      |
| $V_{SHIFT\_BAT}$    | Battery Voltage Shift ( $V_{SHIFT\_BAT} = V_{BATTERY} - V_{SHIFT\_GND} - V_{BAT}$ )  | 0.0           | —   | $11.5\%V_{BAT}$ | V             | (23) |

**Notes**

20. Guaranteed by design and characterization.
21.  $V_{BAT}$  is the voltage at the input of the control unit.
22. Current flowing inside the pin. A transceiver must be capable to sink at least 40 mA.
23.  $V_{BAT}$ : voltage across the battery connectors of the vehicle.  $V_{GND\_ECU}$ : voltage on the local ECU ground connector with respect to battery ground of the vehicle ( $V_{GND\_BATTERY}$ ).

**Table 4. Operating range (continued)**

$T_{CASE}$  = -40 °C to 125 °C, unless otherwise specified.  $V_{SUP}$  =  $V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When 28 V <  $V_{SUP}$  < 40 V, thermal dissipation must be considered ([Figure 25](#)).

| Symbol                            | Parameter  | Min.            | Typ. | Max.            | Unit | Notes |
|-----------------------------------|--|-----------------|------|-----------------|------|-------|
| <b>LIN output pin (continued)</b> |  |                 |      |                 |      |       |
| $V_{SHIFT\_DIF}$                  | Difference Between Battery Shift and Ground Shift<br>( $V_{SHIFT\_DIF} = V_{SHIFT\_BAT} - V_{SHIFT\_GND}$ )  | 0.0             | –    | 8.0% $V_{BAT}$  | V    | (24)  |
| $V_{BUS\_CNT}$                    | $V_{BUS\_CNT} = (V_{TH\_REC} + V_{TH\_DOM})/2$   | 0.475 $V_{SUP}$ | –    | 0.525 $V_{SUP}$ | V    | (25)  |
| $V_{HYST}$                        | $V_{HYST} = V_{TH\_REC} - V_{TH\_DOM}$   | –               | –    | 0.175 $V_{SUP}$ | V    |       |
| $I_{BUS\_NO\_GND}$                | Ground Disconnection. $GND = V_{SUP}$ , 0 V < $V_{BUS} < 18$ V, $V_{BAT} = 12$ V. Loss of Local GND does not affect communication in the remaining network | -1.0            | –    | 1.0             | mA   | (26)  |
| $I_{BUS\_NO\_BAT}$                | VBAT disconnection. $V_{SUP} = GND$ , 0 V < $V_{BUS} < 18$ V. Node sustains the current that can flow under this condition. BUS remains operational.       | –               | –    | 100             | μA   |       |
| $LIN_{TSD}$                       | LIN Thermal Shutdown   | –               | 180  | –               | °C   | (27)  |
| $LIN_{TSD\_HYST}$                 | LIN Thermal Shutdown Hysteresis  |                 | 20   |                 | °C   |       |
| $C_{LIN}$                         | LIN internal capacitor   | –               | –    | 10              | pF   | (27)  |

**Notes**

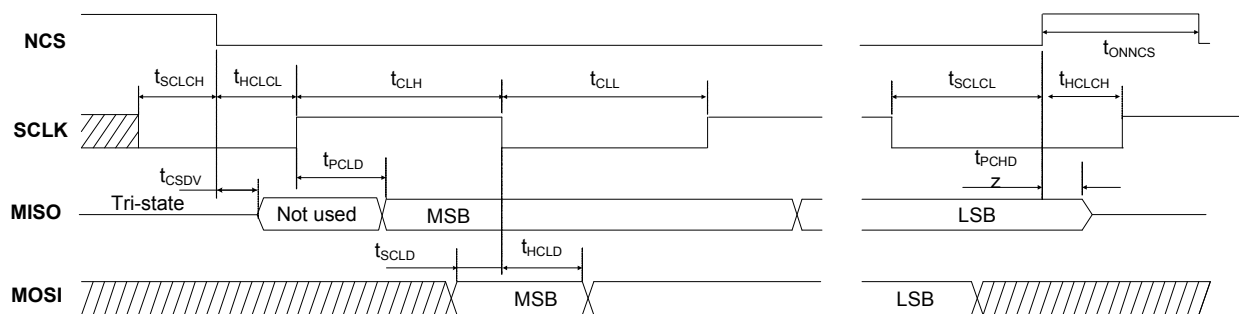
24. This constraint refers to duty cycle D1 and D2 only.
25.  $V_{TH\_DOM}$ : receiver threshold of the recessive to dominant LIN bus edge.  $V_{TH\_REC}$  receiver threshold of the dominant to recessive LIN bus edge.
26.  $V_{SUP}$  is the voltage at the input of the device (different from  $V_{bat}$  when a reverse current protection diode is implemented).
27. Guaranteed by design.

## 4.3 Dynamic electrical characteristics

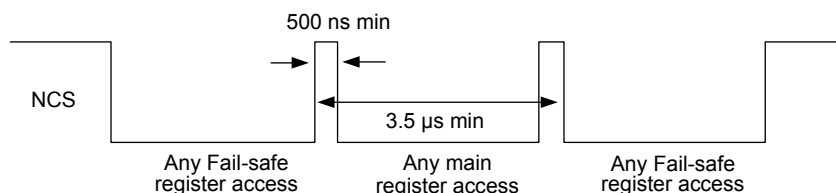
**Table 5. Dynamic electrical characteristics**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to  $40\text{ V}$ , unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered ([Figure 25](#)).

| Symbol            | Parameter   | Min.       | Typ.   | Max.     | Unit | Notes |
|-------------------|---|------------|--------|----------|------|-------|
| $f_{SPI}$         | SPI Operation Frequency (50% DC)  | 0.5        | —      | 8.0      | MHz  |       |
| $t_{MISO\_TRANS}$ | MISO Transition Speed, 20 - 80% <ul style="list-style-type: none"> <li><math>V_{DDIO} = 5.0\text{ V}</math>, <math>C_{LOAD} = 50\text{ pF}</math></li> <li><math>V_{DDIO} = 5.0\text{ V}</math>, <math>C_{LOAD} = 150\text{ pF}</math></li> </ul> | 5.0<br>5.0 | —<br>— | 30<br>50 | ns   |       |
| $t_{CLH}$         | Minimum Time SCLK = HIGH  | 62         | —      | —        | ns   |       |
| $t_{CLL}$         | Minimum Time SCLK = LOW   | 62         | —      | —        | ns   |       |
| $t_{PCLD}$        | Propagation Delay (SCLK to data at 10% of MISO rising edge)   | —          | —      | 30       | ns   |       |
| $t_{CSDV}$        | NCS = LOW to Data at MISO Active  | —          | —      | 75       | ns   |       |
| $t_{SCLCH}$       | SCLK Low Before NCS Low (setup time SCLK to NCS change H/L)   | 75         | —      | —        | ns   |       |
| $t_{HCLCL}$       | SCLK Change L/H after NCS = low   | 75         | —      | —        | ns   |       |
| $t_{SCLD}$        | SDI Input Setup Time (SCLK change H/L after MOSI data valid)  | 40         | —      | —        | ns   |       |
| $t_{HCLD}$        | SDI Input Hold Time (MOSI data hold after SCLK change H/L)  | 40         | —      | —        | ns   |       |
| $t_{SCLCL}$       | SCLK Low Before NCS High  | 100        | —      | —        | ns   |       |
| $t_{HCLCH}$       | SCLK High After NCS High  | 100        | —      | —        | ns   |       |
| $t_{PCHD}$        | NCS L/H to MISO at High-impedance   | —          | —      | 75       | ns   |       |
| $t_{ONNCS}$       | NCS Min. High Time  | 500        | —      | —        | ns   |       |
| $t_{NCS\_MIN}$    | NCS Filter Time   | 10         | —      | 40       | ns   |       |



**Figure 7. SPI timing diagram**



**Figure 8. Register access restriction**

**Table 5. Dynamic electrical characteristics (continued)**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|--------|-----------|------|------|------|------|-------|
|--------|-----------|------|------|------|------|-------|

**CAN dynamic characteristics**

|                  |   |     |     |     |               |      |
|------------------|---|-----|-----|-----|---------------|------|
| $t_{DOUT}$       | TXD Dominant State Timeout  | 0.8 | –   | 5.0 | ms            |      |
| $t_{DOM}$        | Bus Dominant Clamping Detection   | 0.8 | –   | 5.0 | ms            |      |
| $t_{LOOP}$       | Propagation Loop Delay TXD to RXD<br>• $R_{LOAD} = 120\text{ }\Omega$ , C between CANH and CANL = 100 pF,<br>C at RxD < 15 pF   | –   | –   | 255 | ns            |      |
| $t_{1PWU}$       | Single Pulse Wake-up Time   | 0.5 | –   | 5.0 | $\mu\text{s}$ |      |
| $t_{3PWU}$       | Multiple Pulse Wake-up Time   | 0.5 | –   | 1.0 | $\mu\text{s}$ |      |
| $t_{3PTO1}$      | Multiple Pulse Wake-up Timeout (120 $\mu\text{s}$ bit selection)  | 110 | 120 | –   | $\mu\text{s}$ |      |
| $t_{3PTO2}$      | Multiple Pulse Wake-up Timeout (360 $\mu\text{s}$ bit selection)  | 350 | 360 | –   | $\mu\text{s}$ |      |
| $t_{CAN\_READY}$ | Delay to Enable CAN by SPI Command (NCS rising edge) to CAN to Transmit (device in normal mode and CAN interface in TX/RX mode) | –   | –   | 100 | $\mu\text{s}$ | (28) |

**Fail-safe state machine**

|                       |  |     |   |     |               |  |
|-----------------------|--|-----|---|-----|---------------|--|
| $OSC_{FSSM}$          | Oscillator   | 405 | – | 495 | kHz           |  |
| $CLK_{FS\_MIN}$       | Fail-safe Oscillator Monitoring                                    | 150 | – | –   | kHz           |  |
| $t_{IC\_ERR}$         | IO_0:5 Filter Time   | 4.0 | – | 20  | $\mu\text{s}$ |  |
| $t_{ACK\_FS}$         | Acknowledgement Counter (used for IC error handling IO_1 and IO_5) | 7.0 | – | 9.7 | ms            |  |
| $t_{DFS\_RECOVERY}$   | IO_0 Filter Time to Recover from Deep Reset and Fail State         | 0.8 | – | 1.3 | ms            |  |
| $t_{IO1\_DRIFT\_MON}$ | IO_1 filter time   | 1.0 | – | 2.0 | ms            |  |

**Fail-safe output**

|                 |   |     |      |      |               |      |
|-----------------|---|-----|------|------|---------------|------|
| $t_{RSTB\_FB}$  | RSTB Feedback Filter Time                               | 8.0 | –    | 15   | $\mu\text{s}$ |      |
| $t_{FSOB\_FB}$  | FS0B Feedback Filter Time                               | 8.0 | –    | 15   | $\mu\text{s}$ |      |
| $t_{RSTB\_BLK}$ | RSTB Feedback Blanking Time                             | 180 | –    | 320  | $\mu\text{s}$ |      |
| $t_{FSOB\_BLK}$ | FS0B Feedback Blanking Time                             | 180 | –    | 320  | $\mu\text{s}$ |      |
| $t_{RSTB\_POR}$ | Reset Delay Time (after a Power On Reset or from LPOFF) | 12  | 15.9 | 23.6 | ms            | (29) |
| $t_{RSTB\_LG}$  | Reset Duration (long pulse)                             | 8.0 | –    | 10   | ms            |      |
| $t_{RSTB\_ST}$  | Reset duration (short pulse)                            | 1.0 | –    | 1.3  | ms            |      |
| $t_{RSTB\_IN}$  | External Reset Delay time                               | 8.0 | –    | 15   | $\mu\text{s}$ |      |
| $t_{DIAG\_SC}$  | Fail-safe Output Diagnostic Counter (FS0B)              | 550 | –    | 800  | $\mu\text{s}$ |      |

**VSUP voltage supply**

|           |                           |    |   |   |               |  |
|-----------|---------------------------|----|---|---|---------------|--|
| $C_{SUP}$ | Minimum capacitor on Vsup | 44 | – | – | $\mu\text{F}$ |  |
|-----------|---------------------------|----|---|---|---------------|--|

**Notes**

28. For proper CAN operation, TXD must be set to high level before CAN enable by SPI, and must remain high for at least  $T_{CAN\_READY}$ .
29. This timing is not guaranteed in case of fault during startup phase (after Power On Reset or from LPOFF)

**Table 5. Dynamic electrical characteristics (continued)**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Notes |
|--------|-----------|------|------|------|------|-------|
|--------|-----------|------|------|------|------|-------|

**V<sub>PRE</sub> voltage pre-regulator**

|                     |  |     |     |     |               |      |
|---------------------|--|-----|-----|-----|---------------|------|
| $f_{SW\_PRE}$       | V <sub>PRE</sub> Switching Frequency   | 418 | 440 | 462 | kHz           |      |
| $t_{SW\_PRE}$       | V <sub>SW\_PRE</sub> On and Off Switching Time                                 | –   | –   | 30  | ns            | (30) |
| $t_{PRE\_SOFT}$     | V <sub>PRE</sub> Soft Start Duration ( $C_{OUT} \leq 100\text{ }\mu\text{F}$ ) | 500 | –   | 700 | $\mu\text{s}$ |      |
| $t_{PRE\_BLK\_LIM}$ | V <sub>PRE</sub> Current Limitation Blanking Time                              | 200 | –   | 600 | ns            |      |
| $t_{IPRE\_OC}$      | V <sub>PRE</sub> Overcurrent Filtering Time                                    | 30  | –   | 120 | ns            | (30) |
| $t_{PRE\_UV}$       | V <sub>PRE</sub> Undervoltage Filtering Time                                   | 20  | –   | 40  | $\mu\text{s}$ |      |
| $t_{PRE\_UV\_4p3}$  | V <sub>PRE</sub> Shut-off Filtering Time                                       | 3.0 | –   | 6.0 | $\mu\text{s}$ |      |
| $d_{IPRE/DT}$       | V <sub>PRE</sub> Load Regulation Variation                                     | –   | –   | 25  | A/ms          | (30) |
| $t_{PRE\_WARN}$     | V <sub>PRE</sub> Thermal Warning Filtering Time                                | 30  | –   | 40  | $\mu\text{s}$ |      |
| $t_{PRE\_TSD}$      | V <sub>PRE</sub> Thermal Detection Filtering Time                              | 1.3 | –   | –   | $\mu\text{s}$ |      |
| $t_{VSUP\_IPFF}$    | I <sub>PFF</sub> Input Voltage Filtering Time                                  | 1.0 | –   | 5.0 | $\mu\text{s}$ |      |
| $t_{IPRE\_IPFF}$    | I <sub>PFF</sub> High-side Peak Current Filter Time                            | 100 | –   | 300 | ns            |      |
| $t_{LS\_RISE/FALL}$ | LS Gate Voltage Switching Time ( $I_{OUT} = 300\text{ mA}$ )                   | –   | –   | 50  | ns            |      |

**V<sub>SENSE</sub> voltage regulator**

|                |  |     |   |     |               |  |
|----------------|--|-----|---|-----|---------------|--|
| $t_{VSNS\_UV}$ | V <sub>SNS</sub> Undervoltage Filtering Time | 1.0 | – | 3.0 | $\mu\text{s}$ |  |
|----------------|--|-----|---|-----|---------------|--|

**V<sub>CORE</sub> voltage regulator**

|                      |  |      |     |      |               |  |
|----------------------|--|------|-----|------|---------------|--|
| $t_{CORE\_BLK\_LIM}$ | V <sub>CORE</sub> Current Limitation Blanking Time                     | 20   | –   | 40   | ns            |  |
| $f_{SW\_CORE}$       | V <sub>CORE</sub> Switching Frequency                                  | 2.28 | 2.4 | 2.52 | MHz           |  |
| $t_{SW\_CORE}$       | V <sub>SW\_CORE</sub> On and Off Switching Time                        | 6.0  | –   | 12   | ns            |  |
| $V_{CORE\_SOFT}$     | V <sub>CORE</sub> Soft Start ( $C_{OUT} = 100\text{ }\mu\text{F}$ max) | –    | –   | 10   | V/ms          |  |
| $t_{CORE\_WARN}$     | V <sub>CORE</sub> Thermal Warning Filtering Time                       | 30   | –   | 40   | $\mu\text{s}$ |  |
| $t_{CORE\_TSD}$      | V <sub>CORE</sub> Thermal Detection Filtering Time                     | 0.5  | –   | –    | $\mu\text{s}$ |  |

**V<sub>CCA</sub> voltage regulator**

|  |  |          |        |        |               |      |
|--|--|----------|--------|--------|---------------|------|
| $t_{CCA\_LIM}$                               | V <sub>CCA</sub> Output Current Limitation Filter Time       | 1.0      | –      | 3.0    | $\mu\text{s}$ |      |
| $t_{CCA\_LIM\_OFF1}$<br>$t_{CCA\_LIM\_OFF2}$ | V <sub>CCA</sub> Output Current Limitation Duration          | 10<br>50 | –<br>– | –<br>– | ms            |      |
| $t_{CCA\_WARN}$                              | V <sub>CCA</sub> Thermal Warning Filtering Time              | 30       | –      | 40     | $\mu\text{s}$ |      |
| $t_{CCA\_TSD}$                               | V <sub>CCA</sub> Thermal Detection Filter Time (int. MOSFET) | 1.5      | –      | –      | $\mu\text{s}$ |      |
| $dI_{LOAD}/dt$                               | V <sub>CCA</sub> Load Transient                              | –        | 2.0    | –      | A/ms          | (30) |
| $V_{CCA\_SOFT}$                              | V <sub>CCA</sub> Soft Start (5.0 V and 3.3 V)                | –        | –      | 50     | V/ms          |      |

## Notes

30. Guaranteed by characterization.

**Table 5. Dynamic electrical characteristics (continued)**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol                                       | Parameter  | Min.     | Typ.   | Max.   | Unit | Notes |
|--|--|----------|--------|--------|------|-------|
| <b>V<sub>AUX</sub> voltage regulator</b>     |  |          |        |        |      |       |
| $t_{AUX\_LIM}$                               | V <sub>AUX</sub> Output Current Limitation Filter Time   | 1.0      | –      | 3.0    | μs   |       |
| $t_{AUX\_LIM\_OFF1}$<br>$t_{AUX\_LIM\_OFF2}$ | V <sub>AUX</sub> Output Current Limitation Duration  | 10<br>50 | –<br>– | –<br>– | ms   |       |
| $t_{AUX\_TSD}$                               | V <sub>AUX</sub> Thermal Detection Filter Time   | 1.5      | –      | –      | μs   |       |
| $dI_{AUX}/dt$                                | V <sub>AUX</sub> Load Transient  | –        | 2.0    | –      | A/ms | (31)  |
| $V_{AUX\_SOFT}$                              | V <sub>AUX</sub> Soft Start (5.0 V and 3.3 V)  | –        | –      | 50     | V/ms |       |
| <b>CAN<sub>5V</sub> voltage regulator</b>    |  |          |        |        |      |       |
| $t_{CAN\_LIM}$                               | Output Current Limitation Filter Time  | 2.0      | –      | 4.0    | μs   |       |
| $t_{CAN\_TSD}$                               | V <sub>CAN</sub> Thermal Detection Filter Time   | 1.0      | –      | –      | μs   |       |
| $t_{CAN\_UV}$                                | V <sub>CAN</sub> Undervoltage Filtering Time   | 4.0      | –      | 7.0    | μs   |       |
| $t_{CAN\_OV}$                                | V <sub>CAN</sub> Overvoltage Filtering Time  | 100      | –      | 200    | μs   |       |
| $dI_{CAN}/dt$                                | V <sub>CAN</sub> Load Transient  | –        | 100    | –      | A/ms | (31)  |
| <b>Fail-safe machine voltage supervisor</b>  |  |          |        |        |      |       |
| $t_{PRE\_OV}$                                | V <sub>PRE</sub> Overvoltage Filtering Time  | 128      | –      | 234    | μs   |       |
| $t_{CORE\_UV}$                               | V <sub>CORE</sub> FB Undervoltage Filtering Time   | 4.0      | –      | 10     | μs   |       |
| $t_{CORE\_OV}$                               | V <sub>CORE</sub> FB Overvoltage Filtering Time  | 128      | –      | 234    | μs   |       |
| $t_{CCA\_UV}$                                | V <sub>CCA</sub> Undervoltage Filtering Time   | 4.0      | –      | 10     | μs   |       |
| $t_{CCA\_OV}$                                | V <sub>CCA</sub> Overvoltage Filtering Time  | 128      | –      | 234    | μs   |       |
| $t_{AUX\_UV}$                                | V <sub>AUX</sub> Undervoltage Filtering Time   | 4.0      | –      | 10     | μs   |       |
| $t_{AUX\_OV}$                                | V <sub>AUX</sub> Overvoltage Filtering Time  | 128      | –      | 234    | μs   |       |
| <b>Digital input - multi-purpose ios</b>     |  |          |        |        |      |       |
| $F_{IO\_IN}$                                 | Digital Input Frequency Range  | 0.0      | –      | 100    | kHz  |       |
| <b>Analog multiplexer</b>                    |  |          |        |        |      |       |
| $t_{MUX\_READY}$                             | SPI Selection to Data Ready to be Sampled on Mux_out<br>• $V_{DDIO} = 5.0\text{ V}$ , $C_{MUX\_OUT} = 1.0\text{ nF}$ | –        | –      | 10     | μs   |       |
| <b>Interrupt</b>                             |  |          |        |        |      |       |
| $t_{INTB\_LG}$                               | INTB Pulse Duration (long)   | 90       | 100    | –      | μs   |       |
| $t_{INTB\_ST}$                               | INTB Pulse Duration (short)  | 20       | 25     | –      | μs   |       |
| <b>Functional sate machine</b>               |  |          |        |        |      |       |
| $t_{WU\_GEN}$                                | General Wake-up Signal Deglitch Time (for any wu signal on IOs)  | 60       | 70     | 80     | μs   |       |

**Notes**

31. Guaranteed by characterization.



**Table 5. Dynamic electrical characteristics (continued)**

$T_{CASE} = -40\text{ }^{\circ}\text{C}$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.  $V_{SUP} = V_{SUP\_UV\_L}$  to 40 V, unless otherwise specified. All voltages referenced to ground. When  $28\text{ V} < V_{SUP} < 40\text{ V}$ , thermal dissipation must be considered (Figure 25).

| Symbol   | Parameter  | Min.  | Typ. | Max.  | Unit          | Notes |
|--|--|-------|------|-------|---------------|-------|
| <b>LIN dynamic characteristics (when <math>7.0\text{ V} &lt; V_{sup1, 2, 3} &lt; 18\text{ V}</math>, unless otherwise specified) (33907L/33908L)</b> |  |       |      |       |               |       |
| $t_{RX\_PD}$   | Receiver Propagation Delay ( $T_{RX\_PD} = \text{MAX}(t_{REC\_PDR}, t_{REC\_PDF})$ )   | –     | –    | 6.0   | $\mu\text{s}$ |       |
| $t_{RX\_SYM}$  | Symmetry of Receiver Propagation Delay ( $T_{RX\_SYM} = t_{REC\_PDF} - t_{REC\_PDR}$ )   | -2.0  | –    | 2.0   | $\mu\text{s}$ |       |
| $t_{BUS\_WU}$  | BUS Wake-up Filter Time  | –     | –    | 250   | $\mu\text{s}$ |       |
| $t_{XD\_DOM}$  | TXD_L Permanent Dominant State Delay   | –     | 5.0  | –     | ms            |       |
| $t_{LIN\_SHORT\_GND}$  | LIN Short-circuit to GND Deglitcher  | –     | 15   | –     | ms            |       |
| $BD_{FAST}$  | Fast Baud Rate   | –     | –    | 100   | KB/s          |       |
| D1   | Duty Cycle D1<br>$TH_{REC}(\text{max}) = 0.744 \times V_{SUP}$ , $TH_{DOM}(\text{max}) = 0.581 \times V_{SUP}$<br>$V_{SUP} 7.0\text{ V to }18\text{ V}$ , $t_{BIT} = 50\text{ }\mu\text{s}$<br>$D1 = t_{BUS-rec}(\text{min})/(2t_{BIT})$ | 0.396 | –    | –     | %             | (32)  |
| D2   | Duty Cycle D2<br>$TH_{REC}(\text{min}) = 0.422 \times V_{SUP}$ , $TH_{DOM}(\text{min}) = 0.284 \times V_{SUP}$<br>$V_{SUP} 7.6\text{ V to }18\text{ V}$ , $t_{BIT} = 50\text{ }\mu\text{s}$<br>$D2 = t_{BUS-rec}(\text{max})/(2t_{BIT})$ | –     | –    | 0.581 | %             | (32)  |
| D3   | Duty Cycle D3<br>$TH_{REC}(\text{max}) = 0.778 \times V_{SUP}$ , $TH_{DOM}(\text{max}) = 0.616 \times V_{SUP}$<br>$V_{SUP} 7.0\text{ V to }18\text{ V}$ , $t_{BIT} = 96\text{ }\mu\text{s}$<br>$D3 = t_{BUS-rec}(\text{min})/(2t_{BIT})$ | 0.417 | –    | –     | %             | (32)  |
| D4   | Duty Cycle D4<br>$TH_{REC}(\text{min}) = 0.389 \times V_{SUP}$ , $TH_{DOM}(\text{min}) = 0.251 \times V_{SUP}$<br>$V_{SUP} 7.6\text{ V to }18\text{ V}$ , $t_{BIT} = 96\text{ }\mu\text{s}$<br>$D4 = t_{BUS-rec}(\text{max})/(2t_{BIT})$ | –     | –    | 0.59  | %             | (32)  |

**Notes**

32. LIN Driver, Bus load conditions (CBUS,RBUS): 1.0 nF;1.0 k $\Omega$  / 6.8 nF;660  $\Omega$  / 10 nF;500  $\Omega$

## 5 Functional pin description

### 5.1 Introduction

The 33907/33908 is the third generation of the System Basis Chip, combining:

- High efficiency switching voltage regulator for MCU, and linear voltage regulators for integrated CAN interface, external ICs such as sensors, and accurate reference voltage for A to D converters.
- Built-in enhanced high-speed CAN interface (ISO11898-2 and -5), and LIN interface (LIN up to Rev. 2.2/ SAEJ2602-2), with local and bus failure diagnostic, protection, and Fail-safe operation mode.
- Low-power mode, with ultra low-current consumption.
- Various wake-up capabilities.
- Enhanced safety features with multiple fail-safe outputs and scheme to support ASIL D applications.

### 5.2 Power supplies (VSUP1, VSUP2, VSUP3)

VSUP1 and VSUP2 are the inputs pins for internal supply dedicated to SMPS regulators. VSUP3 is the input pin for internal voltage reference. VSUP1, 2, and 3 are robust against ISO7637 pulses.

VSUP1,2, and 3 shall be connected to the same supply ([Figure 58](#)).

### 5.3 Vsense input (VSENSE)

This pin must be connected to the battery line (before the reverse battery protection diode), via a serial resistor. It incorporates a threshold detector to sense the battery voltage, and provide a battery early warning. It also includes a resistor divider to measure the VSENSE voltage via the MUX-OUT pin. VSENSE pin is robust against ISO7637 pulses.

### 5.4 Pre-regulator (VPRE)

A highly flexible SMPS pre-regulator is implemented in the 33907/33908. It can be configured as a “non-inverting buck-boost converter” ([Figure 27](#)) or “standard buck converter” ([Figure 26](#)), depending on the external configuration (connection of pin GATE\_LS). The configuration is detected automatically during start-up sequence.

The SMPS pre-regulator is working in current mode control and the compensation network is fully integrated in the device. The high-side switching MOSFET is also integrated to make the current control easier. The pre-regulator delivers a typical output voltage of 6.5 V, which is used internally. Current limitation, overcurrent, overvoltage, and undervoltage detectors are provided. VPRE is enabled by default.

### 5.5 VCORE Output (from 1.2 V to 3.3 V range)

The VCORE block is an SMPS regulator. The voltage regulator is a step down DC-DC converter operating in voltage control mode. The output voltage is configurable from 1.2 V to 3.3 V range thanks to an external resistor divider connected between VCORE and the feedback pin (FB\_CORE) (as example in [Figure 1](#), [Figure 2](#), and [Figure 58](#)).

The stability of the converter is done externally, by using the COMP\_CORE pin. Current limitation, overvoltage, and undervoltage detectors are provided. VCORE can be turned ON or OFF via a SPI command, however it is not recommended to turn OFF VCORE by SPI when VCORE is configured safety critical (both overvoltage and undervoltage have an impact on RSTB and FS0B). VCORE overvoltage information disables VCORE. Diagnostics are reported in the dedicated register and generate an Interrupt. VCORE is enabled by default.

## 5.6 VCCA output, 5.0 V or 3.3 V selectable

The VCCA voltage regulator is used to provide an accurate voltage output (5.0 V, 3.3 V) selectable through an external resistor connected to the SELECT pin.

The VCCA output voltage regulator can be configured using an internal transistor delivering very good accuracy ( $\pm 1.0\%$  for 5.0 V configuration and  $\pm 1.5\%$  for 3.3 V configuration), with a limited current capability (100 mA) for an analog to digital converter, or with an external PNP transistor, giving higher current capability (up to 300 mA) with lower output voltage accuracy ( $\pm 3.0\%$  for 300 mA) when using a local ECU supply.

Current limitation, overvoltage, and undervoltage detectors are provided. VCCA can be turned ON or OFF via a SPI command, however it is not recommended to turn OFF VCCA by SPI when VCCA is configured safety critical (both overvoltage and undervoltage have an impact on RSTB and FS0B). VCCA overcurrent (with the use of external PNP only) and overvoltage information disables VCCA. Diagnostics are reported in the dedicated register and generate an Interrupt. VCCA is enabled by default.

## 5.7 VAUX output, 5.0 V or 3.3 V selectable

The VAUX pin provides an auxiliary output voltage (5.0 V, 3.3 V) selectable through an external resistor connected to SELECT pin. It uses an external PNP ballast transistor for flexibility and power dissipation constraints. The VAUX output voltage regulator can be used as “auxiliary supply” (local ECU supply) or “sensor supply” (external ECU supply) with the possibility to be configured as a tracking regulator following VCCA.

Current limitation, overvoltage, and undervoltage detectors are provided. VAUX can be turned ON or OFF via a SPI command, however it is not recommended to turn OFF VAUX by SPI when VAUX is configured safety critical (both overvoltage and undervoltage have an impact on RSTB and FS0B). VAUX overcurrent and overvoltage information disables  $V_{AUX}$ , reported in the dedicated register, and generates an Interrupt.  $V_{AUX}$  is enabled by default.

## 5.8 SELECT Input (VCCA, VAUX voltage configuration)

VCCA and VAUX output voltage configurations are set by connecting an external resistor between SELECT pin and Ground. According to the value of this resistor, the voltage of VCCA and VAUX are configured after each Power On Reset, and after a wake-up event when device is in LPOFF. Information latches until the next hardware configuration read. Regulator voltage values can be read on the dedicated register via the SPI.

**Table 6.  $V_{CCA}/V_{AUX}$  Voltage Selection** ([Figure 59](#))

| $V_{CCA}(V)$ | $V_{AUX}(V)$ | R Select                      | Recommended value              |
|--------------|--------------|-------------------------------|--------------------------------|
| 3.3          | 3.3          | $<7.0\text{ K}\Omega$         | $5.1\text{ K}\Omega \pm 5.0\%$ |
| 5.0          | 5.0          | $10.8 << 13.2\text{ K}\Omega$ | $12\text{ K}\Omega \pm 5.0\%$  |
| 3.3          | 5.0          | $21.6 << 26.2\text{ K}\Omega$ | $24\text{ K}\Omega \pm 5.0\%$  |
| 5.0          | 3.3          | $45.9 << 56.1\text{ K}\Omega$ | $51\text{ K}\Omega \pm 5.0\%$  |

When VAUX is not used, the output VCCA voltage configuration is set using an external resistor connected between the SELECT and the VPRES pin.

**Table 7.  $V_{CCA}$  Voltage Selection ( $V_{AUX}$  not used, [Figure 60](#), [Figure 61](#))**

| $V_{CCA}(V)$ | R Select                      | Recommended Value              |
|--------------|-------------------------------|--------------------------------|
| 3.3          | $<7.0\text{ K}\Omega$         | $5.1\text{ K}\Omega \pm 5.0\%$ |
|              | $21.6 << 26.2\text{ K}\Omega$ | $24\text{ K}\Omega \pm 5.0\%$  |
| 5.0          | $10.8 << 13.2\text{ K}\Omega$ | $12\text{ K}\Omega \pm 5.0\%$  |
|              | $45.9 << 56.1\text{ K}\Omega$ | $51\text{ K}\Omega \pm 5.0\%$  |

## 5.9 CAN\_5V voltage regulator

The CAN\_5V voltage regulator is a linear regulator dedicated to the internal HSCAN interface. An external capacitor is required. Current limitation, overvoltage, and undervoltage detectors are provided. If the internal CAN transceiver is not used, the CAN\_5V regulator can supply an external load ([CAN\\_5V voltage regulator](#)). CAN\_5V is enabled by default.

## 5.10 INTERRUPT (INTB)

The INTB output pin generates a low pulse when an Interrupt condition occurs. The INTB behavior as well as the pulse duration are set through the SPI during INIT phase. INTB has an internal pull-up resistor connected to VDDIO.

## 5.11 CANH, CANL, TXD, RXD

These are the pins of the high speed CAN physical interface. The CAN transceivers provides the physical interface between the CAN protocol controller of an MCU and the physical dual wires CAN bus. The CAN interface is connected to the MCU via the RXD and TXD pins.

### 5.11.1 TXD

TXD is the device input pin to control the CAN bus level. TXD is a digital input with an internal pull-up resistor connected to VDDIO. In the application, this pin is connected to the microcontroller transmit pin.

In Normal mode, when TXD is high or floating, the CANH and CANL drivers are OFF, setting the bus in a recessive state. When TXD is low, the CANH and CANL drivers are activated and the bus is set to a dominant state. TXD has a built-in timing protection that disables the bus when TXD is dominant for more than  $T_{\text{DOU}}T$ . In LPOFF mode, VDDIO is OFF, pulling down this pin to GND.

### 5.11.2 RXD

RXD is the bus output level report pin. In the application, this pin is connected to the microcontroller receive pin. In Normal mode, RXD is a push-pull structure. When the bus is in a recessive state, RXD is high. When the bus is dominant, RXD is low. In LPOFF mode, this pin is in high-impedance state.

### 5.11.3 CANH and CANL

These are the CAN bus pins. CANL is a low side driver to GND, and CANH is a high side driver to CAN\_5V. In Normal mode and TXD high, the CANH and CANL drivers are OFF, and the voltage at CANH and CANL is approximately 2.5 V, provided by the internal bus biasing circuitry. When TXD is low, CANL is pulled to GND and CANH to CAN\_5V, creating a differential voltage on the CAN bus.

In LPOFF mode, the CANH and CANL drivers are OFF, and these pins are pulled down to GND via the device  $R_{\text{IN\_CHCL}}$  resistors. CANH and CANL have integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients. These pins have current limitation and thermal protection.

## 5.12 LIN, TXDL, RXDL

These pins apply to 33907L and 33908L versions.

These are the pins of the LIN physical interface. The LIN transceivers provides the physical interface between the MCU and the physical single wire LIN bus. The LIN interface is connected to the MCU via the RXDL and TXDL pins.

### 5.12.1 TXDL

The TXDL input pin is the MCU interface to control the state of the LIN output. TXDL is a digital input with an internal pull-up resistor connected to VDDIO. In the application, this pin is connected to the microcontroller transmit pin.

In Normal mode, when TXDL is high or floating, the LIN output transistor is OFF, setting the bus in recessive state. When TXDL is low, the LIN output transistor is ON and the bus is set to a dominant state. TXDL has a built-in timing protection that disables the bus when TXDL is dominant for more than  $T_{XD\_DOM}$ . In LPOFF mode, VDDIO is OFF, pulling down this pin to GND.

### 5.12.2 RXDL

RXDL is the bus output level report pin. In the application, this pin is connected to the microcontroller receive pin. In Normal mode, RXD is a push-pull structure. When the bus is in a recessive state, RXD is high. When the bus is dominant, RXD is low. In LPOFF mode, this pin is in high-impedance state.

### 5.12.3 LIN

This is the LIN bus pin. The LIN driver is a low-side MOSFET with internal overcurrent thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated so no external pull-up components are required for the application in a slave node. An additional pull-up resistor of 1.0 k $\Omega$  must be added when the device is used in the master node. In Normal mode and TXDL high, the LIN transistor is OFF, and the voltage at LIN is approximately VSUP3, provided by the pull up resistor with a serial diode structure. When TXD is low, LIN is pulled to GND.

The device has two selectable baud rates: 20 kBits/s for Normal Baud rate and 10 kBits/s for slow baud rate. An additional fast baud rate (100 kBits/s) is implemented. It can be used to flash the MCU or in the garage for diagnostic. The LIN Consortium specification does not specify electrical parameters for this baud rate. The communication only must be guaranteed. In LPOFF mode, the LIN transistor is OFF, and this pin is pulled up to VSUP3. LIN has integrated ESD protection and extremely high robustness versus external disturbance, such as EMC and electrical transients.

## 5.13 Multiplexer output MUX\_OUT

The MUX\_OUT pin ([Figure 9](#)) delivers analog voltage to the MCU ADC input. The voltage to be delivered to MUX\_OUT is selected via the SPI, from one of the following parameters:

- VSENSE
  - VIO\_0
  - VIO\_1
  - Internal 2.5 V reference
  - Die temperature sensor  $T(^{\circ}\text{C}) = (V_{AMUX} - V_{AMUX\_TP}) / V_{AMUX\_TP\_CO} + 165$
- Voltage range at MUX\_OUT is from GND to VDDIO (3.3 V or 5.0 V)

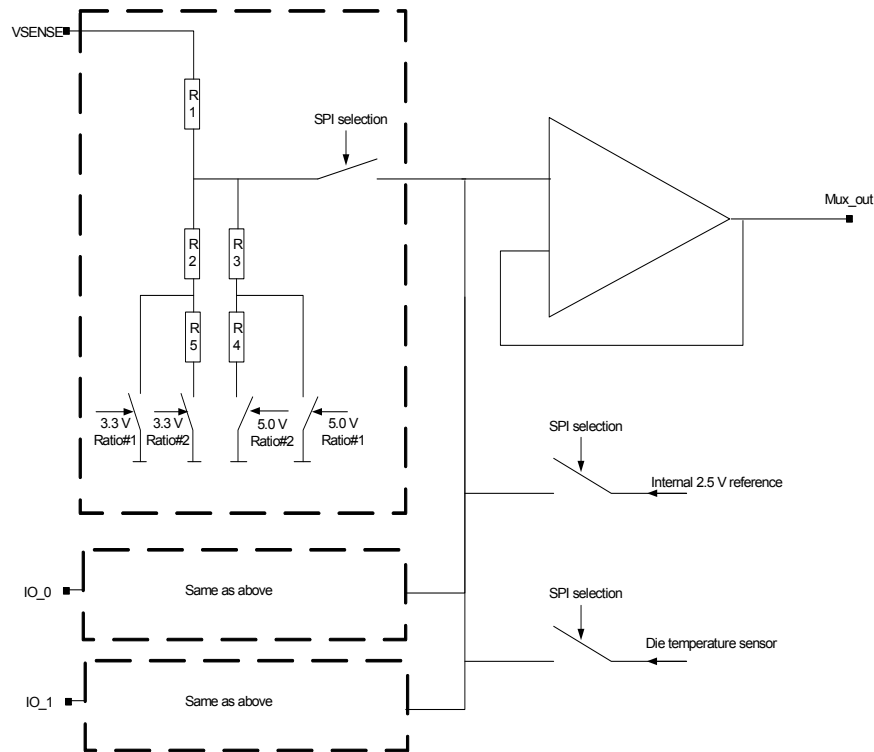


Figure 9. Simplified analog multiplexer block diagram

## 5.14 I/O pins (I/O\_0:I/O\_5)

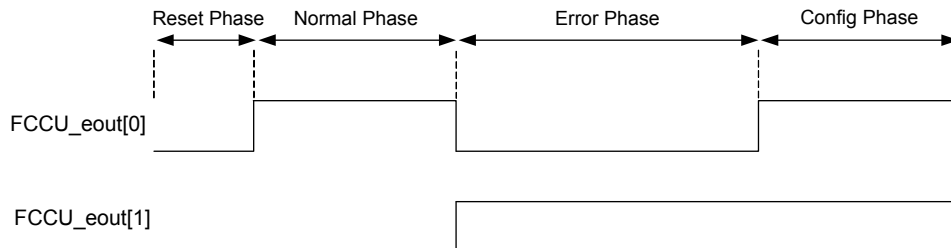
The 33907/33908 includes six multi-purpose I/Os (I/O\_0 to I/O\_5). I/O\_0, I/O\_1, I/O\_4, and I/O\_5 are load dump proof and robust against ISO7637 pulses. An external serial resistor must be connected to those pins to limit the current during ISO pulses. I/O\_2 and I/O\_3 are not load dump proof.

Table 8. I/Os configuration

| I/O number | Analog input | Digital input | Wake-up capability | Output gate driver |
|------------|--------------|---------------|--------------------|--------------------|
| IO_0       | X            | X             | X                  |                    |
| IO_1       | X            | X             | X                  |                    |
| IO_2       |              | X             | X                  |                    |
| IO_3       |              | X             | X                  |                    |
| IO_4       |              | X             | X                  | X                  |
| IO_5       |              | X             | X                  | X                  |

- IO\_0:1 are selectable as follows:  
Analog input (load dump proof) sent to the MCU through the MUX\_OUT pin. Wake-up input on the rising or falling edge or based on the previous state. Digital input (logic level) sent to the MCU through the SPI. **Safety purpose:** Digital input (logic level) to perform an IC error monitoring (both IO\_0 AND IO\_1 are used if configured as safety inputs, see [Figure 11](#)).
- IO\_1 is also selectable as follow:  
Safety purpose: FB\_Core using a second resistor bridge (R3/R4 duplicated) connected to IO\_1, to detect external resistor drift and trigger when  $FB\_Core - IO\_1 > \pm 150 \text{ mV max.}$
- IO\_2:3 are selectable as follows:  
Digital input (logic level) sent to the MCU through the SPI. Wake-up input (logic level) on the rising or falling edge or based on the previous state. **Safety purpose:** Digital input (logic level) to monitor MCU error signals (both IO\_2 AND IO\_3 are used if configured as safety inputs). Only bi-stable protocol is available.

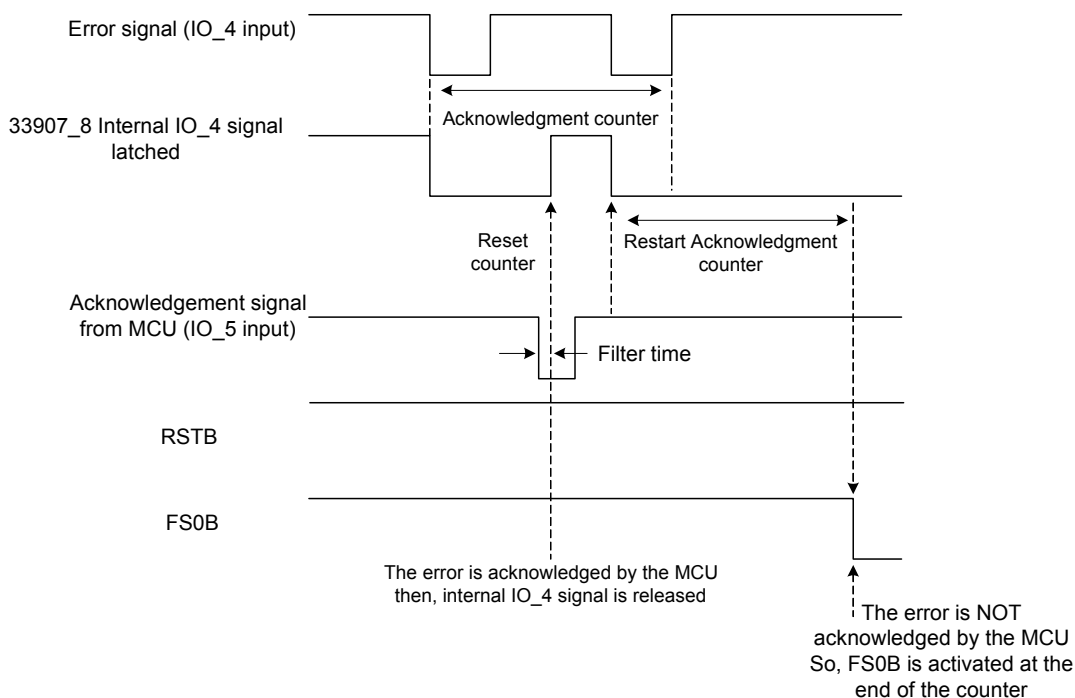
When IO\_2:3 are used as safety inputs to monitor FCCU error outputs from the NXP MCU, the monitoring is active only when the Fail-safe state machine is in “normal WD running” state ([Figure 14](#)) and all the phases except the “Normal Phase” are considered as an Error.



**Figure 10. IO\_2:3 MCU error monitoring: bi-stable protocol**

- IO\_4:5 are selectable as follows:

Digital input (logic level) sent to the MCU through the SPI. Wake-up input (load dump proof) on rising or falling edge or based on previous state. Output gate driver (from  $V_{PRE}$ ) for low-side logic level MOSFET. **Safety purpose:** Digital input (logic level) to perform an IC error monitoring (both IO\_4 AND IO\_5 are used if configured as safety inputs, see [Figure 11](#)).



**Figure 11. External error signal handling**

## 5.15 SAFE output pins (FS0B, RSTB)

FS0B is asserted low when a fault event occurs ([See Faults triggering FS0B activation on page 45](#)). The objective of this pin is to drive an electrical safe circuitry independent from MCU to deactivate the whole system and set the ECU in a protected and known state.

After each power on reset or after each wake-up event (LPOFF) the FS0B pin is asserted low. Then the MCU can decide to release the FS0B pin, when the application is ready to start. An external pull-up circuitry is mandatory connected to VDDIO or VSUP3.

- If the pull-up is connected to VDDIO, the value recommended is 5.0kΩ, there will be no current in LPOFF since VDDIO is OFF in LPOFF mode.
- If the pull-up is connected to VSUP3, the value must be above 10 kΩ, there will be a current in the pull-up resistor to consider at application level in LPOFF mode.

The RSTB pin must be connected to MCU and is active low. An external pull-up resistor must be connected to VDDIO. In default configuration, the RST delay time has three possible values depending on the mode and product configuration:

- The longest one is used automatically following a Power On Reset or when resulting from LPOFF mode (Low Power Off).
- The two reset durations are then available in the INIT\_FSSM1 register, which are 1.0 ms and 10 ms. The configured duration is finally used in the normal operation when a fault occurs leading to a reset activation. The INIT\_FSSM1 register is available (writing) in the INIT FS phase.

## 5.16 DEBUG input (entering in debug mode)

The DEBUG pin allows the product to enter Debug mode. To activate the Debug mode, voltage applied to the DEBUG pin must be within the  $V_{\text{DEBUG\_IL}}$  and  $V_{\text{DEBUG\_IH}}$  range at start-up. If the voltage applied to DEBUG pin is out of these limits, before  $V_{\text{CORE}}$  ramp-up, the device settles into Normal mode. When the Debug mode is activated, the FS0B output is asserted low at start-up. As soon as the FS0B is released to “high” via SPI (Good WD answer and FS\_OUT writing) this pin is never activated whatever the fault is reported.

In Debug mode, any errors from watchdog are ignored (No reset and No fail-safe), even if the whole functionality of the watchdog is kept ON (Seed, LFSR, Wd\_refresh counter, WD error counter). This allows an easy debug of the hardware and software routines (i.e. SPI commands). When the Debug mode is activated, the CAN transceiver is set to Normal operation mode. This allows communication with the MCU, in case SPI communication is not available (case of MCU not programmed). To exit Debug mode, the pin must be tied to Ground through an external pull-down resistor or to VPRES through an external pull-up resistor and a Power On Reset occurs.



## 6 Functional device operation

### 6.1 Mode and state description of main state machine

The device has several operation modes. The transition and conditions to enter or leave each mode are illustrated in the functional state diagram ([Figure 13](#)). Two state machines are working in parallel. The Main state machine is in charge of the power management (VPRE, VCORE, VCCA, VAUX,...) and the fail-safe state machine is in charge of all the safety aspect (WD, RSTB, FS0B,...).

#### 6.1.1 Buck or buck boost configuration

An external low side logic level MOSFET (N-type) is required to operate in non-inverting buck-boost converter. The connection of the external MOSFET is detected automatically during the start-up phase (after a Power On Reset or From LPOFF).

- If the external low-side MOSFET is NOT connected (GATE\_LS pin connected to PGND), the product is configured as a standard buck converter.
- If the external low-side MOSFET is connected (GATE\_LS pin connected to external MOSFET gate), the product is configured as a non-inverting buck-boost converter.

The automatic detection is done by pushing 300  $\mu$ A current on Gate\_LS pin and monitoring the corresponding voltage generated. If a voltage  $>120$  mV is detected before the 120  $\mu$ s timeout, the non-inverting buck-boost configuration is locked. Otherwise, the standard buck configuration is locked. The boost driver has a current capability of  $\pm 300$  mA.

#### 6.1.2 VPRE on

Pre-regulator is an SMPS regulator. In this phase, the pre-regulator is switched ON and a softstart with a specified duration  $t_{\text{PRE\_SOFT}}$  is started to control the VPRE output capacitor charge.

#### 6.1.3 Select pin configuration

This phase is detecting the required voltage level on VAUX and VCCA, according to resistor value connected between the SELECT pin and ground. If the SELECT pin is connected to VPRE via the resistor, it disables the VAUX regulator at start-up.

#### 6.1.4 VCORE/VAUX/VCCA on

In this stage, the three regulators VCORE, VAUX, VCCA are switched ON at the same time with a specified soft start duration. The CAN\_5V is also started at that time.

#### 6.1.5 INIT main

This mode is automatically entered after the device is "Powered ON". When RSTB is released, initialization phase starts where the device can be configured via the SPI. During INIT phase, some registers can only be configured in this mode (refer to [Table 15](#) and [Table 16](#)). Other registers can be written in this mode, and also in Normal mode.

Once the INIT registers configurations are complete, a last register called "INIT INT" must be configured to switch to Normal mode. Writing data in this register (even same default values), automatically locks the INIT registers, and the product switches automatically to Normal mode in the Main state machine.

#### 6.1.6 Normal

In this mode, all device functions are available. This mode is entered by a SPI command from the INIT phase by writing in the INIT INT register. While in Normal mode, the device can be set to Low Power mode (LPOFF) using secured SPI command.

## 6.1.7 Low power mode off

The Main State Machine has 3 LPOFF modes with different conditions to enter and exit each LPOFF mode as described here after. After wake up from LPOFF, all the regulators are enabled by default. In LPOFF, all the regulators are switched OFF. The register configuration, the Vpre behavior and the ISO pulse requirement are valid for the 3 LPOFF modes.

### 6.1.7.1 LPOFF - sleep

Entering in Low Power mode LPOFF - SLEEP is only available if the product is in Normal mode by sending a secured SPI command. In this mode, all the regulators are turned OFF and the MCU connected to the VCore regulator is unsupplied.

Before entering in LPOFF Power mode OFF-sleep, the Reset Error Counter must go back to value "0" ("N" consecutive good watchdog refresh decreases the reset error counter to 0). "N" = RSTb\_err\_2:0 x (WD\_refresh\_2:0 + 1). Once the 33907/33908 is in LPOFF - SLEEP, the device monitors external events to wake-up and leave the Low Power mode. The wake-up events can occur and depending of the device configuration from:

- CAN
- LIN
- I/O inputs

When a wake-up event is detected, the device starts the main state machine again by detecting the VPRES configuration (BUCK or BUCK-BOOST), the wake-up source is reported to the dedicated SPI register, and the Fail-safe state machine is also restarted.

### 6.1.7.2 LPOFF - V<sub>PRE\_UV</sub>

LPOFF- V<sub>PRE\_UV</sub> is entered when the device is in the INIT or Normal mode, and if the VPRES voltage level is passing the V<sub>PRE\_UV\_L\_4P3</sub> threshold (typ 4.3 V). After 1.0 ms the device attempts to recover by switching ON the VPRES again.

### 6.1.7.3 LPOFF - deep FS

LPOFF - DEEP FS is entered when the device is in Deep Fail-safe and if the Key is OFF (IO\_0 is low). To exit this mode, a transition to high level on IO\_0 is required. IO\_0 is usually connected to key ON key OFF signal.

### 6.1.7.4 Register configuration in LPOFF

In LPOFF, the register settings of the Main State Machine are kept because the internal 2.5 V main digital regulator is available for wake-up operation. However, the register settings of the Fail-safe state machine are erased because the 2.5 V fail safe digital regulator is not available in LPOFF. As a consequence, after a wake-up event, the configuration of the Fail-safe registers must be done again during initialization phase (256 ms open window).

### 6.1.7.5 V<sub>PRE</sub> behavior in LPOFF

When device is in LPOFF Sleep mode, and if the  $V_{SUP} < V_{SUP\_UV\_7}$ , VPRES is switched on to maintain internal biasing and wake-up capabilities on IOs, CAN or LIN.

- If V<sub>PRE</sub> is configured as a non-inverting buck-boost converter, VPRES is switched ON in SMPS mode with boost functionality.
- If V<sub>PRE</sub> is configured as a standard buck converter, VPRES is switched ON in Linear mode following V<sub>SUP</sub>.

### 6.1.7.6 ISO pulse in LPOFF

If the application has to sustain ISO pulses on V<sub>BAT</sub> in LPOFF mode, the connection of an external zener diode and a serial resistor to the ground is mandatory (see [Figure 12](#)). During repetitive ISO pulses on Vbat, the capacitors connected on V<sub>SUP</sub> line are more and more charged and cannot be discharged thanks to the extremely low-current needed to maintain wake-up capabilities on IOs, CAN, and LIN.

As a consequence, if a leakage path is not created artificially with those discrete components the voltage on V<sub>SUP</sub> line can exceed the absolute maximum rating supported by this pin.

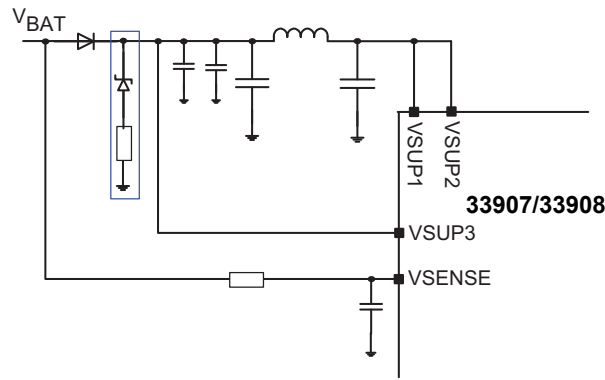


Figure 12. Components involved under ISO pulse in LPOFF

## 6.2 Mode and state description of fail-safe state machine

### 6.2.1 LBIST

Included in the fail-safe machine, the Logic Built-in Self Test (LBIST) verifies the correct functionality of the FSSM at start-up. The fail-safe state machine is fully checked and if an issue is reported, the RSTB stays low and after 8 s, the device enters in DEEP Fail-safe. LBIST is run at start-up and after each wake-up event when the device is in LPOFF mode.

### 6.2.2 Select pin configuration

This phase detects the required voltage level to apply on VAUX and VCCA, according to the resistor value connected between the SELECT pin and ground, ( $V_{AUX}$  used) or between the SELECT pin and VPRE ( $V_{AUX}$  not used). This mode is the equivalent mode seen in the main state machine. Difference is in the fail-safe machine, this detection is used to internally set the UV/OV threshold on VCCA and VAUX for the voltage supervision.

### 6.2.3 ABIST

Included in the fail-safe machine, the Analog Built-in Self Test (ABIST) verifies the correct functionality of the analog part of the device, like the overvoltage and undervoltage detections of the voltage supervisor and the RTSTB and FS0B fail-safe outputs feedback (Table 9). The ABIST is run at start-up and after each wake-up event when device is in LPOFF mode.

Table 9. Regulators and fail-safe pins checked during ABIST

| Parameters         | Overvoltage | Undervoltage | OK/NOK |
|--------------------|-------------|--------------|--------|
| VPRE               | X           |              |        |
| VCORE              | X           | X            |        |
| VCCA               | X           | X            |        |
| VAUX               | X           | X            |        |
| IO_1 FB_Core Delta |             |              | X      |
| RSTB               |             |              | X      |
| FS0B               |             |              | X      |

### 6.2.4 Release RSTB

In this state, the device releases the RSTB pin.

## 6.2.5 INIT FS

This mode is automatically entered after the device is “powered on” and only if Built-in Self Tests (Logic and Analog) have been passed successfully. This INIT FS mode starts as soon as RSTB is released (means no “Activate RST” faults are present and no external reset is requested). Faults leading to an “Activate RST” are described in [Reset error counter](#).

In this mode, the device can be configured via the SPI within a maximum time of 256 ms, including first watchdog refresh. Some registers can only be configured in this mode and is locked when leaving INIT FS mode (refer to [Table 15](#) and [Table 16](#)). It is recommended, to configure first the device before sending the first WD refresh. As soon as the first good watchdog refresh is sent by the MCU, the device leaves this mode and goes into Normal WD mode.

## 6.2.6 Normal WD is running

In this mode, the device waits for a periodic watchdog refresh coming from the MCU, within a specific configured window timing. Configuration of the watchdog window period can be set during INIT FS phase or in this mode. This mode is exited if there are consecutive bad watchdog refreshes if there is an external reset request, or if a fault occurs leading to a RSTB activation.

## 6.2.7 RST delay

When the reset pin is asserted low by the device, a delay runs, to release the RSTB, if there are no faults present. The reset low duration time is configurable via the SPI in the INIT\_ FSSM1 register, which is accessible for writing only in the INIT FS phase.

## 6.3 Deep fail safe state

The Fail-safe state machine monitors the RSTB pin of the device and count the number of reset(s) happening in case of fault detection (see [Reset error counter](#)). As soon as either the Reset Error Counter reach its final value or the RESET pin remains asserted low for more than 8.0 s, the device moves to Deep Fail-safe state, identified by the “Wait Deep Fail-safe” state in the functional state diagram ([Figure 13](#)).

When the device is in Deep Fail-safe state, all the regulators are OFF. To exit this state, a Key OFF / Key ON action is needed. IO\_0 is usually connected to key signal. Key OFF (IO\_0 low) will move the device to LPOFF-Deep FS, and Key ON (IO\_0 high) will wake-up the device.

The final value of the Reset Error Counter can be configured to 2 or 6 in the register INIT FSSM 2. During power up phase, the 8.0 s timer starts when the Fail-safe state machine enters in the “Select pin config detection” state and stop when the RSTB pin is released. During “INIT FS” state, the 8.0 s timer can be disabled in the register INIT SUPERVISOR 2. During “Normal WD running” state, the 8.0 s timer is activated at each RSTB pin assertion.

## 6.4 Functional state diagram

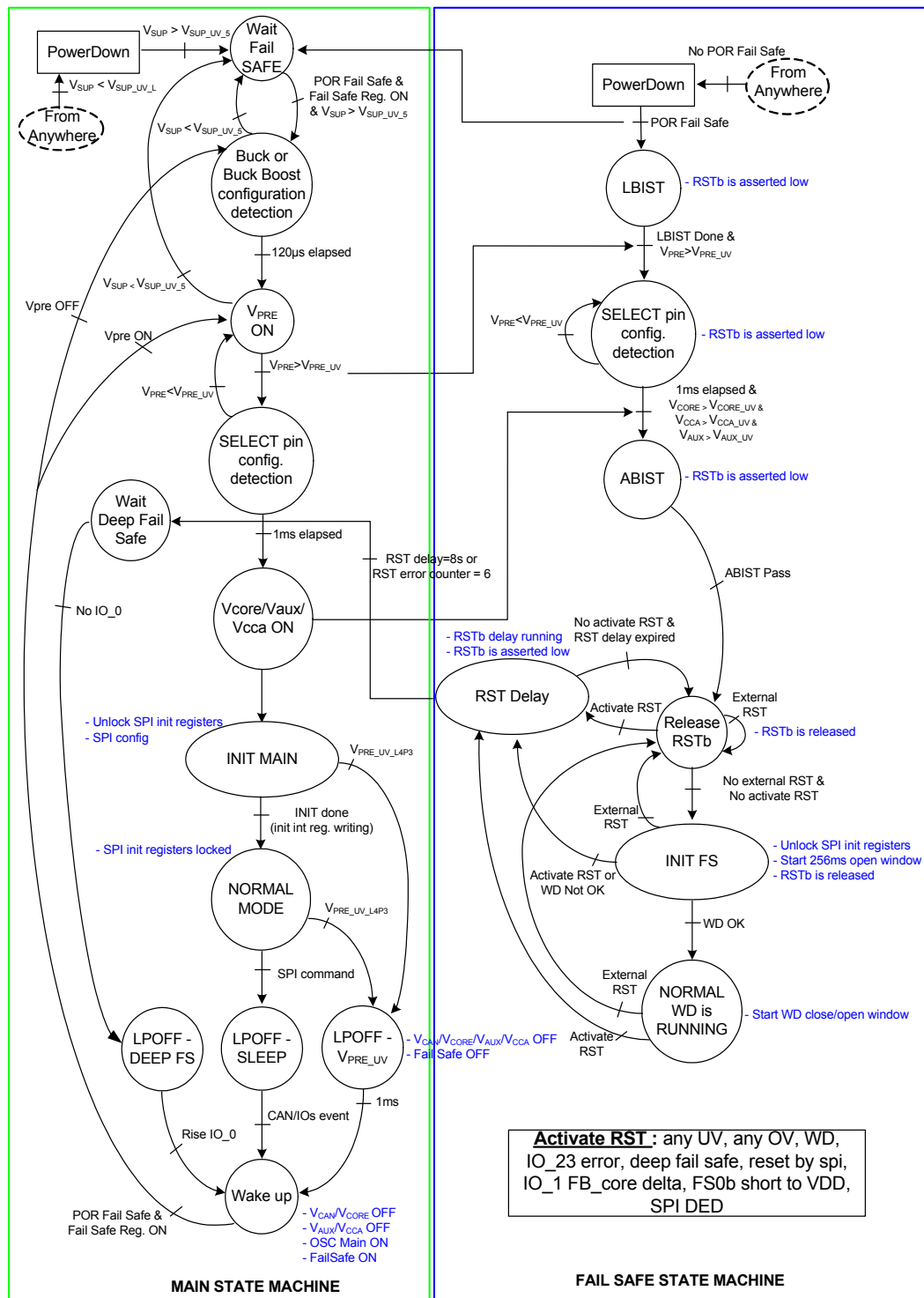


Figure 13. Simplified state diagram

## 6.5 Fail-safe machine

To fulfill safety critical applications, the 33907/33908 integrates a dedicated fail-safe machine (FSM). The FSM is composed of three main sub-blocks: the Voltage Supervisor (VS), the Fail-safe state machine (FSSM), and the Fail-safe output driver (FSO). The FSM is electrically independent from the rest of the circuitry, to avoid common cause failure.

For this reason, the FSM has its own voltage regulators (analog and digital), dedicated bandgap, and its own oscillator. Three power supply pins (VSUP 1, 2, & 3) are used to overcome a pin lift issue. The internal voltage regulators are directly connected on VSUP (one bonding wire per pin is used). Additionally, the ground connection is redundant as well to avoid any loss of ground.

All the voltages generated in the device are monitored by the voltage supervisor (under & overvoltage) owing to a dedicated internal voltage reference (different from the one used for the voltage regulators). The result is reported to the MCU through the SPI and delivered to the Fail-safe state machine (FSSM) for action, in case of a fault. All the safety relevant signals feed the FSSM, which handles the error handling and controls the fail-safe outputs.

There are two fail-safe outputs: RSTb (asserted low to reset the MCU), and FS0b (asserted low to control any fail-safe circuitry). The Fail-safe machine is in charge of bringing and maintaining the application in a Fail-safe state. Four sub Fail-safe states are implemented to handle the different kinds of failures, and to give a chance for the system to come back to a normal state.

### 6.5.1 Fail-safe machine state diagram

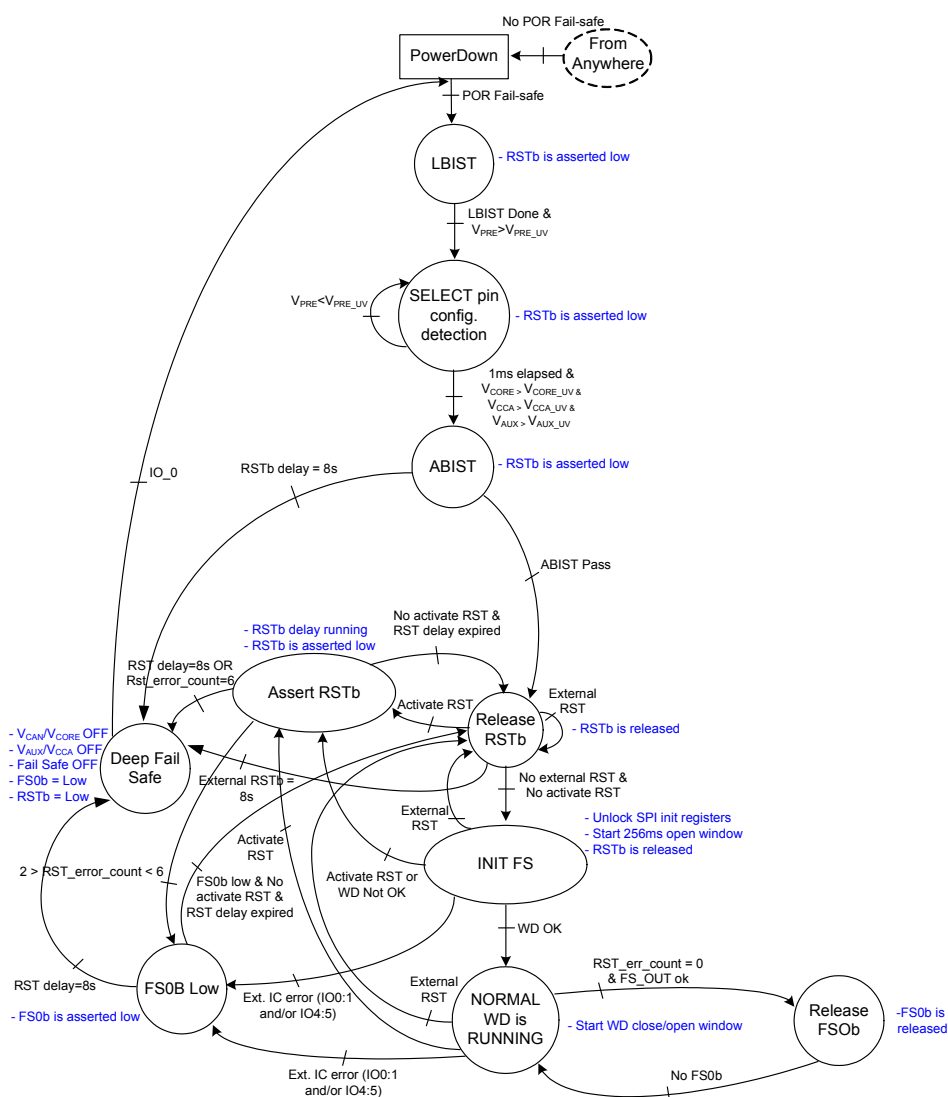


Figure 14. Detailed fail-safe state diagram

## 6.5.2 Watchdog operation

A windowed watchdog is implemented in the 33907/33908 and is based on “question/answer” principle (Challenger). The watchdog must be continuously triggered by the MCU in the open watchdog window, otherwise an error is generated. The error handling and watchdog operations are managed by the Fail-safe state machine. For debugging purpose, this functionality can be inhibited by setting the right voltage on the DEBUG pin at start-up.

The watchdog window duration is selectable through the SPI during the INIT FS phase or in Normal mode. The following values are available: 1.0 ms, 2.0 ms, 3.0 ms, 4.0 ms, 6.0 ms, 8.0 ms, 12 ms, 16.0 ms, 24 ms, 32 ms, 64 ms, 128 ms, 256 ms, 512 ms, and 1024 ms. The watchdog can also be inhibited through the SPI register to allow “reprogramming” (ie.at vehicle level through CAN).

An 8-bit pseudo-random word is generated, due to a Linear Feedback Shift Register implemented in the 33907/33908. The MCU can send the seed of the LFSR or use the LFSR generated by the 33907/33908 during the INIT phase and performs a pre-defined calculation. The result is sent through the SPI during the “open” watchdog window and verified by the 33907/33908. When the result is right, a new LFSR is generated and the watchdog window is restarted. When the result is wrong, the WD error counter is incremented, the watchdog window is restarted, an INTB is generated, and the LFSR value is not changed. Any access to the WD register during the “closed” watchdog window is considered a wrong WD refresh.

### 6.5.2.1 Normal operation (first watchdog refresh)

At power up, when the RSTB is released as high (after around 16 ms), the INIT phase starts for a maximum duration of 256 ms and this is considered as a fully open watchdog window. During this initialization phase the MCU sends the seed for the LFSR, or uses the default LFSR value generated by the 33907/33908 (0xB2), available in the WD\_LFSR register (Table 75). Using this LFSR, the MCU performs a simple calculation based on this formula. As an example, the result of this calculation based on LFSR default value (0xB2) is 0x4D.

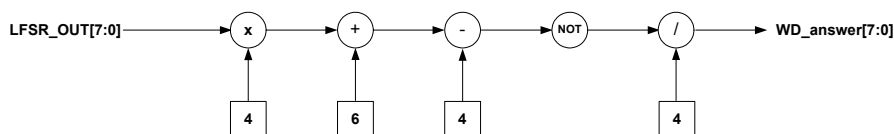


Figure 15. Watchdog answer calculation

The MCU sends the results in the WD answer register (Table 77). When the watchdog is properly refreshed during the open window, the 256 ms open window is stopped and the initialization phase is finished. A new LFSR is generated and available in the WD LFSR register, Table 74. If the watchdog refresh is wrong or if the watchdog is not refreshed during this 256 ms open window (INIT FS phase), the device asserts the reset low and the RSTB error counter is incremented by “1”.

After a good watchdog refresh, the device enters the Normal WD refresh mode, where open and closed windows are defined either by the configuration made during initialization phase in the watchdog window register (Table 73), or by the default value already present in this register (3.0 ms).

### 6.5.2.2 Normal watchdog refresh

The watchdog must be refreshed during every open window of the window period configured in the register Table 73. Any WD refresh restarts the window. This ensures the synchronization between MCU and 33907/33908.

The duration of the “window” is selectable through the SPI with no access restriction, means the window duration can be changed in the INIT phase or Normal mode. Doing the change in normal operation allow the system integrator to configure the watchdog window duration on the fly:

- The new WD window duration (except after disable) will be taken into account when a write in the WD\_answer register occurs (good or bad WD answer) or when the previous WD window is finished without any writing (WD timeout)
- The new WD window duration after disable will be taken into account when SPI command is validated

The duty cycle of the window is set to 50% and is not modifiable.

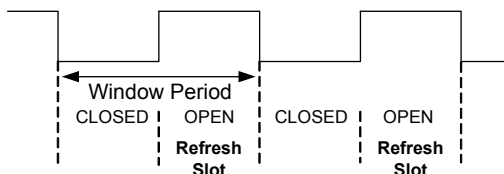


Figure 16. Windowed watchdog

### 6.5.2.3 Watchdog in debug mode

When the device is in debug mode (entered via the DEBUG pin), the watchdog continues to operate, but does not affect the device operation by asserting a reset or fail-safe pins. For the user, operation appears without the watchdog. If needed and to debug the watchdog itself, the user can operate as in Normal mode and check LFSR values, the watchdog refresh counter, the watchdog error counter, and reset counter. This allows the user to debug their software and ensure a good watchdog strategy in the application.

### 6.5.2.4 Wrong watchdog refresh handling

Error counters and strategy are implemented in the device to manage wrong watchdog refreshes from the MCU. According to consecutive numbers of wrong watchdog refreshes, the device can decide to assert the RSTB only, or to go in deep Fail-safe mode where only a Power On Reset or a transition on IO\_O helps the system to recover.

### 6.5.2.5 Watchdog error counter

The watchdog error counter is implemented in the device to filter the incorrect watchdog refresh. Each time a watchdog failure occurs, the device increments this counter by 2. The WD error counter is decremented by 1 each time the watchdog is properly refreshed. This principle ensures that a cyclic “OK/NOK” behavior converges to a failure detection. To allow flexibility in the application, the maximum value of this counter is configurable in the INIT\_WD register, but only when device is in INIT FS mode.

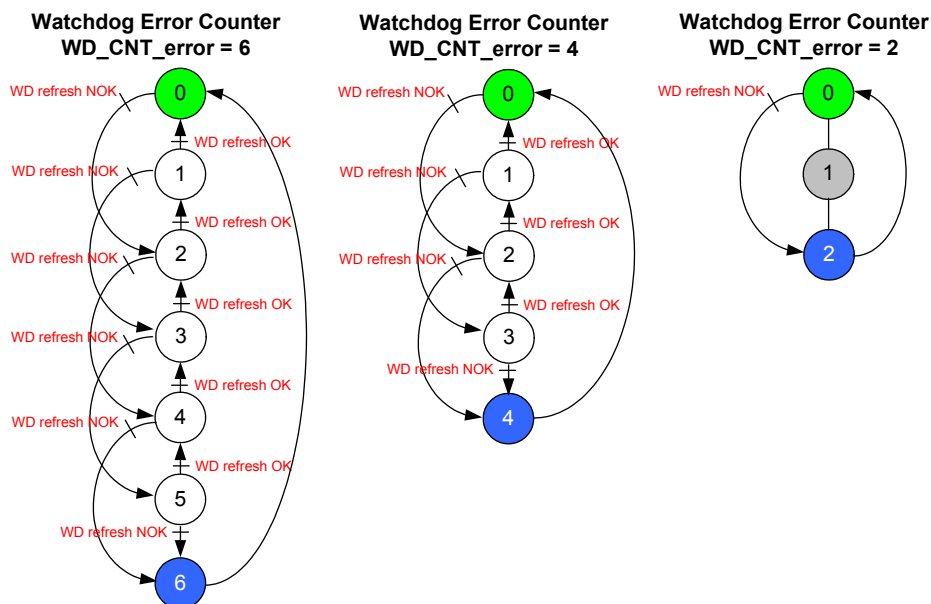


Figure 17. Watchdog error counter configuration (INIT\_WD register, Bits WD\_CNT\_error\_1:0)



## 6.5.2.6 Watchdog refresh counter

The watchdog refresh counter is used to decrement the RST error counter. Each time the watchdog is properly refreshed, the watchdog refresh counter is incremented by "1". Each time the watchdog refresh counter reaches "6" and if next WD refresh is also good, the RST error counter is decremented by "1" (case with WD\_CNT\_refresh\_1:0 configured at 6).

Whatever the position is in the watchdog refresh counter, each time there is a wrong refresh watchdog, the watchdog refresh counter is reset to "0". To allow flexibility in the application, the maximum value of this watchdog refresh counter is configurable in the INIT\_WD register, but only when device is in INIT FS mode.

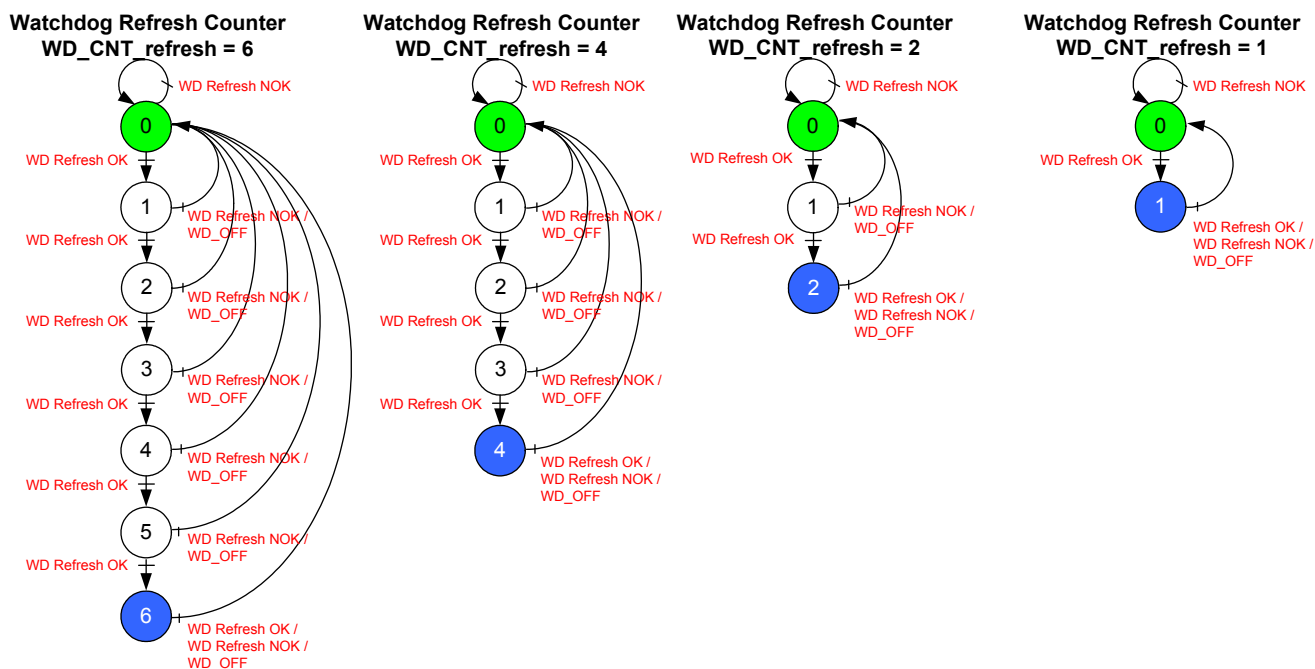


Figure 18. Watchdog refresh counter configuration (INIT\_WD register, WD\_CNT\_refresh\_1:0)

Table 10. Watchdog error table

|     |                 | Window   |        |
|-----|-----------------|----------|--------|
|     |                 | CLOSED   | OPEN   |
| SPI | BAD Key         | WD_NOK   | WD_NOK |
|     | GOOD Key        | WD_NOK   | WD_OK  |
|     | None (time out) | No_issue | WD_NOK |

Any access to the watchdog register during the "closed" watchdog window is considered as a wrong watchdog refresh. Watchdog timeout, meaning no WD refresh during closed or open windows, is considered as a wrong WD refresh.

## 6.5.3 Reset error counter

The reset error counter manages the reset events and counts the number of resets occurring in the application. This counter is incremented not only for the reset linked to consecutive wrong refresh watchdogs, but also for other sources of reset (undervoltage, overvoltage, external reset). The RST error counter is incremented by 1, each time a reset is generated.

The reset error counter has two output values (intermediate and final). The intermediate output value is used to handle the transition from reset (RSTB is asserted low) to reset and fail where RSTB and FS0B are activated. The final value is used to handle the transition from reset and fail to deep reset and fail (Deep Fail-safe mode), where regulators are off, RSTB and FS0B are activated, and a power on reset or a transition on IO\_0 is needed to recover. The intermediate value of the reset error counter is configurable to "1" or "3" using the RSTB\_err\_FS bit in the INIT FSSM2 register ([Table 71](#)).

If RSTB\_err\_FS is set to "0", it means the device activates FS0B when the reset error counter reaches level "3".

If RSTB\_err\_FS is set to "1", it means the device activates FS0B when the reset error counter reaches level "1".

This configuration must be done during INIT FS phase.

The final value of the reset error counter is based on the intermediate configuration.

- RSTB\_err\_FS = 0 / Intermediate = 3; Final = 6 ([Figure 19](#)). When reset error counter reaches 6, the device goes into deep reset and fails.
- RSTB\_err\_FS = 1 / Intermediate = 1; Final = 2 ([Figure 20](#)). When reset error counter reaches 2, the device goes into deep reset and fails.

In any condition, if the RSTB is asserted LOW for a duration longer than eight seconds, the device goes into deep reset and fails.

Conditions that leads to an increment of the RSTB error counter, and according to the product configuration are:

- Watchdog error counter = 6
- Watchdog refresh NOK during INIT phase or Watchdog timeout
- IO\_23 error detection (FCCU)
- Undervoltage
- Overvoltage
- IO\_1 FB\_Core Delta
- FS0B shorted to VDD
- SPI DED
- Reset request by the SPI
- External reset

Conditions leading to a transition go to FS, according to the product configuration are:

- IO\_01/IO\_23/IO\_45 error detection
- Undervoltage
- Overvoltage
- IO\_1 FB\_Core Delta
- Analog BIST fail
- SPI DED
- RSTB shorted to high

### Reset Error Counter (Cfg SPI RSTb\_err\_FS=0; WD\_CNT\_refresh=6)

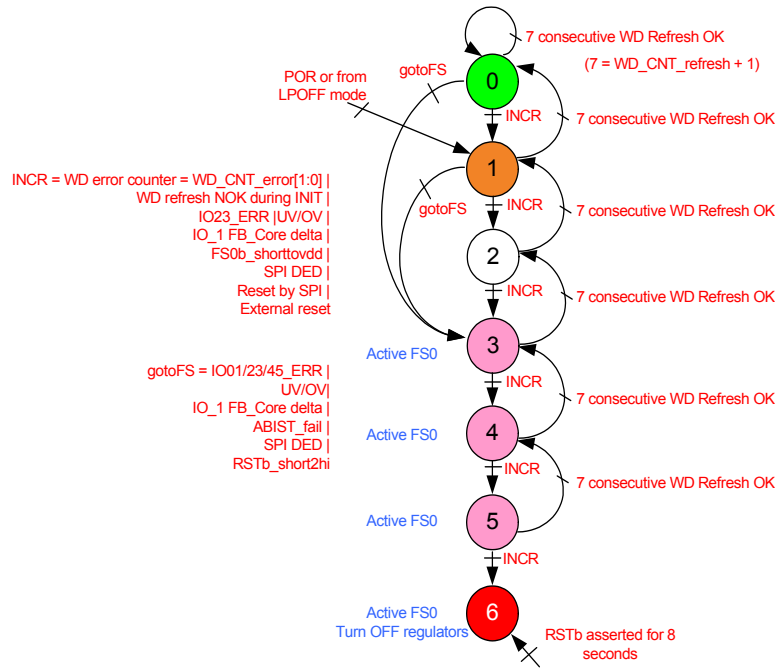


Figure 19. RSTB error counter (RSTB\_err\_FS = 0)

### Reset Error Counter (Cfg SPI RSTb\_err\_FS=1; WD\_CNT\_refresh=6)

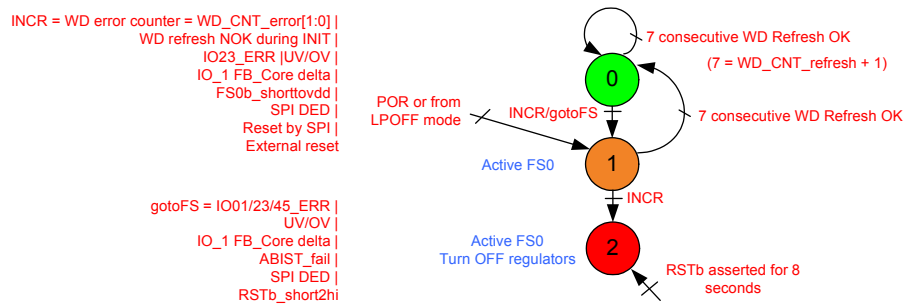


Figure 20. RSTB error counter(RSTb\_err\_FS = 1)

### 6.5.3.1 RST error counter at start-up or resuming from LPOFF mode

At start-up or when resuming from LPOFF mode the reset error counter starts at level 1 and FS0B is asserted low. To remove activation of FS0B, the RST error counter must go back to value "0" (seven consecutive good watchdog refresh decreases the reset error counter down to 0) and a right command is sent to FS\_OUT register ([Figure 23](#)).

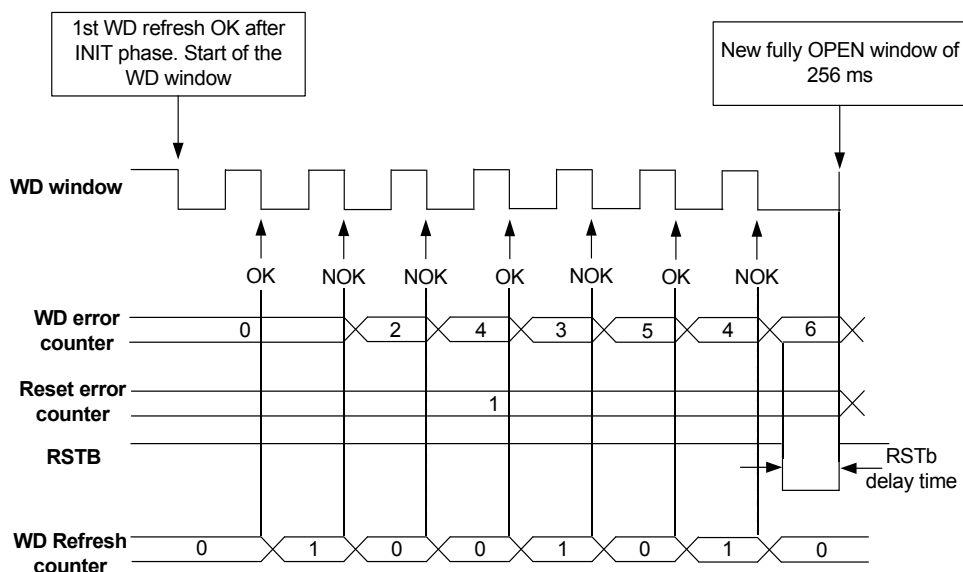


Figure 21. Example of WD operation generating a reset (WD\_error\_cnt = 6)

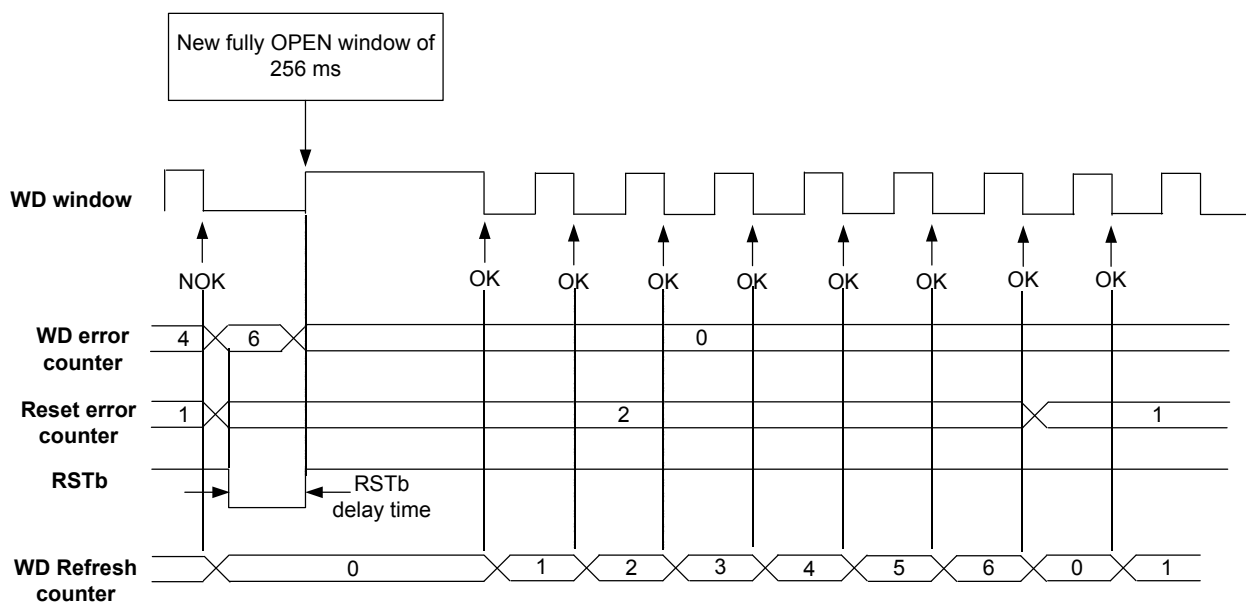


Figure 22. Example of WD operation leading a decrement of the reset error counter (WD\_refresh\_cnt = 6)

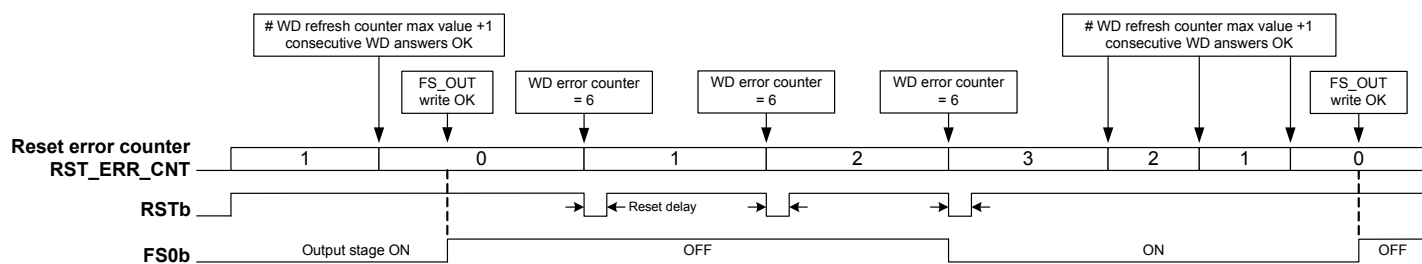


Figure 23. Reset error counter and FS0B deactivation sequence (RSTb\_err\_FS = 0 & WD\_CNT\_error1:0 = 6)

## 6.5.4 Fail-safe output (FS0B) deactivation

When the fail-safe output FS0B is asserted low by the device due to a fault, some conditions must be validated before allowing the FS0B pin to be deactivated by the device. These conditions are:

- Fault is removed
- Reset error counter must be at “0”
- FS\_OUT register must be filled with the right value.

### 6.5.4.1 Faults triggering FS0B activation

The activation of the FS0B is clearly dependent on the product configuration, but the following items can be settled:

- IO\_01/IO\_23/IO\_45 error detection
- Undervoltage
- Overvoltage
- IO\_1 FB\_Core Delta
- Analog BIST fail (not configurable)
- SPI DED (not configurable)
- RSTB shorted to high (not configurable)
- RSTB error counter level

## 6.5.5 SPI DED

Some SPI registers affect some safety critical aspects of the fail-safe functions, and thus are required to be protected against SEU (Single Event Upset). Only fail-safe registers are concerned. During INIT FS mode, access to fail-safe registers for product configuration is open. Then once the INIT FS phase is over, the Hamming circuitry is activated to protect registers content.

At this stage, if there is 1 single bit flip, the detection is made due to hamming code, and the error is corrected automatically (fully transparent for the user), and a flag is sent. If there are two errors (DED - Dual Error Detection), the detection is made due to hamming code but detected errors cannot be corrected. Flag is sent, RSTB and FS0B are activated.

## 6.5.6 FS\_OUT register

When fault is removed and reset error counter changes back to level “0”, a right word must be filled in the FS\_OUT register. The value is dependant on the current WD\_LFSR. LSB and MSB must be swapped and negative operation per bit must be applied.

|              |                 |                 |                 |                 |                 |                 |                 |                 |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| WD_LFSR_7:0= | b7              | b6              | b5              | b4              | b3              | b2              | b1              | b0              |
| FS_OUT_7:0 = | $\overline{b0}$ | $\overline{b1}$ | $\overline{b2}$ | $\overline{b3}$ | $\overline{b4}$ | $\overline{b5}$ | $\overline{b6}$ | $\overline{b7}$ |

Figure 24. FS\_OUT register based on LFSR value

## 6.6 Input voltage range

Due to the flexibility of the pre-regulator, the device can cover a wide battery input voltage range. However, a more standard voltage range can still be covered using only the Buck configuration.

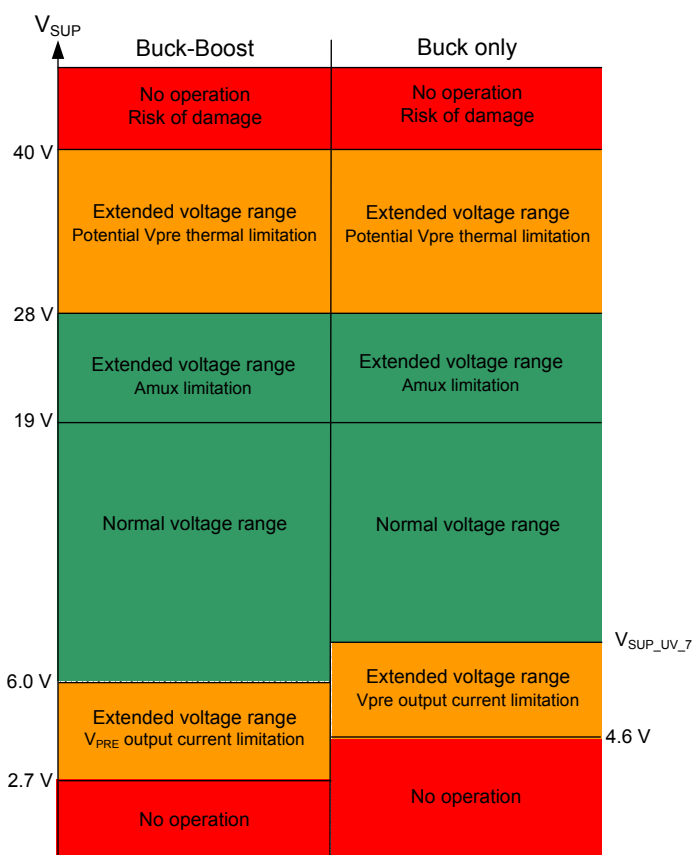


Figure 25. Input voltage range

- $V_{SUP} > 28\text{ V}$ : Potential  $V_{PRE}$  thermal limitation

$R_{DS(on)}$ , Current limitation and Overcurrent detection are specified for  $V_{SUP} < 28\text{ V}$ .

- $V_{SUP} < 19\text{ V}$ :  $Mux\_out$  limitation

$IO\_0$  and  $IO\_1$  maximum analog input voltage range is  $19\text{ V}$ . Internal  $2.5\text{ V}$  reference voltage accuracy degraded.

- Buck only,  $V_{SUP} < V_{SUP\_UV\_7}$ :

CAN communication is guaranteed for  $V_{SUP} > 6.0\text{ V}$ . LIN communication according to SAEJ2602-2 specification is stopped ( $V_{SUP} < 7.0\text{ V}$ ). For  $V_{CCA}$  and  $V_{AUX}$   $5.0\text{ V}$  configuration, undervoltage triggers at low  $V_{SUP}$  (refer to  $V_{CCA\_UV\_5}$  and  $V_{AUX\_UV\_5}$ ).

## 6.7 Power management operation

A thermal sensor is implemented as close as possible to the pass transistor of each regulator ( $V_{PRE}$ ,  $V_{CORE}$ ,  $V_{CCA}$ ,  $V_{CAN}$ ) and an associated individual Thermal Shutdown (TSD) protect these regulators independently. When the TSD threshold of a specific regulator is reached, this regulator only is switched OFF and the information is reported in the main state machine. The regulator restarts automatically when the junction temperature of the pass transistor decrease below the TSD threshold.

## 6.7.1 VPRE voltage pre-regulator

A highly flexible SMPS pre-regulator is implemented in the 33907/33908. Depending on the input voltage requirement, the device can be configured as “non-inverting buck-boost converter” (Figure 27) or “standard buck converter” (Figure 26). An external logic level MOSFET (N-type) is required to operate in “non-inverting buck-boost converter”. The connection of the external MOSFET is detected automatically during the start-up phase.

The converter operates in Current Control mode in any configuration. The high-side switching MOSFET is integrated to make the current control easier. The PWM frequency is fixed at 440 kHz typical. The compensation network is fully integrated. VPRE output voltage is regulated between 6.0 V and 7.0 V.

If the full current capability is not used for V<sub>CORE</sub>, V<sub>CCA</sub>, V<sub>AUX</sub> and CAN\_5V, additional external LDO can be connected to VPRE to fulfill application needs while the current load remains below the maximum current capability in all conditions.

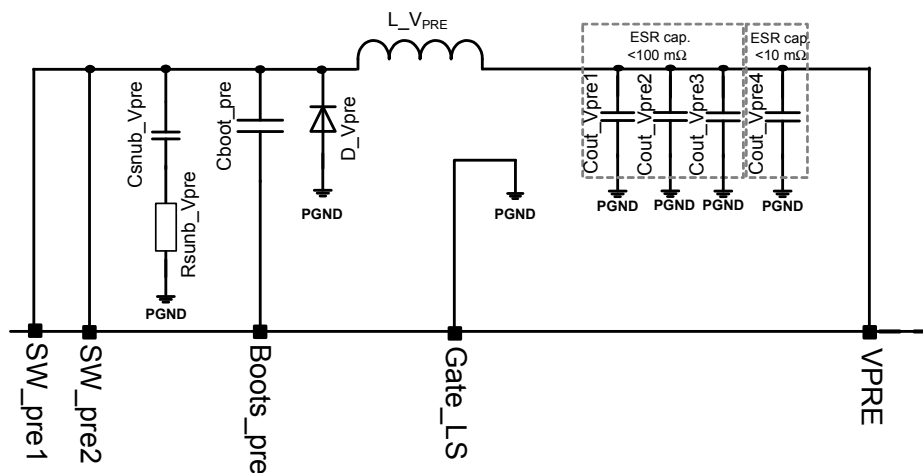


Figure 26. Pre-regulator: buck configuration

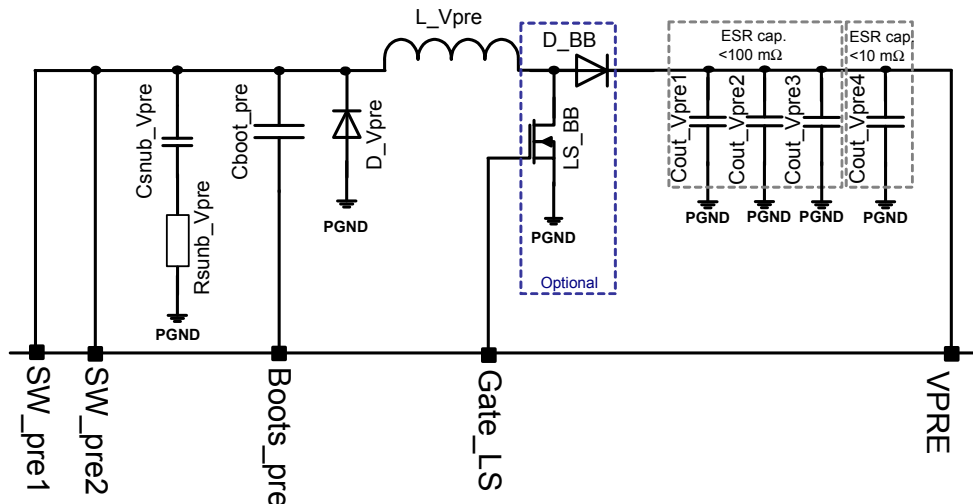


Figure 27. Pre-regulator: buck boost configuration

When the converter is set up to work in boost mode at low V<sub>SUP</sub>, the transition between buck and boost mode is automatically handled by the device at V<sub>SUP\_UV\_7</sub> threshold. Transition between buck mode and boost mode is based on hysteresis (Figure 28).

- When V<sub>SUP</sub> > V<sub>SUP\_UV\_7</sub>, the converter works in buck mode and VPRE output is regulated at 6.5 V typic.
- When V<sub>SUP</sub> < V<sub>SUP\_UV\_7</sub>, the converter works in boost mode and VPRE output is regulated at 6.3 V typic.

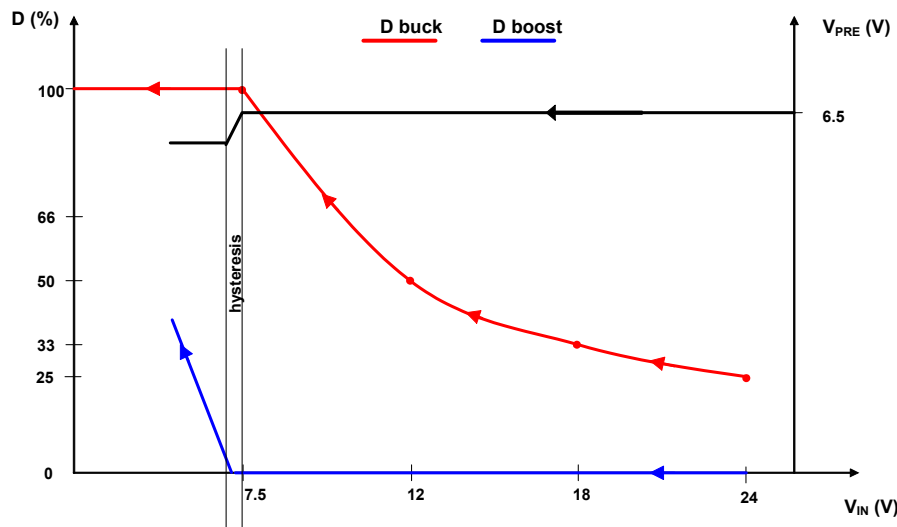


Figure 28. Transition between buck and boost

### 6.7.1.1 Power up and power down sequence

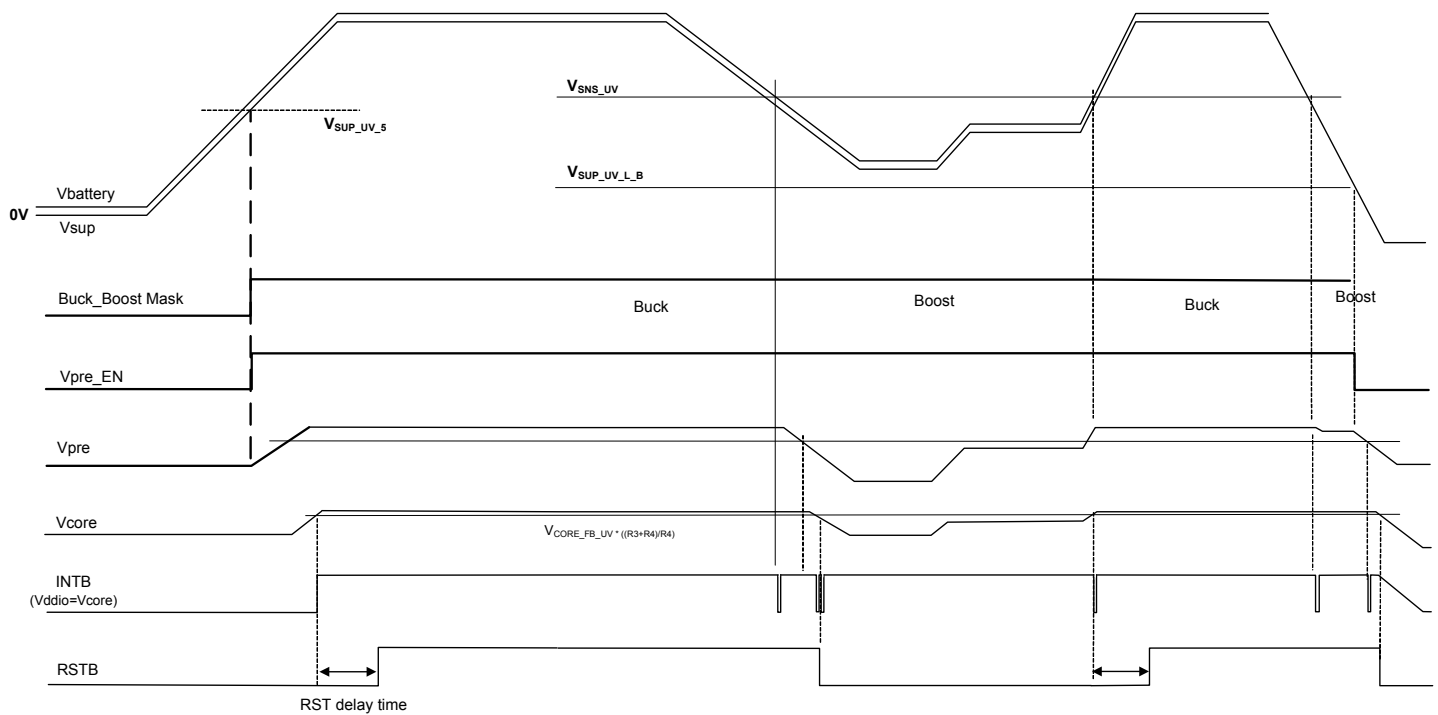
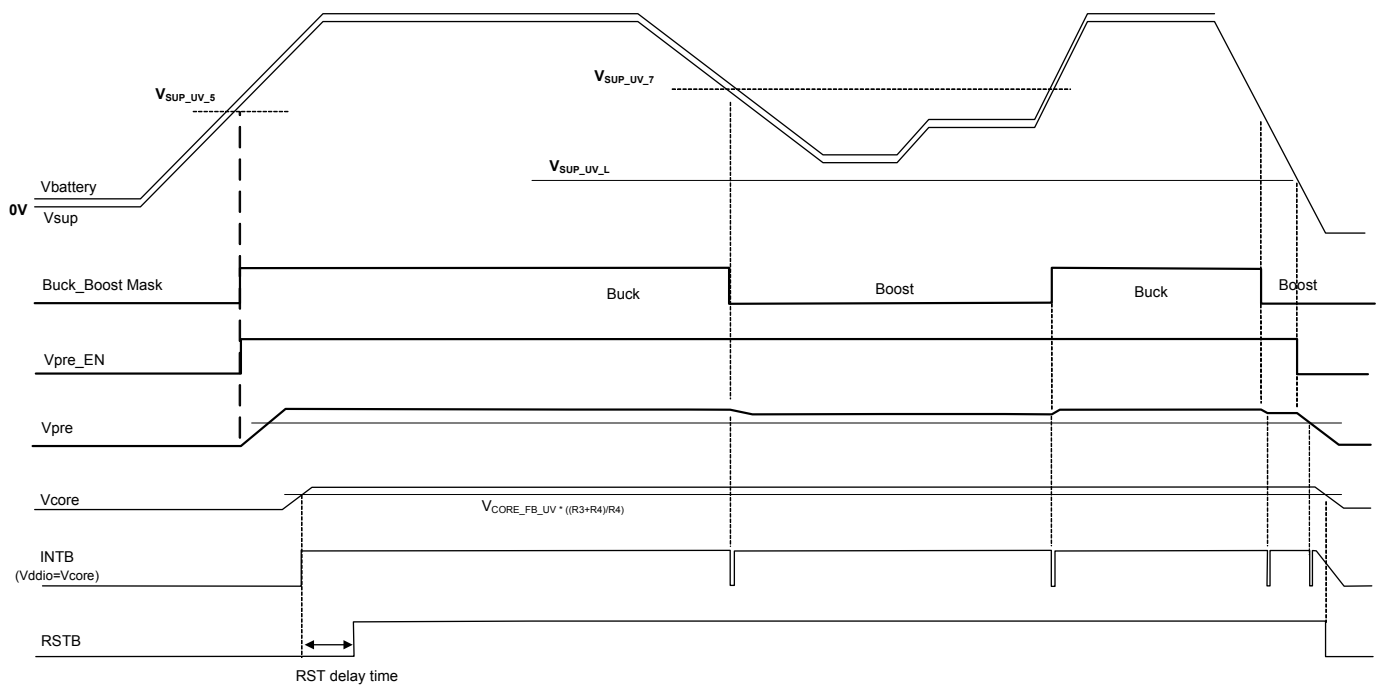


Figure 29. Buck configuration power-up and power-down

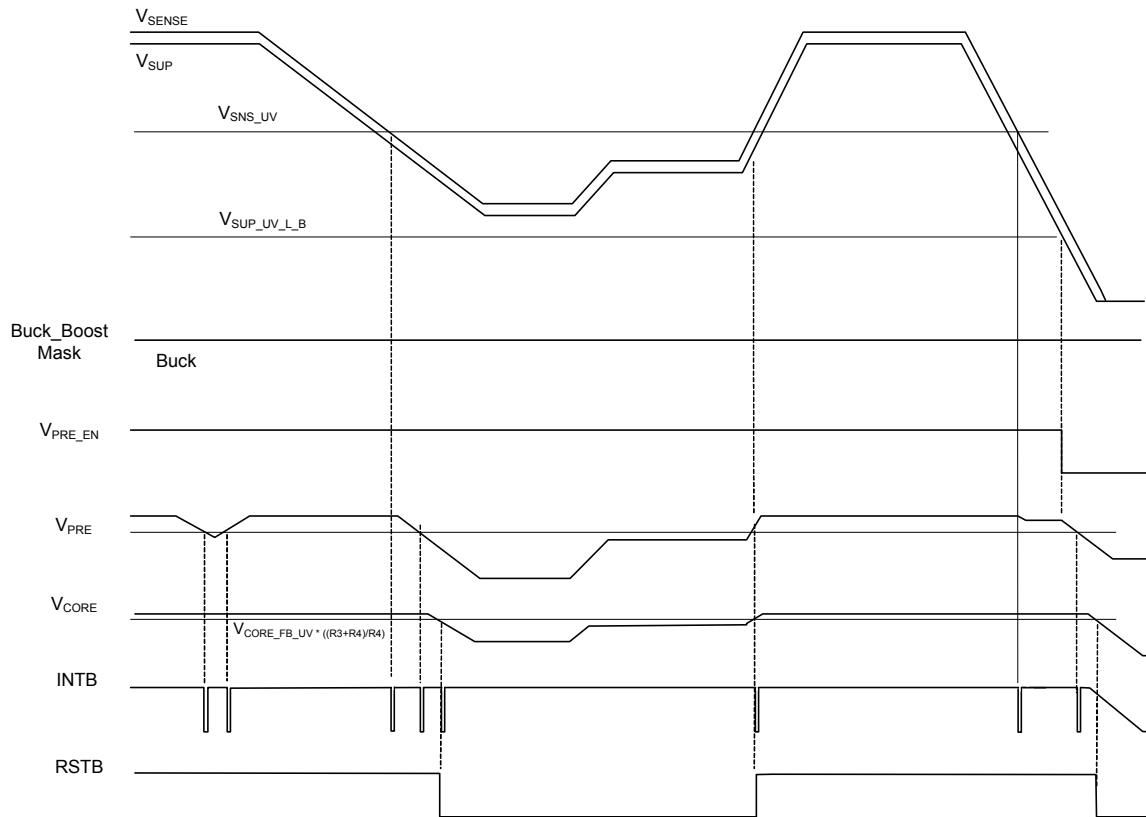




**Figure 30. Buck boost configuration power-up and power-down**

### 6.7.1.2 Cranking management

When VPRE is set up to work in buck only mode, the application can work down to  $V_{SUP} = V_{SUP\_UV\_L\_B} = 4.6V$  with a minimum of 500 mA current guaranteed on VPRE.



**Figure 31. Behavior during cranking (buck configuration)**

When VPRE is set up to work in boost mode, the application can work down to  $V_{SUP} = V_{SUP\_UV\_L} = 2.7V$  with a minimum of 300 mA current guaranteed on VPRE. The boost mode configuration help to pass LV124 specification requiring a minimum of 3.2 V on  $V_{BAT}$  supply during cold cranking conditions.

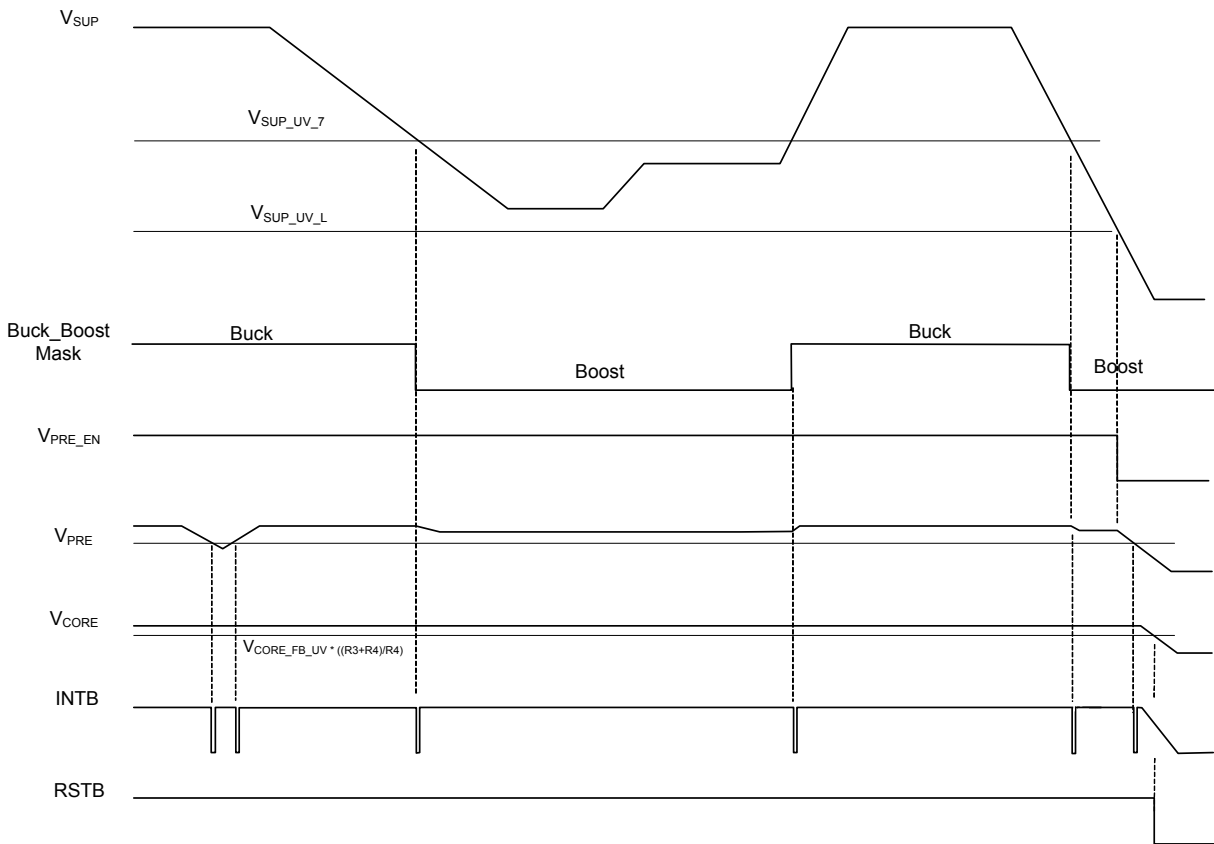


Figure 32. Behavior during cranking (buck boost configuration)

### 6.7.1.3 Light load condition

In order to improve the converter efficiency and avoid any unwanted output voltage increase, VPRE voltage regulator operates in Pulse Skipping mode during light load condition.

The transition between Normal mode and Pulse Skipping mode is based on the comparison between the error amplifier output (EA\_out) and pre-defined thresholds  $V_{PRE\_LL\_H}$  and  $V_{PRE\_LL\_L}$ . When the Error Amplifier output reaches  $V_{PRE\_LL\_L}$ , VPRE high-side transistor is switched OFF. When the Error Amplifier output reaches  $V_{PRE\_LL\_H}$ , VPRE high-side transistor is switched ON again for the next switching period (Figure 33).

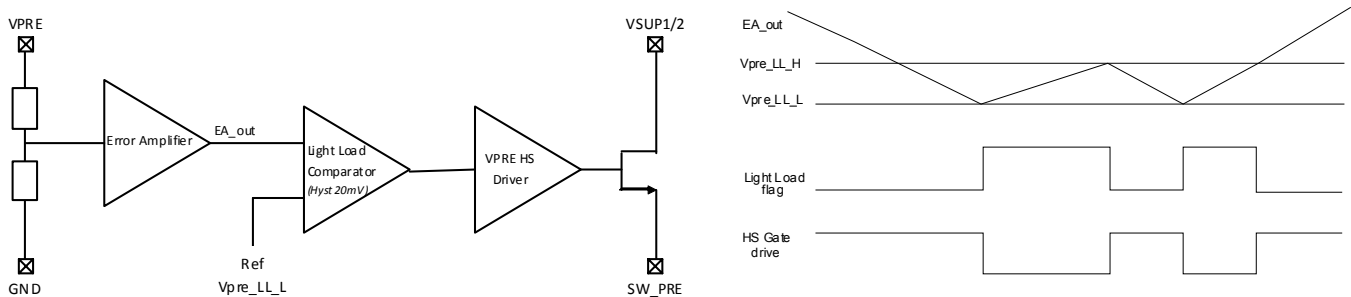


Figure 33. Description of light load condition

### 6.7.1.4 Input power feed forward condition

In order to improve the converter efficiency during high input power condition, VPRE switching frequency is reduced from 440 kHz to 220 kHz when  $V_{SUP} > V_{SUP\_IPFF}$  and  $I_{PRE} > I_{PRE\_IPFF\_PK}$  to decrease the switching losses. The transition between the two frequencies is transparent for the application.

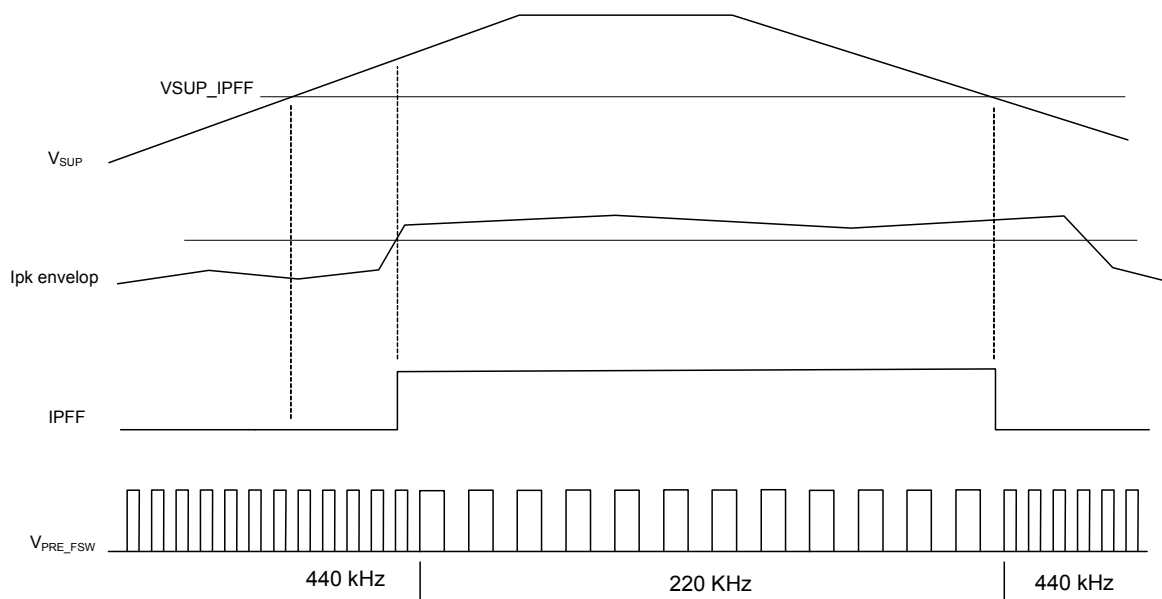


Figure 34. Input power feed forward principle

### 6.7.1.5 Overcurrent detection and current limitation

#### 6.7.1.5.1 Overcurrent protection:

In order to ensure the integrity of the high-side MOSFET, an overcurrent detection is implemented. The regulator is switched OFF by the Main State machine when the over-current detection threshold  $I_{PRE\_OC}$  is reached three consecutive times. The overcurrent detection is blanked when the pass transistor is switched ON during  $T_{PRE\_OC}$  to avoid parasitic switch OFF of the high-side gate driver.

The VPRE output voltage decrease causes an undervoltage condition on one of the cascaded regulators (VCORE, VCCA, VAUX) and bring the device in Fail-safe state. The overcurrent protects the regulator in case of SW\_PRE pin shorted to GND. The overcurrent works in Buck mode only.

#### 6.7.1.5.2 Current limitation:

A current limitation is also implemented to avoid uncontrolled power dissipation inside the device (duty cycle control) and limits the current below  $I_{PRE\_LIM}$ . The current limitation is blanked when the pass transistor is switched ON during  $T_{PRE\_BLK\_LIM}$  to allow short-circuit detection on SW\_PRE pin.

When  $I_{PRE\_LIM}$  threshold is reached during Buck mode, the high-side integrated MOSFET is switched OFF. When  $I_{PRE\_LIM}$  threshold is reached during Boost mode, the external low-side MOSFET is switched OFF. In both cases, the MOSFET is not switched ON again before the next rising edge of the switching clock.

The current limitation will induce a duty cycle reduction and will lead to VPRE output voltage to fall down gradually and may cause an undervoltage condition on one of the cascaded regulators (VCORE, VCCA, VAUX) and bring the device in Fail-safe state. The current limitation does not switch OFF the regulator. The current limitation protects the regulator when VPRE pin is shorted to GND.

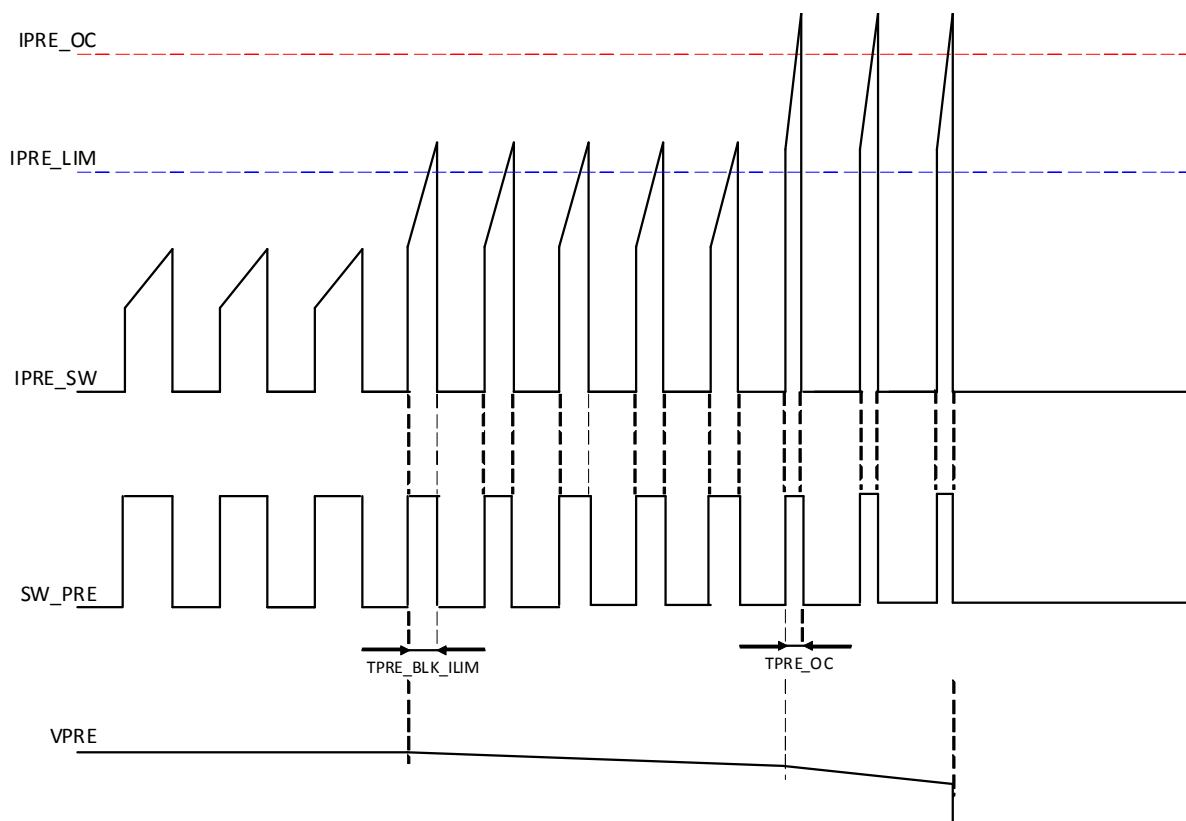


Figure 35. Overcurrent and current limitation scheme

### 6.7.1.6 VPRE voltage monitoring

The overvoltage detection switches OFF the regulator. The undervoltage detector is disabled when the regulator is switched OFF reporting an undervoltage. Diagnostic is reported in the dedicated register and generate an Interrupt.

The undervoltage detection does not switches OFF the regulator. However,  $V_{PRE}$  decrease may induce an undervoltage on a regulator attached to  $V_{PRE}$  (VCORE, VCCA, VAUX, or CAN\_5V), and bring the application in Fail-safe state depending on the supervisor configuration (registers INIT SUPERVISOR 1,2,3).

### 6.7.1.7 VPRE efficiency

VPRE efficiency versus current load is given for information based on typical external component criteria described in the table close to the graph and at three different  $V_{SUP}$  voltages (8.0 V, 14 V, and 18 V) covering typical automotive operating range. The efficiency is valid in buck mode only and above 200 mA load on VPRE in order to be in continuous mode in the 22  $\mu$ H inductor. The efficiency is calculated and has to be verified by measurement at application level.

| Ext. Devices  |                  |
|---------------|------------------|
| Cout          | 57 $\mu$ F       |
| ESR Cout      | 100.0 m $\Omega$ |
| L coil        | 22.0 $\mu$ H     |
| DCR coil      | 60.0 m $\Omega$  |
| Vdiode        | 0.35 V           |
| MOSFET switch |                  |
| Rdson         | 200.0 m $\Omega$ |
| Cg            | 600 pF           |
| Tsw_on        | 30.00 ns         |
| Tsw_off       | 30.00 ns         |
| Overdrive     | 10.0 V           |
| Converter     |                  |
| Vpre          | 6.50 V           |
| Freq          | 440 kHz          |

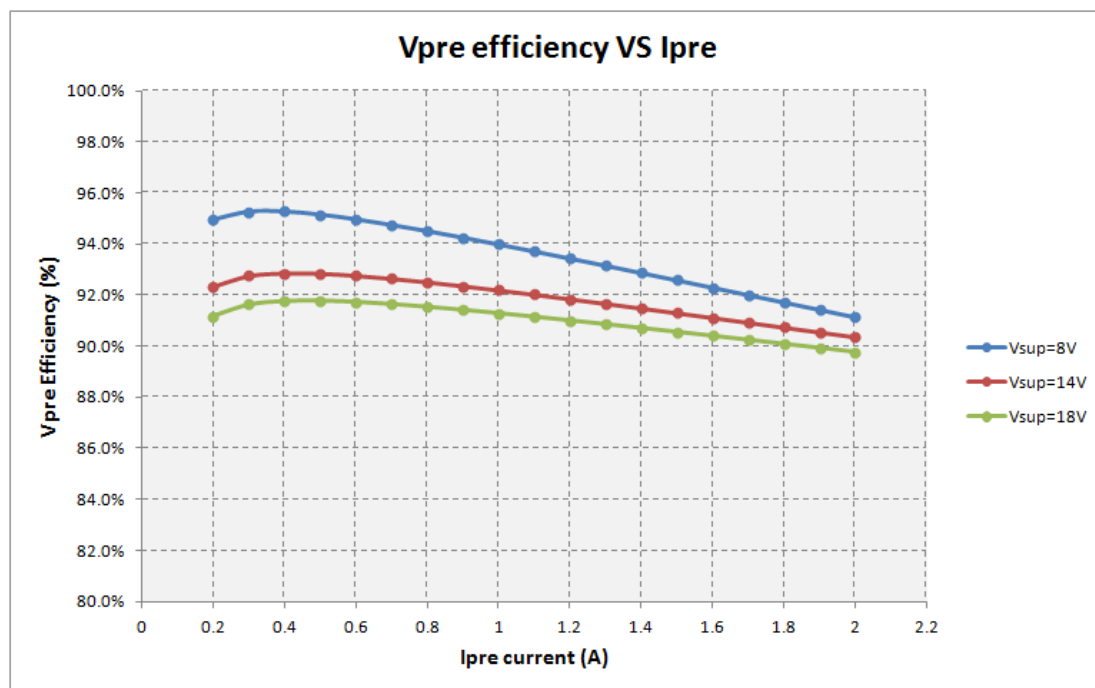


Figure 36. V<sub>PRE</sub> efficiency

## 6.7.2 VCORE voltage regulator

This voltage regulator is a step-down DC-DC converter operating in Voltage Control mode. The high side switching MOSFET is integrated in the device and the PWM frequency is fixed at 2.4 MHz typical. The output voltage is configurable from 1.2 V to 3.3 V range and adjustable around these voltages with an external resistor divider (R3/R4) connected between V<sub>CORE</sub> and the feedback pin (FB<sub>CORE</sub>) (Figure 37).

$$V_{CORE} = V_{CORE\_FB} \times ((R3 + R4) / R4)$$

The voltage accuracy is  $\pm 2.0\%$  (without the external resistor bridge R3/R4 accuracy) and the max output current is 1.5 A. The stability of the overall converter is done by an external compensation network (R1/C1/R2/C2) connected to the pin COMP<sub>CORE</sub>. It is recommended to use 1% accuracy resistors and set R4 = 8.06 k $\Omega$  and adjust R3 to obtain the final VCORE voltage needed for the MCU core supply.

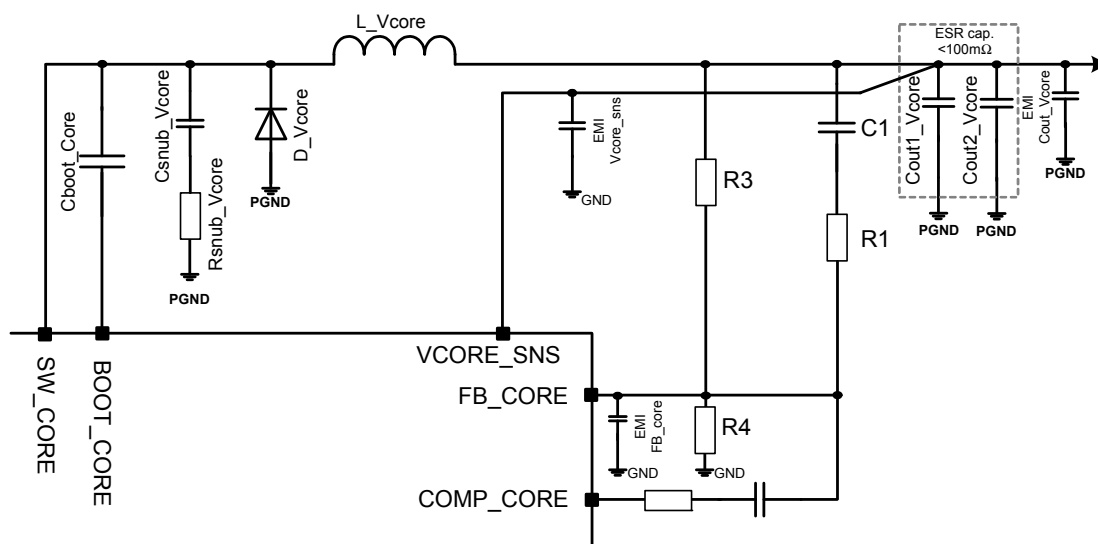


Figure 37. VCORE buck regulator

### 6.7.2.1 Light load condition

In order to improve the converter efficiency and avoid any unwanted output voltage increase, V<sub>CORE</sub> voltage regulator operates in Pulse Skipping mode during light load condition. The principle is the same as the V<sub>PRE</sub> implementation described in details in [Light load condition](#).

### 6.7.2.2 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation inside the device (duty cycle control) and limits the current below I<sub>CORE\_LIM</sub>. The current limitation is banked when the pass transistor is switched ON during T<sub>CORE\_BLK\_LIM</sub> to avoid parasite detection. When I<sub>CORE\_LIM</sub> threshold is reached, the high-side integrated MOSFET is switched OFF. The MOSFET is not switched ON again before the next rising edge of the switching clock.

The current limitation will induce a duty cycle reduction and will lead to V<sub>CORE</sub> output voltage to fall down gradually and may cause an undervoltage condition and bring the device in Fail-safe state. The current limitation does not switch OFF the regulator.

### 6.7.2.3 Voltage monitoring

The overvoltage detection switches OFF the regulator. The regulator remains ON in case of undervoltage detection. Diagnostic is reported in the dedicated register, generate an Interrupt and may bring the application in Fail-safe state depending on the supervisor configuration (registers INIT SUPERVISOR 1,2, 3).

### 6.7.2.4 V<sub>CORE</sub> efficiency

V<sub>core</sub> efficiency versus current load is given for information based on typical external component criteria described in the table close to the graph and at two different V<sub>CORE</sub> voltages (3.3 V, and 1.2 V) covering most of the 32-bit MCU supply range. The efficiency is valid above 200 mA load on V<sub>CORE</sub> in order to be in continuous mode in the 2.2  $\mu$ H inductor. The efficiency is calculated and has to be verified by measurement at application level. One of the major contributor degrading the efficiency at V<sub>CORE</sub> = 1.2 V is the external diode during the recirculation phase. Lower the diode Forward Voltage (V<sub>F</sub>) is, the better the efficiency.

| Ext. Devices  |                  |
|---------------|------------------|
| Cout          | 20 $\mu$ F       |
| ESR Cout      | 5.0 m $\Omega$   |
| L coil        | 2.2 $\mu$ H      |
| DCR coil      | 20.0 m $\Omega$  |
| Vdiode        | 0.35 V           |
| MOSFET switch |                  |
| Rdson         | 200.0 m $\Omega$ |
| Cg            | 300 pF           |
| Tsw_on        | 12.00 ns         |
| Tsw_off       | 12.00 ns         |
| Overdrive     | 10.0 V           |
| Converter     |                  |
| Vcore         | 3.30 V           |
| Freq          | 2400 kHz         |

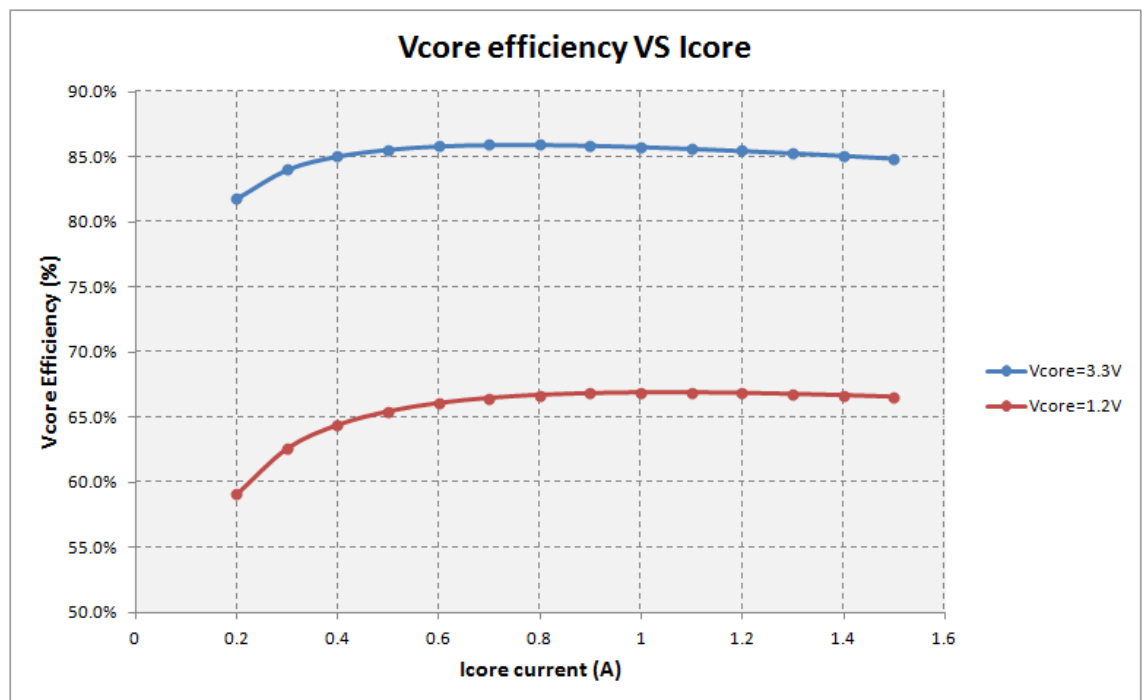


Figure 38. V<sub>CORE</sub> efficiency

### 6.7.3 Charge pump and bootstrap

Both switching MOSFETs of VPRE and VCore SMPS are driven by external bootstrap capacitors. Additionally, a charge pump is implemented to ensure 100% duty cycle for both converters. Each converter uses a 100 nF external capacitor minimum to operate properly.

### 6.7.4 VCCA voltage regulator

VCCA is a linear voltage regulator mainly dedicated to supply the MCU I/Os, especially the ADC. The output voltage is selectable at 5.0 V or 3.3 V. Since this output voltage can be used to supply MCU I/Os, the output voltage selection is done using an external resistor connected to the SELECT pin and ground if VAUX is used. When VAUX is not used, the resistor is connected between the SELECT pin and VPRE.

When VCCA is used with the internal MOS transistor, VCCA\_E pin must be connected to VPRE. The voltage accuracy is  $\pm 1.0\%$  for 5.0 V configuration and  $\pm 1.5\%$  for 3.3 V configuration with an output current capability at 100 mA.

When VCCA is used with an external PNP transistor to boost the current capability up to 300 mA, the connection is detected automatically during the start-up sequence of the 33907/33908. In such condition, the internal pass transistor is switched OFF and all the current is driven through the external PNP to reduce the internal power dissipation. The output voltage accuracy with an external PNP is reduced to  $\pm 3.0\%$  at 300 mA current load. The VCCA output voltage is used as a reference for the Auxiliary voltage supply (VAUX) when VAUX is configured as a tracking regulator.

#### 6.7.4.1 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation of the internal MOSFET or external PNP transistor. By default, the current limitation threshold is selected based on the auto detection of the external PNP during start up phase.

- When the internal MOSFET transistor is used, the current is limited to  $I_{CCA\_LIM\_INT}$  and the regulator is kept ON
- When the external PNP transistor is used, the current is limited to  $I_{CCA\_LIM\_OUT}$  and the regulator is switch OFF after a dedicated duration  $T_{CCA\_LIM\_OFF}$  under current limitation. A SPI command is needed to restart the regulator.

In case of external PNP configuration only, the lowest current limitation threshold can be selected by SPI in the register INIT VREG 2 instead of the highest one. In order to limit the power dissipation in the external PNP transistor in case of short circuit to GND of VCCA pin, a current limitation foldback scheme is implemented to reduce the current limitation to  $I_{CCA\_LIM\_FB}$  when  $V_{CCA}$  is below  $V_{CCA\_LIM\_FB}$ .

#### 6.7.4.2 Voltage monitoring

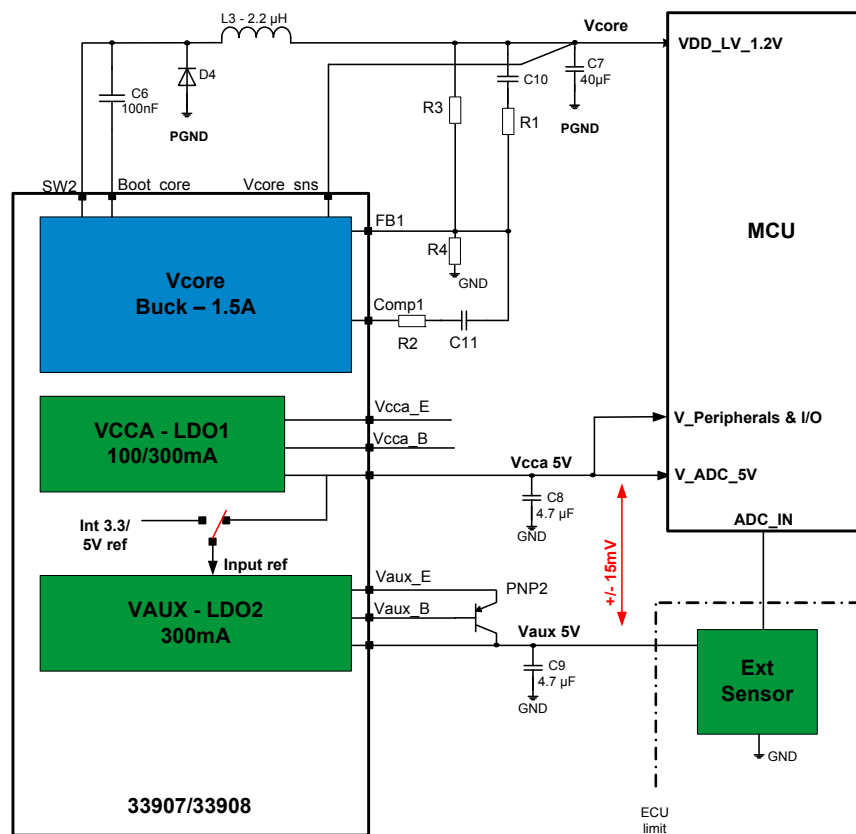
The overvoltage detection switches OFF the regulator. The regulator remains ON in case of undervoltage detection. Diagnostic is reported in the dedicated register, generate an Interrupt and may bring the application in Fail-safe state depending on the supervisor configuration (registers INIT SUPERVISOR 1, 2, 3).

### 6.7.5 VAUX voltage regulator

VAUX is a highly flexible linear voltage regulator that can be used either as an auxiliary supply dedicated to additional device in the ECU or as a sensor supply (i.e. outside the ECU). An external PNP transistor must be used (no internal current capability). If VAUX is not used in the application, VAUX\_E and SELECT pins must be connected to VPRE in order to not populate the external PNP as described in [Figure 60](#).

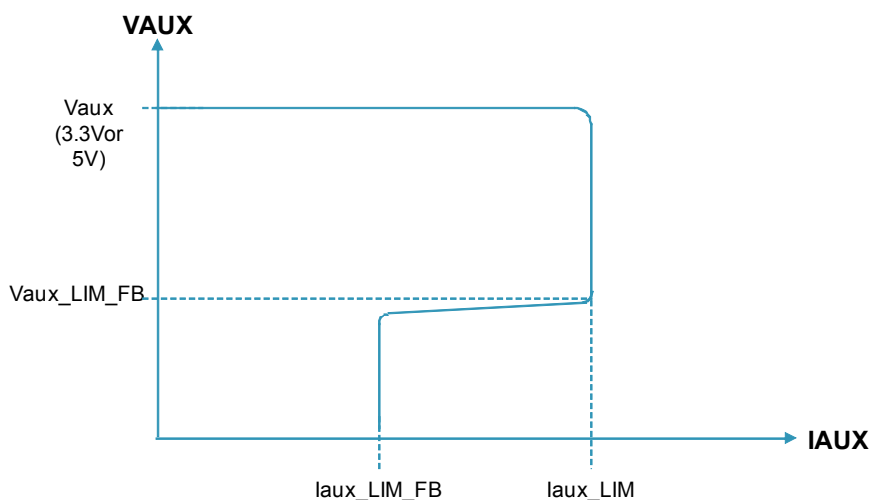
If VAUX is used as an auxiliary supply, the output voltage is selectable between 5.0 V, 3.3 V. Since this voltage rail can be used to supply MCU IOs, the selection is done with an external resistor connected between the SELECT pin and ground. In such case, the voltage accuracy is  $\pm 3.0\%$  with a maximum output current capability at 300 mA. If VAUX is used as a sensor supply rail, the output voltage is selectable between 5.0 V and 3.3 V. VCCA can be used as reference for the sensor supply used as tracker. The selection is done during the INIT phase and secured (bit  $V_{AUX\_TRK\_EN}$  in the register INIT VREG2). The tracking accuracy is  $\pm 15$  mV.





#### 6.7.5.1 Current limitation

A current limitation is implemented to avoid uncontrolled power dissipation of the external PNP transistor. The current is limited to  $I_{AUX\_LIM}$  and the regulator is switch OFF after a dedicated duration  $T_{AUX\_LIM\_OFF}$  under current limitation. A SPI command is needed to restart the regulator. In order to limit the power dissipation in the external PNP transistor in case of short-circuit to GND of VAUX pin, a current limitation foldback scheme is implemented to reduce the current limitation to  $I_{AUX\_LIM\_FB}$  when  $V_{AUX}$  is below  $V_{AUX\_LIM\_FB}$ .



### 6.7.5.2 Voltage monitoring

The overvoltage detection switches OFF the regulator. The regulator remains ON in case of undervoltage detection. Diagnostic is reported in the dedicated register, generate an Interrupt and may bring the application in Fail-safe state depending on the supervisor configuration (registers INIT SUPERVISOR 1, 2, 3).

### 6.7.6 CAN\_5V voltage regulator

The CAN\_5V voltage regulator is a linear regulator fully dedicated to the internal HSCAN interface. By default, the CAN\_5V regulator and the undervoltage detector are enabled, the overvoltage detector is disabled. The overvoltage detector can be enabled by SPI during INIT\_MAIN state.

If the overvoltage detector is enabled, the CAN\_5V regulator switches OFF when an overvoltage is detected. The undervoltage detector is disabled when the regulator is switched OFF reporting an undervoltage. Diagnostic is reported in the dedicated register and generate an Interrupt. The CAN\_5V regulator is not safety regulator. Consequently, the CAN\_5V voltage monitoring (overvoltage, undervoltage) will never assert RSTB or FS0B Fail-safe pins.

If the 33907/33908 internal CAN transceiver is not used in the application, the CAN\_5V regulator can be used to supply an external standalone CAN or FLEX-RAY transceiver, providing that the current load remains below the maximum current capability in all conditions. In that case, the internal CAN transceiver must be put in Sleep mode without wake-up capability.

### 6.7.7 Power dissipation

The 33907/33908 provides high performance SMPS and Linear regulators to supply high end MCU in automotive applications. Each regulator can deliver:

- $V_{PRE}$  (6.5V) up to 2.0 A
- $V_{CORE}$  (from 1.2 V to 3.3 V range) up to 0.8 A (33907) or up to 1.5 A (33908)
- $V_{CCA}$  (3.3 V or 5.0 V) up to 100 mA (with internal MOS) or up to 300 mA (with external PNP)
- $V_{AUX}$  (3.3 V or 5.0 V) up to 300 mA (with external PNP)
- $V_{CAN}$  (5.0 V) up to 100 mA

A thermal dissipation analysis has to be performed based on application use case to ensure the maximum silicon junction temperature does not exceed 150 °C.

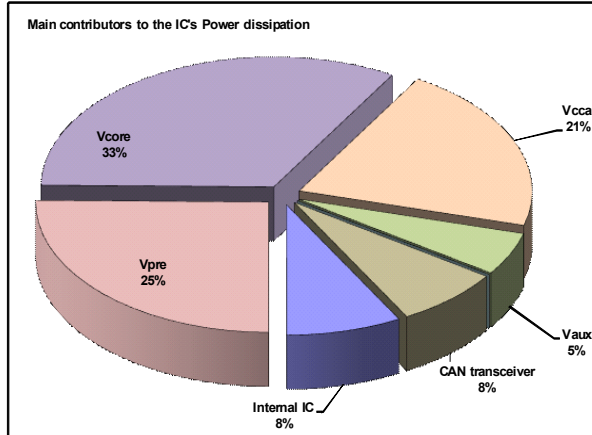
Two use cases covering the two main  $V_{CORE}$  voltage configurations are provided in [Figure 41](#).

- use case 1:  $V_{CORE} = 3.3$  V,  $I_{CORE} = 0.7$  A,  $V_{CCA}$  with int. MOS
- use case 2:  $V_{CORE} = 1.2$  V,  $I_{CORE} = 1.4$  A,  $V_{CCA}$  with ext. PNP

Both use cases have a total internal power dissipation below 0.9 W. A junction to ambient thermal resistivity of 30 °C/W allows the application to work up to 125 °C ambient temperature. A good soldering of the package expose pad is highly recommended to achieve such thermal performance.

Vsup = 14V and 25% of CAN traffic

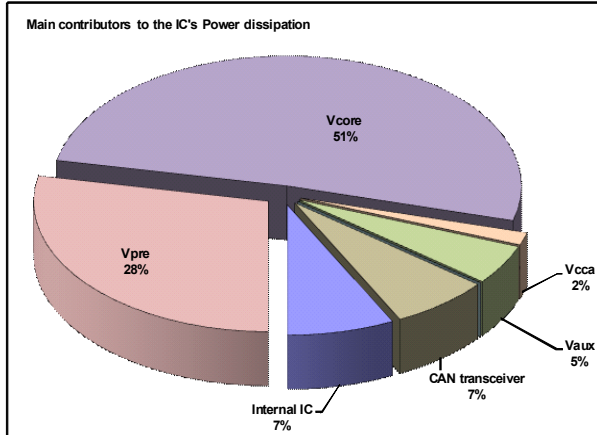
| Regulator | Voltage | Current | Comment  |
|-----------|---------|---------|----------|
| Vpre      | 6.V     | 670mA   |          |
| Vcore     | 3.3V    | 700mA   |          |
| Vcca      | 3.3V    | 50mA    | int. MOS |
| Vaux      | 5V      | 200mA   |          |



**TOTAL PDIS = 0.765 W**

use case 1: Vcore=3.3V, Icore=0.7A, Vcca with int. MOS

| Regulator | Voltage | Current | Comment  |
|-----------|---------|---------|----------|
| Vpre      | 6.V     | 800mA   |          |
| Vcore     | 3.3V    | 1.4A    |          |
| Vcca      | 3.3V    | 200mA   | ext. PNP |
| Vaux      | 5V      | 200mA   |          |



**TOTAL PDIS = 0.829 W**

use case 2: Vcore=1.2V, Icore=1.4A, Vcca with ext. PNP

- 1) CAN transceiver dissipation includes CAN\_5V regulator dissipation.
- 2) 25% CAN traffic means the CAN bus is dominant for 25% of time and recessive for the remaining 75%.

**Figure 41. Power dissipation use case**

The main contributors to the device power dissipation are VPRES, VCPRES, and VCPA (when used with internal PMOS) regulators. In comparison, the power dissipation from the Internal IC, VAUX and CAN transceiver are negligible. VPRES power dissipation is mainly induced by the loading of the regulators it is supplying, mainly VCPRES, VCPA and VAUX which are application dependant. The total device power dissipation, depending on the variation of these three regulators, is detailed in [Figure 42](#) with the environmental conditions in the associated table.

|        | Pdis VS Icore              | Pdis VS Icca               | Pdis VS Ipre   |
|--------|----------------------------|----------------------------|----------------|
| Vpre   | 6.5V                       | 6.5V                       | 6.5V           |
| Ipre   | Icore + Icca + Iaux + Ican | Icore + Icca + Iaux + Ican | From 0.5 to 2A |
| Vcore  | 3.3V and 1.2V              | 3.3V                       | 3.3V           |
| Icore  | from 0.25 to 1.5A          | 0.7A                       | 0.3A           |
| Vcca   | 3.3V                       | 3.3V and 5V                | 3.3V           |
| Icca   | 50mA                       | 20 to 100mA                | 50mA           |
| Vaux   | 3.3V                       | 3.3V                       | 3.3V           |
| Iaux   | 200mA                      | 200mA                      | 200mA          |
| CAN_5V | 5V                         | 5V                         | 5V             |
| Ican   | 33mA                       | 33mA                       | 33mA           |

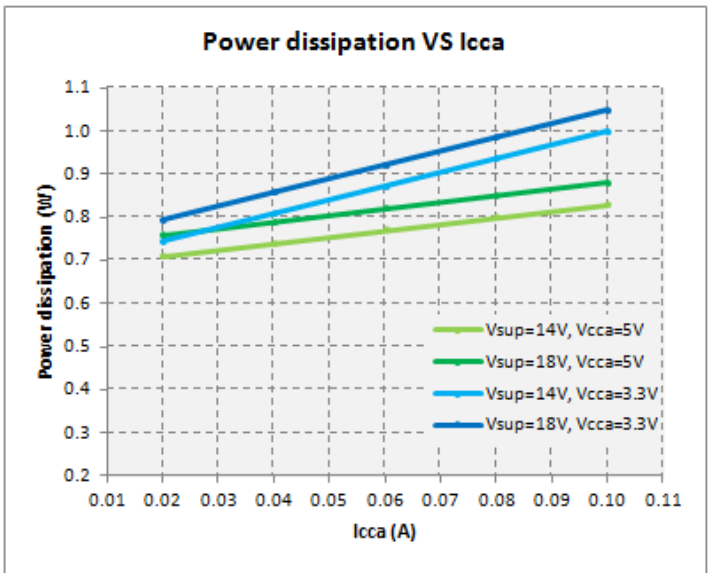
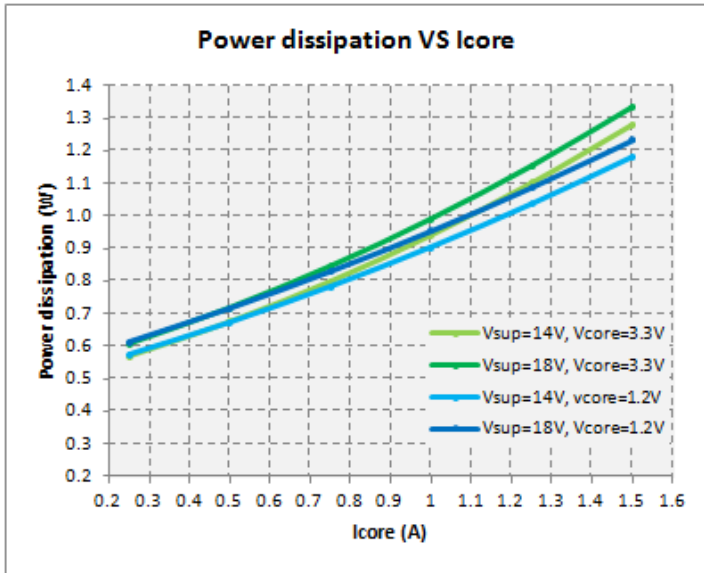
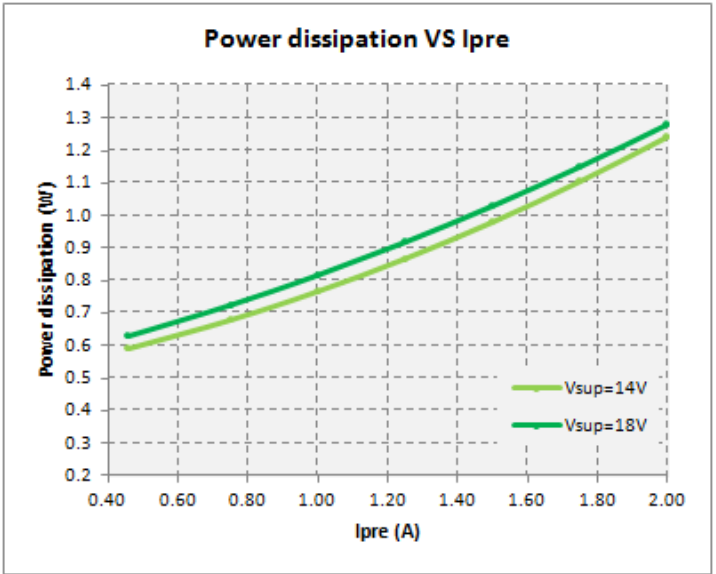
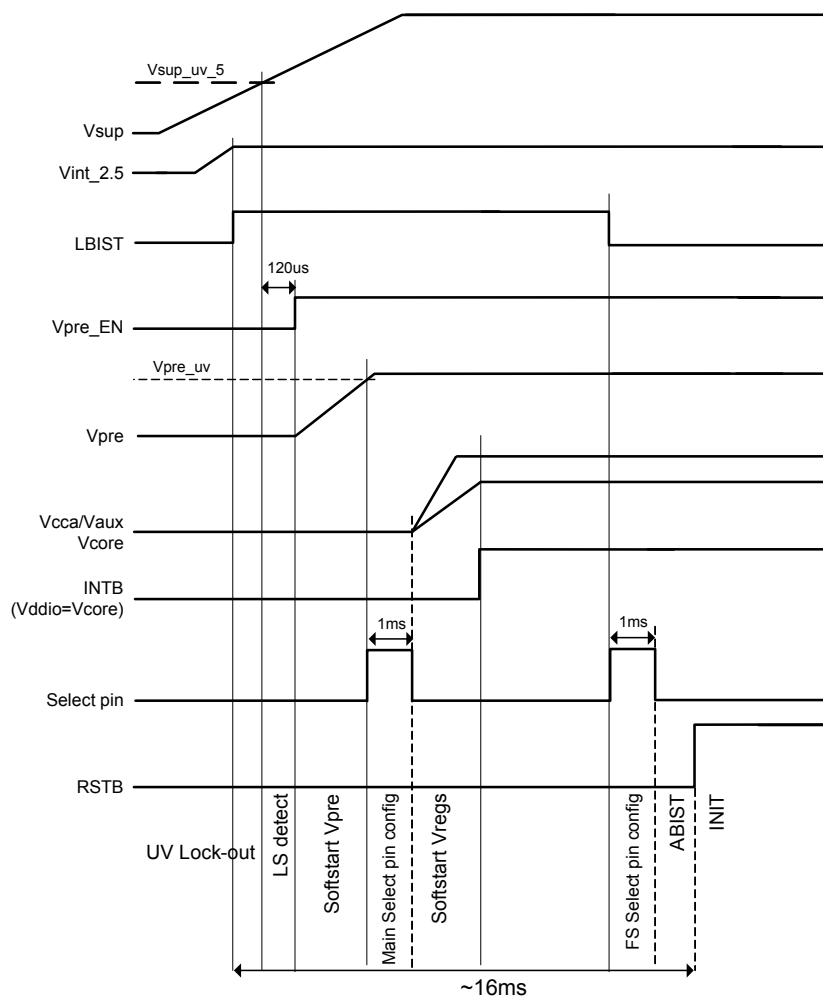


Figure 42. Power dissipation versus I<sub>CORE</sub>, I<sub>CCA</sub>, or I<sub>PRE</sub>

## 6.7.8 Start-up sequence

In order to provide a safe and well known start-up sequence, the 33907/33908 includes an undervoltage lock-out. This undervoltage lock-out is only applicable when the device is under a Power-On-Reset condition, which means the initial condition is  $V_{SUP} < V_{SUP\_UV\_L}$  (i.e. below 2.7 V max). In all the other conditions (i.e. LPOFF), the device is able to operate (and therefore to restart) down to  $V_{SUP\_UV\_L}$ . The other different voltage rails automatically start, as described in [Figure 43](#).



**Figure 43. Start-up scheme**

The final value of VAUX and VCCA depends on the hardware configuration (resistor values on the SELECT pin). The typical start up sequence takes around 16 ms to release RSTB. RSTB can be pulled low after those 16 ms by the MCU, if it is not ready to run after power up.

If an internal or external fault happen during this start up phase (ABIST fault due to regulator shorted for example), the 8.0 s timer monitoring the RSTB pin low, will finally send the device in Deep Fail-safe mode after 8.0 s.

## 6.8 CAN transceiver

The high speed CAN (Controller Area Network) transceiver provides the physical interface between the CAN protocol controller of an MCU and the physical dual wires CAN bus. It offers excellent EMC and ESD performance and meets the ISO 11898-2 and ISO11898-5 standards.

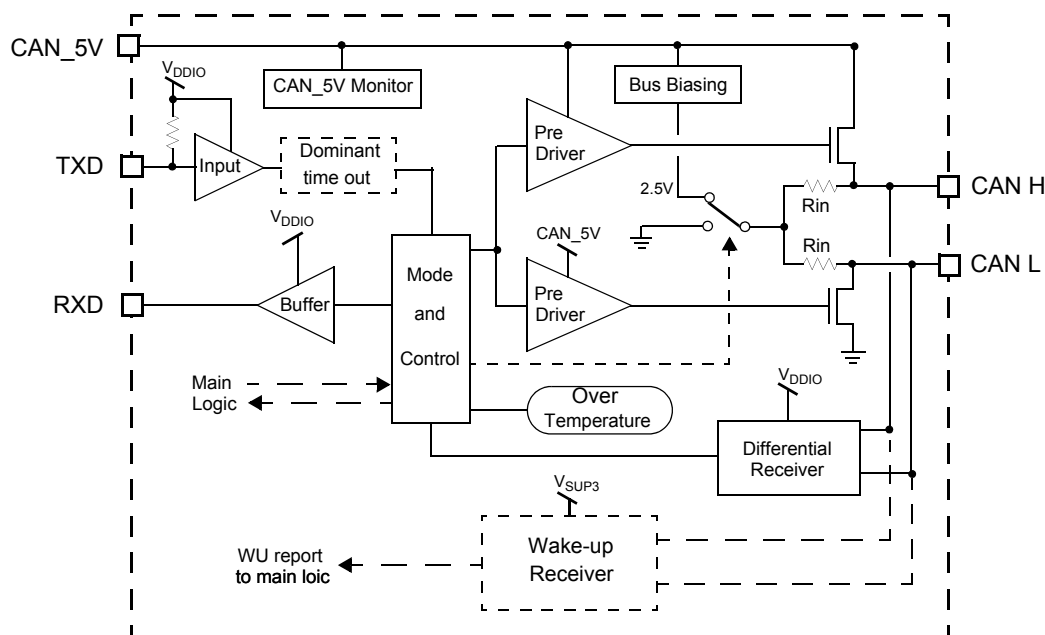


Figure 44. CAN simplified block diagram

### 6.8.1 Operating modes

#### 6.8.1.1 Normal mode

When CAN mode bits configuration is “11” (CAN in normal operation), the device is able to transmit information from TXD to the bus and report the bus level to the RXD pin. When TXD is high, CANH and CANL drivers are off and the bus is in the recessive state (unless it is in an application where another device drives the bus to the dominant state). When TXD is low, CANH and CANL drivers are ON and the bus is in the dominant state. When CAN mode bits configuration is “01” (CAN in listen only), the device is only able to report the bus level to the RXD pin. TXD driver is OFF and the device is NOT able to transmit information from TXD to the bus. TXD is maintained high by internal pull up resistor  $TXD_{PULL-UP}$  connected to VDDIO.

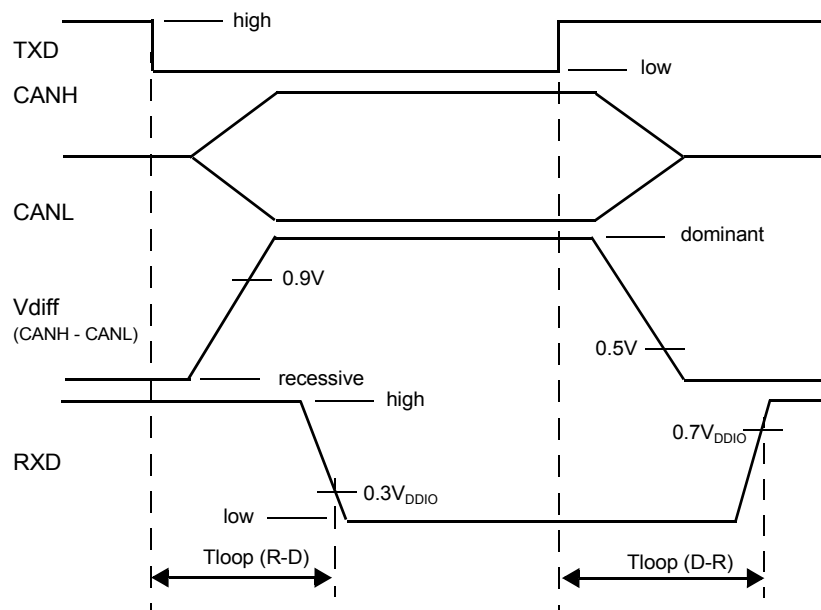


Figure 45. CAN timing diagram

### 6.8.1.2 Sleep mode

When the device is in LPOFF mode, the CAN transceiver is automatically set in Sleep mode with or without wake-up capability depending on CAN mode bits configuration. In that case, the CANH and CANL pins are pulled down to GND via the internal  $R_{IN}$  resistor, the TXD and RXD pins are pulled down to GND, both driver and receiver are OFF.

The CAN mode is automatically changed to Sleep with wake-up capability if not configured to Sleep without wake-up capability when the device enters is LPOFF. After LPOFF, the initial CAN mode prior to enter LPOFF is restored ([Figure 46](#)).

| CAN state before entering LPOFF |                              | CAN state in LPOFF |                              | CAN state after LPOFF |                              |
|---------------------------------|------------------------------|--------------------|------------------------------|-----------------------|------------------------------|
| CAN_mode [1:0]                  | CAN state                    | CAN_mode [1:0]     | CAN state                    | CAN_mode [1:0]        | CAN state                    |
| 0                               | Sleep, no wake-up capability | 0                  | Sleep, no wake-up capability | 0                     | Sleep, no wake-up capability |
| 1                               | Listen Only                  | 10                 | Sleep, wake-up capability    | 1                     | Listen Only                  |
| 10                              | Sleep, wake-up capability    |                    |                              | 10                    | Sleep, wake-up capability    |
| 11                              | Normal                       |                    |                              | 11                    | Normal                       |

Figure 46. CAN transition when device goes to LPOFF

## 6.8.2 Fault detection

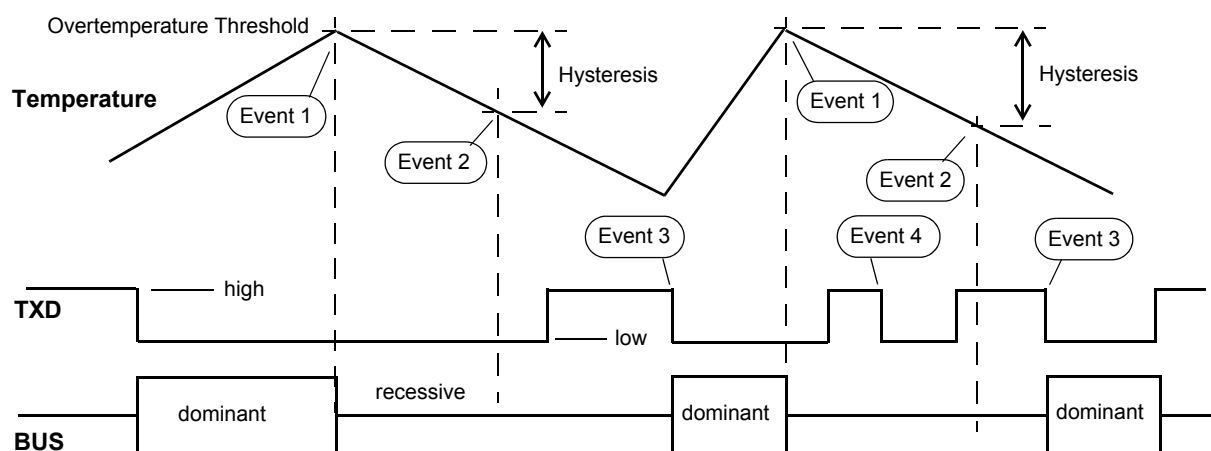
### 6.8.2.1 TXD permanent dominant (timeout)

If TXD is set low for a time longer than  $T_{DOUT}$  parameter, the CAN drivers are disabled, and the CAN bus will return to recessive state. The CAN receiver continues to operate. This prevent the bus to be set in dominant state permanently in case a failure set the TXD input to low level permanently.

The CAN\_mode MSB bit is set to 0 and the flag TXD\_dominant is reported in the Diag CAN1 register. The device recovers from this error detection after setting the CAN\_mode to Normal Operation and when a high level is detected on TXD. The TXD failure detection is operating when the CAN transceiver is in Normal mode and Listen only mode.







Event 1: over temperature detection. CAN driver disable.  
 Event 2: temperature falls below "overtemp. threshold minus hysteresis" => CAN driver remains disable.  
 Event 3: temperature below "overtemp. threshold minus hysteresis" and TxD high to low transition => CAN driver enable.  
 Event 4: temperature above "overtemp. threshold minus hysteresis" and TxD high to low transition => CAN driver remains disable.

**Figure 48. Overtemperature behavior**

## 6.8.2.6 Distinguish CAN diagnostics and CAN errors

The CAN errors can generate an interruption while the CAN diagnostics are reported in the digital for information only. The interruption generated by the CAN errors can be inhibited setting INT\_inh\_CAN bit at "1" in the "INIT INT" register.

The list of CAN Diagnostic and CAN Error bits is provided in [Table 11](#).

**Table 11. CAN diagnostic and CAN error bits**

| Register     | Bit           | Flag type  | Effect                       |
|--------------|---------------|------------|------------------------------|
| DIAG CAN1    | CANH_batt     | Diagnostic | No impact on CAN transceiver |
|              | CANH_gnd      | Diagnostic | No impact on CAN transceiver |
|              | CANL_batt     | Diagnostic | No impact on CAN transceiver |
|              | CANL_gnd      | Diagnostic | No impact on CAN transceiver |
|              | CAN_dominant  | Error      | Turn OFF CAN transceiver     |
|              | RXD_recessive | Error      | Turn OFF CAN transceiver     |
|              | TXD_dominant  | Error      | Turn OFF CAN transceiver     |
| DIAG CAN_LIN | CAN_OT        | Error      | Turn OFF CAN transceiver     |
|              | CAN_OC        | Diagnostic | No impact on CAN transceiver |

## 6.8.3 Wake-up mechanism

The device include bus monitoring circuitry to detect and report bus wake-ups when the device is in LPOFF and CAN mode configuration is different than Sleep/NO wake-up capability. Two wake-up detection are implemented: single dominant pulse and multiple dominants pulses. The wake-up mechanism is selected by SPI in the main logic and wake-up events are reported. The event must occur within the  $T_{3PTOX}$  timeout.  $T_{3PTOX} = T_{3PTO1}$  or  $T_{3PTO2}$  depending on the SPI selection.

### 6.8.3.1 Single pulse detection

In order to activate wake-up report, 1 event must occur on the CAN bus:

- event 1: a dominant level for a time longer than  $T_{1PWU}$

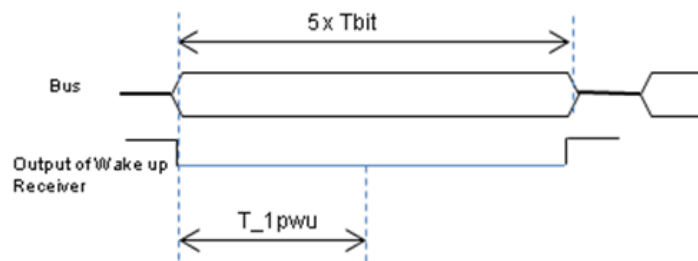


Figure 49. Single pulse wake-up pattern illustration

### 6.8.3.2 Multiple pulse detection

In order to activate wake-up report, three events must occur on the CAN bus:

- event 1: a dominant level for a time longer than  $t_{1PWU}$  followed by
- event 2: a recessive level (event 2) longer than  $t_{3PWU}$  followed by
- event 3: a dominant level (event 3) longer than  $t_{3PWU}$ .

The three events and the timeout function avoid that a permanent dominant state on the bus generates permanent wake-up situation which would prevent system to enter in low-power mode.

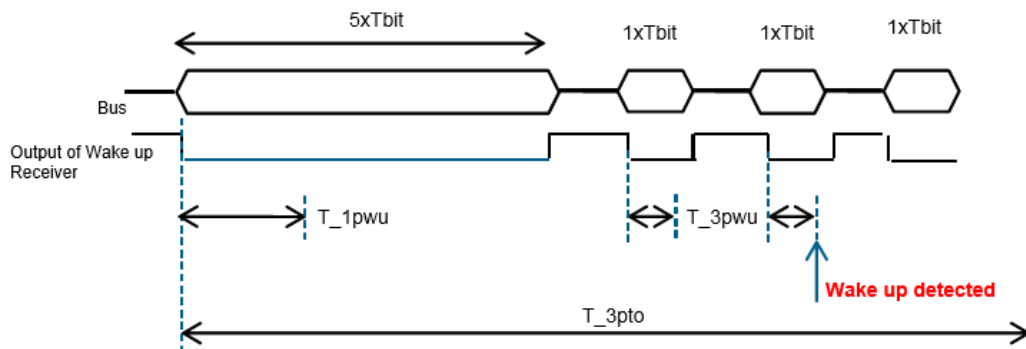


Figure 50. Multiple pulse wake-up pattern illustration

## 6.9 LIN transceiver

This chapter applies to 33907L and 33908L versions.

The Local Interconnect Network (LIN) is a serial communication protocol, designed to support automotive networks in conjunction with a Controller Area Network (CAN). The LIN transceiver is operational from a  $V_{SUP}$  of 7.0 V to 18 V DC and compatible with LIN Protocol Specification 1.3, 2.0, 2.1, 2.2 and SAEJ2602-2.

### 6.9.1 Simplified block diagram

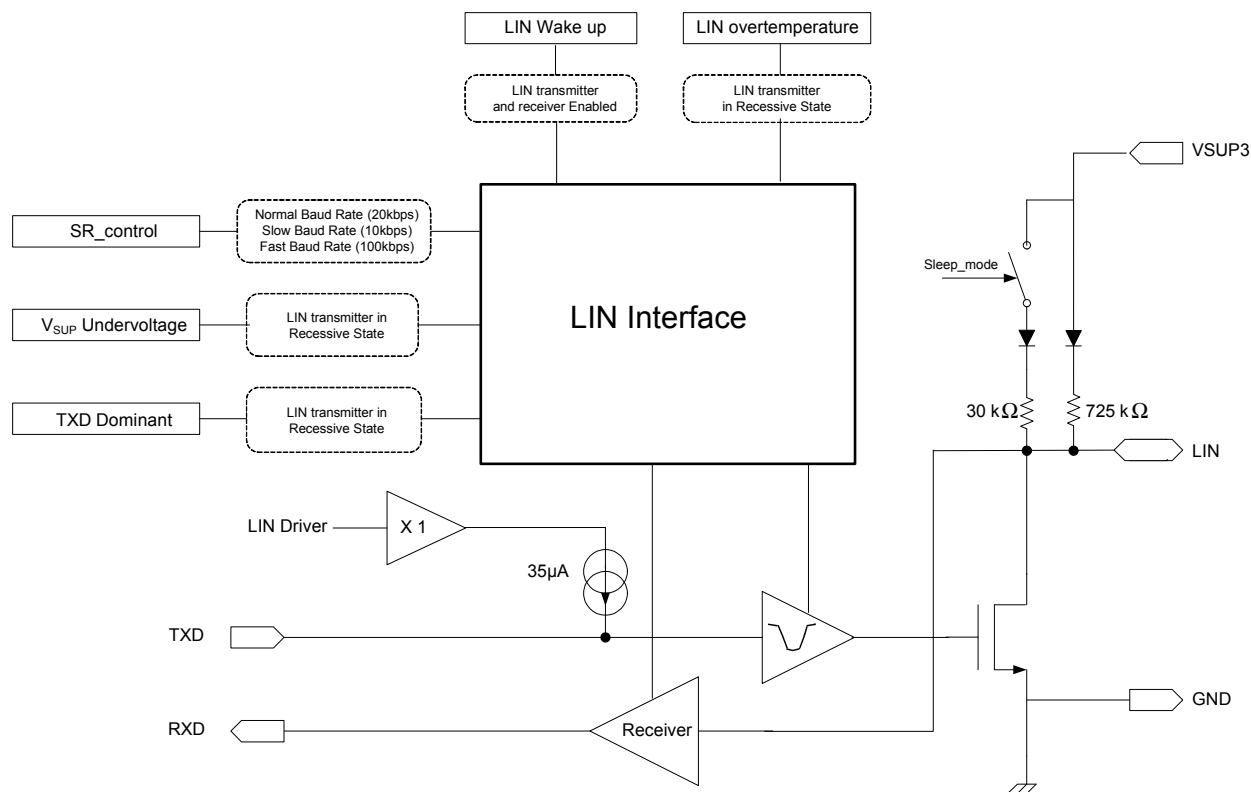


Figure 51. LIN simplified block diagram

### 6.9.2 Operating modes

#### 6.9.2.1 Normal mode

When LIN mode bits configuration is “11” (LIN in normal operation), the device is able to transmit information from TXDL to the bus and report the bus level to the RXDL pin. When TXDL is high, LIN driver is OFF and the bus is in the recessive state (unless it is in an application where another device drives the bus to the dominant state). When TXDL is low, LIN driver is ON and the bus is in the dominant state.

When LIN mode bits configuration is “01” (LIN in listen only), the device is only able to report the bus level to the RXDL pin. TXDL driver is OFF and the device is NOT able to transmit information from TXDL to the bus. TXDL is maintained high by internal pull-up resistor TXDL<sub>PULL-UP</sub> connected to VDDIO.

#### 6.9.2.2 Sleep mode

When the device is in LPOFF mode, the LIN transceiver is automatically set in Sleep mode with or without wake-up capability depending on LIN mode bits configuration. In that case, the LIN pin is pulled up to  $V_{SUP}$  via the internal resistor and diode structure, the TXDL and RXDL pins are pulled down to GND.

### 6.9.3 Baud rate selection

The device has two selectable baud rates: 20 kB/s for Normal Baud rate and 10 kB/s for slow baud rate. An additional fast baud rate (100 kB/s) can be used to flash the MCU or in the garage for diagnostic. The LIN Consortium specification does not specified electrical parameters for this baud rate. The communication only is guaranteed. The baud rate selection is done by SPI setting during the INIT phase of the main logic. Depending of the baud rate setting, the corresponding LIN slope control is automatically selected.

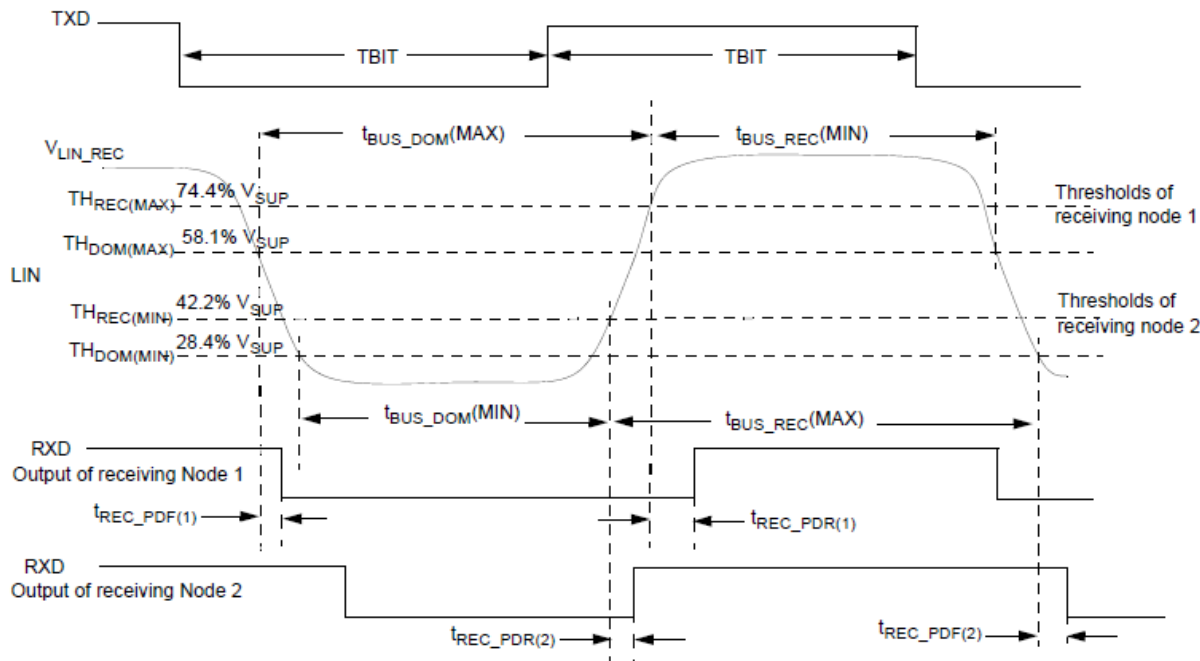


Figure 52. LIN timings for normal baud rate (20 kB/s)

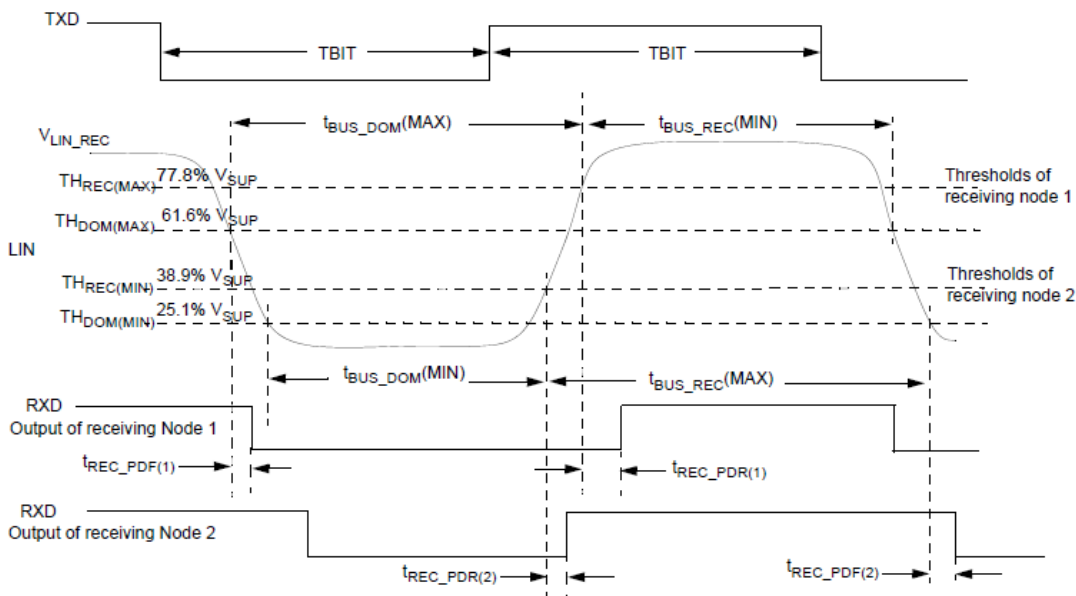


Figure 53. LIN timings for slow baud rate (10 kB/s)

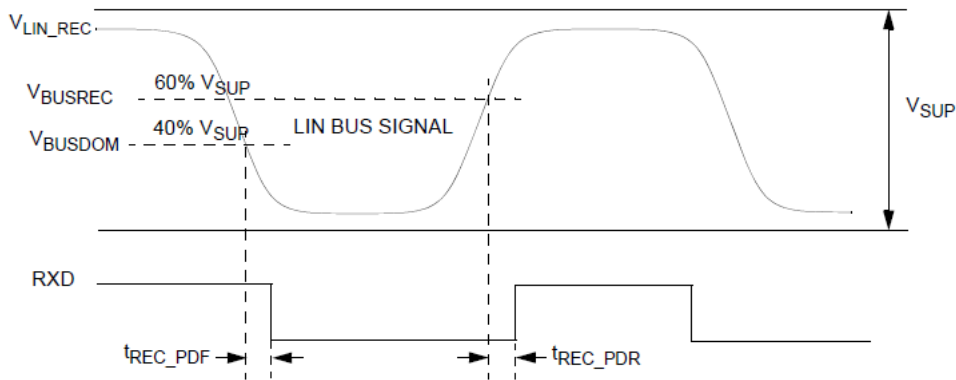


Figure 54. LIN receiver timings

## 6.9.4 Fault detection

### 6.9.4.1 VSUP undervoltage

A  $V_{SUP}$  undervoltage ( $V_{LIN\_UV}$ ) detection is implemented to be compliant with SAEJ2602-2 standard. At low  $V_{SUP}$  voltage ( $V_{SUP} < V_{LIN\_UV}$ ), the LIN bus goes in recessive state to avoid wrong communication.

### 6.9.4.2 TXDL permanent dominant (timeout)

If TXDL is set low for a time longer than  $t_{XD\_DOM}$  parameter, the LIN driver is disabled and the LIN bus will return to recessive state. This prevents the bus to be set in dominant state permanently, in case a failure sets the TXDL input permanently to a low level.

The LIN receiver continues to operate. The LIN\_mode MSB bit is set to 0 and the flag TXDL\_dominant is reported in the Diag CAN\_LIN register. The device recovers from this error detection after setting the LIN\_mode to normal operation and when a high level is detected on TXDL. The TXDL failure detection is operating when the LIN transceiver is in Normal mode and Listen Only mode.

### 6.9.4.3 RXDL permanent recessive

If RXDL is detected high for seven consecutive receive/dominant cycles, the LIN driver and receiver are disabled and the LIN bus returns to recessive state. The LIN\_mode MSB bit is set to 0 and the flag RXDL\_recessive is reported in the Diag CAN\_LIN register. The device recovers from this error detection after setting the LIN\_mode to normal operation, and when a high level is detected on TXDL. The RXDL failure detection is operating when the LIN transceiver is in Normal mode and Listen Only mode.

### 6.9.4.4 LIN bus short-circuit

If the LIN bus is dominant for a time longer than  $t_{LIN\_SHORT\_GND}$ , due for instance to an external short-circuit to GND, the detection is reported to the device main logic. The BUS bus failure detection is operating when the LIN transceiver is in Normal mode and Listen Only mode.

### 6.9.4.5 LIN current limitation

In case of LIN short-circuit to Battery, the current flowing out of the LIN driver is limited to 200 mA (parameter  $I_{BUS\_LIM}$ ), and the LIN driver is not shut down. The LIN bus goes in recessive state when the current limitation occurs and returns in the same functional mode as before failure when the current falls below the current limitation value.

### 6.9.4.6 LIN overtemperature

If the driver temperature exceeds the TSD ( $t_{LIN\_SD}$ ), the LIN driver is disabled and the LIN bus will return to recessive state. The LIN receiver continues to operate. The LIN\_mode MSB bit is set to 0 and the flag LIN\_OT is reported in the Diag CAN\_LIN register.

A hysteresis is implemented in this protection feature. The LIN driver remain disabled until the temperature has fallen below the OT threshold minus hysteresis. The device recovers from this error detection after setting the LIN\_mode to normal operation, and when a high level is detected on TXDL.

### 6.9.4.7 LIN errors

The interruption generated by the LIN errors can be inhibited setting INT\_inh\_LIN bit at “1” in the “INIT INT” register. The list of LIN error bits is provided in [Table 12](#).

Table 12. LIN error bits

| Register     | Bit            | Flag type | Effect                   |
|--------------|----------------|-----------|--------------------------|
| DIAG CAN_LIN | LIN_dominant   | Error     | Turn OFF LIN transceiver |
|              | RXDL_recessive | Error     | Turn OFF LIN transceiver |
|              | TXDL_dominant  | Error     | Turn OFF LIN transceiver |
|              | LIN_OT         | Error     | Turn OFF LIN transceiver |

### 6.9.5 Wake-up mechanism

The device can wake-up by a LIN dominant pulse longer than  $t_{BUS\_WU}$ . Dominant pulse means: a recessive to dominant transition, wait for  $t > t_{BUS\_WU}$ , then a dominant to recessive transition.

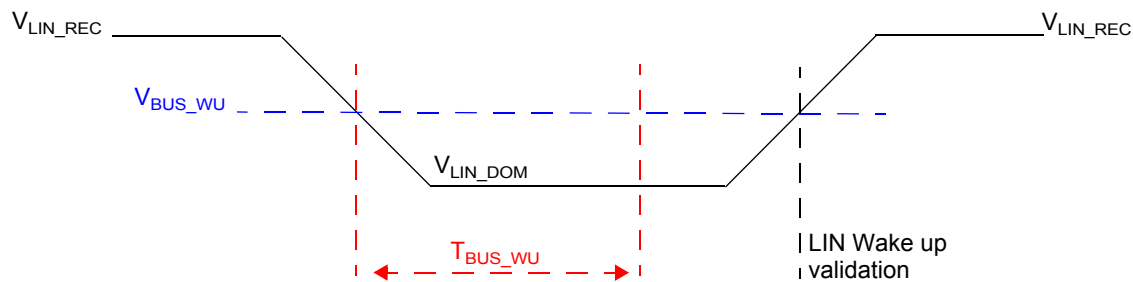


Figure 55. LIN wake-up pattern illustration

# 7 Serial peripheral interface

## 7.1 High level overview

### 7.1.1 SPI

The device is using a 16 bits SPI, with the following arrangement:

MOSI, Master Out Slave In bits:

- Bit 15 read/write
- Bit 14 Main or fail-safe register target
- bit 13 to 9 (A4 to A0) to select the register address. Bit 8 is a parity bit in write mode, Next bit (=0) in read mode.
- bit7 to 0 (D7 to D0): control bits

MISO, Master IN Slave Out bits:

- bits 15 to 8 (S15 to S8) are device status bits
- bits 7 to 0 (Do7 to Do0) are either extended device status bits, device internal control register content or device flags.

[Figure 56](#) is an overview of the SPI implementation.

### 7.1.2 Parity bit 8 calculation

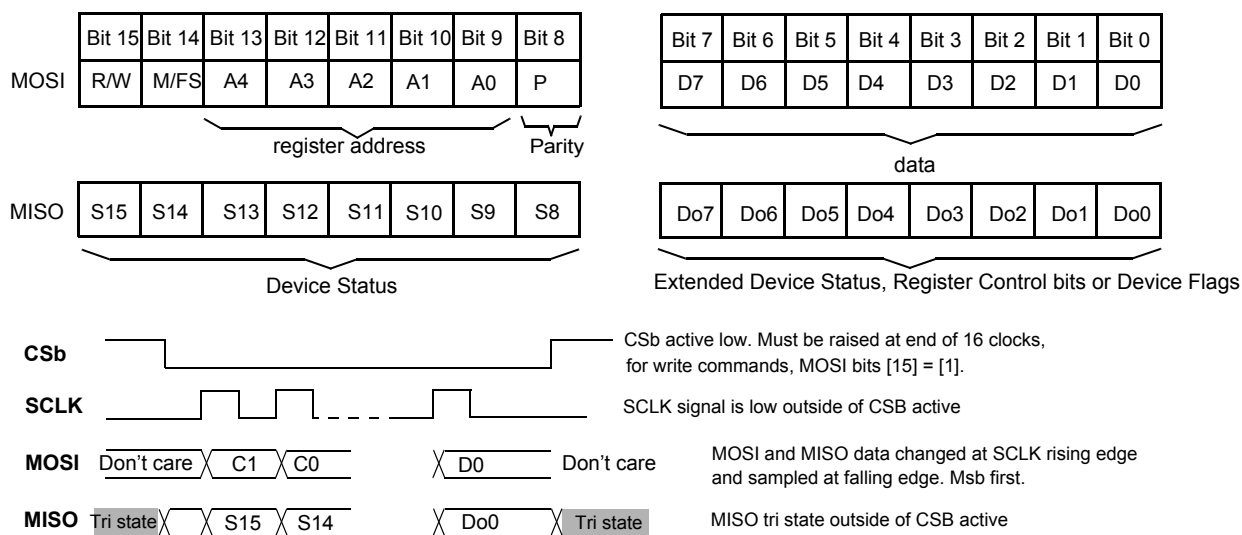
The parity is used for write to register command (bit 15,14 = 01). It is calculated based on the number of logic ones contained in bits 15-9, 7-0 sequence (this is the whole 16-bits of the write command except bit 8).

Bit 8 must be set to 0 if the number of 1 is odd.

Bit 8 must be set to 1 if the number of 1 is even.

### 7.1.3 Device status on MISO

When a write operation is performed to store data or control bit into the device, MISO pin reports a 16-bit fixed device status composed of two bytes: Device Fixed Status (bits 15 to 8) + extended Device Status (bits 7 to 0). In a read operation, MISO reports the fixed device status (bits 15 to 8), and the next eight bits are content of the selected register. A standard serial peripheral interface (SPI) is integrated to allow bi-directional communication between the 33907/33908 and the MCU. The SPI is used for configuration and diagnostic purposes.



SPI wave form, and signals polarity

Figure 56. SPI overview

The device contains several registers. Their address is coded on 7 bits (bits 15 to 9). Each register controls or reports part of the device function. Data can be written to the register, to control the device operation or set default value or behavior. Every register can also be read back in order to ensure that its content (default setting or value previously written) is correct.

## 7.1.4 Register description

Although the minimum time between two NCS low sequences is defined by  $t_{ONNCS}$  (Figure 57), two consecutive accesses to the fail-safe registers must be done with a 3.5  $\mu$ s minimum NCS high time in between. Although the minimum time between two fail-safe registers accesses is 3.5  $\mu$ s, some SPI accesses to the main registers can be done in between (Figure 57).

## 7.2 Detail operation

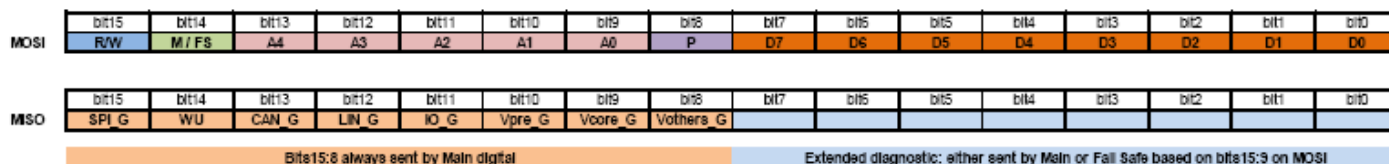


Figure 57. MOSI / MISO SPI command organization

Table 13. MOSI bits description

|        |             |  |
|--------|-------------|--|
| R / W  | Description | Set if it is a READ or WRITE Command                               |
|        | 0           | READ   |
|        | 1           | WRITE  |
| M / FS | Description | Split the addresses between Fail-safe State machine and main Logic |
|        | 0           | Main   |
|        | 1           | Fail-safe  |
| A4:0   | Description | Set the address to Read or Write                                   |
|        | 0           | See Register Mapping   |
|        | 1           |  |
| P      | Description | Parity bit (only use in Write mode). Set to 0 in Read mode         |
|        | 0           | Number of "1" (bit15:9 and bit 7:0) is odd                         |
|        | 1           | Number of "1" (bit15:9) and bit 7:0) is even                       |
| D7:0   | Description | Data in Write mode. Shall be set to 00h in Read mode               |
|        | 0           | See Register Details   |
|        | 1           |  |



**Table 14. MISO bits description**

|           |                 |  |
|-----------|-----------------|--|
| SPI_G     | Description     | Report an error in the SPI communication   |
|           | 0               | No Failure   |
|           | 1               | Failure  |
|           | Reset Condition | Power On Reset / When initial event cleared on read  |
| WU        | Description     | Report a wake-up event. Logical OR of all wake-up sources  |
|           | 0               | No WU event  |
|           | 1               | WU event   |
|           | Reset Condition | Power On Reset / When initial event cleared on read  |
| CAN_G     | Description     | Report a CAN event (Diagnostic)  |
|           | 0               | No event   |
|           | 1               | CAN event  |
|           | Reset Condition | Power On Reset / When initial event cleared on read  |
| LIN_G     | Description     | Report a LIN event (diagnostic)  |
|           | 0               | No event   |
|           | 1               | LIN event  |
|           | Reset Condition | Power On Reset / When initial event cleared on read  |
| IO_G      | Description     | Report a change in IOs state   |
|           | 0               | No IO transition   |
|           | 1               | IO transition  |
|           | Reset Condition | Power On Reset / when initial event cleared on read  |
| VPRE_G    | Description     | Report an event from V <sub>PRE-REGULATOR</sub> and battery monitoring (status change or failure)                    |
|           | 0               | No event   |
|           | 1               | Event occurred   |
|           | Reset Condition | Power On Reset / when initial event cleared on read  |
| VCORE_G   | Description     | Report an event from V <sub>CORE</sub> regulator (status change or failure)  |
|           | 0               | No event   |
|           | 1               | Event occurred   |
|           | Reset Condition | Power On Reset / when initial event cleared on read  |
| VOTHERS_G | Description     | Report an event from V <sub>CCA</sub> , V <sub>AUX</sub> , or V <sub>CAN</sub> regulators (status change or failure) |
|           | 0               | No event   |
|           | 1               | Event occurred   |
|           | Reset Condition | Power On Reset / when initial event cleared on read  |

SPI\_G = SPI\_err or SPI\_clk or SPI\_Req or SPI\_Parity or SPI\_FS\_err or SPI\_FS\_clk or SPI\_FS\_Req or SPI\_FS\_Parity

WU\_G = IO\_5\_WU or IO\_4\_WU or IO\_3\_WU or IO\_2\_WU or IO\_1\_WU or IO\_0\_WU or PHY\_WU

CAN\_G = CANH\_BATT or CANH\_GND or CANL\_BATT or CANL\_GND or CAN\_dominant or RXD\_recessive or TXD\_dominant or CAN\_OT or CAN\_OC

LIN\_G = LIN\_OT or RXDL\_recessive or TXDL\_dominant or LIN\_dominant

IO\_G = IO\_5 or IO\_4 or IO\_3 or IO\_2 or IO\_1 or IO\_0

Vpre\_G = VSNS\_UV or VSUP\_UV\_7 or IPFF or ILIM\_PRE or TWARN\_PRE or BOB or VPRE\_STATE\_flag or VPRE\_OV or VPRE\_UV

Vcore\_G = ILIM\_CORE or TWARN\_CORE or VCORE\_STATE\_flag or VCORE\_OV or VCORE\_UV

Vothers\_G = ILIM\_CCA or TWARN\_CCA or TSD\_CCA or ILIM\_CCA\_OFF or VCCA\_UV or VCCA\_OV or ILIM\_AUX or VAUX\_TSD or ILIM\_AUX\_OFF or VAUX\_OV or VAUX\_UV or ILIM\_CAN or VCAN\_UV or VCAN\_OV or TSD\_CAN

## 7.2.1 Register address table

Table 15 is a list of device registers and addresses coded in bits 13 to 9 in MOSI for main logic.

**Table 15. Register mapping of main logic**

| Register      | Address |    |    |    |    |    |          | Write description                      | Table ref                |
|---------------|---------|----|----|----|----|----|----------|--|--------------------------|
|               | FS/M    | A4 | A3 | A2 | A1 | A0 | Hex      |  |                          |
| NOT USED      | 0       | 0  | 0  | 0  | 0  | 0  | #0(00h)  | N/A                                    | N/A                      |
| INIT Vreg 1   | 0       | 0  | 0  | 0  | 0  | 1  | #1(01h)  | Write during INIT phase then read only | <a href="#">Table 18</a> |
| INIT Vreg2    | 0       | 0  | 0  | 0  | 1  | 0  | #2(02h)  | Write during INIT phase then read only | <a href="#">Table 20</a> |
| INIT CAN_LIN  | 0       | 0  | 0  | 0  | 1  | 1  | #3(03h)  | Write during INIT phase then read only | <a href="#">Table 22</a> |
| INIT IO_WU1   | 0       | 0  | 0  | 1  | 0  | 0  | #4(04h)  | Write during INIT phase then read only | <a href="#">Table 24</a> |
| INIT IO_WU2   | 0       | 0  | 0  | 1  | 0  | 1  | #5(05h)  | Write during INIT phase then read only | <a href="#">Table 26</a> |
| INIT INT      | 0       | 0  | 0  | 1  | 1  | 0  | #6(06h)  | Write during INIT phase then read only | <a href="#">Table 28</a> |
| NOT USED      | 0       | 0  | 0  | 1  | 1  | 1  | #7(07h)  | N/A                                    | N/A                      |
| HW Config     | 0       | 0  | 1  | 0  | 0  | 0  | #8(08h)  | Read only                              | <a href="#">Table 30</a> |
| WU Source     | 0       | 0  | 1  | 0  | 0  | 1  | #9(09h)  | Read only                              | <a href="#">Table 32</a> |
| NOT USED      | 0       | 0  | 1  | 0  | 1  | 0  | #10(0Ah) | N/A                                    | N/A                      |
| IO_input      | 0       | 0  | 1  | 0  | 1  | 1  | #11(0Bh) | Read only                              | <a href="#">Table 34</a> |
| Status Vreg#1 | 0       | 0  | 1  | 1  | 0  | 0  | #12(0Ch) | Read only                              | <a href="#">Table 36</a> |
| Status Vreg#2 | 0       | 0  | 1  | 1  | 0  | 1  | #13(0Dh) | Read only                              | <a href="#">Table 38</a> |
| Diag Vreg#1   | 0       | 0  | 1  | 1  | 1  | 0  | #14(0Eh) | Read only                              | <a href="#">Table 40</a> |
| Diag Vreg#2   | 0       | 0  | 1  | 1  | 1  | 1  | #15(0Fh) | Read only                              | <a href="#">Table 42</a> |
| Diag Vreg#3   | 0       | 1  | 0  | 0  | 0  | 0  | #16(10h) | Read only                              | <a href="#">Table 44</a> |
| Diag CAN1     | 0       | 1  | 0  | 0  | 0  | 1  | #17(11h) | Read only                              | <a href="#">Table 46</a> |
| Diag CAN_LIN  | 0       | 1  | 0  | 0  | 1  | 0  | #18(12h) | Read only                              | <a href="#">Table 48</a> |
| Diag SPI      | 0       | 1  | 0  | 0  | 1  | 1  | #19(13h) | Read only                              | <a href="#">Table 50</a> |
| NOT USED      | 0       | 1  | 0  | 1  | 0  | 0  | #20(14h) | N/A                                    | N/A                      |
| MODE          | 0       | 1  | 0  | 1  | 0  | 1  | #21(15h) | Write during Normal and Read           | <a href="#">Table 52</a> |
| Vreg Mode     | 0       | 1  | 0  | 1  | 1  | 0  | #22(16h) | Write during Normal and Read           | <a href="#">Table 54</a> |
| IO_OUT/AMUX   | 0       | 1  | 0  | 1  | 1  | 1  | #23(17h) | Write during Normal and Read           | <a href="#">Table 56</a> |
| CAN_LIN Mode  | 0       | 1  | 1  | 0  | 0  | 0  | #24(18h) | Write during Normal and Read           | <a href="#">Table 58</a> |
| CAN Mode 2    | 0       | 1  | 1  | 0  | 0  | 1  | #25(19h) | Write during Normal and Read           | <a href="#">Table 60</a> |

Table 16 is a list of device registers and addresses coded in bits 13 to 9 in MOSI for fail-safe logic

**Table 16. Register mapping of fail-safe logic**

| Register          | Address |    |    |    |    |    |          | Write description                      | Table ref                |
|-------------------|---------|----|----|----|----|----|----------|--|--------------------------|
|                   | FS/M    | A4 | A3 | A2 | A1 | A0 | Hex      |  |                          |
| INIT Supervisor#1 | 1       | 0  | 0  | 0  | 0  | 1  | #33(21h) | Write during INIT phase then Read only | <a href="#">Table 62</a> |
| INIT Supervisor#2 | 1       | 0  | 0  | 0  | 1  | 0  | #34(22h) | Write during INIT phase then Read only | <a href="#">Table 64</a> |
| INIT Supervisor#3 | 1       | 0  | 0  | 0  | 1  | 1  | #35(23h) | Write during INIT phase then Read only | <a href="#">Table 66</a> |
| INIT FSSM#1       | 1       | 0  | 0  | 1  | 0  | 0  | #36(24h) | Write during INIT phase then Read only | <a href="#">Table 68</a> |
| INIT FSSM#2       | 1       | 0  | 0  | 1  | 0  | 1  | #37(25h) | Write during INIT phase then Read only | <a href="#">Table 70</a> |
| WD_Window         | 1       | 0  | 0  | 1  | 1  | 0  | #38(26h) | Write (No restriction) and Read        | <a href="#">Table 72</a> |

**Table 16. Register mapping of fail-safe logic (continued)**

| Register     | Address |    |    |    |    |    |          | Write description                      | Table ref                |
|--------------|---------|----|----|----|----|----|----------|--|--------------------------|
|              | FS/M    | A4 | A3 | A2 | A1 | A0 | Hex      |  |                          |
| WD_LFSR      | 1       | 0  | 0  | 1  | 1  | 1  | #39(27h) | Write (No restriction) and Read        | <a href="#">Table 74</a> |
| WD_answer    | 1       | 0  | 1  | 0  | 0  | 0  | #40(28h) | Write (No restriction) and Read        | <a href="#">Table 76</a> |
| FS_OUT       | 1       | 0  | 1  | 0  | 0  | 1  | #41(29h) | Write (No restriction)                 | <a href="#">Table 78</a> |
| RSTb request | 1       | 0  | 1  | 0  | 1  | 0  | #42(2Ah) | Write (No restriction)                 | <a href="#">Table 80</a> |
| INIT WD      | 1       | 0  | 1  | 0  | 1  | 1  | #43(2Bh) | Write during INIT phase then Read only | <a href="#">Table 82</a> |
| Diag FS1     | 1       | 0  | 1  | 1  | 0  | 0  | #44(2Ch) | Read only                              | <a href="#">Table 84</a> |
| WD_Counter   | 1       | 0  | 1  | 1  | 0  | 1  | #45(2Dh) | Read only                              | <a href="#">Table 86</a> |
| Diag_FS2     | 1       | 0  | 1  | 1  | 1  | 0  | #46(2Eh) | Read only                              | <a href="#">Table 88</a> |

## 7.2.2 Secured SPI command

Some SPI commands must be secured to avoid unwanted change of the critical bits. In the fail-safe machine and in the main state machine, the secured bits are calculated from the data bits sent as follows:

**Table 17. Secured SPI**

| Bit7   | Bit6   | Bit5   | Bit4   | Bit3     | Bit2    | Bit1     | Bit0     |
|--------|--------|--------|--------|----------|---------|----------|----------|
| Data 3 | Data 2 | Data 1 | Data 0 | Secure 3 | Secure2 | Secure 1 | Secure 0 |

- Secure 3 = NOT(Bit5)
- Secure 2 = NOT(Bit4)
- Secure 1 = Bit7
- Secure 0 = Bit6

## 7.3 Detail of register mapping

### 7.3.1 Init VREG 1

Table 18. INIT VREG1 register configuration

| Write |       |       |       |       |       |        |         |           |      |           |          |           |      |      |           |          |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|------|-----------|----------|-----------|------|------|-----------|----------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7 | bit6      | bit5     | bit4      | bit3 | bit2 | bit1      | bit0     |
| MOSI  | 1     | 0     | 0     | 0     | 0     | 0      | 1       | P         | 0    | 0         | Ipff_DIS | 0         | 0    | 0    | 0         | Vcore_FB |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | 0    | Reserve_d | Ipff_DIS | Reserve_d | 0    | 0    | Reserve_d | Vcore_FB |
| Read  |       |       |       |       |       |        |         |           |      |           |          |           |      |      |           |          |
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7 | bit6      | bit5     | bit4      | bit3 | bit2 | bit1      | bit0     |
| MOSI  | 0     | 0     | 0     | 0     | 0     | 0      | 1       | 0         | 0    | 0         | 0        | 0         | 0    | 0    | 0         | 0        |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | 0    | Reserve_d | Ipff_DIS | Reserve_d | 0    | 0    | Reserve_d | Vcore_FB |

Table 19. Description and configuration of the bits (Default value in bold)

|          |                 |  |
|----------|-----------------|--|
| IPFF_DIS | Description     | DISABLE the input Power Feed Forward (IPFF) function of $V_{PRE}$                            |
|          | 0               | <b>ENABLED</b>   |
|          | 1               | DISABLED   |
|          | Reset condition | Power On Reset   |
| Vcore_FB | Description     | Configure the monitoring of the second $V_{CORE}$ resistor string                            |
|          | 0               | <b>No Monitoring (IO_1 is used as analog &amp; digital input)</b>                            |
|          | 1               | Monitoring enabled (IO_1 can NOT be used for analog/digital input neither for WU from LPOFF) |
|          | Reset condition | Power On Reset   |

### 7.3.2 Init Vreg 2

Table 20. INIT VREG2 register configuration

| Write |       |       |       |       |       |        |         |           |      |              |          |      |      |              |             |          |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|------|--------------|----------|------|------|--------------|-------------|----------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7 | bit6         | bit5     | bit4 | bit3 | bit2         | bit1        | bit0     |
| MOSI  | 1     | 0     | 0     | 0     | 0     | 1      | 0       | P         | 0    | Tcca_lim_off | Icca_lim | 0    | 0    | Taux_lim_off | Vaux_trk_EN | 0        |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | 0    | Tcca_lim_off | Icca_lim | 0    | 0    | Taux_lim_off | Vaux_trk_EN | reserved |

Table 20. INIT VREG2 register configuration (continued)

| Read |       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| MOSI | 0     | 0     | 0     | 0     | 0     | 1     | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

|      |       |    |       |       |      |        |         |           |   |              |          |   |   |              |             |          |
|------|-------|----|-------|-------|------|--------|---------|-----------|---|--------------|----------|---|---|--------------|-------------|----------|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vothers_G | 0 | Tcca_lim_off | Icca_lim | 0 | 0 | Taux_lim_off | Vaux_trk_EN | reserved |
|------|-------|----|-------|-------|------|--------|---------|-----------|---|--------------|----------|---|---|--------------|-------------|----------|

Table 21. INIT VREG2. description and configuration of the bits (default value in bold)

|                          |                 |  |
|--------------------------|-----------------|--|
| T <sub>CCA_LIM_OFF</sub> | Description     | Configure the current limitation duration before regulator is switched off. Only used for external PNP |
|                          | 0               | 10 ms  |
|                          | <b>1</b>        | <b>50 ms</b>   |
|                          | Reset condition | Power On Reset   |
| I <sub>CCA_LIM</sub>     | Description     | Configure the current limitation threshold. Only available for external PNP                            |
|                          | <b>0</b>        | <b>I<sub>CCA_LIM_OUT</sub></b>   |
|                          | 1               | I <sub>CCA_LIM_INT</sub>   |
|                          | Reset condition | Power On Reset   |
| T <sub>AUX_LIM_OFF</sub> | Description     | Configure the current limitation duration before regulator is switched off. Only used for external PNP |
|                          | 0               | 10 ms  |
|                          | <b>1</b>        | <b>50 ms</b>   |
|                          | Reset condition | Power On Reset   |
| V <sub>AUX_TRK_EN</sub>  | Description     | Configure V <sub>AUX</sub> regulator as a tracker  |
|                          | <b>0</b>        | <b>No tracking. HW configuration is used</b>   |
|                          | 1               | Tracking enabled   |
|                          | Reset condition | Power On Reset   |

### 7.3.3 Init CAN\_LIN

Table 22. INIT CAN\_LIN register description

| Write |       |       |       |       |       |       |      |      |      |             |      |      |           |      |          |          |
|-------|-------|-------|-------|-------|-------|-------|------|------|------|-------------|------|------|-----------|------|----------|----------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6        | bit5 | bit4 | bit3      | bit2 | bit1     | bit0     |
| MOSI  | 1     | 0     | 0     | 0     | 0     | 1     | 1    | P    | 0    | CAN_wu_conf | 0    | 0    | CAN_wu_TO | 0    | LIN_SR_1 | LIN_SR_0 |

|      |       |    |       |       |      |        |         |           |   |             |          |          |           |          |          |          |
|------|-------|----|-------|-------|------|--------|---------|-----------|---|-------------|----------|----------|-----------|----------|----------|----------|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vothers_G | 0 | CAN_wu_conf | Reserved | Reserved | CAN_wu_TO | Reserved | LIN_SR_1 | LIN_SR_0 |
|------|-------|----|-------|-------|------|--------|---------|-----------|---|-------------|----------|----------|-----------|----------|----------|----------|

Table 22. INIT CAN\_LIN register description (continued)

| Read |       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| MOSI | 0     | 0     | 0     | 0     | 0     | 1     | 1    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

|      |       |    |       |       |      |        |         |           |   |             |           |           |           |           |          |          |
|------|-------|----|-------|-------|------|--------|---------|-----------|---|-------------|-----------|-----------|-----------|-----------|----------|----------|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vothers_G | 0 | CAN_wu_conf | Reserve_d | Reserve_d | CAN_wu_TO | Reserve_d | LIN_SR_1 | LIN_SR_0 |
|------|-------|----|-------|-------|------|--------|---------|-----------|---|-------------|-----------|-----------|-----------|-----------|----------|----------|

Table 23. INIT CAN\_LIN. description and configuration of the bits (default value in bold)

|             |                 |   |
|-------------|-----------------|---|
| CAN_wu_conf | Description     | Define the CAN wake-up mechanism                            |
|             | <b>0</b>        | <b>3 dominant pulses</b>                                    |
|             | 1               | Single dominant pulse                                       |
|             | Reset condition | Power On Reset  |
| CAN_wu_to   | Description     | Define the CAN wake-up timeout (in case of CAN_wu_conf = 0) |
|             | <b>0</b>        | <b>120 <math>\mu</math>s</b>                                |
|             | 1               | 360 $\mu$ s   |
|             | Reset condition | Power On Reset  |
| LIN_SR_1:0  | Description     | Configure the LIN slew rate                                 |
|             | <b>00</b>       | <b>20 kbits/s</b>   |
|             | 01              | 10 kbits/s  |
|             | 1X              | Fast baud rate (Max: 100 kbits/s)                           |
|             | Reset condition | Power On Reset  |

## 7.3.4 INIT IO\_WU1

Table 24. INIT IO\_WU1 register description

| Write |       |       |       |       |       |       |      |      |        |        |        |        |        |        |              |              |
|-------|-------|-------|-------|-------|-------|-------|------|------|--------|--------|--------|--------|--------|--------|--------------|--------------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7   | bit6   | bit5   | bit4   | bit3   | bit2   | bit1         | bit0         |
| MOSI  | 1     | 0     | 0     | 0     | 1     | 0     | 0    | P    | WU_0_1 | WU_0_0 | WU_1_1 | WU_1_0 | WU_2_1 | WU_2_0 | INT_inh_IO_1 | INT_inh_IO_0 |

|      |       |    |       |       |      |        |         |           |        |        |        |        |        |        |              |              |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------|--------|--------|--------|--------|--------|--------------|--------------|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vothers_G | WU_0_1 | WU_0_0 | WU_1_1 | WU_1_0 | WU-2-1 | WU_2_0 | INT_inh_IO_1 | INT_inh_IO_0 |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------|--------|--------|--------|--------|--------|--------------|--------------|

| Read |       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| MOSI | 0     | 0     | 0     | 0     | 1     | 0     | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

|      |       |    |       |       |      |        |         |           |        |        |        |        |        |        |              |              |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------|--------|--------|--------|--------|--------|--------------|--------------|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vothers_G | WU_0_1 | WU_0_0 | WU_1_1 | WU_1_0 | WU-2-1 | WU_2_0 | INT_inh_IO_1 | INT_inh_IO_0 |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------|--------|--------|--------|--------|--------|--------------|--------------|

**Table 25. INIT IO\_WU1. description and configuration of the bits (default value in bold)**

|              |                 |  |
|--------------|-----------------|--|
| WU_0_1:0     | Description     | Wake-up configuration for IO_0   |
|              | <b>00</b>       | <b>NO wake-up capability</b>   |
|              | 01              | Wake-up on rising edge only  |
|              | 10              | Wake-up on falling edge only   |
|              | 11              | Wake-up on any edge  |
|              | Reset condition | Power On Reset   |
| WU_1_1:0     | Description     | Wake-up configuration for IO_1   |
|              | <b>00</b>       | <b>NO wake-up capability</b>   |
|              | 01              | Wake-up on rising edge only  |
|              | 10              | Wake-up on falling edge only   |
|              | 11              | Wake-up on any edge  |
|              | Reset condition | Power On Reset   |
| WU_2_1:0     | Description     | Wake-up configuration for IO_2   |
|              | <b>00</b>       | <b>NO wake-up capability</b>   |
|              | 01              | Wake-up on rising edge only  |
|              | 10              | Wake-up on falling edge only   |
|              | 11              | Wake-up on any edge  |
|              | Reset condition | Power On Reset   |
| INT_inh_IO_1 | Description     | Inhibit the INT pulse for IO_1. IO_1 masked in IO_G. Avoid INT when used in FS |
|              | <b>0</b>        | <b>INT NOT masked</b>  |
|              | 1               | INT masked   |
|              | Reset condition | Power On Reset   |
| INT_inh_IO_0 | Description     | Inhibit the INT pulse for IO_0. IO_0 masked in IO_G. Avoid INT when used in FS |
|              | <b>0</b>        | <b>INT NOT masked</b>  |
|              | 1               | INT masked   |
|              | Reset condition | Power On Reset   |

## 7.3.5 INIT IO\_WU2

**Table 26. INIT IO\_WU2 register description**

| Write |       |       |       |       |       |       |      |      |        |        |        |        |        |        |               |               |
|-------|-------|-------|-------|-------|-------|-------|------|------|--------|--------|--------|--------|--------|--------|---------------|---------------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7   | bit6   | bit5   | bit4   | bit3   | bit2   | bit1          | bit0          |
| MOSI  | 1     | 0     | 0     | 0     | 1     | 0     | 1    | P    | WU_3_1 | WU_3_0 | WU_4_1 | WU_4_0 | WU_5_1 | WU_5_0 | INT_inh_IO_23 | INT_inh_IO_45 |

|      |       |    |       |       |      |        |         |           |        |        |        |        |        |        |               |               |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------|--------|--------|--------|--------|--------|---------------|---------------|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vothers_G | WU_3_1 | WU_3_0 | WU_4_1 | WU_4_0 | WU_5_1 | WU_5_0 | INT_inh_IO_23 | INT_inh_IO_45 |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------|--------|--------|--------|--------|--------|---------------|---------------|

**Table 26. INIT IO\_WU2 register description (continued)**

| Read |       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| MOSI | 0     | 0     | 0     | 0     | 1     | 0     | 1    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

|      |       |    |       |       |      |        |         |           |        |        |        |        |        |        |               |               |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------|--------|--------|--------|--------|--------|---------------|---------------|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vothers_G | WU_3_1 | WU_3_0 | WU_4_1 | WU_4_0 | WU_5_1 | WU_5_0 | INT_inh_IO_23 | INT_inh_IO_45 |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------|--------|--------|--------|--------|--------|---------------|---------------|

**Table 27. INIT IO\_WU2. description and configuration of the bits (default value in bold)**

|               |                 |  |
|---------------|-----------------|--|
| WU_3_1:0      | Description     | Wake-up configuration for IO_3   |
|               | <b>00</b>       | <b>NO wake-up capability</b>   |
|               | 01              | Wake-up on rising edge only  |
|               | 10              | Wake-up on falling edge only   |
|               | 11              | Wake-up on any edge  |
|               | Reset condition | Power On Reset   |
| WU_4_1:0      | Description     | Wake-up configuration for IO_4   |
|               | <b>00</b>       | <b>NO wake-up capability</b>   |
|               | 01              | Wake-up on rising edge only  |
|               | 10              | Wake-up on falling edge only   |
|               | 11              | Wake-up on any edge  |
|               | Reset condition | Power On Reset   |
| WU_5_1:0      | Description     | Wake-up configuration for IO_5   |
|               | <b>00</b>       | <b>NO wake-up capability</b>   |
|               | 01              | Wake-up on rising edge only  |
|               | 10              | Wake-up on falling edge only   |
|               | 11              | Wake-up on any edge  |
|               | Reset condition | Power On Reset   |
| INT_inh_IO_45 | Description     | Inhibit the INT pulse for IO_4 & IO_5. IO_4 & IO_5 masked in IO_G. Avoid INT when used in FS |
|               | <b>0</b>        | <b>INT NOT masked</b>  |
|               | 1               | INT masked   |
|               | Reset condition | Power On Reset   |
| INT_inh_IO_23 | Description     | Inhibit the INT pulse for IO_2 & IO_3. IO_2 & IO_3 masked in IO_G. Avoid INT when used in FS |
|               | 0               | INT NOT masked   |
|               | <b>1</b>        | <b>INT masked</b>  |
|               | Reset condition | Power On Reset   |



## 7.3.6 INIT INT

Table 28. INIT INT register description

| Write |       |       |       |       |       |       |      |      |              |             |             |              |              |               |                 |             |
|-------|-------|-------|-------|-------|-------|-------|------|------|--------------|-------------|-------------|--------------|--------------|---------------|-----------------|-------------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7         | bit6        | bit5        | bit4         | bit3         | bit2          | bit1            | bit0        |
| MOSI  | 1     | 0     | 0     | 0     | 1     | 1     | 0    | P    | INT_duration | INT_inh_LIN | INT_inh_all | INT_inh_Vsns | INT_inh_Vpre | INT_inh_Vcore | INT_inh_Vothers | INT_inh_CAN |

|      |       |    |       |       |      |        |         |           |              |             |             |              |              |               |                 |             |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------------|-------------|-------------|--------------|--------------|---------------|-----------------|-------------|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vothers_G | INT_duration | INT_inh_LIN | INT_inh_all | INT_inh_Vsns | INT_inh_Vpre | INT_inh_Vcore | INT_inh_Vothers | INT_inh_CAN |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------------|-------------|-------------|--------------|--------------|---------------|-----------------|-------------|

| Read |       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| MOSI | 0     | 0     | 0     | 0     | 1     | 1     | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

|      |       |    |       |       |      |        |         |           |              |             |             |              |              |               |                 |             |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------------|-------------|-------------|--------------|--------------|---------------|-----------------|-------------|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vothers_G | INT_duration | INT_inh_LIN | INT_inh_all | INT_inh_Vsns | INT_inh_Vpre | INT_inh_Vcore | INT_inh_Vothers | INT_inh_CAN |
|------|-------|----|-------|-------|------|--------|---------|-----------|--------------|-------------|-------------|--------------|--------------|---------------|-----------------|-------------|

Table 29. INIT INT. description and configuration of the bits (default value in bold)

|              |                 |   |
|--------------|-----------------|---|
| INT_duration | Description     | Define the duration of the INTerrupt pulse                                    |
|              | <b>0</b>        | <b>100 µs</b>   |
|              | 1               | 25 µs   |
|              | Reset condition | Power On Reset  |
| INT_inh_LIN  | Description     | Inhibit the INT for LIN error bits  |
|              | <b>0</b>        | <b>All INT sources</b>  |
|              | 1               | LIN error bits changed INHIBITED  |
|              | Reset condition | Power On Reset  |
| INT_inh_all  | Description     | Inhibit ALL the INT   |
|              | <b>0</b>        | <b>All INT sources</b>  |
|              | 1               | All INT INHIBITED   |
|              | Reset condition | Power On Reset  |
| INT_inh_Vsns | Description     | Inhibit the INT for V <sub>SNS_UV</sub>                                       |
|              | <b>0</b>        | <b>All INT sources</b>  |
|              | 1               | V <sub>SNS_UV</sub> INT INHIBITED   |
|              | Reset condition | Power On Reset  |
| INT_inh_Vpre | Description     | Inhibit the INT for V <sub>PRE</sub> status event (cf. register status Vreg1) |
|              | <b>0</b>        | <b>All INT sources</b>  |
|              | 1               | V <sub>PRE</sub> status changed INHIBITED                                     |
|              | Reset condition | Power On Reset  |

**Table 29. INIT INT. description and configuration of the bits (default value in bold) (continued)**

|                 |                 |   |
|-----------------|-----------------|---|
| INT_inh_Vcore   | Description     | Inhibit the INT for V <sub>CORE</sub> status event (cf. register status Vreg2)  |
|                 | <b>0</b>        | <b>All INT sources</b>  |
|                 | 1               | V <sub>CORE</sub> status changed INHIBITED  |
|                 | Reset condition | Power On Reset  |
| INT_inh_Vothers | Description     | Inhibit the INT for V <sub>CCA</sub> / V <sub>AUX</sub> and V <sub>CAN</sub> status event (cf. register status Vreg2) |
|                 | <b>0</b>        | <b>All INT sources</b>  |
|                 | 1               | V <sub>CCA</sub> / V <sub>AUX</sub> / V <sub>CAN</sub> status changed INHIBITED                                       |
|                 | Reset condition | Power On Reset  |
| INT_inh_CAN     | Description     | Inhibit the INT for CAN error bits  |
|                 | <b>0</b>        | <b>All INT sources</b>  |
|                 | 1               | CAN error bits changed INHIBITED  |
|                 | Reset condition | Power On Reset  |

## 7.3.7 HW config

**Table 30. HW config register description**

|      |       |       |       |       |       |        |         |           |           |               |                 |         |         |      |      |      |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|-----------|---------------|-----------------|---------|---------|------|------|------|
| Read |       |       |       |       |       |        |         |           |           |               |                 |         |         |      |      |      |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7      | bit6          | bit5            | bit4    | bit3    | bit2 | bit1 | bit0 |
| MOSI | 0     | 0     | 0     | 1     | 0     | 0      | 0       | 0         | 0         | 0             | 0               | 0       | 0       | 0    | 0    | 0    |
|      |       |       |       |       |       |        |         |           |           |               |                 |         |         |      |      |      |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | LS_detect | Vaux not used | Vcca_PNP_detect | Vcca_HW | Vaux_HW | 1    | 0    | DBG  |

**Table 31. HW config. description and configuration of the bits (default value in bold)**

|                             |                 |   |
|-----------------------------|-----------------|---|
| LS_detect                   | Description     | Report the hardware configuration of V <sub>PRE</sub> (Buck only or Buck-Boost)   |
|                             | <b>0</b>        | <b>Buck-Boost</b>   |
|                             | 1               | Buck only   |
|                             | Reset condition | Power On Reset / Refresh after LPOFF  |
| V <sub>AUX</sub> not used   | Description     | Report if V <sub>AUX</sub> is used  |
|                             | 0               | V <sub>AUX</sub> is used (external PNP is assumed to be connected, V <sub>AUX</sub> can be switched OFF/ON through SPI) |
|                             | 1               | V <sub>AUX</sub> is not used  |
|                             | Reset condition | Power On Reset / Refresh after LPOFF  |
| V <sub>CCA_PNP_DETECT</sub> | Description     | Report the connection of an external PNP on V <sub>CCA</sub>  |
|                             | 0               | External PNP connected  |
|                             | 1               | Internal MOSFET   |
|                             | Reset condition | Power On Reset / Refresh after LPOFF  |
| V <sub>CCA_HW</sub>         | Description     | Report the hardware configuration for V <sub>CCA</sub>  |
|                             | <b>0</b>        | <b>3.3 V</b>  |
|                             | 1               | 5.0 V   |
|                             | Reset condition | Power On Reset / Refresh after LPOFF  |

**Table 31. HW config. description and configuration of the bits (default value in bold) (continued)**

|                     |                 |  |
|---------------------|-----------------|--|
| V <sub>AUX_HW</sub> | Description     | Report the hardware configuration for V <sub>AUX</sub> |
|                     | 0               | 5.0 V  |
|                     | <b>1</b>        | <b>3.3 V</b>   |
|                     | Reset condition | Power On Reset / Refresh after LPOFF                   |
| DBG                 | Description     | Report the configuration of the DEBUG mode             |
|                     | 0               | Normal operation                                       |
|                     | 1               | DEBUG mode selected                                    |
|                     | Reset condition | Power On Reset / Refresh after LPOFF                   |

## 7.3.8 WU source

**Table 32. WU source register description**

|      |       |       |       |       |       |        |         |           |         |         |         |         |         |         |      |        |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|---------|---------|---------|---------|---------|---------|------|--------|
| Read |       |       |       |       |       |        |         |           |         |         |         |         |         |         |      |        |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7    | bit6    | bit5    | bit4    | bit3    | bit2    | bit1 | bit0   |
| MOSI | 0     | 0     | 0     | 1     | 0     | 0      | 1       | 0         | 0       | 0       | 0       | 0       | 0       | 0       | 0    | 0      |
|      |       |       |       |       |       |        |         |           |         |         |         |         |         |         |      |        |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | IO_5_WU | IO_4_WU | IO_3_WU | IO_2_WU | IO_1_WU | IO_0_WU | 0    | Phy_WU |

**Table 33. WU source. description and configuration of the bits (default value in bold)**

|         |                 |                                  |
|---------|-----------------|----------------------------------|
| IO_5_WU | Description     | Report a wake-up event from IO_5 |
|         | <b>0</b>        | <b>No Wake-up</b>                |
|         | 1               | WU event detected                |
|         | Reset condition | Power On Reset / Read            |
| IO_4_WU | Description     | Report a wake-up event from IO_4 |
|         | <b>0</b>        | <b>No Wake-up</b>                |
|         | 1               | WU event detected                |
|         | Reset condition | Power On Reset / Read            |
| IO_3_WU | Description     | Report a wake-up event from IO_3 |
|         | <b>0</b>        | <b>No Wake-up</b>                |
|         | 1               | WU event detected                |
|         | Reset condition | Power On Reset / Read            |
| IO_2_WU | Description     | Report a wake-up event from IO_2 |
|         | <b>0</b>        | <b>No Wake-up</b>                |
|         | 1               | WU event detected                |
|         | Reset condition | Power On Reset / Read            |
| IO_1_WU | Description     | Report a wake-up event from IO_1 |
|         | <b>0</b>        | <b>No Wake-up</b>                |
|         | 1               | WU event detected                |
|         | Reset condition | Power On Reset / Read            |

**Table 33. WU source. description and configuration of the bits (default value in bold)(continued)**

|         |                 |  |
|---------|-----------------|--|
| IO_0_WU | Description     | Report a wake-up event from IO_0           |
|         | <b>0</b>        | <b>No Wake-up</b>                          |
|         | 1               | WU event detected                          |
|         | Reset condition | Power On Reset / Read                      |
| Phy_WU  | Description     | Report a wake-up event from CAN or LIN     |
|         | <b>0</b>        | <b>No Wake-up</b>                          |
|         | 1               | WU event detected                          |
|         | Reset condition | Power On Reset / Read CAN_wu or/and LIN_wu |

## 7.3.9 IO input

**Table 34. IO input register description**

|      |       |       |       |       |       |        |         |           |      |      |      |      |      |      |      |      |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|------|------|------|------|------|------|------|------|
| Read |       |       |       |       |       |        |         |           |      |      |      |      |      |      |      |      |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| MOSI | 0     | 0     | 0     | 1     | 0     | 1      | 1       | 0         | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |
|      |       |       |       |       |       |        |         |           |      |      |      |      |      |      |      |      |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | IO_5 | IO_4 | 0    | IO_3 | IO_2 | 0    | IO_1 | IO_0 |

**Table 35. IO input. description and configuration of the bits**

|      |                 |  |
|------|-----------------|--|
| IO_5 | Description     | Report IO_5 digital state in Normal mode. No update in LPOFF mode since wake-up features available |
|      | 0               | Low  |
|      | 1               | High   |
|      | Reset condition | Power On Reset   |
| IO_4 | Description     | Report IO_4 digital state in Normal mode. No update in LPOFF mode since wake-up features available |
|      | 0               | Low  |
|      | 1               | High   |
|      | Reset condition | Power On Reset   |
| IO_3 | Description     | Report IO_3 digital state in Normal mode. No update in LPOFF mode since wake-up features available |
|      | 0               | Low  |
|      | 1               | High   |
|      | Reset condition | Power On Reset   |
| IO_2 | Description     | Report IO_2 digital state in Normal mode. No update in LPOFF mode since wake-up features available |
|      | 0               | Low  |
|      | 1               | High   |
|      | Reset condition | Power On Reset   |
| IO_1 | Description     | Report IO_1 digital state in Normal mode. No update in LPOFF mode since wake-up features available |
|      | 0               | Low  |
|      | 1               | High   |
|      | Reset condition | Power On Reset   |

**Table 35. IO input. description and configuration of the bits(continued)**

|      |                 |  |
|------|-----------------|--|
| IO_0 | Description     | Report IO_0 digital state in Normal mode. No update in LPOFF mode since wake-up features available |
|      | 0               | Low  |
|      | 1               | High   |
|      | Reset condition | Power On Reset   |

## 7.3.10 Status Vreg1

**Table 36. STATUS VREG1 register description**

|      |       |       |       |       |       |        |         |           |      |          |           |      |           |      |      |      |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|------|----------|-----------|------|-----------|------|------|------|
| Read |       |       |       |       |       |        |         |           |      |          |           |      |           |      |      |      |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7 | bit6     | bit5      | bit4 | bit3      | bit2 | bit1 | bit0 |
| MOSI | 0     | 0     | 0     | 1     | 1     | 0      | 0       | 0         | 0    | 0        | 0         | 0    | 0         | 0    | 0    | 0    |
|      |       |       |       |       |       |        |         |           |      |          |           |      |           |      |      |      |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | IpFF | llim_pre | Twarn_pre | BoB  | Vpre_stat | 0    | 0    | 0    |

**Table 37. Status Vreg1. description and configuration of the bits (default value in bold)**

|                        |                 |  |
|------------------------|-----------------|--|
| IpFF                   | Description     | Input Power Feed Forward   |
|                        | 0               | <b>Normal Operation</b>  |
|                        | 1               | Ipff mode activated  |
|                        | Reset condition | Power On Reset / Read  |
| IlIM_PRE               | Description     | Report a current limitation condition on V <sub>PRE</sub>                  |
|                        | 0               | <b>No current limitation (I<sub>PRE_PK</sub> &lt; I<sub>PRE_LIM</sub>)</b> |
|                        | 1               | Current limitation (I <sub>PRE_PK</sub> > I <sub>PRE_LIM</sub> )           |
|                        | Reset condition | Power On Reset / Read  |
| T <sub>WARN_PRE</sub>  | Description     | Report a thermal warning from V <sub>PRE</sub>                             |
|                        | 0               | <b>No thermal warning (T<sub>J</sub> &lt; T<sub>WARN_PRE</sub>)</b>        |
|                        | 1               | Thermal warning (T <sub>J</sub> > T <sub>WARN_PRE</sub> )                  |
|                        | Reset condition | Power On Reset / Read  |
| BoB                    | Description     | Report a running mode of V <sub>PRE</sub>                                  |
|                        | 0               | <b>Buck</b>  |
|                        | 1               | Boost  |
|                        | Reset condition | Power On Reset   |
| V <sub>PRE_STATE</sub> | Description     | Report the activation state of V <sub>PRE</sub> SMPS                       |
|                        | 0               | SMPS OFF   |
|                        | 1               | <b>SMPS ON</b>   |
|                        | Reset condition | Power On Reset   |

## 7.3.11 Status VREG2

**Table 38. STATUS VREG2 register description**

|      |       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
| Read |       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| MOSI | 0     | 0     | 0     | 1     | 1     | 0     | 1    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**Table 38. STATUS VREG2 register description**

|      |       |    |       |       |      |        |         |            |           |            |             |           |          |          |          |   |
|------|-------|----|-------|-------|------|--------|---------|------------|-----------|------------|-------------|-----------|----------|----------|----------|---|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vother_s_G | llim_core | Twarn_core | Vcore_state | Twarn_cca | llim_cca | llim_aux | llim_can | 0 |
|------|-------|----|-------|-------|------|--------|---------|------------|-----------|------------|-------------|-----------|----------|----------|----------|---|

**Table 39. Status Vreg2. description and configuration of the bits (default value in bold)**

|                         |                 |  |
|-------------------------|-----------------|--|
| I <sub>LIM_CORE</sub>   | Description     | Report a current limitation condition on V <sub>CORE</sub>                               |
|                         | <b>0</b>        | <b>No current limitation (I<sub>CORE_PK</sub> &lt; I<sub>CORE_LIM</sub>)</b>             |
|                         | 1               | Current limitation (I <sub>CORE_PK</sub> > I <sub>CORE_LIM</sub> )                       |
|                         | Reset condition | Power On Reset / Read  |
| T <sub>WARN_CORE</sub>  | Description     | Report a thermal warning from V <sub>CORE</sub>  |
|                         | <b>0</b>        | <b>No thermal warning (T<sub>J</sub> &lt; T<sub>WARN_CORE</sub>)</b>                     |
|                         | 1               | Thermal warning (T <sub>J</sub> > T <sub>WARN_CORE</sub> )                               |
|                         | Reset condition | Power On Reset / Read  |
| V <sub>CORE_STATE</sub> | Description     | Report the activation state of V <sub>CORE</sub> SMPS                                    |
|                         | 0               | SMPS OFF   |
|                         | <b>1</b>        | <b>SMPS ON</b>   |
|                         | Reset condition | Power On Reset   |
| T <sub>WARN_CCA</sub>   | Description     | Report a thermal warning from V <sub>CCA</sub> . Available only for internal pass MOSFET |
|                         | <b>0</b>        | <b>No thermal warning (T<sub>J</sub> &lt; T<sub>WARN_CCA</sub>)</b>                      |
|                         | 1               | Thermal warning (T <sub>J</sub> > T <sub>WARN_CCA</sub> )                                |
|                         | Reset condition | Power On Reset   |
| I <sub>LIM_CCA</sub>    | Description     | Report a current limitation condition on V <sub>CCA</sub>                                |
|                         | <b>0</b>        | <b>No current limitation (I<sub>CCA</sub> &lt; I<sub>CCA_LIM</sub>)</b>                  |
|                         | 1               | Current limitation (I <sub>CCA</sub> > I <sub>CCA_LIM</sub> )                            |
|                         | Reset condition | Power On Reset / Read  |
| I <sub>LIM_AUX</sub>    | Description     | Report a current limitation condition on V <sub>AUX</sub>                                |
|                         | <b>0</b>        | <b>No current limitation (I<sub>AUX</sub> &lt; I<sub>AUX_LIM</sub>)</b>                  |
|                         | 1               | Current limitation (I <sub>AUX</sub> > I <sub>AUX_LIM</sub> )                            |
|                         | Reset condition | Power On Reset / Read  |
| I <sub>LIM_CAN</sub>    | Description     | Report a current limitation condition on V <sub>CAN</sub>                                |
|                         | <b>0</b>        | <b>No current limitation (I<sub>CAN</sub> &lt; I<sub>CAN_LIM</sub>)</b>                  |
|                         | 1               | Current limitation (I <sub>CAN</sub> > I <sub>CAN_LIM</sub> )                            |
|                         | Reset condition | Power On Reset / Read  |

## 7.3.12 Diag Vreg1

**Table 40. DIAG VREG1 register description**

|      |       |       |       |       |       |        |         |            |          |            |         |         |          |          |             |             |
|------|-------|-------|-------|-------|-------|--------|---------|------------|----------|------------|---------|---------|----------|----------|-------------|-------------|
| Read |       |       |       |       |       |        |         |            |          |            |         |         |          |          |             |             |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8       | bit7     | bit6       | bit5    | bit4    | bit3     | bit2     | bit1        | bit0        |
| MOSI | 0     | 0     | 0     | 1     | 1     | 1      | 0       | 0          | 0        | 0          | 0       | 0       | 0        | 0        | 0           | 0           |
|      |       |       |       |       |       |        |         |            |          |            |         |         |          |          |             |             |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vother_s_G | Vsns_u_v | Vsup_u_v_7 | Tsd_pre | Vpre_OV | Vpre_u_v | Tsd_core | Vcore_FB_OV | Vcore_FB_uv |

**Table 41. Diag Vreg1. description and configuration of the bits (default value in bold)**

|                         |                 |   |
|-------------------------|-----------------|---|
| V <sub>SNS_UV</sub>     | Description     | Detection of V <sub>BATTERY</sub> below V <sub>SNS_UV</sub>             |
|                         | 0               | V <sub>BAT</sub> > V <sub>SNS_UV</sub>                                  |
|                         | <b>1</b>        | <b>V<sub>BAT</sub> &lt; V<sub>SNS_UV</sub></b>                          |
|                         | Reset condition | Power On Reset / Read   |
| V <sub>SUP_UV_7</sub>   | Description     | Detection of V <sub>SUP</sub> below V <sub>SUP_UV_7</sub>               |
|                         | 0               | V <sub>SUP</sub> > V <sub>SUP_UV_7</sub>                                |
|                         | <b>1</b>        | <b>V<sub>SUP</sub> &lt; V<sub>SUP_UV_7</sub></b>                        |
|                         | Reset condition | Power On Reset / Read   |
| T <sub>SD_PRE</sub>     | Description     | Thermal shutdown of V <sub>PRE</sub>                                    |
|                         | <b>0</b>        | <b>No TSD (T<sub>J</sub> &lt; T<sub>SD_PRE</sub>)</b>                   |
|                         | 1               | TSD occurred (T <sub>J</sub> > T <sub>SD_PRE</sub> )                    |
|                         | Reset condition | Power On Reset / Read   |
| V <sub>PRE_OV</sub>     | Description     | V <sub>PRE</sub> overvoltage detection                                  |
|                         | <b>0</b>        | <b>No overvoltage (V<sub>PRE</sub> &lt; V<sub>PRE_OV</sub>)</b>         |
|                         | 1               | Overvoltage detected (V <sub>PRE</sub> > V <sub>PRE_OV</sub> )          |
|                         | Reset condition | Power On Reset  |
| V <sub>PRE_UV</sub>     | Description     | V <sub>PRE</sub> undervoltage detection                                 |
|                         | 0               | No undervoltage (V <sub>PRE</sub> > V <sub>PRE_UV</sub> )               |
|                         | <b>1</b>        | <b>Undervoltage detected (V<sub>PRE</sub> &lt; V<sub>PRE_UV</sub>)</b>  |
|                         | Reset condition | Power On Reset / Read   |
| T <sub>SD_CORE</sub>    | Description     | Thermal shutdown of V <sub>CORE</sub>                                   |
|                         | <b>0</b>        | <b>No TSD (T<sub>J</sub> &lt; T<sub>SD_CORE</sub>)</b>                  |
|                         | 1               | TSD occurred (T <sub>J</sub> > T <sub>SD_CORE</sub> )                   |
|                         | Reset condition | Power On Reset / Read   |
| V <sub>CORE_FB_OV</sub> | Description     | V <sub>CORE</sub> overvoltage detection                                 |
|                         | <b>0</b>        | <b>No overvoltage (V<sub>CORE_FB</sub> &lt; V<sub>CORE_FB_OV</sub>)</b> |
|                         | 1               | Overvoltage detected (V <sub>CORE_FB</sub> > V <sub>CORE_FB_OV</sub> )  |
|                         | Reset condition | Power On Reset / Read   |
| V <sub>CORE_FB_UV</sub> | Description     | V <sub>CORE</sub> undervoltage detection                                |
|                         | 0               | No undervoltage (V <sub>CORE_FB</sub> > V <sub>CORE_FB_UV</sub> )       |
|                         | <b>1</b>        | <b>Undervoltage (V<sub>CORE_FB</sub> &lt; V<sub>CORE_FB_UV</sub>)</b>   |
|                         | Reset condition | Power On Reset / Read   |

### 7.3.13 Diag Vreg2

**Table 42. DIAG VREG2 register description**

| Read |       |       |       |       |       |        |         |            |         |         |         |      |         |              |         |         |
|------|-------|-------|-------|-------|-------|--------|---------|------------|---------|---------|---------|------|---------|--------------|---------|---------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8       | bit7    | bit6    | bit5    | bit4 | bit3    | bit2         | bit1    | bit0    |
| MOSI | 0     | 0     | 0     | 1     | 1     | 1      | 1       | 0          | 0       | 0       | 0       | 0    | 0       | 0            | 0       | 0       |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vother_s_G | Tsd_Can | Vcan_OV | Vcan_uv | 0    | Tsd_aux | llim_aux_off | Vaux_OV | Vaux_uv |

**Table 43. Diag Vreg2. description and configuration of the bits (default value in bold)**

|                     |                 |  |
|---------------------|-----------------|--|
| $T_{SD\_CAN}$       | Description     | Thermal shutdown of $V_{CAN}$  |
|                     | <b>0</b>        | <b>NO TSD (<math>T_J &lt; T_{SD\_CAN}</math>)</b>                    |
|                     | 1               | TSD occurred ( $T_J > T_{SD\_CAN}$ )                                 |
|                     | Reset condition | Power On Reset / Read  |
| $V_{CAN\_OV}$       | Description     | $V_{CAN}$ Overvoltage detection                                      |
|                     | <b>0</b>        | <b>No Overvoltage (<math>V_{CAN} &lt; V_{CAN\_OV}</math>)</b>        |
|                     | 1               | Overvoltage detected ( $V_{CAN} > V_{CAN\_OV}$ )                     |
|                     | Reset condition | Power On Reset / Read  |
| $V_{CAN\_UV}$       | Description     | $V_{CAN}$ undervoltage detection                                     |
|                     | 0               | No undervoltage ( $V_{CAN} > V_{CAN\_UV}$ )                          |
|                     | <b>1</b>        | <b>Undervoltage detected (<math>V_{CAN} &lt; V_{CAN\_UV}</math>)</b> |
|                     | Reset condition | Power On Reset / Read  |
| $T_{SD\_AUX}$       | Description     | Thermal shutdown of $V_{AUX}$  |
|                     | <b>0</b>        | <b>No TSD (<math>T_J &lt; T_{SD\_AUX}</math>)</b>                    |
|                     | 1               | TSD occurred ( $T_J > T_{SD\_AUX}$ )                                 |
|                     | Reset condition | Power On Reset   |
| $I_{LIM\_AUX\_OFF}$ | Description     | Maximum current limitation duration                                  |
|                     | <b>0</b>        | <b><math>T_{LIMITATION} &lt; T_{AUX\_LIM\_OFF}</math></b>            |
|                     | 1               | $T_{LIMITATION} > T_{AUX\_LIM\_OFF}$                                 |
|                     | Reset condition | Power On Reset / Read  |
| $V_{AUX\_OV}$       | Description     | $V_{AUX}$ overvoltage detection                                      |
|                     | <b>0</b>        | <b>No overvoltage (<math>V_{AUX} &lt; V_{AUX\_OV}</math>)</b>        |
|                     | 1               | Overvoltage detected ( $V_{AUX} > V_{AUX\_OV}$ )                     |
|                     | Reset condition | Power On Reset / Read  |
| $V_{AUX\_UV}$       | Description     | $V_{AUX}$ undervoltage detection                                     |
|                     | 0               | No undervoltage ( $V_{AUX} > V_{AUX\_UV}$ )                          |
|                     | <b>1</b>        | <b>Undervoltage detected (<math>V_{AUX} &lt; V_{AUX\_UV}</math>)</b> |
|                     | Reset condition | Power On Reset / Read  |

### 7.3.14 Diag Vreg3

**Table 44. DIAG VREG3 register description**

|      |       |       |       |       |       |        |         |           |         |      |              |      |         |      |         |      |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|---------|------|--------------|------|---------|------|---------|------|
| Read |       |       |       |       |       |        |         |           |         |      |              |      |         |      |         |      |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7    | bit6 | bit5         | bit4 | bit3    | bit2 | bit1    | bit0 |
| MOSI | 0     | 0     | 1     | 0     | 0     | 0      | 0       | 0         | 0       | 0    | 0            | 0    | 0       | 0    | 0       | 0    |
|      |       |       |       |       |       |        |         |           |         |      |              |      |         |      |         |      |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | Tsd_cca | 0    | llim-cca_off | 0    | Vcca_OV | 0    | Vcca_UV | 0    |



**Table 45. Diag Vreg3. description and configuration of the bits (default value in bold)**

|                     |                 |   |
|---------------------|-----------------|---|
| $T_{SD\_CCA}$       | Description     | Thermal shutdown of $V_{CCA}$   |
|                     | <b>0</b>        | <b>NO TSD (<math>T_J &lt; T_{SD\_CCA}</math>)</b>                                     |
|                     | 1               | TSD occurred ( $T_J > T_{SD\_CCA}$ )  |
|                     | Reset condition | Power On Reset / Read   |
| $I_{LIM\_CCA\_OFF}$ | Description     | Maximum current limitation duration. Available only when an external PNP is connected |
|                     | <b>0</b>        | <b><math>T_{LIMITATION} &lt; T_{CCA\_LIM\_OFF}</math></b>                             |
|                     | 1               | $T_{LIMITATION} > T_{CCA\_LIM\_OFF}$  |
|                     | Reset condition | Power On Reset / Read   |
| $V_{CCA\_OV}$       | Description     | $V_{CCA}$ overvoltage detection   |
|                     | <b>0</b>        | <b>No overvoltage (<math>V_{CCA} &lt; V_{CCA\_OV}</math>)</b>                         |
|                     | 1               | Overvoltage detected ( $V_{CCA} > V_{CCA\_OV}$ )                                      |
|                     | Reset condition | Power On Reset / Read   |
| $V_{CCA\_UV}$       | Description     | $V_{CCA}$ undervoltage detection  |
|                     | 0               | No undervoltage ( $V_{CCA} > V_{CCA\_UV}$ )   |
|                     | <b>1</b>        | <b>Undervoltage detected (<math>V_{CCA} &lt; V_{CCA\_UV}</math>)</b>                  |
|                     | Reset condition | Power On Reset  |

## 7.3.15 Diag CAN1

**Table 46. DIAG CAN1 register description**

|      |       |       |       |       |       |        |         |            |           |          |           |          |              |      |               |              |
|------|-------|-------|-------|-------|-------|--------|---------|------------|-----------|----------|-----------|----------|--------------|------|---------------|--------------|
| Read |       |       |       |       |       |        |         |            |           |          |           |          |              |      |               |              |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8       | bit7      | bit6     | bit5      | bit4     | bit3         | bit2 | bit1          | bit0         |
| MOSI | 0     | 0     | 1     | 0     | 0     | 0      | 1       | 0          | 0         | 0        | 0         | 0        | 0            | 0    | 0             | 0            |
|      |       |       |       |       |       |        |         |            |           |          |           |          |              |      |               |              |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vother_s_G | CANH_batt | CANH_gnd | CANL_batt | CANL_gnd | CAN_dominant | 0    | RXD_recessive | TXD_dominant |

**Table 47. Diag CAN1. description and configuration of the bits (default value in bold)**

|               |                 |   |
|---------------|-----------------|---|
| CANH_batt     | Description     | CANH short-circuit to battery detection                   |
|               | <b>0</b>        | <b>No failure</b>   |
|               | 1               | Failure detected  |
|               | Reset condition | Power On Reset / Read                                     |
| CANH_gnd      | Description     | CANH short-circuit to GND detection                       |
|               | <b>0</b>        | <b>No failure</b>   |
|               | 1               | Failure detected  |
|               | Reset condition | Power On Reset / Read                                     |
| CANL_batt     | Description     | CANL short-circuit to battery detection                   |
|               | <b>0</b>        | <b>No failure</b>   |
|               | 1               | Failure detected  |
|               | Reset condition | Power On Reset / Read                                     |
| CANL_gnd      | Description     | CANL short-circuit to GND detection                       |
|               | <b>0</b>        | <b>No failure</b>   |
|               | 1               | Failure detected  |
|               | Reset condition | Power On Reset / Read                                     |
| CAN_dominant  | Description     | CAN Bus dominant clamping detection                       |
|               | <b>0</b>        | <b>No failure</b>   |
|               | 1               | Failure detected  |
|               | Reset condition | Power On Reset / Read                                     |
| RXD_recessive | Description     | RXD recessive clamping detection (short-circuit to 5.0 V) |
|               | <b>0</b>        | <b>No failure</b>   |
|               | 1               | Failure detected  |
|               | Reset condition | Power On Reset / Read                                     |
| TXD_dominant  | Description     | TXD dominant clamping detection (short-circuit to GND)    |
|               | <b>0</b>        | <b>No failure</b>   |
|               | 1               | Failure detected  |
|               | Reset condition | Power On Reset / Read                                     |

## 7.3.16 Diag CAN\_LIN

**Table 48. DIAG CAN\_LIN register description**

| Read |       |       |       |       |       |        |         |           |              |               |      |                |        |      |        |        |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|--------------|---------------|------|----------------|--------|------|--------|--------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7         | bit6          | bit5 | bit4           | bit3   | bit2 | bit1   | bit0   |
| MOSI | 0     | 0     | 1     | 0     | 0     | 1      | 0       | 0         | 0            | 0             | 0    | 0              | 0      | 0    | 0      | 0      |
|      |       |       |       |       |       |        |         |           |              |               |      |                |        |      |        |        |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | LIN_dominant | TXDL_dominant | 0    | RXDL_recessive | LIN_OT | 0    | CAN_OT | CAN_OC |

**Table 49. Diag CAN\_LIN. description and configuration of the bits (default value in bold)**

|                |                 |   |
|----------------|-----------------|---|
| LIN_dominant   | Description     | LIN bus dominant clamping detection                           |
|                | <b>0</b>        | <b>No failure</b>   |
|                | 1               | Failure detected  |
|                | Reset condition | Power On Reset / Read   |
| TXDL_dominant  | Description     | LIN TXD dominant clamping detection (short-circuit to GND)    |
|                | <b>0</b>        | <b>No failure</b>   |
|                | 1               | Failure detected  |
|                | Reset condition | Power On Reset / Read   |
| RXDL_recessive | Description     | LIN RXD recessive clamping detection (short-circuit to 5.0 V) |
|                | <b>0</b>        | <b>No failure</b>   |
|                | 1               | Failure detected  |
|                | Reset condition | Power On Reset / Read   |
| LIN_OT         | Description     | LIN overtemperature detection                                 |
|                | <b>0</b>        | <b>No failure</b>   |
|                | 1               | Failure detected  |
|                | Reset condition | Power On Reset / Read   |
| CAN_OT         | Description     | CAN overtemperature detection                                 |
|                | <b>0</b>        | <b>No failure</b>   |
|                | 1               | Failure detected  |
|                | Reset condition | Power On Reset / Read   |
| CAN_OC         | Description     | CAN overcurrent detection                                     |
|                | <b>0</b>        | <b>No failure</b>   |
|                | 1               | Failure detected  |
|                | Reset condition | Power On Reset / Read   |

## 7.3.17 Diag SPI

**Table 50. DIAG SPI register description**

|      |       |       |       |       |       |        |         |           |         |      |         |      |         |      |            |      |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|---------|------|---------|------|---------|------|------------|------|
| Read |       |       |       |       |       |        |         |           |         |      |         |      |         |      |            |      |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7    | bit6 | bit5    | bit4 | bit3    | bit2 | bit1       | bit0 |
| MOSI | 0     | 0     | 1     | 0     | 0     | 1      | 1       | 0         | 0       | 0    | 0       | 0    | 0       | 0    | 0          | 0    |
|      |       |       |       |       |       |        |         |           |         |      |         |      |         |      |            |      |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_err | 0    | SPI_clk | 0    | SPI_req | 0    | SPI_parity | 0    |

**Table 51. Diag SPI. description and configuration of the bits (default value in bold)**

|            |                 |   |
|------------|-----------------|---|
| SPI_err    | Description     | Secured SPI communication check   |
|            | <b>0</b>        | <b>No error</b>   |
|            | 1               | Error detected in the secured bits  |
|            | Reset condition | Power On Reset / Read   |
| SPI_CLK    | Description     | SCLK error detection  |
|            | <b>0</b>        | <b>16 clock cycles during NCS low</b>   |
|            | 1               | Wrong number of clock cycles (<16 or > 16)  |
|            | Reset condition | Power On Reset / Read   |
| SPI_req    | Description     | Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address) |
|            | <b>0</b>        | <b>No error</b>   |
|            | 1               | SPI violation   |
|            | Reset condition | Power On Reset / Read   |
| SPI_parity | Description     | SPI parity bit error detection  |
|            | <b>0</b>        | <b>Parity bit OK</b>  |
|            | 1               | Parity bit error  |
|            | Reset condition | Power On Reset / Read   |

## 7.3.18 Mode

**Table 52. Mode register description**

| Write |       |       |       |       |       |        |              |               |              |              |                |                 |              |              |              |              |
|-------|-------|-------|-------|-------|-------|--------|--------------|---------------|--------------|--------------|----------------|-----------------|--------------|--------------|--------------|--------------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9         | bit8          | bit7         | bit6         | bit5           | bit4            | bit3         | bit2         | bit1         | bit0         |
| MOSI  | 1     | 0     | 1     | 0     | 1     | 0      | 1            | P             | 0            | 0            | Goto_L<br>POFF | INT_re<br>quest | Secure<br>_3 | Secure<br>_2 | Secure<br>_1 | Secure<br>_0 |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_<br>_G | Vothers<br>_G | Reserv<br>ed | Reserv<br>ed | Reserv<br>ed   | Reserv<br>ed    | INIT         | Normal       | Reserv<br>ed | Reserv<br>ed |
| Read  |       |       |       |       |       |        |              |               |              |              |                |                 |              |              |              |              |
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9         | bit8          | bit7         | bit6         | bit5           | bit4            | bit3         | bit2         | bit1         | bit0         |
| MOSI  | 0     | 0     | 1     | 0     | 1     | 0      | 1            | 0             | 0            | 0            | 0              | 0               | 0            | 0            | 0            | 0            |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_<br>_G | Vothers<br>_G | Reserv<br>ed | Reserv<br>ed | Reserv<br>ed   | Reserv<br>ed    | INIT         | Normal       | Reserv<br>ed | Reserv<br>ed |

**Table 53. Mode. description and configuration of the bits (default value in bold)**

|             |                 |  |
|-------------|-----------------|--|
| Goto_LPOFF  | Description     | Configure the device in Low Power mode $V_{REG}$ OFF (LPOFF)                           |
|             | <b>0</b>        | <b>No action</b>   |
|             | 1               | LPOFF mode   |
|             | Reset condition | Power On Reset   |
| INIT        | Description     | Report if INIT mode of the main logic state machine is entered                         |
|             | 0               | Not in INIT mode   |
|             | <b>1</b>        | <b>INIT MODE</b>   |
|             | Reset condition | Power On Reset   |
| Normal      | Description     | Report if Normal mode of the main logic state machine is entered                       |
|             | <b>0</b>        | <b>Not in Normal mode</b>  |
|             | 1               | Normal mode  |
|             | Reset condition | Power On Reset   |
| INT_request | Description     | Request for an INT pulse   |
|             | 0               | No Request   |
|             | 1               | Request for an INT pulse   |
|             | Reset condition | Power On Reset   |
| Secure 3:0  | Description     | Secured bits based on write bits   |
|             |                 | secured_3 = NOT(bit5)<br>Secured_2 = NOT(bit4)<br>Secured_1 = bit7<br>Secured_0 = bit6 |

## 7.3.19 Vreg mode

**Table 54. VREG mode register description**

| Write |       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|-------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |

**Table 54. VREG mode register description**

|      |       |       |       |       |       |        |         |           |           |           |           |           |          |          |          |          |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|-----------|-----------|-----------|-----------|----------|----------|----------|----------|
| MOSI | 1     | 0     | 1     | 0     | 1     | 1      | 0       | P         | Vcore_EN  | Vcca_EN   | Vaux_EN   | Vcan_EN   | Secure_3 | Secure_2 | Secure_1 | Secure_0 |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | Reserv ed | Reserv ed | Reserv ed | Reserv ed | Vcore_EN | Vcca_EN  | Vaux_EN  | Vcan_EN  |
| Read |       |       |       |       |       |        |         |           |           |           |           |           |          |          |          |          |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7      | bit6      | bit5      | bit4      | bit3     | bit2     | bit1     | bit0     |
| MOSI | 0     | 0     | 1     | 0     | 1     | 1      | 0       | 0         | 0         | 0         | 0         | 0         | 0        | 0        | 0        | 0        |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | Reserv ed | Reserv ed | Reserv ed | Reserv ed | Vcore_EN | Vcca_EN  | Vaux_EN  | Vcan_EN  |

**Table 55. VREG mode. description and configuration of the bits (default value in bold)**

|                      |                 |  |
|----------------------|-----------------|--|
| V <sub>CORE_EN</sub> | Description     | V <sub>CORE</sub> control (Switch OFF NOT recommended if V <sub>CORE</sub> is SAFETY critical) |
|                      | 0               | DISABLED   |
|                      | <b>1</b>        | <b>ENABLED</b>   |
|                      | Reset condition | Power On Reset   |
| V <sub>CCA_EN</sub>  | Description     | V <sub>CCA</sub> control (Switch OFF NOT recommended if V <sub>CCA</sub> is SAFETY critical)   |
|                      | 0               | DISABLED   |
|                      | <b>1</b>        | <b>ENABLED</b>   |
|                      | Reset condition | Power On Reset   |
| V <sub>AUX_EN</sub>  | Description     | V <sub>AUX</sub> control (Switch OFF NOT recommended if V <sub>AUX</sub> is SAFETY critical)   |
|                      | 0               | DISABLED   |
|                      | <b>1</b>        | <b>ENABLED</b>   |
|                      | Reset condition | Power On Reset   |
| V <sub>CAN_EN</sub>  | Description     | V <sub>CAN</sub> control   |
|                      | 0               | DISABLED   |
|                      | <b>1</b>        | <b>ENABLED</b>   |
|                      | Reset condition | Power On Reset   |
| Secure 3:0           | Description     | Secured bits based on write bits   |
|                      |                 | secured_3 = NOT(bit5)  |
|                      |                 | Secured_2 = NOT(bit4)  |
|                      |                 | Secured_1 = bit7   |
|                      |                 | Secured_0 = bit6   |

## 7.3.20 IO\_OUT-AMUX

**Table 56. IO\_OUT-AMUX register description**

|       |       |       |       |       |       |        |         |           |             |          |             |          |           |        |        |        |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|-------------|----------|-------------|----------|-----------|--------|--------|--------|
| Write |       |       |       |       |       |        |         |           |             |          |             |          |           |        |        |        |
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7        | bit6     | bit5        | bit4     | bit3      | bit2   | bit1   | bit0   |
| MOSI  | 1     | 0     | 1     | 0     | 1     | 1      | 1       | P         | IO_out_4_EN | IO_out_4 | IO_out_5_EN | IO_out_5 | 0         | Amux_2 | Amux_1 | Amux_0 |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | IO_out_4_EN | IO_out_4 | IO_out_5_EN | IO_out_5 | Reserv ed | Amux_2 | Amux_1 | Amux_0 |

**Table 56. IO\_OUT-AMUX register description**

| Read |       |       |       |       |       |        |         |           |             |          |             |          |          |        |        |        |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|-------------|----------|-------------|----------|----------|--------|--------|--------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7        | bit6     | bit5        | bit4     | bit3     | bit2   | bit1   | bit0   |
| MOSI | 0     | 0     | 1     | 0     | 1     | 1      | 1       | 0         | 0           | 0        | 0           | 0        | 0        | 0      | 0      | 0      |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | IO_out_4_EN | IO_out_4 | IO_out_5_EN | IO_out_5 | Reserved | Amux_2 | Amux_1 | Amux_0 |

**Table 57. IO\_OUT-AMUX. description and configuration of the bits (default value in bold)**

|             |                 |   |
|-------------|-----------------|---|
| IO_out_4_EN | Description     | Enable the output gate driver capability for IO_4 |
|             | <b>0</b>        | <b>High-impedance (IO_4 configured as input)</b>  |
|             | 1               | ENABLED (IO_4 configured as output gate driver)   |
|             | Reset condition | Power On Reset                                    |
| IO_out_4    | Description     | Configure IO_4 output gate driver state           |
|             | <b>0</b>        | <b>LOW</b>  |
|             | 1               | HIGH  |
|             | Reset condition | Power On Reset                                    |
| IO_out_5_EN | Description     | Enable the output gate driver capability for IO_5 |
|             | <b>0</b>        | <b>High-impedance (IO_5 configured as input)</b>  |
|             | 1               | ENABLED (IO_5 configured as output gate driver)   |
|             | Reset condition | Power On Reset                                    |
| IO_out_5    | Description     | Configure IO_5 output gate driver state           |
|             | <b>0</b>        | <b>LOW</b>  |
|             | 1               | HIGH  |
|             | Reset condition | Power On Reset                                    |
| AMUX_2:0    | Description     | Select AMUX output                                |
|             | <b>000</b>      | <b>Vref</b>                                       |
|             | 001             | Vsns wide range                                   |
|             | 010             | IO_0 wide range                                   |
|             | 011             | IO_1 wide range                                   |
|             | 100             | Vsns tight range                                  |
|             | 101             | IO_0 tight range                                  |
|             | 110             | IO_1 tight range                                  |
|             | 111             | Die Temperature Sensor                            |
|             | Reset condition | Power On Reset                                    |

## 7.3.21 CAN\_LIN mode

**Table 58. CAN\_LIN mode register description**

| Write |       |       |       |       |       |       |      |      |            |            |                           |                         |                         |                           |      |      |
|-------|-------|-------|-------|-------|-------|-------|------|------|------------|------------|---------------------------|-------------------------|-------------------------|---------------------------|------|------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7       | bit6       | bit5                      | bit4                    | bit3                    | bit2                      | bit1 | bit0 |
| MOSI  | 1     | 0     | 1     | 1     | 0     | 0     | 0    | P    | CAN_mode_1 | CAN_mode_0 | CAN_au <sub>to</sub> _dis | LIN_m <sub>ode</sub> _1 | LIN_m <sub>ode</sub> _0 | LIN_au <sub>to</sub> _dis | 0    | 0    |

**Table 58. CAN\_LIN mode register description**

| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vother_s_G | CAN_mode_1 | CAN_mode_0 | CAN_au_dis | LIN_mode_1 | LIN_mode_0 | LIN_au_dis | CAN_wu | LIN_wu |
|------|-------|-------|-------|-------|-------|--------|---------|------------|------------|------------|------------|------------|------------|------------|--------|--------|
| Read |       |       |       |       |       |        |         |            |            |            |            |            |            |            |        |        |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8       | bit7       | bit6       | bit5       | bit4       | bit3       | bit2       | bit1   | bit0   |
| MOSI | 0     | 0     | 1     | 1     | 0     | 0      | 0       | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0      | 0      |
|      |       |       |       |       |       |        |         |            |            |            |            |            |            |            |        |        |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vother_s_G | CAN_mode_1 | CAN_mode_0 | CAN_au_dis | LIN_mode_1 | LIN_mode_0 | LIN_au_dis | CAN_wu | LIN_wu |

**Table 59. CAN\_LIN mode. description and configuration of the bits (default value in bold)**

|              |                 |   |
|--------------|-----------------|---|
| CAN_mode_1:0 | Description     | Configure the CAN mode  |
|              | 00              | Sleep / NO wake-up capability   |
|              | 01              | LISTEN ONLY   |
|              | <b>10</b>       | <b>Sleep / Wake-up capability</b>   |
|              | 11              | Normal operation mode   |
|              | Reset condition | Power On Reset  |
| CAN_au_dis   | Description     | Automatic CAN Tx disable  |
|              | 0               | NO auto disable   |
|              | <b>1</b>        | <b>Reset CAN_mode from “11” to “01” on CAN over temp or TXD dominant or RXD recessive event</b>   |
|              | Reset condition | Power On Reset  |
| LIN_mode_1:0 | Description     | Configure the LIN mode  |
|              | 00              | Sleep / NO wake-up capability   |
|              | 01              | LISTEN ONLY   |
|              | <b>10</b>       | <b>Sleep / Wake-up capability</b>   |
|              | 11              | Normal operation mode   |
|              | Reset condition | Power On Reset  |
| LIN_au_dis   | Description     | Automatic LIN Tx Disable  |
|              | 0               | No Auto disable   |
|              | <b>1</b>        | <b>Reset LIN_mode from “11” to “01” on LIN over temp or TXDL dominant or RXDL recessive event</b> |
|              | Reset condition |   |
| CAN_wu       | Description     | Report a wake-up event from the CAN   |
|              | <b>0</b>        | <b>No wake-up</b>   |
|              | 1               | Wake-up detected  |
|              | Reset condition | Power On Reset / Read   |
| LIN_WU       | Description     | Report a wake-up event from the LIN   |
|              | <b>0</b>        | <b>No wake-up</b>   |
|              | 1               | Wake-up detected  |
|              | Reset condition | Power On Reset / Read   |

**Notes**

33. CAN mode is automatically configured to “sleep + wake-up capability[10]” if CAN mode was different than “sleep + no wake-up capability [00]” before the device enters in LPOFF. After LPOFF, the initial CAN mode prior to enter LPOFF is restored.



## 7.3.22 Can\_Mode\_2

**Table 60. CAN\_MODE\_2 register description**

| Write |       |       |       |       |       |        |         |           |      |      |      |             |             |           |           |           |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|------|------|------|-------------|-------------|-----------|-----------|-----------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7 | bit6 | bit5 | bit4        | bit3        | bit2      | bit1      | bit0      |
| MOSI  | 1     | 0     | 1     | 1     | 0     | 0      | 1       | P         | 0    | 0    | 0    | Vcan_OV_Mon | secure_3    | secure_2  | secure_1  | secure_0  |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | 0    | 0    | 0    | 0           | Vcan_OV_Mon | Reserv ed | Reserv ed | Reserv ed |

| Read |       |       |       |       |       |        |         |           |      |      |      |      |             |           |           |           |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|------|------|------|------|-------------|-----------|-----------|-----------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7 | bit6 | bit5 | bit4 | bit3        | bit2      | bit1      | bit0      |
| MOSI | 0     | 0     | 1     | 1     | 0     | 0      | 1       | 0         | 0    | 0    | 0    | 0    | 0           | 0         | 0         | 0         |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | 0    | 0    | 0    | 0    | Vcan_OV_Mon | Reserv ed | Reserv ed | Reserv ed |

**Table 61. CAN\_MODE\_2. description and configuration of the bits (default value in bold)**

|             |                 |   |
|-------------|-----------------|---|
| Vcan_OV_Mon | Description     | VCAN OV Monitoring  |
|             | <b>0</b>        | <b>OFF. V<sub>CAN</sub> OV is not monitored. Flag is ignored</b>  |
|             | 1               | ON. V <sub>CAN</sub> OV flag is under monitoring. In case of OV the V <sub>CAN</sub> regulator is switched OFF. |
|             | Reset condition | Power On Reset  |
| Secure 3:0  | Description     | Secured bits based on write bits  |
|             |                 | Secured_3 = NOT(bit5)<br>Secured_2 = NOT(bit4)<br>Secured_1 = bit7<br>Secured_0 = bit6                          |

## 7.3.23 INIT SUPERVISOR1

**Table 62. INIT SUPERVISOR1 register description**

| Write |       |       |       |       |       |        |         |           |            |            |            |               |           |            |            |            |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|------------|------------|------------|---------------|-----------|------------|------------|------------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7       | bit6       | bit5       | bit4          | bit3      | bit2       | bit1       | bit0       |
| MOSI  | 1     | 1     | 0     | 0     | 0     | 0      | 1       | P         | Vcore_FS1  | Vcore_FS_0 | Vcca_F_S_1 | Vcca_F_S_0    | secure_3  | Secure_2   | Secure_1   | Secure_0   |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_FS_err | SPI_FS_CLK | SPI_FS_Req | SPI_FS_Parity | Vcore_FS1 | Vcore_FS_0 | Vcca_F_S_1 | Vcca_F_S_0 |

| Read |       |       |       |       |       |       |      |      |      |      |      |      |      |      |      |      |
|------|-------|-------|-------|-------|-------|-------|------|------|------|------|------|------|------|------|------|------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10 | bit9 | bit8 | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
| MOSI | 0     | 1     | 0     | 0     | 0     | 0     | 1    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**Table 62. INIT SUPERVISOR1 register description**

|      |       |    |       |       |      |        |         |           |            |            |            |               |           |            |            |            |
|------|-------|----|-------|-------|------|--------|---------|-----------|------------|------------|------------|---------------|-----------|------------|------------|------------|
| MISO | SPI_G | WU | CAN_G | LIN_G | IO_G | Vpre_G | Vcore_G | Vothers_G | SPI_FS_err | SPI_FS_CLK | SPI_FS_Req | SPI_FS_Parity | Vcore_FS1 | Vcore_FS_0 | Vcca_F_S_1 | Vcca_F_S_0 |
|------|-------|----|-------|-------|------|--------|---------|-----------|------------|------------|------------|---------------|-----------|------------|------------|------------|

**Table 63. INIT SUPERVISOR1. description and configuration of the bits (default value in bold)**

|               |                 |  |
|---------------|-----------------|--|
| Vcore_FS1:0   | Description     | V <sub>CORE</sub> safety input.  |
|               | 00              | No effect of V <sub>CORE_FB_OV</sub> and V <sub>CORE_FB_UV</sub> on RSTb and FSxx  |
|               | 01              | V <sub>CORE_FB_OV</sub> DOES HAVE an impact on RSTb and FSxx. V <sub>CORE_FB_UV</sub> DOES HAVE an impact on RSTb only   |
|               | 10              | V <sub>CORE_FB_OV</sub> DOES HAVE an impact on RSTb and FSxx. No effect of V <sub>CORE_FB_UV</sub> on RSTb and FSxx  |
|               | <b>11</b>       | <b>Both V<sub>CORE_FB_OV</sub> and V<sub>CORE_FB_UV</sub> DO HAVE an impact on RSTb and FSxx</b>   |
|               | Reset condition | Power On Reset   |
| Vcca_FS1:0    | Description     | V <sub>CCA</sub> safety input.   |
|               | 00              | No effect of V <sub>CCA_OV</sub> and V <sub>CCA_UV</sub> on RSTb and FSxx  |
|               | 01              | V <sub>CCA_OV</sub> DOES HAVE an impact on RSTb and FSxx. V <sub>CCA_UV</sub> DOES HAVE an impact on RSTb only   |
|               | 10              | V <sub>CCA_OV</sub> DOES HAVE an impact on RSTb and FSxx. No effect of V <sub>CCA_UV</sub> on RSTb and FSxx  |
|               | <b>11</b>       | <b>Both V<sub>CCA_OV</sub> and V<sub>CCA_UV</sub> DO HAVE an impact on RSTb and FSxx</b>   |
|               | Reset condition | Power On Reset   |
| Secure3:0     | Description     | Secured bits based on write bits   |
|               |                 | Secured_3 = NOT(bit5)<br>Secured_2 = NOT(bit4)<br>Secured_1 = bit7<br>Secured_0 = bit6   |
| SPI_FS_err    | Description     | Secured SPI communication check, concerns Fail-safe logic only   |
|               | <b>0</b>        | <b>No error</b>  |
|               | 1               | Error detected in the secured bits   |
|               | Reset condition | Power On Reset   |
| SPI_FS_CLK    | Description     | SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by the SPI_CLK_bit |
|               | <b>0</b>        | <b>16 clock cycles during NCS low</b>  |
|               | 1               | Wrong number of clock cycles (<16 or >16)  |
|               | Reset condition | Power On Reset   |
| SPI_FS_Req    | Description     | Invalid SPI access (Wrong Write or Read, Write to INIT registers in Normal mode, wrong address), concerns fail-safe logic only.  |
|               | <b>0</b>        | <b>No error</b>  |
|               | 1               | SPI violation  |
|               | Reset condition | Power On Reset   |
| SPI_FS_Parity | Description     | SPI parity bit error detection, concerns fail-safe logic only  |
|               | <b>0</b>        | <b>Parity bit OK</b>   |
|               | 1               | Parity bit ERROR   |
|               | Reset condition | Power On Reset   |

## 7.3.24 INIT SUPERVISOR2

**Table 64. INIT SUPERVISOR2 register description**

| Write |       |       |       |       |       |        |         |           |            |            |            |               |          |          |          |          |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|------------|------------|------------|---------------|----------|----------|----------|----------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7       | bit6       | bit5       | bit4          | bit3     | bit2     | bit1     | bit0     |
| MOSI  | 1     | 1     | 0     | 0     | 0     | 1      | 0       | P         | Vaux_FS1   | Vaux_FS0   | 0          | DIS_8s        | Secure_3 | Secure_2 | Secure_1 | Secure_0 |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_FS_err | SPI_FS_CLK | SPI_FS_req | SPI_FS_Parity | 0        | DIS_8s   | Vaux_FS1 | Vaux_FS0 |

| Read |       |       |       |       |       |        |         |           |            |            |            |               |      |        |          |          |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|------------|------------|------------|---------------|------|--------|----------|----------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7       | bit6       | bit5       | bit4          | bit3 | bit2   | bit1     | bit0     |
| MOSI | 0     | 1     | 0     | 0     | 0     | 1      | 0       | 0         | 0          | 0          | 0          | 0             | 0    | 0      | 0        | 0        |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_FS_err | SPI_FS_CLK | SPI_FS_req | SPI_FS_Parity | 0    | DIS_8s | Vaux_FS1 | Vaux_FS0 |

**Table 65. INIT SUPERVISOR2. description and configuration of the bits (default value in bold)**

|            |                 |  |
|------------|-----------------|--|
| Vaux_FS1:0 | Description     | V <sub>AUX</sub> safety input.   |
|            | 00              | No effect of V <sub>AUX_OV</sub> and V <sub>AUX_UV</sub> on RSTb and FSxx  |
|            | 01              | V <sub>AUX_OV</sub> DOES HAVE an impact on RSTb and FSxx. V <sub>AUX_UV</sub> DOES HAVE an impact on RSTb only   |
|            | 10              | V <sub>AUX_OV</sub> DOES HAVE an impact on RSTb and FSxx. No effect of V <sub>AUX_UV</sub> on RSTb and FSxx  |
|            | <b>11</b>       | <b>Both V<sub>AUX_OV</sub> and V<sub>AUX_UV</sub> DO HAVE an impact on RSTb and FSxx</b>   |
|            | Reset condition | Power On Reset   |
| DIS_8s     | Description     | Disable the 8.0 s timer used to enter Deep Fail-safe mode  |
|            | <b>0</b>        | <b>ENABLED</b>   |
|            | 1               | DISABLED   |
|            | Reset condition | Power On Reset   |
| Secure3:0  | Description     | Secured bits based on write bits   |
|            |                 | Secured_3 = NOT(bit5)<br>Secured_2 = NOT(bit4)<br>Secured_1 = bit7<br>Secured_0 = bit6   |
| SPI_FS_err | Description     | Secured SPI communication check, concerns fail-safe logic only.  |
|            | <b>0</b>        | <b>No error</b>  |
|            | 1               | Error detected in the secured bits   |
|            | Reset condition | Power On Reset   |
| SPI_FS_CLK | Description     | SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by SPI_CLK_bit |
|            | <b>0</b>        | <b>16 clock cycles during NCS low</b>  |
|            | 1               | Wrong number of clock cycles (<16 or >16)  |
|            | Reset condition | Power On Reset   |

**Table 65. INIT SUPERVISOR2. description and configuration of the bits (default value in bold) (continued)**

|               |                 |  |
|---------------|-----------------|--|
| SPI_FS_Req    | Description     | Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe Logic only |
|               | <b>0</b>        | <b>No error</b>  |
|               | 1               | SPI violation  |
|               | Reset condition | Power On Reset   |
| SPI_FS_Parity | Description     | SPI parity bit error detection, concerns fail-safe logic only  |
|               | <b>0</b>        | <b>Parity bit OK</b>   |
|               | 1               | Parity bit ERROR   |
|               | Reset condition | Power On Reset   |

## 7.3.25 INIT SUPERVISOR3

**Table 66. INIT SUPERVISOR3 register description**

| Write |       |       |       |       |       |        |         |           |            |            |            |               |          |          |          |          |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|------------|------------|------------|---------------|----------|----------|----------|----------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7       | bit6       | bit5       | bit4          | bit3     | bit2     | bit1     | bit0     |
| MOSI  | 1     | 1     | 0     | 0     | 0     | 1      | 1       | P         | 0          | Vcca_5_D   | Vaux_5_D   | 0             | Secure_3 | Secure_2 | Secure_1 | Secure_0 |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_FS_err | SPI_FS_CLK | SPI_FS_req | SPI_FS_Parity | 0        | Reserved | Vcca_5_D | Vaux_5_D |

| Read |       |       |       |       |       |        |         |           |            |            |            |               |      |          |          |          |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|------------|------------|------------|---------------|------|----------|----------|----------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7       | bit6       | bit5       | bit4          | bit3 | bit2     | bit1     | bit0     |
| MOSI | 0     | 1     | 0     | 0     | 0     | 1      | 1       | 0         | 0          | 0          | 0          | 0             | 0    | 0        | 0        | 0        |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_FS_err | SPI_FS_CLK | SPI_FS_req | SPI_FS_Parity | 0    | Reserved | Vcca_5_D | Vaux_5_D |

**Table 67. INIT SUPERVISOR3. description and configuration of the bits (default value in bold)**

|                     |                 |  |
|---------------------|-----------------|--|
| V <sub>CCA_5D</sub> | Description     | Configure the V <sub>CCA</sub> undervoltage in degraded mode. Only valid for 5.0 V   |
|                     | <b>0</b>        | <b>Normal 5.0 V undervoltage detection threshold (V<sub>CCA_UV_5</sub>)</b>  |
|                     | 1               | Degraded mode, i.e lower undervoltage detection threshold applied (V <sub>CCA_UV_D</sub> )   |
|                     | Reset condition | Power On Reset   |
| V <sub>AUX_5D</sub> | Description     | Configure the V <sub>AUX</sub> undervoltage in degraded mode. Only valid for 5.0 V   |
|                     | <b>0</b>        | <b>Normal 5.0 V undervoltage detection threshold (V<sub>AUX_UV_5</sub>)</b>  |
|                     | 1               | Degraded mode, i.e lower undervoltage detection threshold applied (V <sub>AUX_UV_5D</sub> )  |
|                     | Reset condition | Power On Reset   |
| Secure3:0           | Description     | Secured bits based on write bits   |
|                     |                 | Secured_3 = NOT(bit5)<br>Secured_2 = NOT(bit4)<br>Secured_1 = bit7<br>Secured_0 = bit6   |
| SPI_FS_err          | Description     | Secured SPI communication check, concerns fail-safe logic only   |
|                     | <b>0</b>        | <b>No error</b>  |
|                     | 1               | Error detected in the secured bits   |
|                     | Reset condition | Power On Reset   |
| SPI_FS_CLK          | Description     | SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by the SPI_CLK_bit |
|                     | <b>0</b>        | <b>16 clock cycles during NCS low</b>  |
|                     | 1               | Wrong number of clock cycles (<16 or >16)  |
|                     | Reset condition | Power On Reset   |
| SPI_FS_Req          | Description     | Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe logic only   |
|                     | <b>0</b>        | <b>No error</b>  |
|                     | 1               | SPI violation  |
|                     | Reset condition | Power On Reset   |

**Table 67. INIT SUPERVISOR3. description and configuration of the bits (default value in bold) (continued)**

|               |                 |   |
|---------------|-----------------|---|
| SPI_FS_Parity | Description     | SPI parity bit error detection, concerns fail-safe logic only |
|               | <b>0</b>        | <b>Parity bit OK</b>  |
|               | 1               | Parity bit ERROR  |
|               | Reset condition | Power On Reset  |

## 7.3.26 Init FSSM1

**Table 68. INIT FSSM1 register description**

|       |       |       |       |       |       |        |         |           |             |             |             |                |          |          |          |          |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|-------------|-------------|-------------|----------------|----------|----------|----------|----------|
| Write |       |       |       |       |       |        |         |           |             |             |             |                |          |          |          |          |
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7        | bit6        | bit5        | bit4           | bit3     | bit2     | bit1     | bit0     |
| MOSI  | 1     | 1     | 0     | 0     | 1     | 0      | 0       | P         | IO_01_FS    | IO_1_FS     | IO_45_FS    | RSTb_low       | Secure_3 | Secure_2 | Secure_1 | Secure_0 |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_F S_err | SPI_F S_CLK | SPI_F S_req | SPI_F S_Parity | IO_01_FS | IO_1_FS  | IO_45_FS | RSTb_low |
| Read  |       |       |       |       |       |        |         |           |             |             |             |                |          |          |          |          |
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7        | bit6        | bit5        | bit4           | bit3     | bit2     | bit1     | bit0     |
| MOSI  | 0     | 1     | 0     | 0     | 1     | 0      | 0       | 0         | 0           | 0           | 0           | 0              | 0        | 0        | 0        | 0        |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_F S_err | SPI_F S_CLK | SPI_F S_req | SPI_F S_Parity | IO_01_FS | IO_1_FS  | IO_45_FS | RSTb_low |

**Table 69. INIT FSSM1. description and configuration of the bits (default value in bold)**

|          |                 |  |
|----------|-----------------|--|
| IO_01_FS | Description     | Configure the couple of IO_1:0 as safety inputs              |
|          | <b>0</b>        | <b>NOT SAFETY</b>  |
|          | 1               | SAFETY CRITICAL  |
|          | Reset condition | Power On Reset   |
| IO_1_FS  | Description     | Configure IO_1 as safety inputs                              |
|          | <b>0</b>        | <b>NOT SAFETY</b>  |
|          | 1               | SAFETY CRITICAL (External resistor bridge monitoring active) |
|          | Reset condition | Power On Reset   |
| IO_45_FS | Description     | Configure the couple of IO_5:4 as safety inputs              |
|          | <b>0</b>        | <b>NOT SAFETY</b>  |
|          | 1               | SAFETY CRITICAL  |
|          | Reset condition | Power On Reset   |
| RSTb_low | Description     | Configure the Rstb LOW duration time                         |
|          | <b>0</b>        | <b>10 ms</b>   |
|          | 1               | 1.0 ms   |
|          | Reset condition | Power On Reset   |

**Table 69. INIT FSSM1. description and configuration of the bits (default value in bold) (continued)**

|               |                 |  |
|---------------|-----------------|--|
| Secure3:0     | Description     | Secured bits based on write bits   |
|               |                 | Secured_3 = NOT(bit5)<br>Secured_2 = NOT(bit4)<br>Secured_1 = bit7<br>Secured_0 = bit6   |
| SPI_FS_err    | Description     | Secured SPI communication check, concerns fail-safe logic only   |
|               | <b>0</b>        | <b>No error</b>  |
|               | 1               | Error detected in the secured bits   |
|               | Reset condition | Power On Reset   |
| SPI_FS_CLK    | Description     | SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by the SPI_CLK_bit |
|               | <b>0</b>        | <b>16 clock cycles during NCS low</b>  |
|               | 1               | Wrong number of clock cycles (<16 or >16)  |
|               | Reset condition | Power On Reset   |
| SPI_FS_Req    | Description     | Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe logic only   |
|               | <b>0</b>        | <b>No error</b>  |
|               | 1               | SPI violation  |
|               | Reset condition | Power On Reset   |
| SPI_FS_Parity | Description     | SPI parity bit error detection, concerns fail-safe logic only  |
|               | <b>0</b>        | <b>Parity bit OK</b>   |
|               | 1               | Parity bit ERROR   |
|               | Reset condition | Power On Reset   |

## 7.3.27 Init FSSM2

**Table 70. INIT FSSM2 register description**

| Write |       |       |       |       |       |        |         |           |             |            |            |               |             |          |          |          |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|-------------|------------|------------|---------------|-------------|----------|----------|----------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7        | bit6       | bit5       | bit4          | bit3        | bit2     | bit1     | bit0     |
| MOSI  | 1     | 1     | 0     | 0     | 1     | 0      | 1       | P         | RSTb_err_FS | IO_23_FS   | PS         | 0             | Secure_3    | Secure_2 | Secure_1 | Secure_0 |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_FS_err  | SPI_FS_CLK | SPI_FS_req | SPI_FS_Parity | RSTb_err_FS | IO_23_FS | PS       | 0        |

**Table 70. INIT FSSM2 register description (continued)**

| Read |       |       |       |       |       |        |         |           |            |            |            |               |             |          |      |      |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|------------|------------|------------|---------------|-------------|----------|------|------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7       | bit6       | bit5       | bit4          | bit3        | bit2     | bit1 | bit0 |
| MOSI | 0     | 1     | 0     | 0     | 1     | 0      | 1       | 0         | 0          | 0          | 0          | 0             | 0           | 0        | 0    | 0    |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_FS_err | SPI_FS_CLK | SPI_FS_req | SPI_FS_Parity | RSTb_err_FS | IO_23_FS | PS   | 0    |

**Table 71. INIT FSSM2. description and configuration of the bits (default value in bold)**

|               |                 |  |
|---------------|-----------------|--|
| IO_23_FS      | Description     | Configure the couple of IO_3:2 as safety inputs for FCCU monitoring  |
|               | 0               | NOT SAFETY   |
|               | 1               | <b>SAFETY CRITICAL</b>   |
|               | Reset condition | Power On Reset   |
| RSTb_err_FS   | Description     | Configure the values of the RSTb error counter   |
|               | 0               | <b>intermediate = 3; final = 6</b>   |
|               | 1               | intermediate = 1; final = 2  |
|               | Reset condition | Power On Reset   |
| PS            | Description     | Configure the F <sub>CCU</sub> polarity  |
|               | 0               | <b>Fccu_eaout_1:0 active HIGH</b>  |
|               | 1               | Fccu_eaout_1:0 active LOW  |
|               | Reset condition | Power On Reset   |
| Secure3:0     | Description     | Secured bits based on write bits   |
|               |                 | Secured_3 = NOT(bit5)<br>Secured_2 = NOT(bit4)<br>Secured_1 = bit7<br>Secured_0 = bit6   |
| SPI_FS_err    | Description     | Secured SPI communication check, concerns fail-safe logic only   |
|               | 0               | <b>No error</b>  |
|               | 1               | Error detected in the secured bits   |
|               | Reset condition | Power On Reset   |
| SPI_FS_CLK    | Description     | SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by SPI_CLK_bit |
|               | 0               | <b>16 clock cycles during NCS low</b>  |
|               | 1               | Wrong number of clock cycles (<16 or >16)  |
|               | Reset condition | Power On Reset   |
| SPI_FS_Req    | Description     | Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe Logic only   |
|               | 0               | <b>No error</b>  |
|               | 1               | SPI violation  |
|               | Reset condition | Power On Reset   |
| SPI_FS_Parity | Description     | SPI parity bit error detection, concerns fail-safe logic only  |
|               | 0               | <b>Parity bit OK</b>   |
|               | 1               | Parity bit ERROR   |
|               | Reset condition | Power On Reset   |



## 7.3.28 WD window

**Table 72. WD window register description**

Write

|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9         | bit8          | bit7           | bit6           | bit5           | bit4              | bit3           | bit2           | bit1           | bit0           |
|------|-------|-------|-------|-------|-------|--------|--------------|---------------|----------------|----------------|----------------|-------------------|----------------|----------------|----------------|----------------|
| MOSI | 1     | 1     | 0     | 0     | 1     | 1      | 0            | P             | WD_wi<br>ndow3 | WD_wi<br>ndow2 | WD_wi<br>ndow1 | WD_wi<br>ndow0    | Secure<br>_3   | Secure<br>_2   | Secure<br>_1   | Secure<br>_0   |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_<br>_G | Vothers<br>_G | SPI_FS<br>_err | SPI_FS<br>_CLK | SPI_FS<br>_req | SPI_FS<br>_Parity | WD_wi<br>ndow3 | WD_wi<br>ndow2 | WD_wi<br>ndow1 | WD_wi<br>ndow0 |

Read

|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9         | bit8          | bit7           | bit6           | bit5           | bit4              | bit3           | bit2           | bit1           | bit0           |
|------|-------|-------|-------|-------|-------|--------|--------------|---------------|----------------|----------------|----------------|-------------------|----------------|----------------|----------------|----------------|
| MOSI | 0     | 1     | 0     | 0     | 1     | 1      | 0            | 0             | 0              | 0              | 0              | 0                 | 0              | 0              | 0              | 0              |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_<br>_G | Vothers<br>_G | SPI_FS<br>_err | SPI_FS<br>_CLK | SPI_FS<br>_req | SPI_FS<br>_Parity | WD_wi<br>ndow3 | WD_wi<br>ndow2 | WD_wi<br>ndow1 | WD_wi<br>ndow0 |

Any WRITE command to the WD\_window in the Normal mode must be followed by a READ command to verify the correct change of the WD window duration

**Table 73. WD window. description and configuration of the bits (default value in bold)**

|               |                 |  |
|---------------|-----------------|--|
| WD_Window_3:0 | Description     | Configure the watchdog window duration. Duty cycle if set to 50%                       |
|               | 0000            | DISABLE  |
|               | 0001            | 1.0 ms   |
|               | 0010            | 2.0 ms   |
|               | <b>0011</b>     | <b>3.0 ms</b>  |
|               | 0100            | 4.0 ms   |
|               | 0101            | 6.0 ms   |
|               | 0110            | 8.0 ms   |
|               | 0111            | 12 ms  |
|               | 1000            | 16 ms  |
|               | 1001            | 24 ms  |
|               | 1010            | 32 ms  |
|               | 1011            | 64 ms  |
|               | 1100            | 128 ms   |
|               | 1101            | 256 ms   |
|               | 1110            | 512 ms   |
|               | 1111            | 1024 ms  |
|               | Reset condition | Power On Reset   |
| Secure3:0     | Description     | Secured bits based on write bits   |
|               |                 | Secured_3 = NOT(bit5)<br>Secured_2 = NOT(bit4)<br>Secured_1 = bit7<br>Secured_0 = bit6 |

**Table 73. WD window. description and configuration of the bits (default value in bold) (continued)**

|               |                 |   |
|---------------|-----------------|---|
| SPI_FS_err    | Description     | Secured SPI communication check, concerns fail-safe logic only  |
|               | <b>0</b>        | <b>No error</b>   |
|               | 1               | Error detected in the secured bits  |
|               | Reset condition | Power On Reset  |
| SPI_FS_CLK    | Description     | SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by the SPI_CLK bit. |
|               | <b>0</b>        | <b>16 clock cycles during NCS low</b>   |
|               | 1               | Wrong number of clock cycles (<16 or >16)   |
|               | Reset condition | Power On Reset  |
| SPI_FS_Req    | Description     | Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe logic only  |
|               | <b>0</b>        | <b>No error</b>   |
|               | 1               | SPI violation   |
|               | Reset condition | Power On Reset  |
| SPI_FS_Parity | Description     | SPI parity bit error detection, concerns fail-safe logic only   |
|               | <b>0</b>        | <b>Parity bit OK</b>  |
|               | 1               | Parity bit ERROR  |
|               | Reset condition | Power On Reset  |

## 7.3.29 WD\_LFSR

**Table 74. WD LFSR register description**

|       |       |       |       |       |       |        |         |            |            |            |            |            |            |            |            |            |
|-------|-------|-------|-------|-------|-------|--------|---------|------------|------------|------------|------------|------------|------------|------------|------------|------------|
| Write |       |       |       |       |       |        |         |            |            |            |            |            |            |            |            |            |
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8       | bit7       | bit6       | bit5       | bit4       | bit3       | bit2       | bit1       | bit0       |
| MOSI  | 1     | 1     | 0     | 0     | 1     | 1      | 1       | P          | WD_LF SR_7 | WD_LF SR_6 | WD_LF SR_5 | WD_LF SR_4 | WD_LF SR_3 | WD_LF SR_2 | WD_LF SR_1 | WD_LF SR_0 |
|       |       |       |       |       |       |        |         |            |            |            |            |            |            |            |            |            |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vother_s_G | WD_LF SR_7 | WD_LF SR_6 | WD_LF SR_5 | WD_LF SR_4 | WD_LF SR_3 | WD_LF SR_2 | WD_LF SR_1 | WD_LF SR_0 |
| Read  |       |       |       |       |       |        |         |            |            |            |            |            |            |            |            |            |
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8       | bit7       | bit6       | bit5       | bit4       | bit3       | bit2       | bit1       | bit0       |
| MOSI  | 0     | 1     | 0     | 0     | 1     | 1      | 1       | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          | 0          |
|       |       |       |       |       |       |        |         |            |            |            |            |            |            |            |            |            |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vother_s_G | WD_LF SR_7 | WD_LF SR_6 | WD_LF SR_5 | WD_LF SR_4 | WD_LF SR_3 | WD_LF SR_2 | WD_LF SR_1 | WD_LF SR_0 |

**Table 75. WD LFSR. description and configuration of the bits**

|             |                 |   |
|-------------|-----------------|---|
| WD_LFSR_7:0 | Description     | WD 8 bits LFSR value. Used to write the seed at any time  |
|             | 0...            | bit7:bit0: 10110010 default value at start-up or after a Power on reset: 0xB2 <sup>(34)</sup> , <sup>(35)</sup> |
|             | 1...            |   |
|             | Reset condition | Power On Reset  |

### Notes

34. Value Bit7:Bit0: 1111 1111 is prohibited.

35. During a write command, MISO reports the previous register content.

## 7.3.30 WD answer

**Table 76. WD answer register description**

| Write |       |       |       |       |       |        |         |           |             |             |             |             |             |             |             |             |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7        | bit6        | bit5        | bit4        | bit3        | bit2        | bit1        | bit0        |
| MOSI  | 1     | 1     | 0     | 1     | 0     | 0      | 0       | P         | WD_answer_7 | WD_answer_6 | WD_answer_5 | WD_answer_4 | WD_answer_3 | WD_answer_2 | WD_answer_1 | WD_answer_0 |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | RSTb        | FS0         | WD          | FS0_G       | IO_FS_G     | 0           | FS_EC_C     | FS_reg_Ecc  |

| Read |       |       |       |       |       |        |         |           |      |      |      |       |         |      |         |            |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|------|------|------|-------|---------|------|---------|------------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7 | bit6 | bit5 | bit4  | bit3    | bit2 | bit1    | bit0       |
| MOSI | 0     | 1     | 0     | 1     | 0     | 0      | 0       | 0         | 0    | 0    | 0    | 0     | 0       | 0    | 0       | 0          |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | RSTb | FS0  | WD   | FS0_G | IO_FS_G | 0    | FS_EC_C | FS_reg_Ecc |

**Table 77. WD answer. description and configuration of the bits (default value in bold)**

|               |                 |  |
|---------------|-----------------|--|
| WD_answer_7:0 | Description     | WD answer from the MCU   |
|               | 0...            | Answer = (NOT(((LFSR x 4)+6)-4))/4   |
|               | 1...            |  |
|               | Reset condition | Power On Reset / RSTb LOW  |
| RSTb          | Description     | Report a reset event   |
|               | <b>0</b>        | <b>No Reset</b>  |
|               | 1               | Reset occurred   |
|               | Reset condition | Power On Reset / Read  |
| FS0b          | Description     | Report a fail-safe event   |
|               | 0               | No fail-safe   |
|               | <b>1</b>        | <b>Fail safe event occurred / Also default state at power-up after LPOFF as FS0b is asserted low</b> |
|               | Reset condition | Power On Reset / Read  |
| WD            | Description     | Report a watchdog refresh ERROR  |
|               | <b>0</b>        | <b>WD refresh OK</b>   |
|               | 1               | WRONG WD refresh   |
|               | Reset condition | Power On Reset / Read  |
| FS0_G         | Description     | Report a fail-safe output failure  |
|               | <b>0</b>        | <b>No failure</b>  |
|               | 1               | Failure  |
|               | Reset condition | Power On Reset / Read  |
| IO_FS_G       | Description     | Report an IO monitoring error  |
|               | <b>0</b>        | <b>No error</b>  |
|               | 1               | Error detected   |
|               | Reset condition | Power On Reset   |

**Table 77. WD answer. description and configuration of the bits (default value in bold) (continued)**

|            |                 |  |
|------------|-----------------|--|
| FS_ECC     | Description     | Report an error code correction on fail-safe state machine |
|            | <b>0</b>        | <b>No ECC</b>  |
|            | 1               | ECC done   |
|            | Reset condition | Power On Reset / Read                                      |
| FS_req_ECC | Description     | Report an error code correction on fail-safe registers     |
|            | <b>0</b>        | <b>No ECC</b>  |
|            | 1               | ECC done   |
|            | Reset condition | Power On Reset / Read                                      |

FS0\_G = RSTB\_short\_high or FS0B\_short\_high or FS0B\_short\_low

IO\_FS\_G = IO\_01\_fail or IO\_1\_fail or IO\_23\_fail or IO\_45\_fail

Values of the three registers WD\_answer, WD\_counter, and DIAG\_FS2 are updated at the end of any SPI access to one of these registers. To always get up to date values, it is recommended to make two consecutive SPI accesses to these registers. Example: read WD\_answer, read again WD\_answer, read WD\_counter, read DIAG\_FS2. The first read updates the three registers and the second read report the latest information.

### 7.3.31 Fail-safe out (FS\_out)

**Table 78. Fail-safe out register description**

|       |       |       |       |       |       |        |         |           |          |          |          |          |          |          |          |          |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|----------|----------|----------|----------|----------|----------|----------|----------|
| Write |       |       |       |       |       |        |         |           |          |          |          |          |          |          |          |          |
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7     | bit6     | bit5     | bit4     | bit3     | bit2     | bit1     | bit0     |
| MOSI  | 1     | 1     | 0     | 1     | 0     | 0      | 1       | P         | FS_out_7 | FS_out_6 | FS_out_5 | FS_out_4 | FS_out_3 | FS_out_2 | FS_out_1 | FS_out_0 |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |

**Table 79. Fail-safe out. description and configuration of the bits**

|            |                 |  |
|------------|-----------------|--|
| FS_out_7:0 | Description     | Secured 8 bits word to release the FS0b  |
|            | 0...            | Depend on LFSR_out value and calculation |
|            | 1...            |  |
|            | Reset condition | Power On Reset -> Default = 00h          |

## 7.3.32 RSTB request

**Table 80. RSTB request register description**

| Write |       |       |       |       |       |        |         |           |      |      |              |      |          |          |          |          |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|------|------|--------------|------|----------|----------|----------|----------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7 | bit6 | bit5         | bit4 | bit3     | bit2     | bit1     | bit0     |
| MOSI  | 1     | 1     | 0     | 1     | 0     | 1      | 0       | P         | 0    | 0    | RSTb_request | 0    | Secure_3 | Secure_2 | Secure_1 | Secure_0 |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | 0    | 0    | 0            | 0    | 0        | 0        | 0        | 0        |

**Table 81. RSTB request. description and configuration of the bits (default value in bold)**

|              |                 |  |
|--------------|-----------------|--|
| RSTb_request | Description     | Request a RSTb low pulse   |
|              | <b>0</b>        | <b>No request</b>  |
|              | 1               | Request a RSTb low pulse   |
|              | Reset condition | Power On Reset / When RSTb done  |
| Secure3:0    | Description     | Secured bits based on write bits   |
|              |                 | Secured_3 = NOT(bit5)<br>Secured_2 = NOT(bit4)<br>Secured_1 = bit7<br>Secured_0 = bit6 |

## 7.3.33 INIT\_WD

**Table 82. INIT WD register description**

| Write |       |       |       |       |       |        |         |           |                  |                  |                    |                    |                  |                  |                    |                    |
|-------|-------|-------|-------|-------|-------|--------|---------|-----------|------------------|------------------|--------------------|--------------------|------------------|------------------|--------------------|--------------------|
|       | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7             | bit6             | bit5               | bit4               | bit3             | bit2             | bit1               | bit0               |
| MOSI  | 1     | 1     | 0     | 1     | 0     | 1      | 1       | P         | WD_C NT_err or_1 | WD_C NT_err or_0 | WD_C NT_refr esh_1 | WD_C NT_refr esh_0 | secure_3         | secure_2         | secure_1           | secure_0           |
| MISO  | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_F S_err      | SPI_F S_CLK      | SPI_F S_Req        | SPI_F S_Parity     | WD_C NT_err or_1 | WD_C NT_err or_0 | WD_C NT_refr esh_1 | WD_C NT_refr esh_0 |

| Read |       |       |       |       |       |        |         |           |             |             |             |                |                  |                  |                    |                    |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|-------------|-------------|-------------|----------------|------------------|------------------|--------------------|--------------------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7        | bit6        | bit5        | bit4           | bit3             | bit2             | bit1               | bit0               |
| MOSI | 0     | 1     | 0     | 1     | 0     | 1      | 1       | 0         | 0           | 0           | 0           | 0              | 0                | 0                | 0                  | 0                  |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | SPI_F S_err | SPI_F S_CLK | SPI_F S_Req | SPI_F S_Parity | WD_C NT_err or_1 | WD_C NT_err or_0 | WD_C NT_refr esh_1 | WD_C NT_refr esh_0 |

**Table 83. INIT WD. description and configuration of the bits (default value in bold)**

|                    |                 |   |
|--------------------|-----------------|---|
| WD_CNT_error_1:0   | Description     | Configure the maximum value of the WD error counter   |
|                    | <b>00</b>       | <b>6</b>  |
|                    | 01              | 6   |
|                    | 10              | 4   |
|                    | 11              | 2   |
|                    | Reset Condition | Power On Reset  |
| WD_CNT_refresh_1:0 | Description     | Configure the maximum value of the WD refresh counter   |
|                    | <b>00</b>       | <b>6</b>  |
|                    | 01              | 4   |
|                    | 10              | 2   |
|                    | 11              | 1   |
|                    | Reset Condition | Power On Reset  |
| Secure3:0          | Description     | Secured bits based on write bits  |
|                    |                 | Secured_3 = NOT(bit5)<br>Secured_2 = NOT(bit4)<br>Secured_1 = bit7<br>Secured_0 = bit6  |
| SPI_FS_err         | Description     | Secured SPI communication check, concerns fail-safe logic only  |
|                    | <b>0</b>        | <b>No error</b>   |
|                    | 1               | Error detected in the secured bits  |
|                    | Reset condition | Power On Reset  |
| SPI_FS_CLK         | Description     | SCLK error detection, concerns internal error in fail-safe logic only and external errors (at pin level) for both main and fail-safe logics. Other errors flagged by the SPI_CLK bit. |
|                    | <b>0</b>        | <b>16 clock cycles during NCS low</b>   |
|                    | 1               | Wrong number of clock cycles (<16 or >16)   |
|                    | Reset condition | Power On Reset  |
| SPI_FS_Req         | Description     | Invalid SPI access (Wrong Write or Read, Write to INIT registers in normal mode, wrong address), concerns fail-safe logic only  |
|                    | <b>0</b>        | <b>No error</b>   |
|                    | 1               | SPI violation   |
|                    | Reset condition | Power On Reset  |
| SPI_FS_Parity      | Description     | SPI parity bit error detection, concerns fail-safe logic only   |
|                    | <b>0</b>        | <b>Parity bit OK</b>  |
|                    | 1               | Parity bit ERROR  |
|                    | Reset condition | Power On Reset  |

## 7.3.34 Diag FS1

**Table 84. DIAG FS1 register description**

| Read |       |       |       |       |       |        |         |           |          |           |      |             |             |      |      |      |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|----------|-----------|------|-------------|-------------|------|------|------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7     | bit6      | bit5 | bit4        | bit3        | bit2 | bit1 | bit0 |
| MOSI | 0     | 1     | 0     | 1     | 1     | 0      | 0       | 0         | 0        | 0         | 0    | 0           | 0           | 0    | 0    | 0    |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | RSTb_ext | RSTb_diag | 0    | FS0b_diag_1 | FS0b_diag_0 | 0    | 0    | 0    |

**Table 85. Diag FS1. description and configuration of the bits (default value in bold)**

|               |                 |                                     |
|---------------|-----------------|-------------------------------------|
| RSTb_diag     | Description     | Report a RSTb short-circuit to HIGH |
|               | <b>0</b>        | <b>No Failure</b>                   |
|               | 1               | Short-circuit HIGH                  |
|               | Reset condition | Power On Reset / Read               |
| RSTb_ext      | Description     | Report an external RSTb             |
|               | <b>0</b>        | <b>No external RSTb</b>             |
|               | 1               | External RSTb                       |
|               | Reset condition | Power On Reset / Read               |
| FS0b_diag_1:0 | Description     | Report a failure on FS0b            |
|               | <b>00</b>       | <b>No Failure</b>                   |
|               | 01              | Short-circuit LOW / open load       |
|               | 1X              | Short-circuit HIGH                  |
|               | Reset condition | Power On Reset / Read               |

## 7.3.35 WD counter

**Table 86. WD counter register description**

| Read |       |       |       |       |       |        |         |           |          |          |          |      |              |              |              |      |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|----------|----------|----------|------|--------------|--------------|--------------|------|
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7     | bit6     | bit5     | bit4 | bit3         | bit2         | bit1         | bit0 |
| MOSI | 0     | 1     | 0     | 1     | 1     | 0      | 1       | 0         | 0        | 0        | 0        | 0    | 0            | 0            | 0            | 0    |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | WD_err_2 | WD_err_1 | WD_err_0 | 0    | WD_refresh_2 | WD_refresh_1 | WD_refresh_0 | 0    |

**Table 87. WD counter. description and configuration of the bits (default value in bold)**

|                |                 |   |
|----------------|-----------------|---|
| WD_err_2:0     | Description     | Report the value of the watchdog error counter  |
|                | <b>000</b>      | From 0 to 5 (6 generates a Reset and this counter is reset to 0)                      |
|                | to 110          |   |
|                | Reset condition | Power On Reset  |
| WD_refresh_2:0 | Description     | Report the value of the watchdog refresh counter                                      |
|                | <b>000</b>      | From 0 to 6 (7 generate a decrease of the RST_err_cnt and this counter is reset to 0) |
|                | to 111          |   |
|                | Reset condition | Power On Reset  |

## 7.3.36 Diag FS2

**Table 88. DIAG FS2 register description**

|      |       |       |       |       |       |        |         |           |            |            |            |      |            |            |           |            |
|------|-------|-------|-------|-------|-------|--------|---------|-----------|------------|------------|------------|------|------------|------------|-----------|------------|
| Read |       |       |       |       |       |        |         |           |            |            |            |      |            |            |           |            |
|      | bit15 | bit14 | bit13 | bit12 | bit11 | bit10  | bit9    | bit8      | bit7       | bit6       | bit5       | bit4 | bit3       | bit2       | bit1      | bit0       |
| MOSI | 0     | 1     | 0     | 1     | 1     | 1      | 0       | 0         | 0          | 0          | 0          | 0    | 0          | 0          | 0         | 0          |
|      |       |       |       |       |       |        |         |           |            |            |            |      |            |            |           |            |
| MISO | SPI_G | WU    | CAN_G | LIN_G | IO_G  | Vpre_G | Vcore_G | Vothers_G | RSTb_err_2 | RSTb_err_1 | RSTb_err_0 | 0    | IO_45_fail | IO_23_fail | IO_1_Fail | IO_01_fail |

**Table 89. Diag FS2. description and configuration of the bits (default value in bold)**

|              |  |  |
|--------------|--|--|
| RSTb_err_2:0 | Description                            | Report the value of the RSTb error counter                                   |
|              | <b>000</b><br><b>001</b><br>...<br>110 | Error counter is set to 1 by default   |
|              | Reset condition                        |  |
|              | Power On Reset                         |  |
| IO_45_fail   | Description                            | Report an error in the IO_45 protocol  |
|              | <b>0</b>                               | <b>No error</b>  |
|              | 1                                      | Error detected   |
|              | Reset condition                        | Power On Reset / Read  |
| IO_23_fail   | Description                            | Report an error in the FCCU protocol   |
|              | <b>0</b>                               | <b>No error</b>  |
|              | 1                                      | Error detected   |
|              | Reset condition                        | Power On Reset / Read  |
| IO_1_fail    | Description                            | Report an error in the IO_1 monitoring (external resistor string monitoring) |
|              | <b>0</b>                               | <b>No error</b>  |
|              | 1                                      | Error detected   |
|              | Reset condition                        | Power On Reset   |
| IO_01_fail   | Description                            | Report an error in the IO_01 protocol  |
|              | <b>0</b>                               | <b>No error</b>  |
|              | 1                                      | Error detected   |
|              | Reset condition                        | Power On Reset / Read  |



## 8 List of interruptions and description

The INTB output pin generates a low pulse when an Interrupt condition occurs. The INTB behavior as well as the pulse duration are set through the SPI during INIT phase. It is possible to mask some Interruption source (see [Detail of register mapping](#)).

**Table 90. Interruptions list**

| Event  | Description  |
|--|--|
| V <sub>SNS_UV</sub>                                  | Detection of V <sub>BATTERY</sub> below 8.5 V  |
| V <sub>SUP_UV_7</sub>                                | Detection of V <sub>SUP</sub> below 7.0 V (after reverse current protection diode)   |
| I <sub>PFF</sub>                                     | Input power feed forward. Based on V <sub>SUP</sub> and I <sub>PRE_PEAK</sub>  |
| I <sub>LIM_PRE</sub>                                 | Pre-regulator Current Limitation   |
| T <sub>WARN_PRE</sub>                                | Temperature warning on the pass transistor   |
| BoB  | Return the running state of V <sub>PRE</sub> converter (Buck or Boost mode)  |
| V <sub>PRE_STATE</sub> (V <sub>PRE_SMPS_EN</sub> )   | Return the activation state of V <sub>PRE</sub> DC/DC converter  |
| V <sub>PRE_OV</sub>                                  | Report a V <sub>PRE</sub> overvoltage detection  |
| V <sub>PRE_UV</sub>                                  | Report a V <sub>PRE</sub> undervoltage detection   |
| I <sub>LIM_CORE</sub>                                | V <sub>CORE</sub> Current limitation   |
| T <sub>WARN_CORE</sub>                               | Temperature warning on the pass transistor   |
| V <sub>CORE_STATE</sub> (V <sub>CORE_SMPS_EN</sub> ) | Return the activation state of V <sub>CORE</sub> DC/DC converter   |
| V <sub>CORE_OV</sub>                                 | Report a V <sub>CORE</sub> overvoltage detection   |
| V <sub>CORE_UV</sub>                                 | Report a V <sub>CORE</sub> undervoltage detection  |
| I <sub>LIM_CCA</sub>                                 | V <sub>CCA</sub> Current limitation  |
| T <sub>WARN_CCA</sub>                                | Temperature warning on the pass transistor (Internal Pass transistor only)   |
| TSD <sub>VCCA</sub>                                  | Temperature shutdown of the VCCA   |
| I <sub>LIM_CCA_OFF</sub>                             | Current limitation maximum duration expiration. Only used when external PNP connected.   |
| V <sub>CCA_OV</sub>                                  | Report a V <sub>CCA</sub> overvoltage detection  |
| V <sub>CCA_UV</sub>                                  | Report a V <sub>CCA</sub> undervoltage detection   |
| I <sub>LIM_AUX</sub>                                 | V <sub>AUX</sub> Current limitation  |
| I <sub>LIM_AUX_OFF</sub>                             | Current limitation maximum duration expiration. Only used when external PNP connected.   |
| V <sub>AUX_OV</sub>                                  | Report a V <sub>AUX</sub> overvoltage detection  |
| V <sub>AUX_UV</sub>                                  | Report a V <sub>AUX</sub> undervoltage detection   |
| TSD <sub>VAUX</sub>                                  | Temperature shutdown of the VAUX   |
| I <sub>LIM_CAN</sub>                                 | V <sub>CAN</sub> Current limitation  |
| V <sub>CAN_OV</sub>                                  | Report a V <sub>CAN</sub> overvoltage detection  |
| V <sub>CAN_UV</sub>                                  | Report a V <sub>CAN</sub> undervoltage detection   |
| TSD <sub>CAN</sub>                                   | Temperature shutdown on the pass transistor. Auto restart when T <sub>J</sub> < (TSD <sub>CAN</sub> - TSD <sub>CAN_HYST</sub> ). |
| IO_0   | Report IO_0 digital state change   |
| IO_1   | Report IO_1 digital state change   |
| IO_2   | Report IO_2 digital state change   |
| IO_3   | Report IO_3 digital state change   |
| IO_4   | Report IO_4 digital state change   |
| IO_5   | Report IO_5 digital state change   |
| IO_0_WU  | Report IO_0 WU event   |
| IO_1_WU  | Report IO_1 WU event   |
| IO_2_WU  | Report IO_2 WU event   |

**Table 90. Interruptions list (continued)**

|                |   |
|----------------|---|
| IO_3_WU        | Report IO_3 WU event  |
| IO_4_WU        | Report IO_4 WU event  |
| IO_5_WU        | Report IO_5 WU event  |
| CAN_WU         | Report a CAN wake-up event  |
| CAN_OT         | CAN overtemperature detection   |
| RXD_recessive  | CAN RXD recessive clamping detection (short-circuit to 5.0 V)                                       |
| TXD_dominant   | CAN TXD dominant clamping detection (short circuit to GND)  |
| CAN_dominant   | CAN bus dominant clamping detection   |
| LIN_WU         | Report a LIN wake-up event  |
| LIN_OT         | LN over-temperature detection   |
| RXDL_recessive | LIN RXDL recessive clamping detection (short to high)   |
| TXDL_dominant  | LIN TXDL dominant clamping detection (short to GND)   |
| LIN_dominant   | LIN bus dominant clamping detection   |
| INT_Request    | MCU request for an Interrupt pulse  |
| SPI_err        | Secured SPI communication check   |
| SPI_CLK        | Report a wrong number of CLK pulse different than 16 during the NCS low pulse in Main state machine |
| SPI_Req        | Invalid SPI access (Wrong write or read, write to INIT registers in normal mode, wrong address)     |
| SPI_Parity     | Report a Parity error in Main state machine   |

## 9 Typical applications

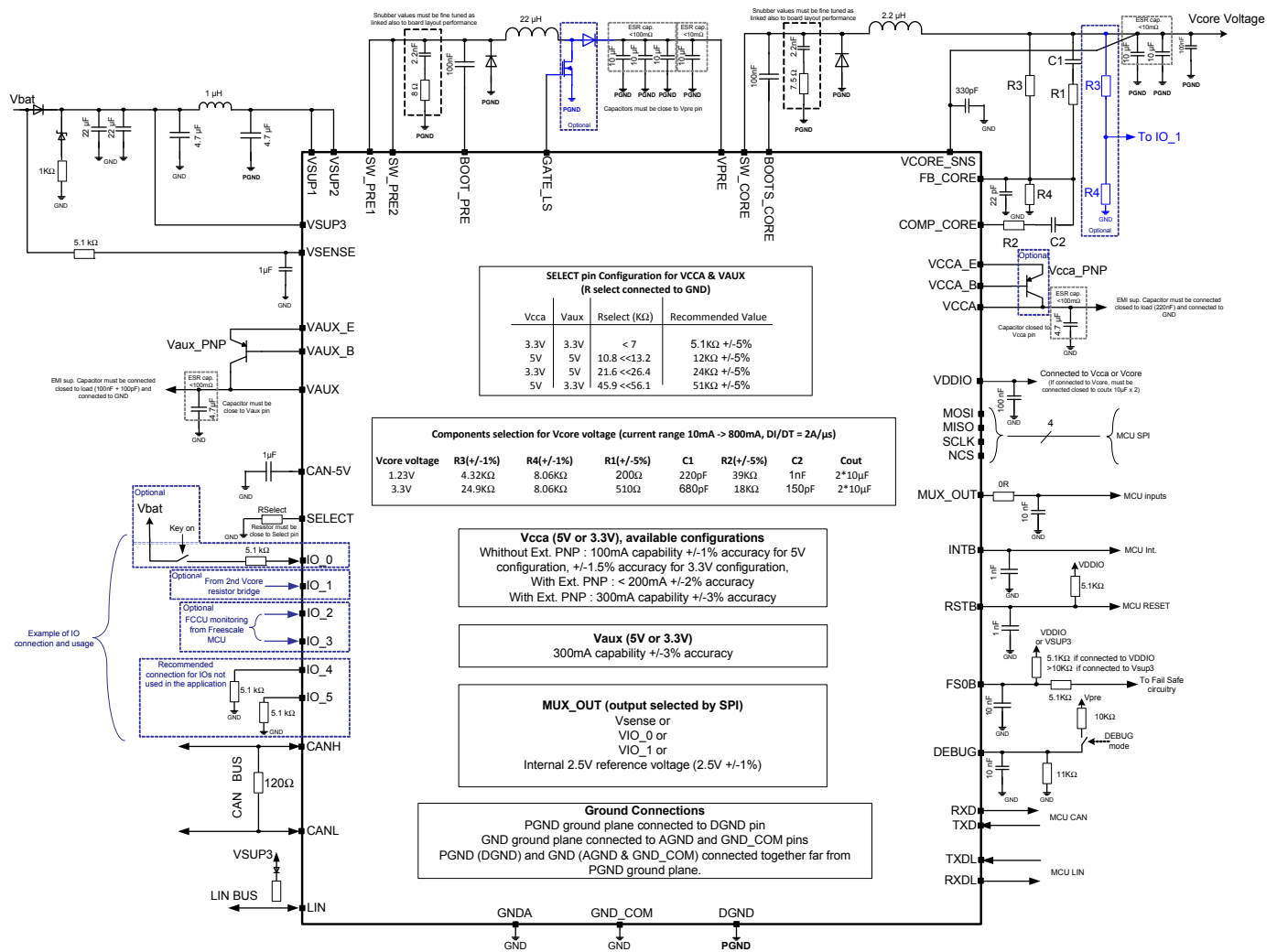


Figure 58. 33907/33908 simplified application schematic with non-inverting buck-boost configuration

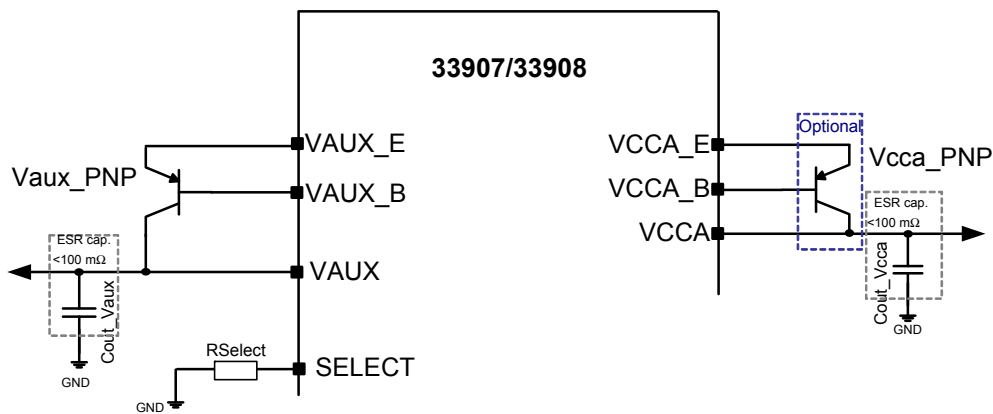


Figure 59. Vaux/VCCA connection

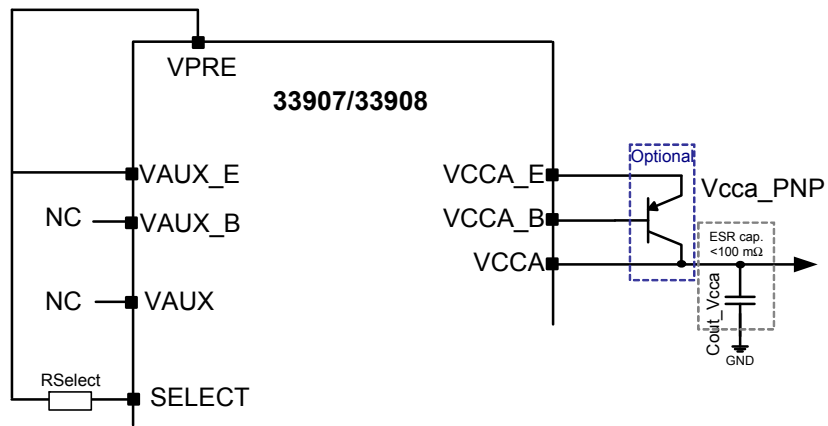


Figure 60. VCCA connection,  $V_{AUX}$  not used

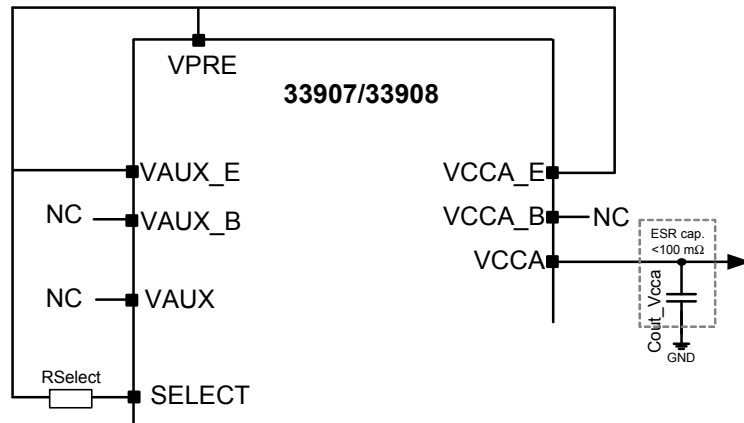


Figure 61.  $V_{AUX}$  not used,  $V_{CCA}$  configuration up to 100 mA

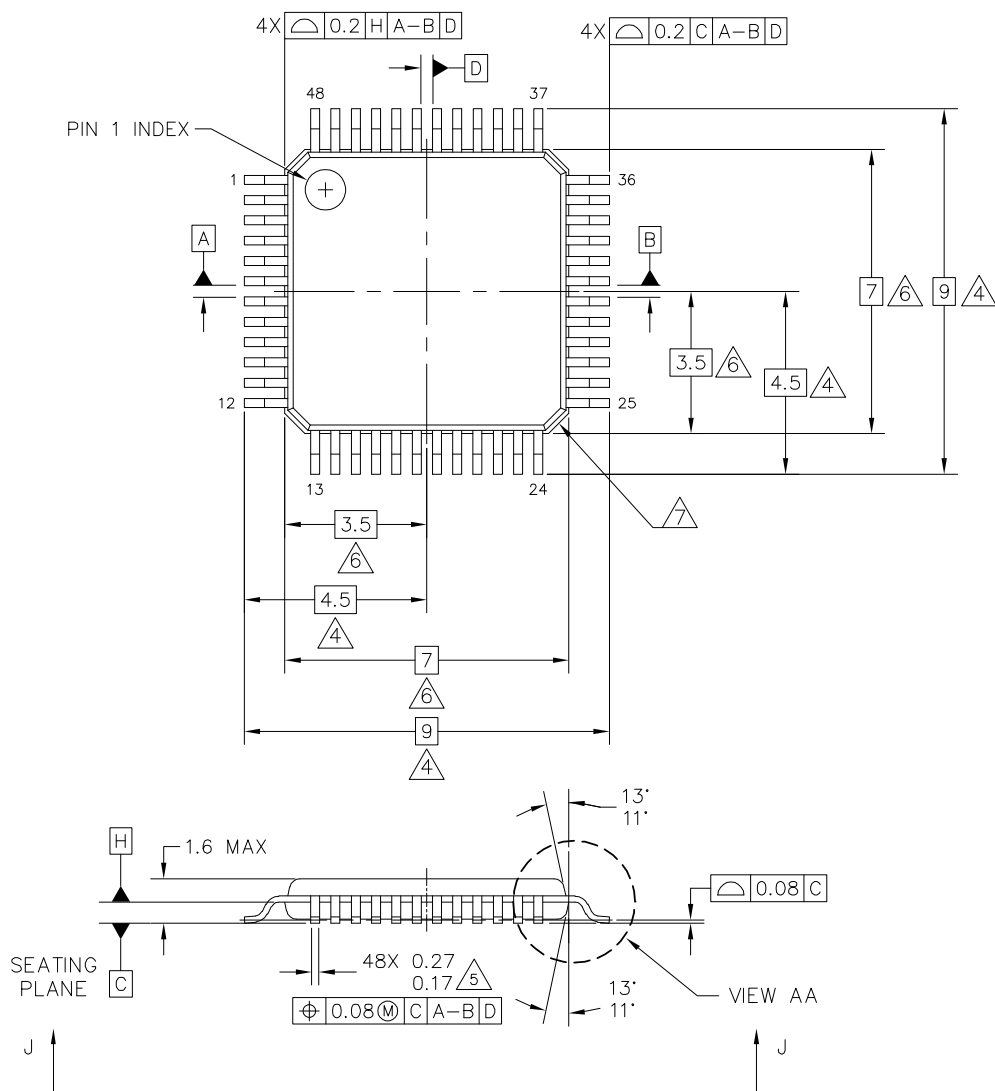
# 10 Packaging

## 10.1 Package mechanical dimensions

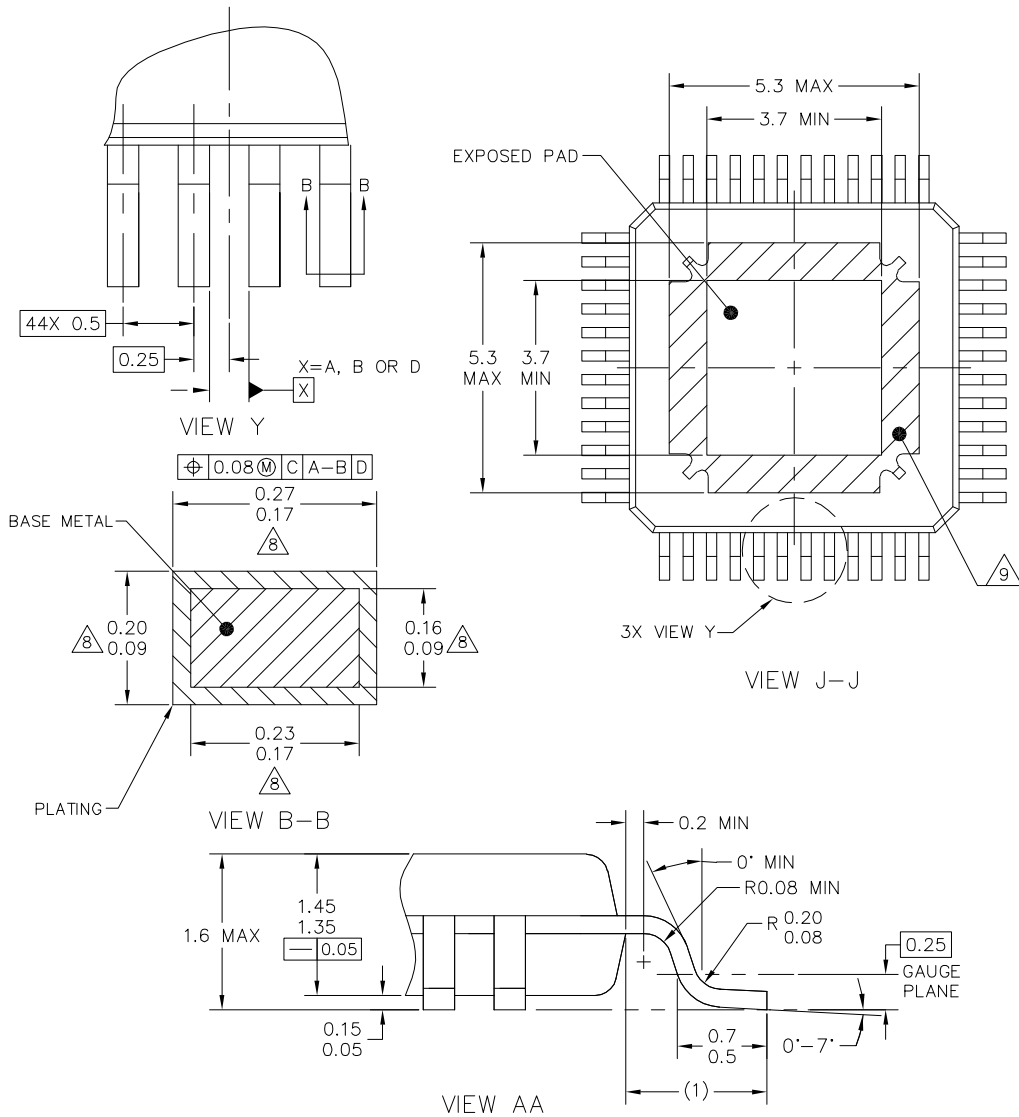
Package dimensions are provided in package drawings. To find the most current package outline drawing, go to [www.nxp.com](http://www.nxp.com) and perform a keyword search for the drawing's document number.

**Table 91. Package mechanical dimensions**

| Package  | Suffix | Package outline drawing number |
|--|--------|--------------------------------|
| 7.0 x 7.0, 48-Pin LQFP Exposed Pad, with 0.5 mm pitch, and a 4.5 x 4.5 exposed pad | AE     | 98ASA00173D                    |



|  |                            |                            |
|--|----------------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                | <b>MECHANICAL OUTLINE</b>  | PRINT VERSION NOT TO SCALE |
| TITLE:<br>48 LEAD LQFP, 7X7X1.4 PKG,<br>0.5 PITCH, 4.5X4.5 EXPOSED PAD | DOCUMENT NO: 98ASA00173D   | REV: A                     |
|  | CASE NUMBER: 2003-02       | 30 JUN 2011                |
|  | STANDARD: JEDEC MS-026 BBC |                            |



|  |  |                            |  |                            |  |
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| TITLE:<br>48 LEAD LQFP, 7X7X1.4 PKG,<br>0.5 PITCH, 4.5X4.5 EXPOSED PAD |  | DOCUMENT NO: 98ASA00173D   |  | REV: A                     |  |
|  |  | CASE NUMBER: 2003-02       |  | 30 JUN 2011                |  |
|  |  | STANDARD: JEDEC MS-026 BBC |  |                            |  |



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1MM AND 0.25MM FROM THE LEAD TIP.
9. HATCHED AREA TO BE KEEP OUT ZONE FOR PCB ROUTING.

|  |                            |  |                            |  |
|--|----------------------------|--|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC.<br>ALL RIGHTS RESERVED.                | MECHANICAL OUTLINE         |  | PRINT VERSION NOT TO SCALE |  |
| TITLE:<br>48 LEAD LQFP, 7X7X1.4 PKG,<br>0.5 PITCH, 4.5X4.5 EXPOSED PAD | DOCUMENT NO: 98ASA00173D   |  | REV: A                     |  |
|  | CASE NUMBER: 2003-02       |  | 30 JUN 2011                |  |
|  | STANDARD: JEDEC MS-026 BBC |  |                            |  |



# 11 References

The following are URLs where you can obtain information on related NXP products and application solutions

| NXP.com support pages               | Description  | URL   |
|-------------------------------------|--|---|
| AN4766                              | MC33907_08 System Basis Chip: Recommendations for PCB layout and external components | <a href="https://www.nxp.com/webapp/Download?colCode=AN4766">https://www.nxp.com/webapp/Download?colCode=AN4766</a>   |
| AN4661                              | Designing the VCORE Compensation Network For The MC33907/MC33908 System Basis Chips  | <a href="http://www.nxp.com/files/analog/doc/app_note/AN4661.pdf">http://www.nxp.com/files/analog/doc/app_note/AN4661.pdf</a>   |
| AN4442                              | Integrating the MPC5643L and MC33907/08 for Safety Applications                      | <a href="http://www.nxp.com/files/analog/doc/app_note/AN4442.pdf">http://www.nxp.com/files/analog/doc/app_note/AN4442.pdf</a>   |
| AN4388                              | Quad Flat Package (QFP)  | <a href="http://www.nxp.com/files/analog/doc/app_note/AN4388.pdf">http://www.nxp.com/files/analog/doc/app_note/AN4388.pdf</a>   |
| Power Dissipation Tool (Excel file) |  | <a href="http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MC33908&amp;fp=1&amp;tab=Design_Tools_Tab">http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MC33908&amp;fp=1&amp;tab=Design_Tools_Tab</a> |
| MC33907_8SMUG                       | MC33907_8 Safety Manual - User Guide   | <a href="https://www.nxp.com/webapp/Download?colCode=MC33907_8SMUG">https://www.nxp.com/webapp/Download?colCode=MC33907_8SMUG</a>   |
| FMEDA                               | MC33907_8 FMEDA  | Upon demand   |
| KIT33907LAEEVB                      | Evaluation Board   | <a href="http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KIT33907LAEEVB">http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KIT33907LAEEVB</a>   |
| KIT33908LAEEVB                      | Evaluation Board   | <a href="http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KIT33908LAEEVB">http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KIT33908LAEEVB</a>   |
| KITMPC5643DBEVM                     | Evaluation Daughter Board (Qorivva MPC5643L)   | <a href="http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KITMPC5643DBEVM">http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=KITMPC5643DBEVM</a>   |
| MC33907 Product Summary Page        |  | <a href="http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MC33907">http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MC33907</a>   |
| MC33908 Product Summary Page        |  | <a href="http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MC33908">http://www.nxp.com/webapp/sps/site/prod_summary.jsp?code=MC33908</a>   |
| Analog Home Page                    |  | <a href="http://www.nxp.com/analog">http://www.nxp.com/analog</a>   |

## 12 Revision history

| Revision | Date    | Description of changes   |
|----------|---------|--|
| 1.0      | 11/2014 | • Product Preview release  |
|          | 12/2014 | • Initial release. No change to content.   |
| 2.0      | 1/2015  | <ul style="list-style-type: none"> <li>• Corrected WD_LFSR register access in read mode</li> <li>• Added (35)</li> <li>• Added clarifications after Table 77</li> <li>• Correct minor typographic errors</li> <li>• Changed document status to Advance Information</li> <li>• Changed the document order number to MC33907-MC33908D2</li> </ul>  |
| 3.0      | 1/2015  | <ul style="list-style-type: none"> <li>• Corrected Revision History</li> <li>• Corrected typo for ICORE_LIM</li> </ul>   |
| 4.0      | 2/2015  | <ul style="list-style-type: none"> <li>• Updated <math>V_{SUP\_UV\_7}</math> max. value from 8.2 to 8.0 V in Table 4</li> <li>• Updated Thermal Resistance values in Table 3</li> <li>• Changed Thermal Resistance Junction to Case Top value from 14.4 to 24.2 in Table 3 on page 10</li> <li>• Corrected a typo on page 46 (changed "For <math>V_{SUP}</math> and <math>V_{AUX}</math> 5.0 V" to "For <math>V_{CCA}</math> and <math>V_{AUX}</math> 5.0 V")</li> <li>• Corrected typo for <math>V_{BUS\_CNT}</math> in Table 4 on page 20</li> <li>• Corrected typo for D2 and D3 in Table 5 on page 25</li> </ul> |
|          | 8/2016  | • Updated to NXP document form and style   |
| 5.0      | 10/2016 | • Corrected format (default values in bold) of the default SPI register values to match Data sheet Rev. 4.0, 2/2015  |



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Document Number: MC33907-MC33908D2

Rev. 5.0

10/2016

