

74F379

Quad Parallel Register with Enable

General Description

The 74F379 is a 4-bit register with buffered common Enable. This device is similar to the 74F175 but features the common Enable rather than common Master Reset.

Features

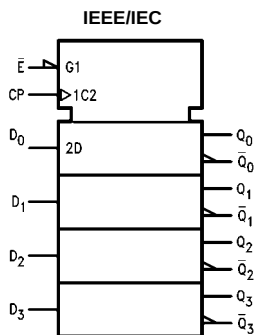
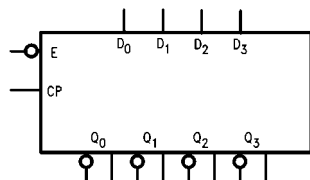
- Edge triggered D-type inputs
- Buffered positive edge-triggered clock
- Buffered common enable input
- True and complement outputs

Ordering Code:

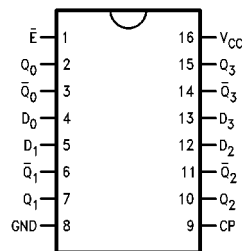
Order Number	Package Number	Package Description
74F379SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F379SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F379PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



74F379 Quad Parallel Register with Enable

Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{E}$	Enable Input (Active LOW)	1.0/1.0	20 μA /–0.6 mA
D_0 – D_3	Data Inputs	1.0/1.0	20 μA /–0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA /–0.6 mA
Q_0 – Q_3	Flip-Flop Outputs	50/33.3	–1 mA/20 mA
$\overline{Q_0}$ – $\overline{Q_3}$	Complement Outputs	50/33.3	–1 mA/20 mA

Functional Description

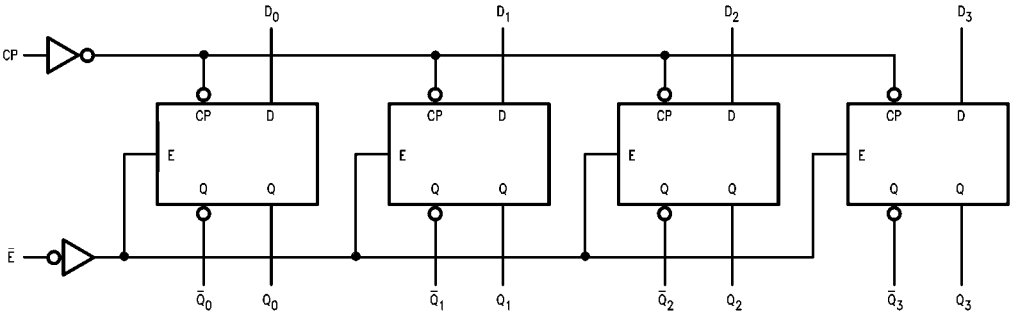
The 74F379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable (E) inputs are common to all flip-flops. When the $\overline{E}$ is input HIGH, the register will retain the present data independent of the CP input. The D_n and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

Truth Table

Inputs			Outputs	
$\overline{E}$	CP	D_n	Q_n	$\overline{Q_n}$
H	$\nearrow$	X	NC	NC
L	$\nearrow$	H	H	L
L	$\nearrow$	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
 $\nearrow$ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	–65°C to +150°C
Ambient Temperature under Bias	–55°C to +125°C
Junction Temperature under Bias	–55°C to +150°C
V _{CC} Pin Potential to Ground Pin	–0.5V to +7.0V
Input Voltage (Note 2)	–0.5V to +7.0V
Input Current (Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	–0.5V to V _{CC}
3-STATE Output	–0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			–1.2	V	Min	I _{IN} = –18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	2.5 2.7		V	Min	I _{OH} = –1 mA I _{OH} = –1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			–0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	–60		–150	mA	Max	V _{OUT} = 0V
I _{CCL}	Power Supply Current		28	40	mA	Max	V _O = LOW

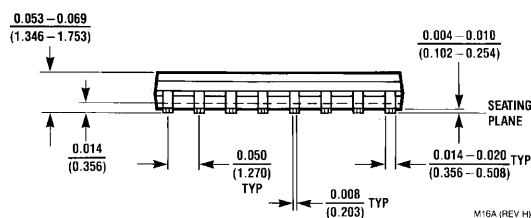
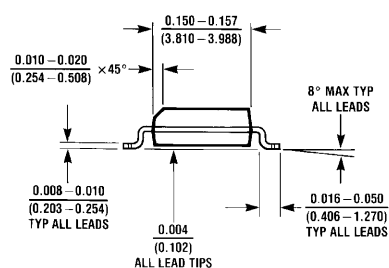
AC Electrical Characteristics

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = -55°C to +125°C V _{CC} = +5.0V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	100	140		75		100		MHz
t _{PLH}	Propagation Delay	3.5	5.0	6.5	3.0	8.5	3.5	7.5	ns
t _{PHL}	CP to Q _n , $\overline{Q}_n$	5.0	6.5	8.5	4.0	10.0	5.0	9.5	

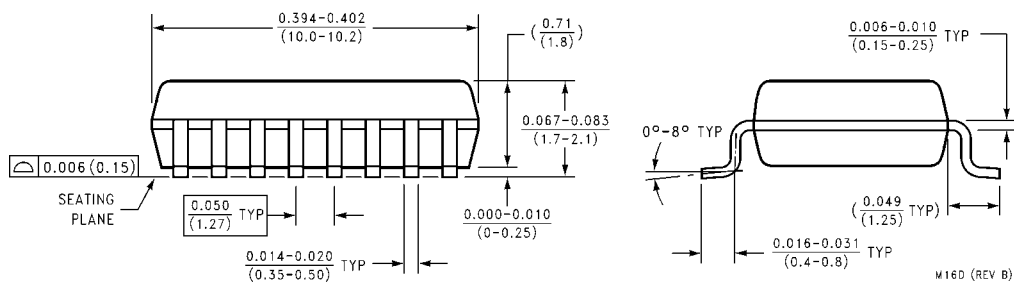
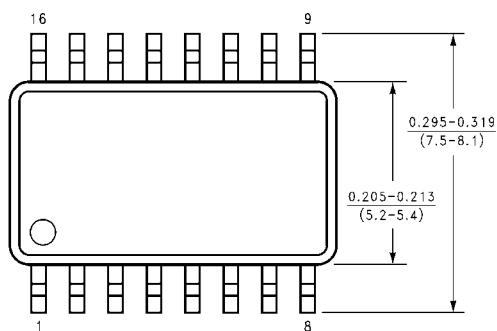
AC Operating Requirements

Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = -55°C to +125°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = +5.0V		Units
		Min	Max	Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	3.0		4.0		3.0		ns
t _S (L)	D _n to CP	3.0		4.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	1.0		2.0		1.0		
t _H (L)	D _n to CP	1.0		2.0		1.0		ns
t _S (H)	Setup Time, HIGH or LOW	6.0		8.0		6.0		
t _S (L)	$\overline{E}$ to CP	6.0		8.0		6.0		
t _H (H)	Hold Time, HIGH or LOW	0		0		0		ns
t _H (L)	$\overline{E}$ to CP	0		0		0		
t _W (H)	CP Pulse Width	4.0		5.0		4.0		ns
t _W (L)	HIGH or LOW	5.0		7.0		5.0		

Physical Dimensions inches (millimeters) unless otherwise noted

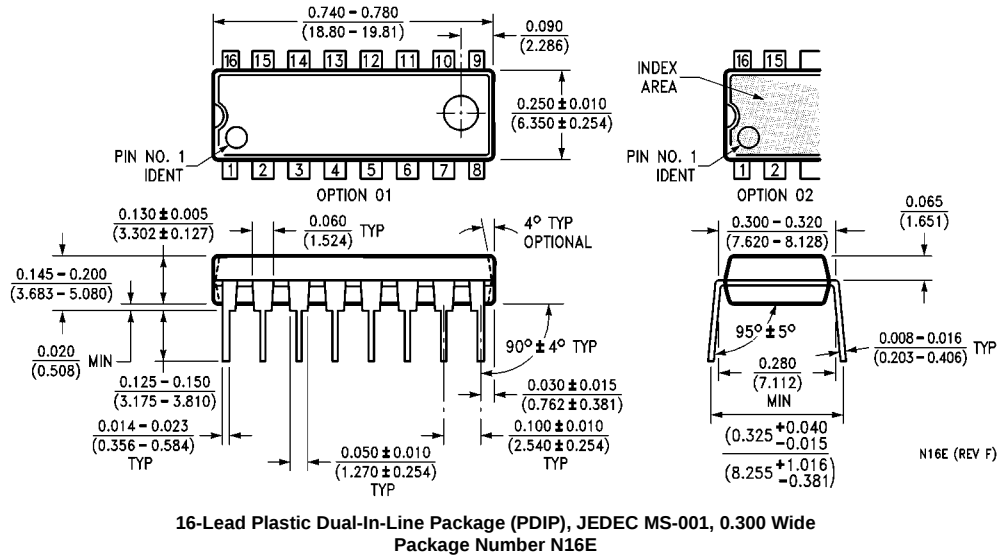


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A**



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com