

SN54HC195, SN74HC195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

D2684, DECEMBER 1982—REVISED JUNE 1989

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- J and $\bar{K}$ Inputs to First Stage
- Complementary Outputs from Last Stage
- Package Options: Plastic and Ceramic DIPs and Ceramic Chip Carriers
- Dependable Texas Instruments Quality and Reliability

description

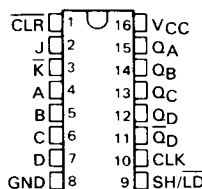
These 4-bit registers feature parallel inputs, parallel outputs, J- $\bar{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load, and shift (in the direction Q_A and Q_D).

Parallel loading is accomplished by applying the 4-bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

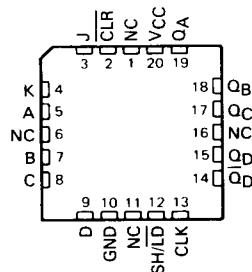
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J- $\bar{K}$ inputs. These inputs permit the first stage to perform as a J- $\bar{K}$ -, D-, or T-type flip-flop as shown in the function table.

The SN54HC195 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC195 is characterized for operation from -40°C to 85°C .

SN54HC195 . . . J PACKAGE
SN74HC195 . . . N PACKAGE
(TOP VIEW)

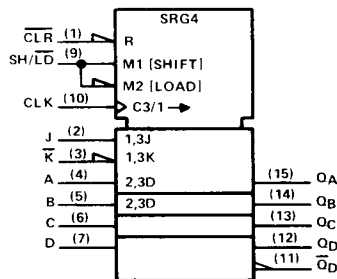


SN54HC195 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

2

HC MOS Devices

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

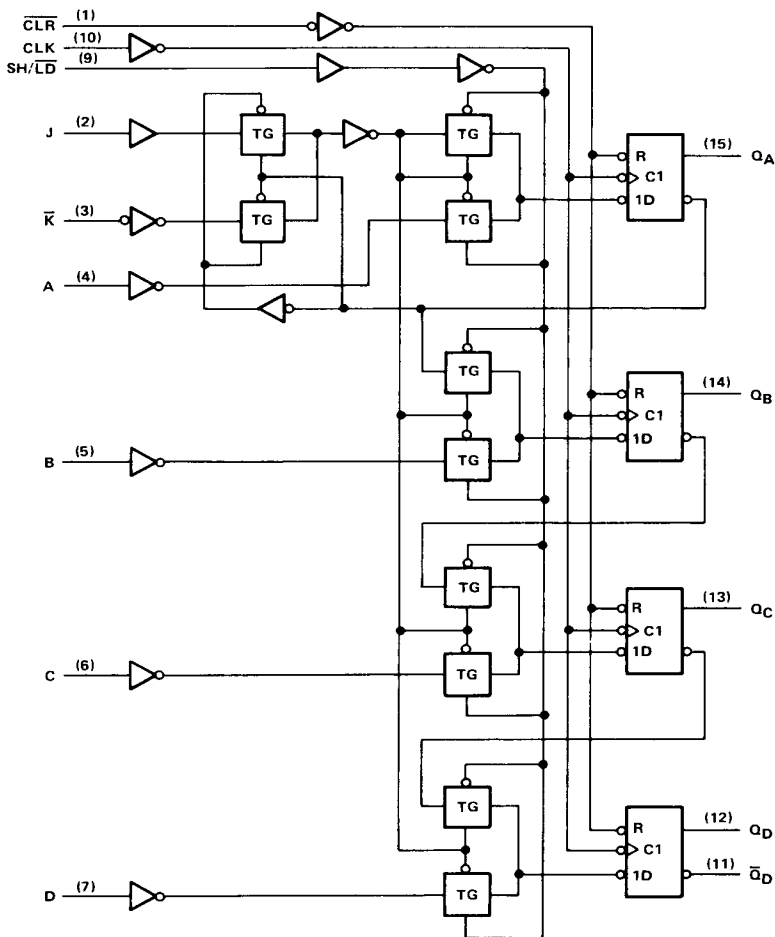
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

Copyright © 1989, Texas Instruments Incorporated

2-285

SN54HC195, SN74HC195 **4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

logic diagram (positive logic)



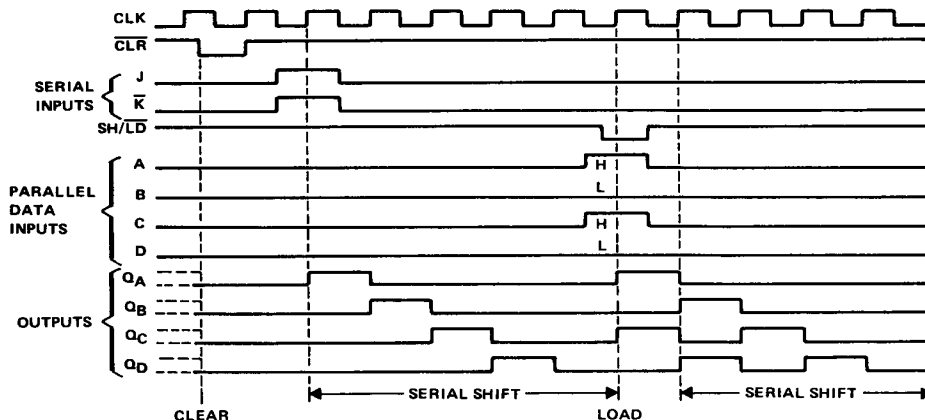
Pin numbers shown are for J and N packages.

SN54HC195, SN74HC195 **4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

FUNCTION TABLE

INPUTS									OUTPUTS					
CLR	SH/LD	CLK	SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D	Q̄ _D	
			J	K	A	B	C	D						
L	X	X	X	X	X	X	X	X	L	L	L	L	H	
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$	
H	H	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	$\overline{Q_{D0}}$	
H	H	↑	L	H	X	X	X	X	Q _{A0}	Q _{A0}	Q _{Bn}	Q _{Cn}	$\overline{Q_{Cn}}$	
H	H	↑	L	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	$\overline{Q_{Cn}}$	
H	H	↑	H	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	$\overline{Q_{Cn}}$	
H	H	↑	H	L	X	X	X	X	Q _{An}	Q _{An}	Q _{Bn}	Q _{Cn}	$\overline{Q_{Cn}}$	

typical clear, shift, and load sequences



2
 HCMOS Devices

SN54HC195, SN74HC195 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300 °C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package	260 °C
Storage temperature range	−65 °C to 150 °C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HC195			SN74HC195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC} Supply voltage		2	5	6	2	5	6	V
V_{IH} High-level input voltage	$V_{CC} = 2$ V	1.5			1.5			V
	$V_{CC} = 4.5$ V	3.15			3.15			
	$V_{CC} = 6$ V	4.2			4.2			
V_{IL} Low-level input voltage	$V_{CC} = 2$ V	0		0.3	0		0.3	V
	$V_{CC} = 4.5$ V	0		0.9	0		0.9	
	$V_{CC} = 6$ V	0		1.2	0		1.2	
V_I Input voltage		0		V_{CC}	0		V_{CC}	V
V_O Output voltage		0		V_{CC}	0		V_{CC}	V
t_t Input transition (rise and fall) times	$V_{CC} = 2$ V	0		1000	0		1000	ns
	$V_{CC} = 4.5$ V	0		500	0		500	
	$V_{CC} = 6$ V	0		400	0		400	
T_A Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25$ °C			SN54HC195		SN74HC195		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20$ μ A	2 V	1.9	1.998		1.9		1.9		V
		4.5 V	4.4	4.499		4.4		4.4		
		6 V	5.9	5.999		5.9		5.9		
	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -4$ mA	4.5 V	3.98	4.30		3.7		3.84		
		6 V	5.48	5.80		5.2		5.34		
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20$ μ A	2 V		0.002	0.1		0.1		0.1	V
		4.5 V		0.001	0.1		0.1		0.1	
		6 V		0.001	0.1		0.1		0.1	
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 4$ mA	4.5 V		0.17	0.26		0.4		0.33	
		6 V		0.15	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	6 V		±0.1	±100		±1000		±1000	nA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	6 V			8		160		80	μ A
C_i		2 to 6 V		3	10		10		10	pF

SN4HC195, SN74HC195 **4-BIT PARALLEL-ACCESS SHIFT REGISTERS**

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			$T_A = 25^\circ\text{C}$			SN54HC195		SN74HC195		UNIT
			V _{CC}	MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	0	6	0	4.2	0	5	MHz
			4.5 V	0	31	0	21	0	25	
			6 V	0	36	0	25	0	29	
t_w	Pulse duration	CLK high or low	2 V	80		120		100		ns
			4.5 V	16		24		20		
			6 V	14		20		17		
	$\overline{\text{CLR}}$ low		2 V	80		120		100		
			4.5 V	16		24		20		
			6 V	14		20		17		
t_{su}	Setup time, before CLK $\uparrow$	SH/ $\overline{\text{LD}}$, or serial and parallel data, or $\overline{\text{CLR}}$ inactive	2 V	100		150		125		ns
			4.5 V	20		30		25		
			6 V	17		26		21		
t_h	Hold time, after CLK $\downarrow$	SH/ $\overline{\text{LD}}$ or serial and parallel data	2 V	0		0		0		ns
			4.5 V	0		0		0		
			6 V	0		0		0		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 50$ pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	$T_A = 25^\circ\text{C}$			SN54HC195		SN74HC195		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			2 V	6	12		4.2		5		MHz
			4.5 V	31	50		21		25		
			6 V	36	60		25		29		
t_{pd}	CLK	Q_A thru Q_D or $\overline{Q_D}$	2 V		67	145		220		180	ns
			4.5 V		17	29		44		36	
			6 V		14	25		37		31	
t_{pd}	$\overline{\text{CLR}}$	Q_A thru Q_D or $\overline{Q_D}$	2 V		67	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		13	26		38		32	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

C_{pd}	Power dissipation capacitance	No load, $T_A = 25^\circ\text{C}$	65 pF typ
-----------------	-------------------------------	-----------------------------------	-----------

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2

HCMS Devices