Features

- **Single Voltage Operation**
  - **5V Read**
  - **5V Reprogramming**
- **Fast Read Access Time - 90 ns**
- **Internal Erase/Program Control**
- **Sector Architecture**
  - **One 8K Words (16K Bytes) Boot Block with Programming Lockout**
  - **Two 8K Words (16K Bytes) Parameter Blocks**
  - **One 488K Words (976K bytes) Main Memory Array Block**
- **Fast Sector Erase Time - 10 seconds**
- **Word-By-Word Programming - 50 µs/Word**
- **Hardware Data Protection**
- **$\overline{\text{DATA}}$ Polling For End Of Program Detection**
- **Low Power Dissipation**
  - **50 mA Active Current**
  - **300 µA CMOS Standby Current**
- **Typical 10,000 Write Cycles**

Description

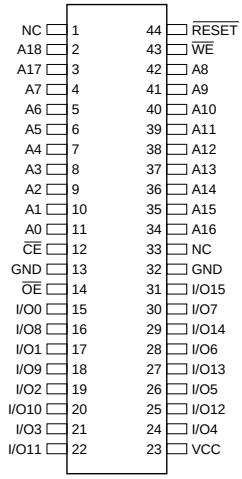
The AT49F8192(T) is a 5-volt-only, 8 megabit Flash Memory organized as 512K words of 16 bits each. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 90 ns with power dissipation of just 275 mW. When deselected, the CMOS standby current is less than 300 µA.

(continued)

Pin Configurations

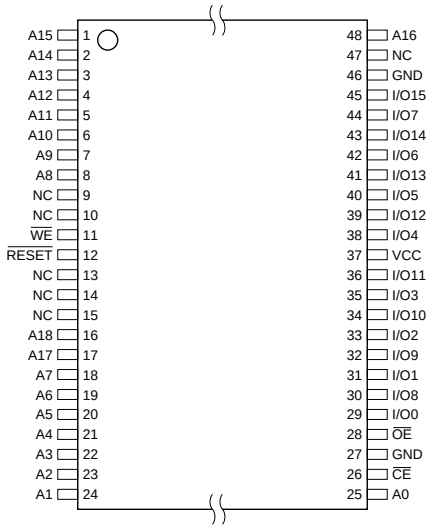
Pin Name	Function
A0 - A18	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
$\overline{\text{RESET}}$	Reset
I/O0 - I/O15	Data Inputs/Outputs
NC	No Connect

SOIC (SOP)



TSOP Top View

Type 1



8-Megabit (512K x 16) 5-volt Only Flash Memory

AT49F8192
AT49F8192T

Recommend using AT49F8192A(T) for new designs.

Rev. 0588F–12/98

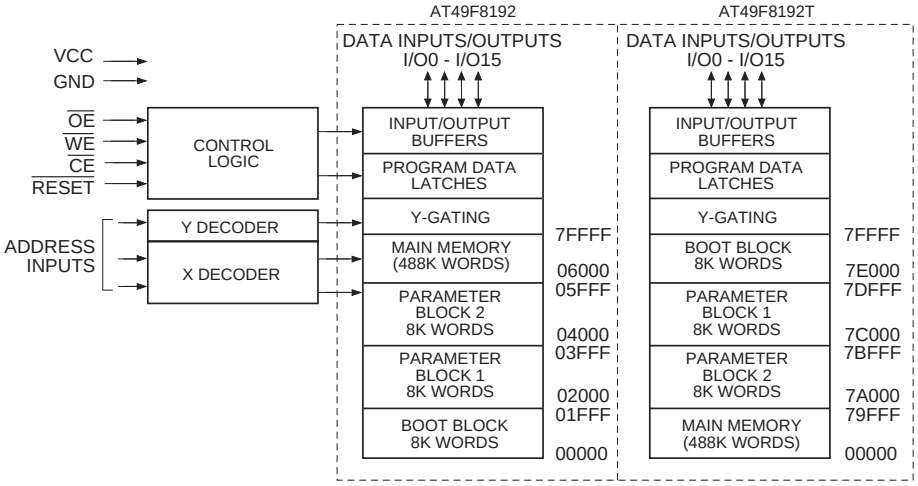
The device contains a user-enabled “boot block” protection feature. Two versions of the feature are available: the AT49F8192 locates the boot block at lowest order addresses (“bottom boot”); the AT49F8192T locates it at highest order addresses (“top boot”).

To allow for simple in-system reprogrammability, the AT49F8192(T) does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ inputs to avoid bus contention. Reprogramming the AT49F8192(T) is performed by first erasing a block of data and then programming on a word-by-word basis.

The device is erased by executing the erase command sequence; the device internally controls the erase operation. The memory is divided into three blocks for erase operations. There are two 8K word parameter block sections and one sector consisting of the boot block and the main memory array block. The AT49F8192(T) is programmed on a word-by-word basis. The device has the capability to protect the data in the boot block; this feature is enabled by a command sequence. Once the boot block programming lockout feature is enabled, the data in the boot block cannot be changed when input levels of 5.5 volts or less are used. The typical number of program and erase cycles is in excess of 10,000 cycles.

The optional 8K word boot block section includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being reprogrammed.

Block Diagram



Device Operation

READ: The AT49F8192(T) is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention.

COMMAND SEQUENCES: When the device is first powered on it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the Command Definitions table (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

RESET: A $\overline{RESET}$ input pin is provided to ease some system applications. When $\overline{RESET}$ is at a logic high level, the device is in its standard operating mode. A low level on the $\overline{RESET}$ input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the $\overline{RESET}$ pin, the device returns to the Read or Standby mode, depending upon the state of the control inputs. By applying a 12V $\pm$ 0.5V input signal to the $\overline{RESET}$ pin the boot block array can be reprogrammed even if the boot block program lockout feature has been enabled (see Boot Block Programming Lockout Override section).

ERASURE: Before a word can be reprogrammed, it must be erased. The erased state of the memory bits is a logical "1". The entire device can be erased at one time by using a 6-byte software code.

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC}.

CHIP ERASE: If the boot block lockout has been enabled, the Chip Erase function is disabled; sector erases for the parameter blocks and main memory block will still operate. After the full chip erase the device will return back to read mode. Any command during chip erase will be ignored.

SECTOR ERASE: As an alternative to a full chip erase, the device is organized into three sectors that can be individually erased. There are two 8K word parameter block sections and one sector consisting of the boot block and the main memory array block. The Sector Erase command is a six bus cycle operation. The sector address is latched on the falling $\overline{WE}$ edge of the sixth cycle while the 30H data input command is latched at the rising edge of $\overline{WE}$. The sector erase starts after the rising edge of $\overline{WE}$ of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion. When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together (from the same sector erase command). Once the boot region has been protected, only the main memory array sector will erase when its sector erase command is issued. Whenever a parameter block is erased and reprogrammed, the other parameter block should be erased and reprogrammed before the first parameter block is erased again.

WORD PROGRAMMING: Once a memory block is erased, it is programmed (to a logical "0") on a word-by-word basis. Programming is accomplished via the internal device command register and is a 4 bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified tBP cycle time. The $\overline{DATA}$ polling feature may also be used to indicate the end of a program cycle.

BOOT BLOCK PROGRAMMING LOCKOUT: The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K words. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block's usage as a write protected region is optional to the user. The address range of the 49F8192 boot block is 00000H to 01FFFH while the address range of the 49F8192T is 7E000H to 7FFFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed when input levels of 5.5V or less are used. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the Command Definitions table.

BOOT BLOCK LOCKOUT DETECTION: A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out for the AT49F8192, and a read from address 7E002H will show if programming the boot block is locked out for the AT498192T. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been enabled and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

BOOT BLOCK PROGRAMMING LOCKOUT OVERRIDE: The user can override the boot block programming lockout by taking the $\overline{RESET}$ pin to 12 volts during the entire chip erase, sector erase or word programming operation. When the $\overline{RESET}$ pin is brought back to TTL levels the boot block programming lockout feature is again active.

PRODUCT IDENTIFICATION: The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see Operating Modes (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

DATA POLLING: The AT49F8192(T) features $\overline{DATA}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. During a chip or sector erase operation, an attempt to read the device will give a "0" on I/O7. Once the program or erase cycle has completed, true data will be read from the device. $\overline{DATA}$ polling may begin at any time during the program cycle.

TOGGLE BIT: In addition to $\overline{DATA}$ polling the AT49F8192(T) provides another method for determining

the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

HARDWARE DATA PROTECTION: Hardware features protect against inadvertent programs to the AT49F8192(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 3.8V (typical), the program function is inhibited. (b) V_{CC} power on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits program cycles. (d) Noise filter: pulses of less than 15 ns (typical) on the $\overline{WE}$ or $\overline{CE}$ inputs will not initiate a program cycle.

Command Definition (in Hex)[1]

Command Sequence	Bus Cycles	1st Bus Cycle		2nd Bus Cycle		3rd Bus Cycle		4th Bus Cycle		5th Bus Cycle		6th Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	Addr	D_{OUT}										
Chip Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	10
Sector Erase	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	SA[4][5]	30
Word Program	4	5555	AA	2AAA	55	5555	A0	Addr	D_{IN}				
Boot Block Lockout [2]	6	5555	AA	2AAA	55	5555	80	5555	AA	2AAA	55	5555	40
Product ID Entry	3	5555	AA	2AAA	55	5555	90						
Product ID Exit[3]	3	5555	AA	2AAA	55	5555	F0						
Product ID Exit[3]	1	xxxx	F0										

Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex)
2. The 8K word boot sector has the address range 00000H to 01FFFH for the AT49F8192 and 7E000H to 7FFFFH for the AT49F8192T.
3. Either one of the Product ID Exit commands can be used.
4. SA = sector addresses:
   For the AT49F8192
   SA = 03XXX for PARAMETER BLOCK 1
   SA = 05XXX for PARAMETER BLOCK 2
   SA = 7FXXX for MAIN MEMORY ARRAY
   For the AT49F8192T
   SA = 7DXXX for PARAMETER BLOCK 1
   SA = 7BXXX for PARAMETER BLOCK 2
   SA = 79XXX for MAIN MEMORY ARRAY
5. When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together (form the same sector erase command). Once the boot region has been protected, only the main memory array sector will erase when its sector erase command is issued.

Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} to +0.6V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyong those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT49F8192(T)-90	AT49F8192(T)-12
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C
V_{CC} Power Supply		5V ± 10%	5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RESET}$	Ai	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Ai	D_{OUT}
Program/Erase (2)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Ai	D_{IN}
Standby/Write Inhibit	V_{IH}	X (1)	X	V_{IH}	X	High Z
Program Inhibit	X	X	V_{IH}	V_{IH}		
Program Inhibit	X	V_{IL}	X	V_{IH}		
Output Disable	X	V_{IH}	X	V_{IH}		High Z
Reset	X	X	X	V_{IL}	X	High Z
Product Identification						
Hardware	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A1 - A18 = V_{IL}, A9 = V_H, (3), A0 = V_{IL}	Manufacturer Code (4)
					A1 - A18 = V_{IL}, A9 = V_H, (3), A0 = V_{IH}	Device Code (4)
Software (5)				V_{IH}	A0 = V_{IL}, A1 - A18 = V_{IL}	Manufacturer Code (4)
					A0 = V_{IH}, A1 - A18 = V_{IL}	Device Code (4)

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC Programming Characteristics.
3. V_H = 12.0V ± 0.5V.
4. Manufacturer Code: 1FH, Device Code: A0H (49F8192), A3H (49F8192T).
5. See details under Software Product Identification Entry/Exit.

DC Characteristics

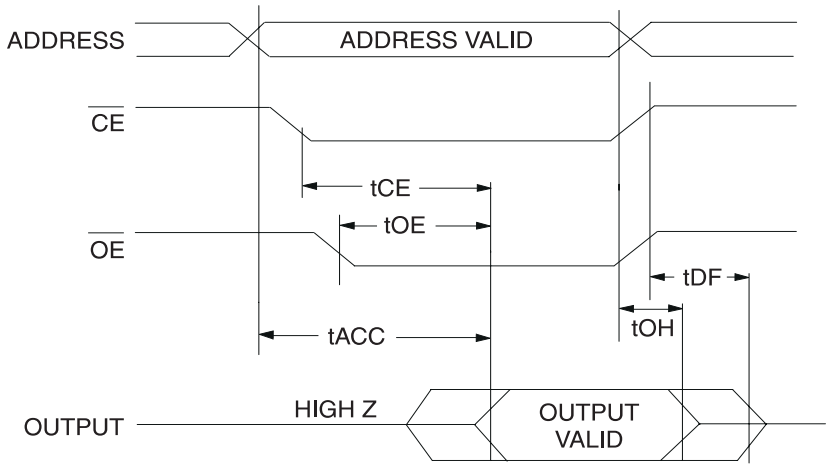
Symbol	Parameter	Condition	Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC}		10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}		10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}		300	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}		3	mA
I_{CC} (1)	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA		50	mA
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -400 µA	2.4		V
V_{OH2}	Output High Voltage CMOS	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2		V

Note: 1. In the erase mode, I_{CC} is 90 mA.

AC Read Characteristics

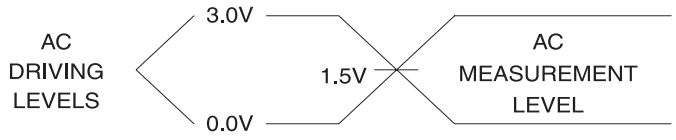
Symbol	Parameter	AT49F8192(T)-90		AT49F8192(T)-12		Units
		Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		90		120	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		90		120	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	0	40	0	50	ns
t_{DF} (3, 4)	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	25	0	30	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		ns

AC Read Waveforms (1)(2)(3)(4)



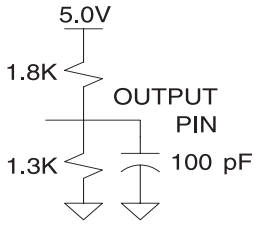
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact in t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 5 ns

Output Test Load



Pin Capacitance(1)

(f = 1 MHz, T = 25°C)

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

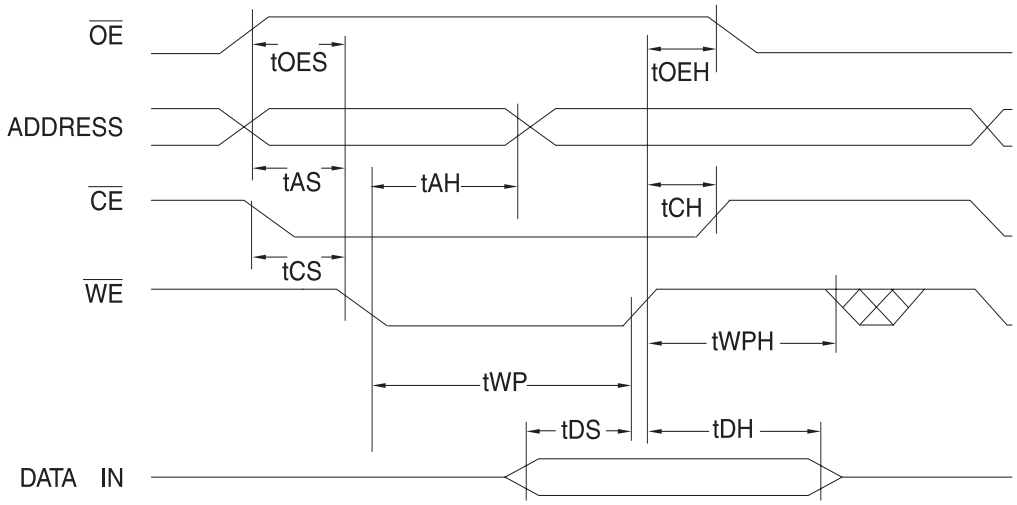
Note: 1. This parameter is characterized and is not 100% tested.

AC Word Load Characteristics

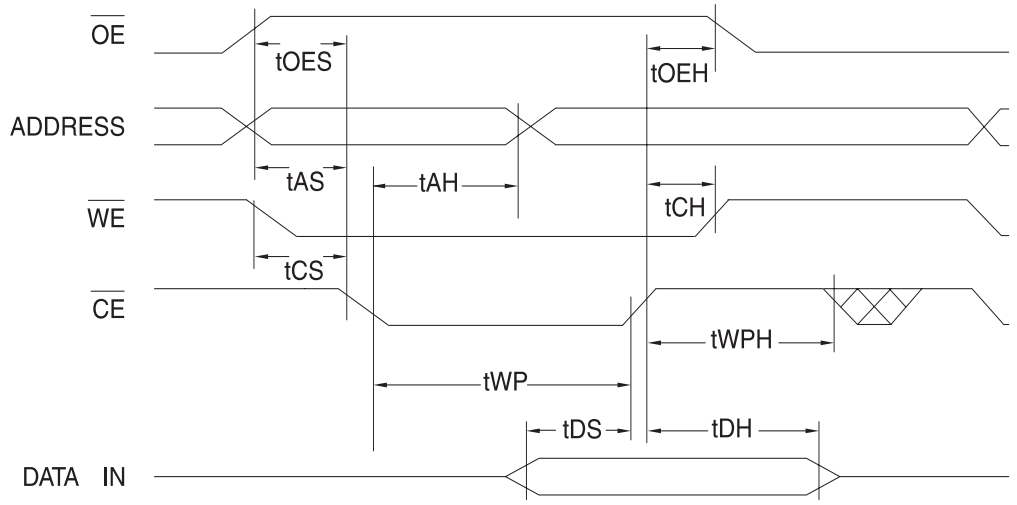
Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Set-up Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	90		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	10		ns
t_{WPH}	Write Pulse Width High	90		ns

AC Word Load Waveforms

$\overline{WE}$ Controlled



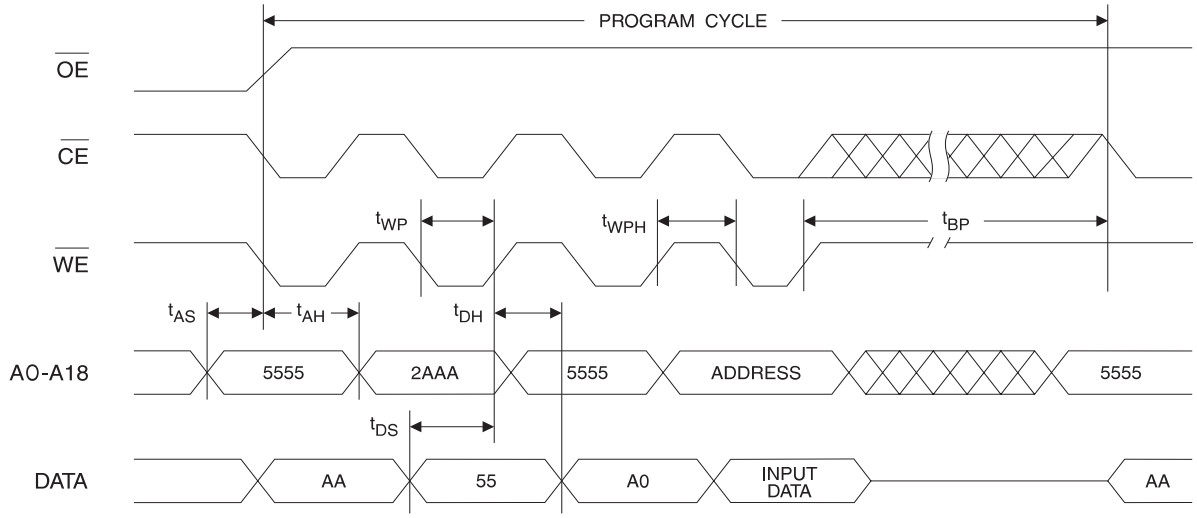
$\overline{CE}$ Controlled



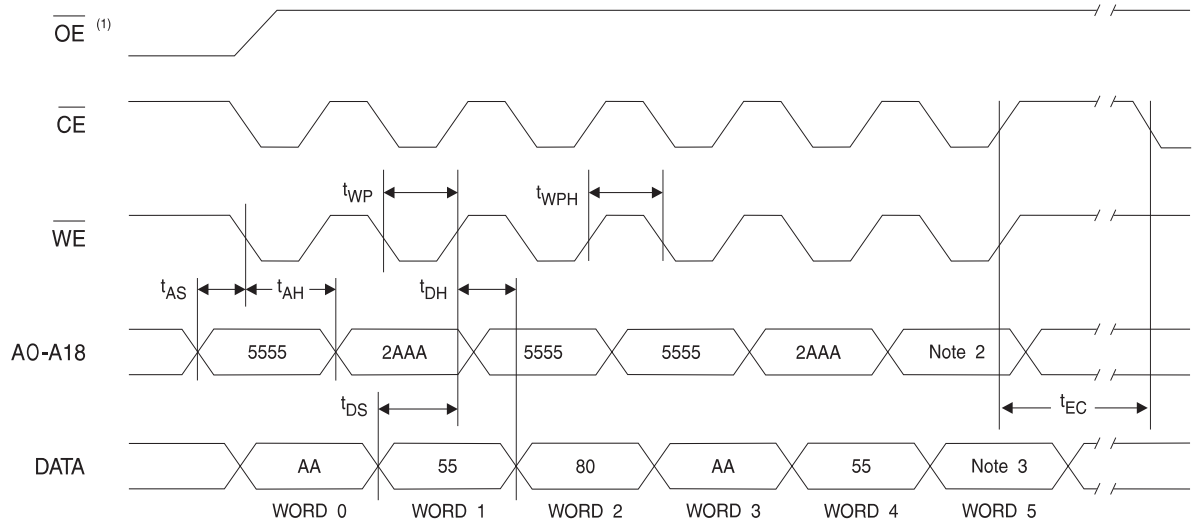
Program Cycle Characteristics

Symbol	Parameter	Min	Max	Units
t_{BP}	Word Programming Time		50	µs
t_{AS}	Address Set-up Time	10		ns
t_{AH}	Address Hold Time	50		ns
t_{DS}	Data Set-up Time	50		ns
t_{DH}	Data Hold Time	10		ns
t_{WP}	Write Pulse Width	90		ns
t_{WPH}	Write Pulse Width High	90		ns
t_{EC}	Erase Cycle Time		10	seconds

Program Cycle Waveforms



Sector or Chip Erase Cycle Waveforms



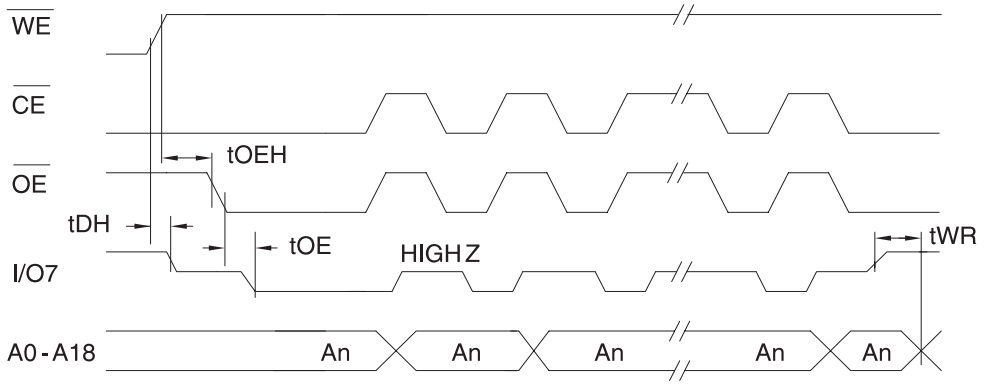
Notes:
1. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.
2. For chip erase, the address should be 5555. For sector erase, the address depends on what sector is to be erased. (See note 4 under command definitions.)
3. For chip erase, the data should be 10_H, and for sector erase, the data should be 30_H.

$\overline{\text{Data}}$ Polling Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

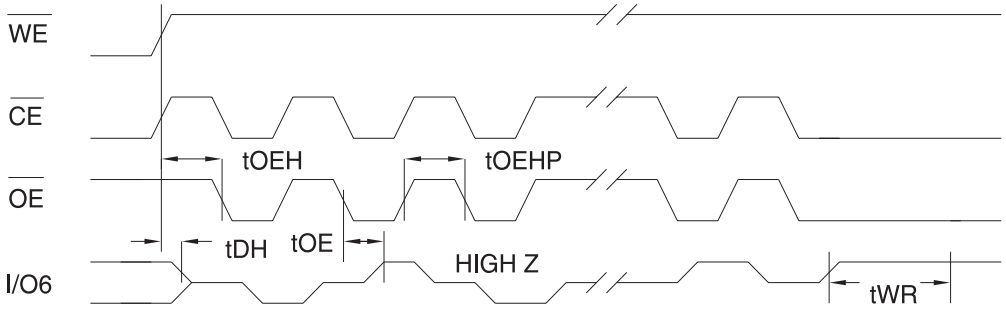


Toggle Bit Characteristics (1)

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay (2)				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

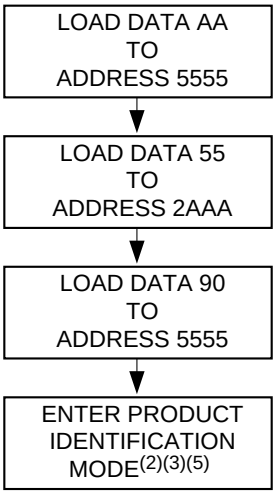
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in AC Read Characteristics.

Toggle Bit Waveforms (1)(2)(3)

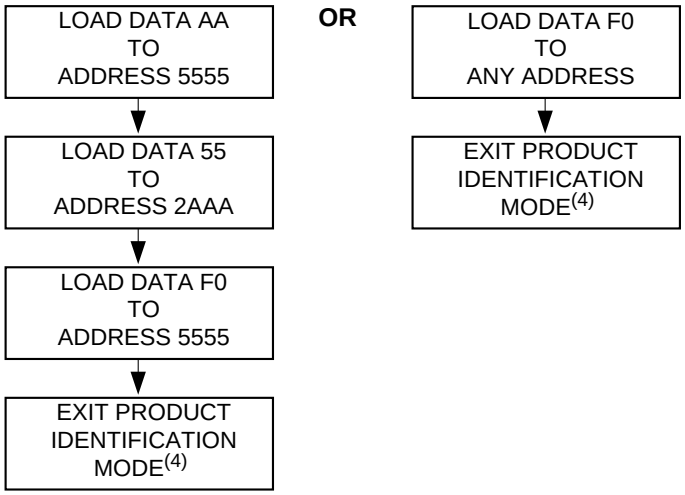


Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit. The t_{OEHP} specification must be met by the toggling the input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

Software Product Identification Entry[1]

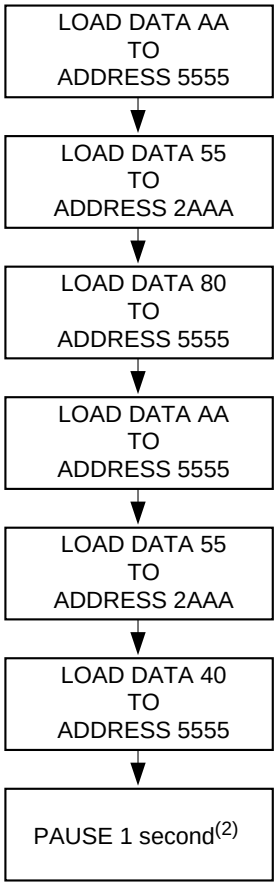


Software Product Identifcation Exit[1][6]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A14 - A0 (Hex).
2. A1 - A18 = V_{IL}.
   Manufacture Code is read for A0 = V_{IL};
   Device Code is read for A0 = V_{IH}.
3. The device does not remain in identification mode if powered down.
4. The device returns to standard operation mode.
5. Manufacturer Code: 1FH
   Device Code: A0H (49F8192), A3H (49F8192T)
6. Either one of the Product ID Exit commands can be used.

Boot Block Lockout Enable Algorithm[1]



Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex) Address Format: A14 - A0 (Hex).
2. Boot block lockout feature enabled.

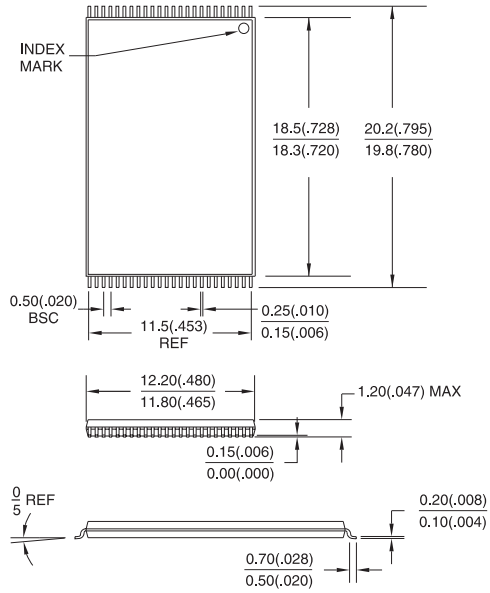
Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	50	0.3	AT49F8192-90TC AT49F8192-90RC	48T 44R	Commercial (0° to 70°C)
	50	0.3	AT49F8192-90TI AT49F8192-90RI	48T 44R	Industrial (-40° to 85°C)
120	50	0.3	AT49F8192-12TC AT49F8192-12RC	48T 44R	Commercial (0° to 70°C)
	50	0.3	AT49F8192-12TI AT49F8192-12RI	48T 44R	Industrial (-40° to 85°C)
90	50	0.3	AT49F8192T-90TC AT49F8192T-90RC	48T 44R	Commercial (0° to 70°C)
	50	0.3	AT49F8192T-90TI AT49F8192T-90RI	48T 44R	Industrial (-40° to 85°C)
120	50	0.3	AT49F8192T-12TC AT49F8192T-12RC	48T 44R	Commercial (0° to 70°C)
	50	0.3	AT49F8192T-12TI AT49F8192T-12RI	48T 44R	Industrial (-40° to 85°C)

Package Type	
48T	48-Lead, Thin Small Outline Package (TSOP)
44R	44-Lead, 0.525" Wide, Plastic Gull Wing Small Outline Package (SOIC/SOP)

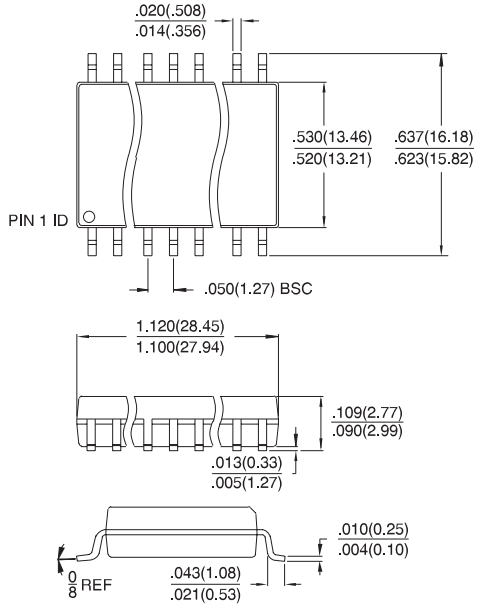
Packaging Information

48T, 48-Lead, Plastic Thin Small Outline Package (TSOP)
Dimensions in Millimeters and (Inches)*
JECED OUTLINE MO-142 DD



*Controlling dimension: millimeters

44R, 44-Lead, 0.525" Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



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