Clock generator for PC

BU2279F

BU2279F is an IC that generates multiple clocks from the built-in PLL by inputting standard clocks from outside. This IC is suitable for digital appliances.
54 MHz for video and 33.333MHz of digital system clock for CPU can be generated from widely used 13.5 MHz clock.

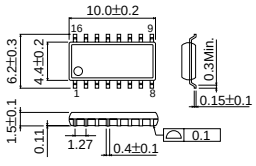
●Applications

DVD recorder, PC

●Features

1) Clock signals are generated by crystal oscillator.
2) SOP16 package.
3) Single power supply 3.3V.
4) No external components for PLL

●External dimensions (Unit : mm)



SOP16

●Absolute maximum rating (Ta=25°C)

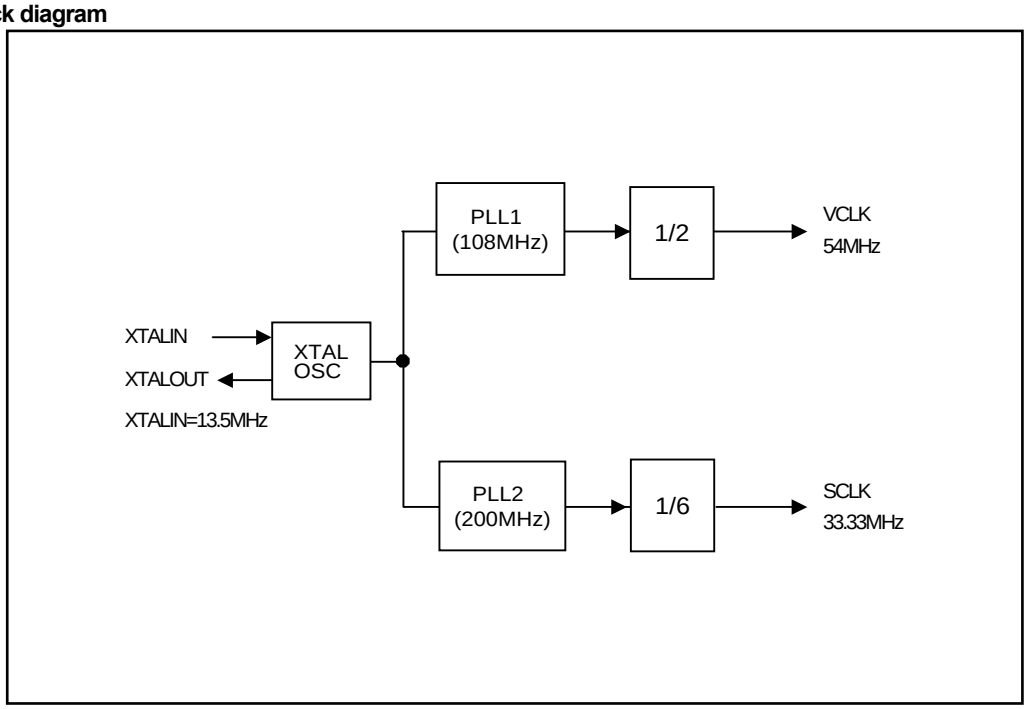
Parameter	Symbol	Limits	Unit
Impressed voltage	V_{DD}	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5 to V_{DD}+0.5	V
Storage temperature range	Pd	500 *	mW
Power dissipation	Tstg	−30 to +125	°C

* Ratio above does not guarantee the operation.
* When the condition is over Ta=25℃, dissipatioin is decreased 5mWper 1℃.
* Radiation resistance design is not used.
* Power dissipation is.

●Recommended operational conditions (Ta=25°C)

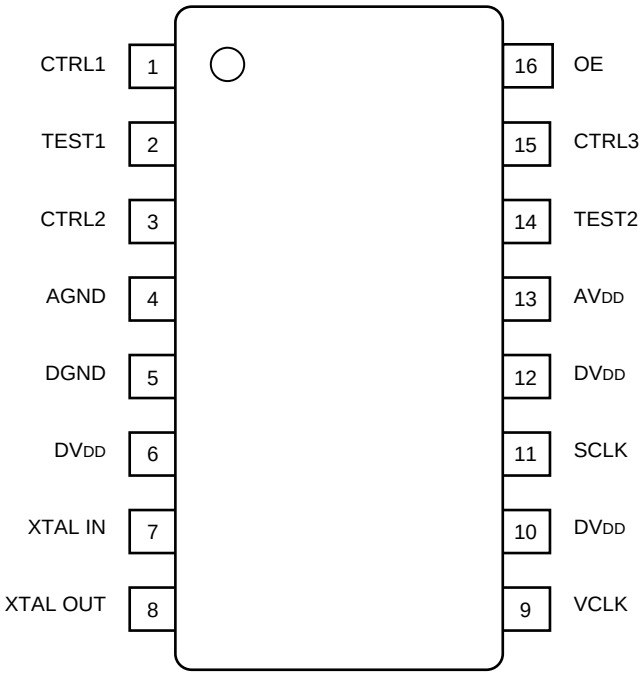
Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.0	–	3.6	V
Voltage range of "H" input	V_{IH}	0.8V_{DD}	–	V_{DD}	V
Voltage range of "L" input	V_{IL}	0	–	0.2V_{DD}	V
Operation temperature range	Topr	−5	–	+70	°C
Maximum output load	CL	–	–	15	pF

●**Block diagram**

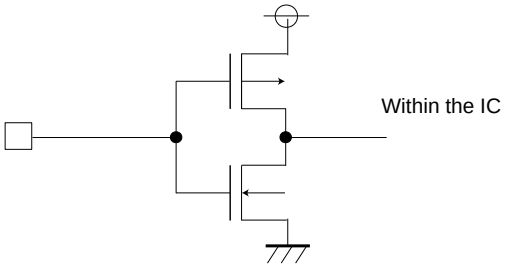
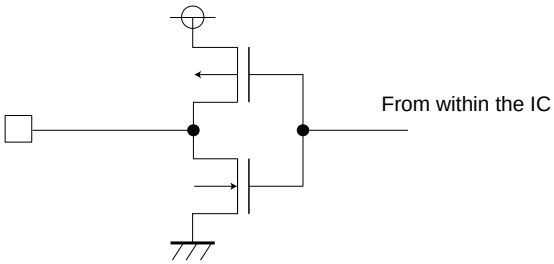
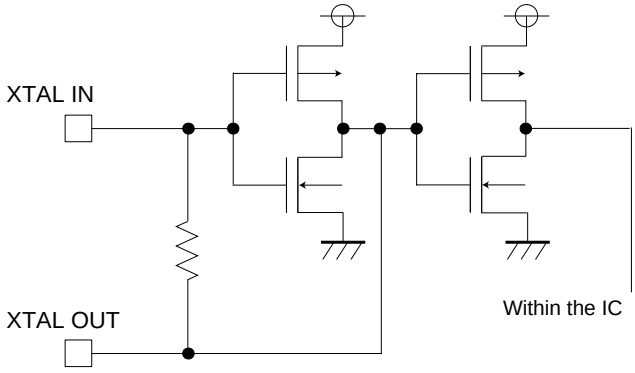


●**Pin descriptions**

Pin No.	Pin name	Functions
1	CTRL1	Test mode selector. Normally "L". pull-up
2	TEST1	TEST1
3	CTRL2	Test mode selector. Normally "L". pull-up
4	AGND	Analog GND
5	DGND	Digital GND
6	DV_{DD}	Digital V_{DD} for crystal
7	$XTAL_{IN}$	Crystal input 13.5MHz
8	$XTAL_{OUT}$	Crystal output
9	VCLK	54.00MHz output
10	DV_{DD}	Digital V_{DD} for VCLK
11	SCLK	33.33MHz output
12	DV_{DD}	Digital V_{DD}
13	AV_{DD}	Analog V_{DD}
14	TEST2	TEST2
15	CTRL3	Test mode selector. Normally "L". pull-up
16	OE	Output selector (NC : enable L : disable) pull-up



●Input output circuits

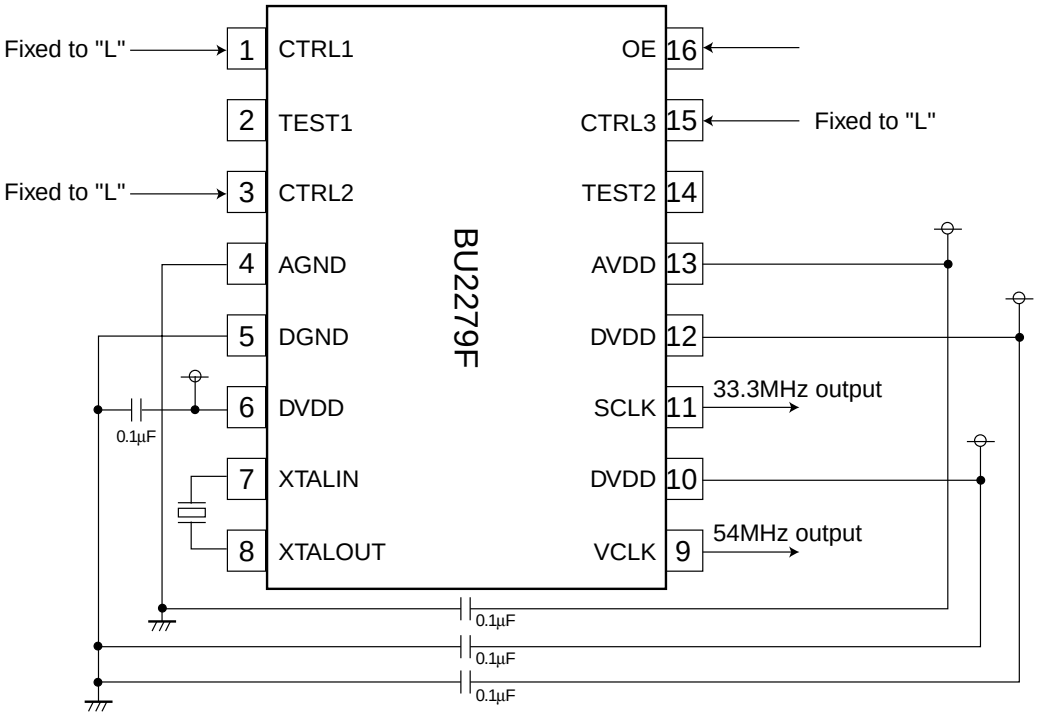
Pin No.	Equivalent circuit
Input Pin 1, 3, 15, 16 with pull-up resistor (about 50kΩ)	
Output Pin 9, 11	
Crystal Pin 7, 8	

●**Electric Characteristics (**Unless any specification, Vcc=3.3V, Ta=25°C, Crystal frequency=13.500MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Output "L" voltage	V_{OL}	–	–	0.4	V	I_{OL}=4.0mA
Output "H" voltage	V_{OH}	24	–	–	V	I_{OH}=–4.0mA
Operation current	I_{DD}	–	30	60	mA	No load
VCLK	VCLK	–	54.00	–	MHz	Xtal ×160 ÷20 ÷2
SCLK	SCLK	–	33.333	–	MHz	Xtal ×400 ÷27 ÷6
Design assurances						
VCLK Duty	Duty V	45	50	55	%	Measured at 1/2V_{DD}
SCLK Duty	Duty S	48	53	58	%	Measured at 1/2V_{DD}
Jitter1	Jstd1	–	80	–	psec	Jitter 1σ
Jitter2	Jstd2	–	400	–	psec	Jitter MIN=MAX
Rise time	tr	–	2.5	–	nsec	
Fall time	tr	–	2.5	–	nsec	
LOCK time of output	tLOCK	–	–	1	msec	*

Remarks) The output frequency is calculated from the input frequency of XTALIN. The value of output frequency above is the case of input frequency is 13.5MHz.
The values of Jitter above are the center value of 10000 sampling by time interval analyzer.
*The time for output frequency to be stabled after the power supply become 3.0V.

●**Application circuit**



Remarks) The IC is basically needed to be on the board. (Unless it is on the board, the characteristics are not guaranteed.)
Decoupling capacitance(0.1µF) is needed to be placed between Pin13(AVDD) and Pin4(AGND).
Decoupling capacitance(0.1µF)is needed to be placed between Pin16(DVDD) Pin10(DVDD), Pin12(DVDD) and Pin5(DGND) each.
To adjust the frequency of crystal, place a certain value of capacitance(pF) between 7 or Pin8 and DGND.
Pin2 and Pin4 are needed to be fixed to "OPEN" through the operation.