National Semiconductor

MICROCIRCUIT DATA SHEET

MNLMC6484AM-X REV 1A2

Original Creation Date: 08/16/95
Last Update Date: 03/10/03
Last Major Revision Date: 02/14/03

CMOS QUAD RAIL-TO-RAIL INPUT AND OUTPUT OPERATIONAL AMPLIFIER

General Description

The LMC6484 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes this device unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6484 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC274 and TLC279.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6484's rail-to-rail output swing. The LMC6484's rail-to-rail output swing is guaranteed for loads down to 600 Ohms.

Guaranteed low voltage characteristics and low power dissipation make the LMC6484 especially well-suited for battery-operated systems.

See the MNLMC6482AM-X data sheet for a Dual CMOS operational amplifier with these same features.

Industry Part Number

LMC6484AM

NS Part Numbers

LMC6484AMJ/883
LMC6484AMWG-QV
LMC6484AMWG/883

Prime Die

LMC6484

Controlling Document

SEE FEATURES SECTION

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

(Typical Unless Otherwise Noted)
- Rail-to-Rail input common-mode voltage range.
  (Guaranteed Over Temperature)
- Rail-to-Rail output swing.
  (within 20mV of supply rail, 100k Ohm load)
- Guaranteed 5V and 15V performance.
- Operates at 3V
- Excellent CMRR and PSRR. 82dB
- Ultra low input current. 20fA
- High voltage gain (Rl = 500k Ohms). 130dB
- Specified for 2k Ohm and 600 Ohm loads.

CONTROLLING DOCUMENTS:

LMC6484AMJ/883	5962-9453402MCA
LMC6484AMWG-QV	5962-9453402VXA
LMC6484AMWG/883	5962-9453402QXA

Applications

- Data Acquisition Systems.
- Transducer Amplifiers.
- Hand-held Analytic Instruments.
- Medical Instrumentation.
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source.
- Improved Replacement for TLC274, TLC279.

(Absolute Maximum Ratings)
(Note 1)

Supply Voltage (V+ - V-)	16V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V+)+0.3V,(V-)-0.3V
Current at Input Pin (Note 6)	±5mA
Current at Output Pin (Note 3, 5)	±30mA
Current at Power Supply Pin	40mA
Maximum Junction Temperature (Note 4)	150 C
Power Dissipation (Note 2)	315mW
Storage Temperature Range	-65 C ≤ Ta ≤ +150 C
Operating Temperature Range	-55 C ≤ Ta ≤ +125 C
Thermal Resistance	
ThetaJA	
14-Pin CERAMIC DIP (Still Air)	86.0 C/W
(500LF/Min Air flow)	49.0 C/W
14-Pin CERAMIC SOIC (Still Air)	116.0 C/W
(500LF/Min Air Flow)	72.0 C/W
ThetaJC	
14-Pin CERAMIC DIP	16.0 C/W
14-Pin CERAMIC SOIC	11.0 C/W
Package Weight	
CERAMIC DIP	TBD
CERAMIC SOIC	460mg
Lead Temperature (Soldering, 10 seconds)	260 C
ESD Tolerance (Note 7)	3.0kV

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: The maximum power dissipation must be derated at elevated temperatures and is dictated by Tjmax (maximum junction temperature), ThetaJA (package junction to ambient thermal resistance), and TA (ambient temperature). The maximum allowable power dissipation at any temperature is Pdmax = (Tjmax - TA)/ThetaJA or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150 C. Output currents in excess of ±30mA over long term may adversely affect reliability.

Note 4: All numbers apply for packages soldered directly into a PC board.

Note 5: Do not short circuit output to V+, when V+ is greater than 13V or reliability will be adversely affected.

(Continued)

Note 6: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.
Note 7: Human body model, 1.5k Ohms in series with 100pF. All pins rated per method 3015.6 of MIL-STD-883. This is a Class 2 device rating.

Recommended Operating Conditions

(Note 1)

Supply Voltage

$3.0V \leq V+ \leq 15.5V$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+=5V, V-=0V, Rl>1M, Vcm=Vo=V+/2

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vio	Input Offset Voltage					0.75	mV	1
						1.35	mV	2, 3
Iib	Input Bias Current					25	pA	1
						100	pA	2, 3
Iio	Input Offset Current					25	pA	1
						100	pA	2, 3
CMRR	Common Mode Rejection Ratio	0V<=Vcm<=15.0V, V+=15V			65		dB	1
					62		dB	2, 3
		0V<=Vcm<=5.0V			65		dB	1
					62		dB	2, 3
+PSRR	Positive Power Supply Rejection Ratio	5V<=V+<=15V, Vo=2.5V			65		dB	1
					62		dB	2, 3
-PSRR	Negative Power Supply Rejection Ratio	-5V<=V-<=-15V, Vo=-2.5V, V+=0V			65		dB	1
					62		dB	2, 3
Vcm	Input Common Mode Voltage Range	5V>=VCM>=15V, For CMRR>=50dB			V++.25	-0.25	V	1
					V+	0	V	2, 3
Isc	Output Short Circuit Current	Sourcing, Vo=0V			16		mA	1
					12		mA	2, 3
		Sinking, Vo=5V			11		mA	1
					9		mA	2, 3
		V+=15V, Sourcing, Vo=0V			28		mA	1
					22		mA	2, 3
		V+=15V, Sinking, Vo=12V	1		30		mA	1
			1		24		mA	2, 3
Icc	Supply Current	All four Amps				2.8	mA	1
						3.6	mA	2, 3
		All four amps, V+=+15V				3.0	mA	1
						4.0	mA	2, 3

Electrical Characteristics

DC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+=5V, V-=0V, Rl>1M, Vcm=Vo=V+/2

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vo	Output Swing	V+=5V, Rl=2K Ohms to V+/2			4.8	0.18	V	4
					4.7	0.24	V	5, 6
		V+=5V, Rl=600 Ohms to V+/2			4.5	0.50	V	4
					4.24	0.65	V	5, 6
		V+=15V, Rl=2K Ohms to V+/2			14.4	0.32	V	4
					14.2	0.45	V	5, 6
		V+=15V, Rl=600 Ohms to V+/2			13.4	1.00	V	4
					13.0	1.30	V	5, 6
Av	Large Signal Voltage Gain	Rl=2K Ohms Sourcing	2		140		V/mV	4
			2		84		V/mV	5, 6
		Rl=2K Ohms Sinking	2		35		V/mV	4
			2		20		V/mV	5, 6
		Rl=600 Ohms Sourcing	2		80		V/mV	4
			2		48		V/mV	5, 6
		Rl=600 Ohms Sinking	2		18		V/mV	4
			2		13		V/mV	5, 6

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: V+=5V, V-=0V, Rl>1M, Vcm=Vo=V+/2

Sr	Slew Rate		3		0.9		V/uS	4
			3		0.6		V/uS	5, 6
Gbw	Gain Bandwidth	V+=15V, set up for non-inverting			1.25		MHz	4
					1.15		MHz	5, 6

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: V+=5V, V-=0V, Rl>1M, Vcm=Vo=V+/2. "Delta Calculations performed on QMLV devices at Group B, Subgroup 5 ONLY".

Vio	Input Offset Voltage				+0.20	-0.20	mV	1
Iib	Input Bias Current				+15	-15	pA	1
Iio	Input Offset Current				+15	-15	pA	1

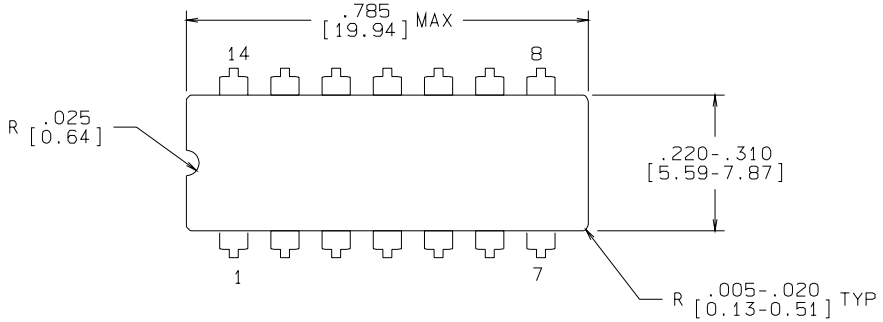
Note 1: Do not short circuit output to V+, when V+ is greater than 13V or reliability will be adversely affected.
Note 2: V+=15V, Vcm=7.5V and Rl connected to 7.5V. For Sourcing tests, 7.5V<=Vo<=11.5V. For Sinking tests, 3.5V<=Vo<=7.5V.
Note 3: V+=15V. Connected as Voltage Follower with 10V step input, 2.5V to 12.5V for +Slew, and 12.5V to 2.5V for -Slew. Number specified is the slower of either the positive or negative slew rates.

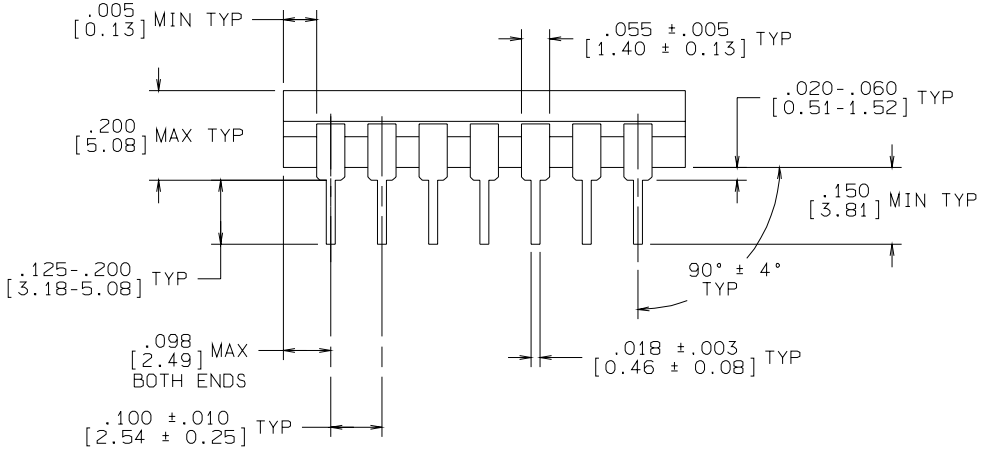
Graphics and Diagrams

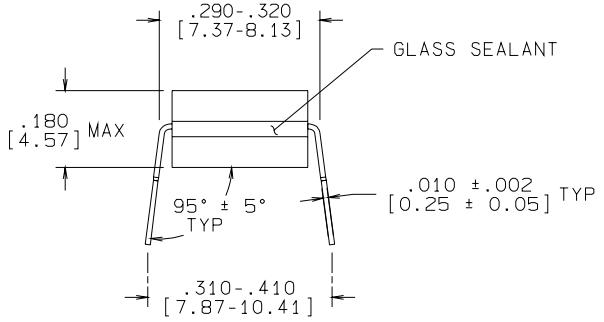
GRAPHICS#	DESCRIPTION
05275HRA5	CERPACK (W), 14 LEAD (B/I CKT)
05276HRG2	CERPACK (W), 14 LEAD (B/I CKT)
06087HRB4	CERDIP (J), 14 LEAD (B/I CKT)
06213HRA3	CERAMIC SOIC (WG), 14LD (B/I CKT)
J14ARH	CERDIP (J), 14 LEAD (P/P DWG)
P000117A	CERDIP (J), 14 LEAD (PIN OUT)
P000359A	CERAMIC SOIC (WG), 14 LEAD (PINOUT)
WG14ARC	CERAMIC SOIC (WG), 14LD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
H	REVISE PER CURRENT STD; REDRAW	10001	09/15/93	TL/







CONTROLLING DIMENSION: INCH

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH TO BE 200 MICROINCHES / 5.08 MICROMETERS MINIMUM SOLDER MEASURED AT THE CREST OF THE MAJOR FLATS.
2. JEDEC REGISTRATION MO-036, VARIATION AB, DATED 04/1981.

APPROVALS	DATE
DRAWN T. LEQUANG	09/15/93
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

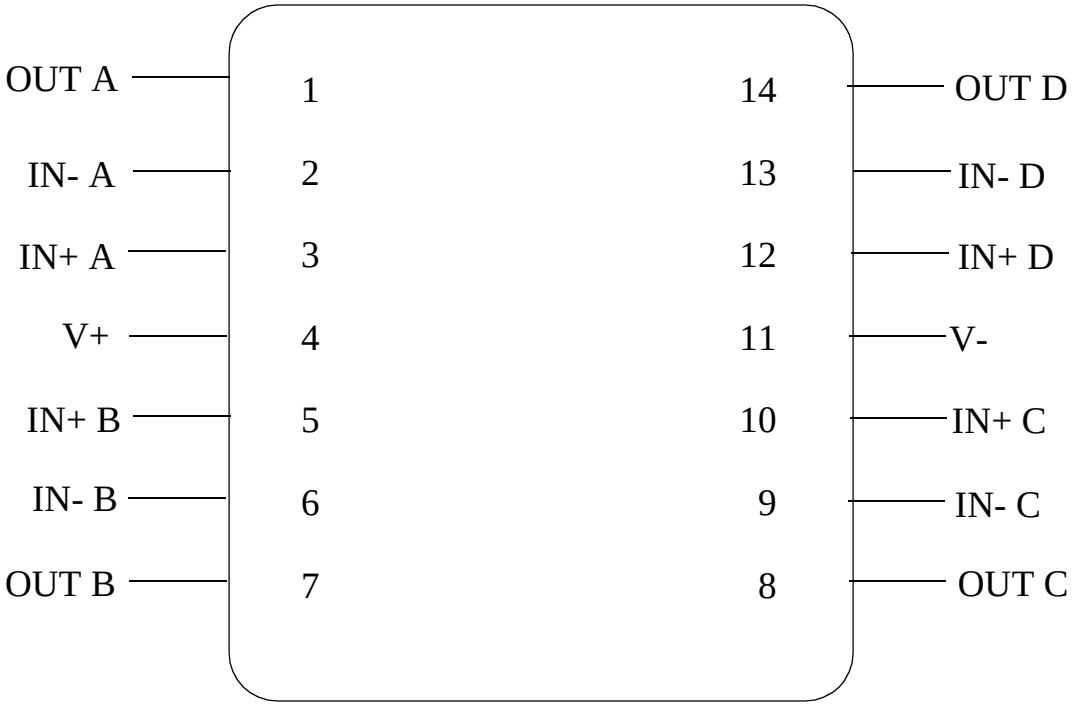
INCH
[MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 14 LEAD,

SCALE	SIZE	DRAWING NUMBER	REV
N/A	B	MKT-J14A	H

DO NOT SCALE DRAWING | SHEET 1 OF 1



LMC6484AMJ

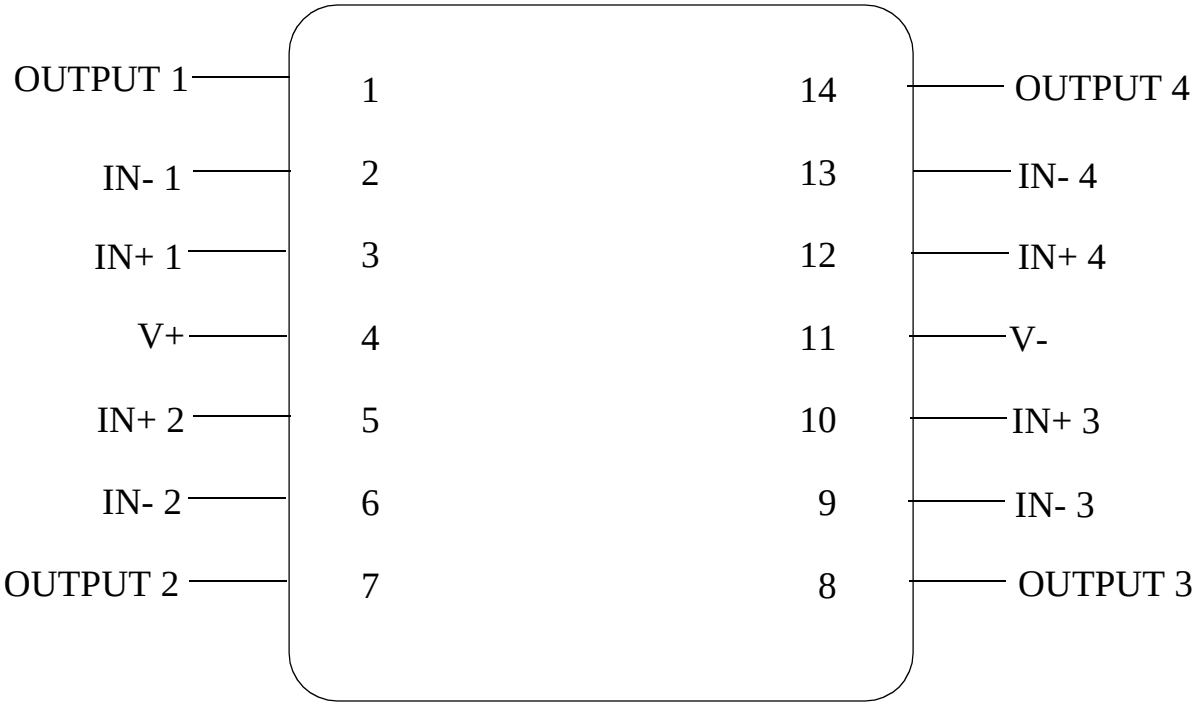
14 - LEAD DIP

CONNECTION DIAGRAM

TOP VIEW

P000117A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

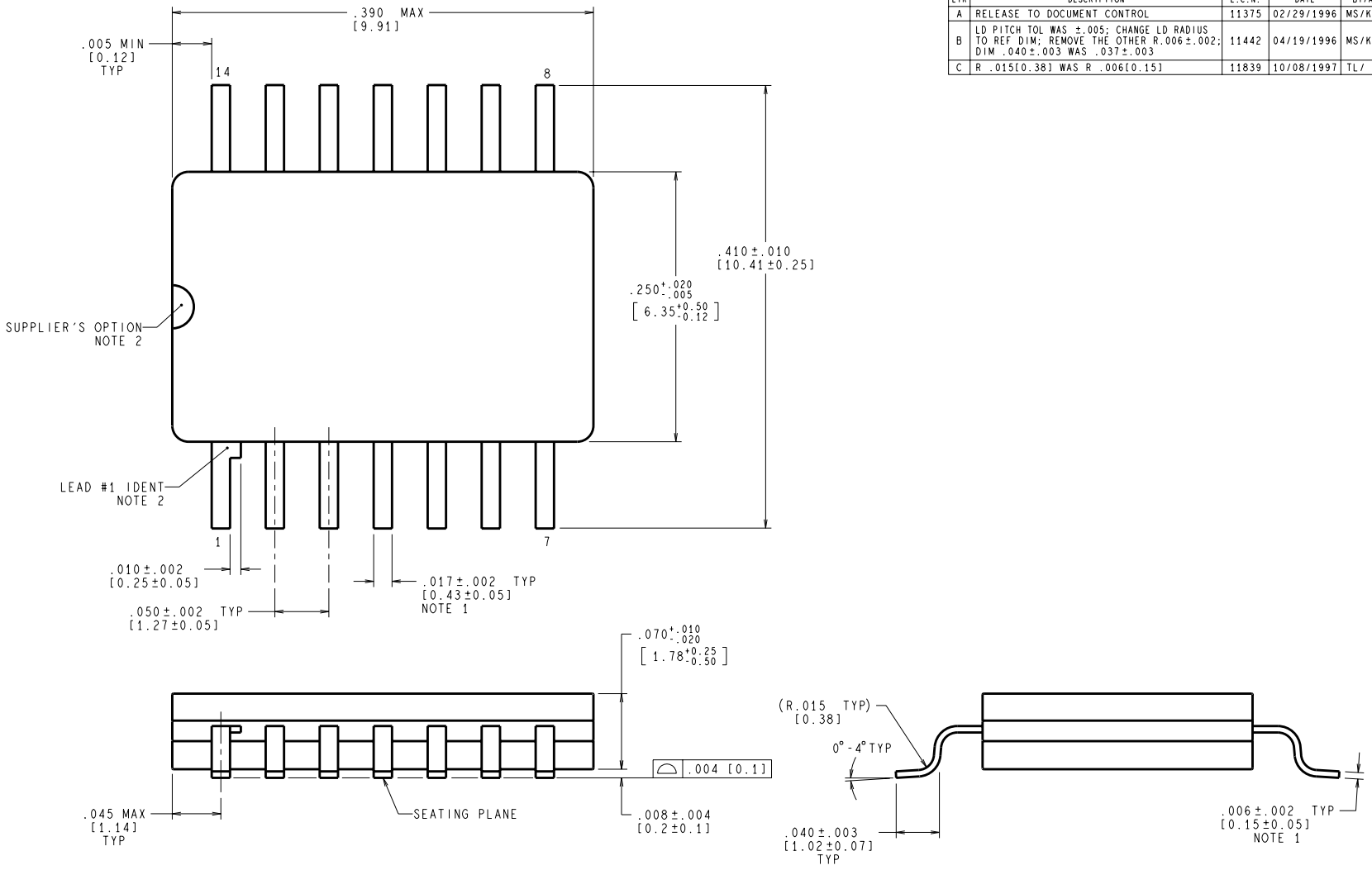


LMC6484AMWG
14 - LEAD CERAMIC SOIC
CONNECTION DIAGRAM

TOP VIEW
P000359A

National Semiconductor™
MIL/AEROSPACE OPERATIONS
2900 SEMICONDUCTOR DRIVE
SANTA CLARA, CA 95050

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	11375	02/29/1996	MS/KH
B	LD PITCH TOL WAS ±.005; CHANGE LD RADIUS TO REF DIM; REMOVE THE OTHER R.006±.002; DIM .040±.003 WAS .037±.003	11442	04/19/1996	MS/KH
C	R .015[0.38] WAS R .006[0.15]	11839	10/08/1997	TL/



NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-PRF-38535 TO A MINIMUM THICKNESS OF 200 MICROINCHES/ 5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE. MAXIMUM LIMIT MAY BE INCREASED BY .003 IN/ 0.08mm AFTER LEAD FINISH APPLIED.
2. LEAD 1 IDENTIFICATION SHALL BE:
   a) A NOTCH OR OTHER MARK WITHIN THIS AREA
   b) A TAB ON LEAD 1, EITHER SIDE
3. NO JEDEC REGISTRATION AS OF FEBRUARY 1996.

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

MIL-PRF-38535
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: MARTA SUCHY	02/29/96
DFTG. CHK.	
ENGR. CHK.	

National Semiconductor
2900 Semiconductor dr, Santa Clara, CA 95052-8090

CERPACK, 14 LEAD, GULL WING

PROJECTION — INCH [MM]

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	(SC)MKT-WG14A	C

DO NOT SCALE DRAWING — SHEET 1 of 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
0B1	M0002884	03/10/03	Rose Malone	Update MDS: MNLMC6484AM-X Rev. 0A0 to MNLMC6484AM-X Rev. 0B1. Updated subgroups to match SMD. Updated Pinout and MKT graphics for WG package. Updated B/I CKT's. Added Package Weight.
1A2	M0004135	03/10/03	Rose Malone	Update MDS: MNLMC6484AM-X, Rev. 0B1 to MNLMC6484AM-X, Rev. 1A2. Moved reference to SMD drawings from Main Table to Features Section and also device LMC6484AMWG-QV. Added Drift Table to Electrical Section and Added B/I Ckts to Graphics Section.