DUAL 16-BIT DAC

GENERAL DESCRIPTION

The TDA1541 is a monolithic integrated dual 16-bit digital-to-analogue converter (DAC) designed for use in hi-fi digital audio equipment such as Compact Disc players, digital tape or cassette recorders.

Features

- Selectable two-channel input format: offset binary or two's complement
- Internal timing and control circuit
- TTL compatible digital inputs
- High maximum input bit-rate and fast settling time

QUICK REFERENCE DATA

Supply voltages			
pin 28	V_{DD}	typ.	5 V
pin 26	V_{DD1}	typ.	−5 V
pin 15	V_{DD2}	typ.	−15 V
Supply currents			
pin 28	I_{DD}	typ.	45 mA
pin 26	I_{DD1}	typ.	45 mA
pin 15	I_{DD2}	typ.	25 mA
Signal-to-noise ratio (full scale sine-wave) at analogue outputs (AOL; AOR)	S/N	typ.	95 dB
Non-linearity at T_{amb} = −20 to + 70 °C		typ.	½ LSB
Current settling time to ± 1 LSB	t_{cs}	typ.	1 μs
Maximum input bit rate at data input (pin 3)	BR_{max}	min.	6 Mbits/s
Maximum clock frequency			
at clock input (pin 2)	f_{BCKmax}	min.	6 MHz
at clock input (pin 4)	f_{SCKmax}	min.	12 MHz
Full scale temperature coefficient at analogue outputs (AOL; AOR)	TC_{FS}	typ.	± 200 x 10^{-6} K^{-1}
Operating ambient temperature range	T_{amb}		−20 to + 70 °C
Total power dissipation	P_{tot}	typ.	850 mW

PACKAGE OUTLINE

28-lead DIL; plastic (with internal heat spreader) (SOT-117).

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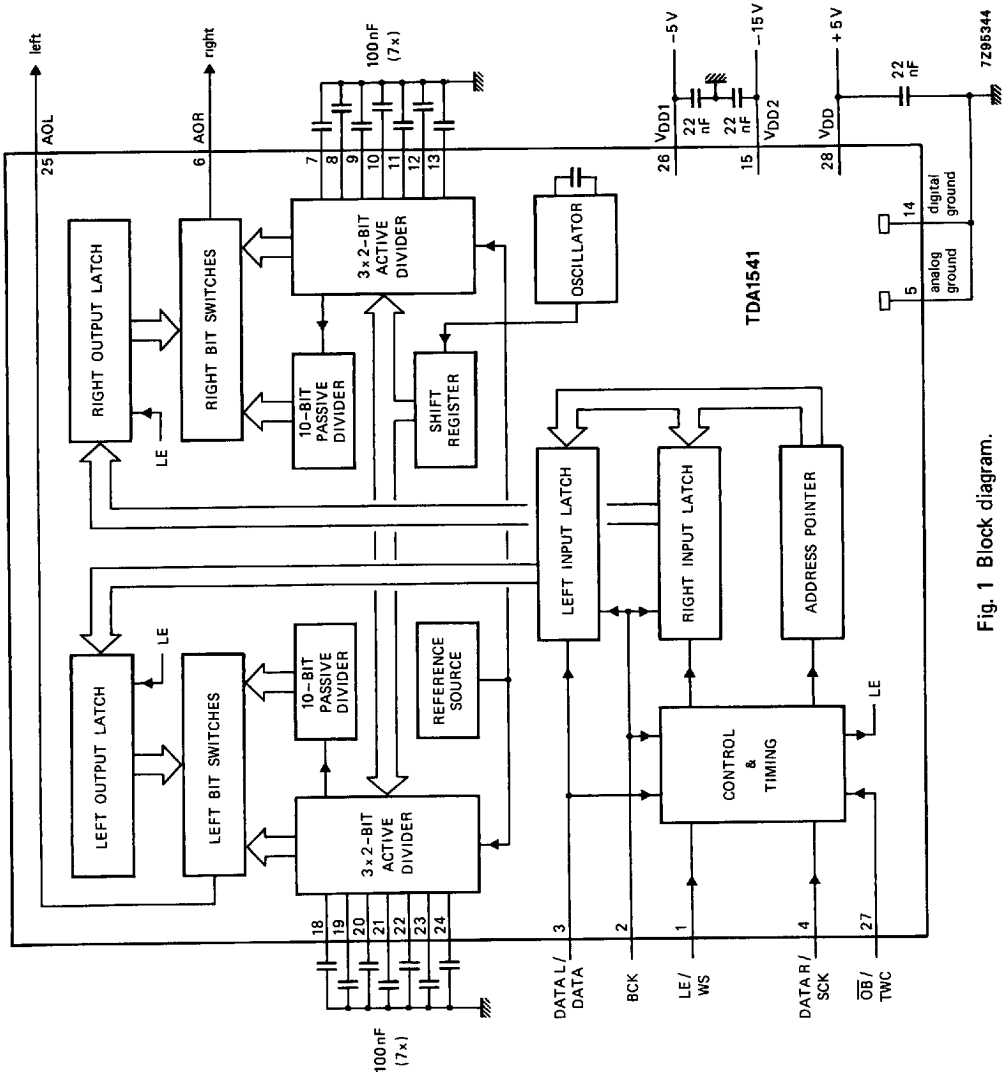

Fig. 1 Block diagram.

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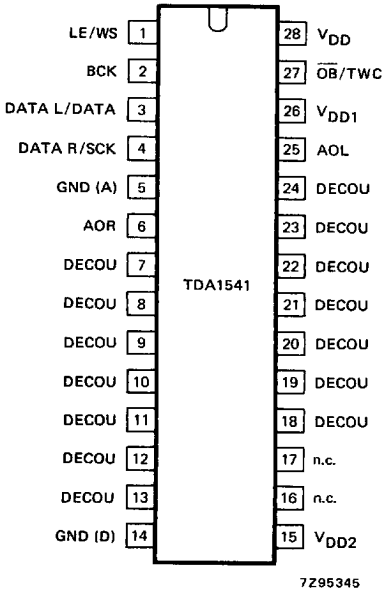

Fig. 2 Pinning diagram.

PINNING

1	LE/WS*	latch enable input / word select input
2	BCK*	bit clock input
3	DATA L/DATA*	data left channel input / data input (selected format)
4	DATA R/SYS*	data right channel input / system clock input
5	GND (A)	analogue ground
6	AOR	right channel output
7	DECOU	decoupling
8	DECOU	
9	DECOU	
10	DECOU	
11	DECOU	
12	DECOU	
13	DECOU	
14	GND (D)	digital ground
15	V_{DD2}	−15 V supply voltage
16	n.c.	not connected
17	n.c.	
18	DECOU	decoupling
19	DECOU	
20	DECOU	
21	DECOU	
22	DECOU	
23	DECOU	
24	DECOU	
25	AOL	left channel output
26	V_{DD1}	−5 V supply voltage
27	$\overline{OB}$/TWC*	mode selection input
28	V_{DD}	+ 5 V supply voltage

* See Table 1 data selection input.

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FUNCTIONAL DESCRIPTION

The TDA1541 accepts input sample formats in time multiplexed mode or simultaneous mode with any bit length. The most significant bit (MSB) must always be first. This flexible input data format allows easy interfacing with signal processing chips such as interpolation filters, error correction circuits, pulse code modulation adaptors and audio signal processors (ASP).

The high maximum input bit-rate and fast settling time facilitates application in 4 x oversampling systems (44,1 kHz to 176,4 kHz) with the associated simple analogue filtering function (low order, linear phase filter).

Input data selection (see also Table 1)

With input $\overline{OB}$/TWC connected to ground, data input (offset binary format) must be in time multiplexed mode. It is accompanied with a word select (WS) and a bit clock input (BCK) signal. A separate system clock input (SCK) is provided for accurate, jitter-free timing of the analogue outputs AOL and AOR.

With $\overline{OB}$/TWC connected to V_{DD} the mode is the same but data format must be in two's complement.

When input $\overline{OB}$/TWC is connected to (V_{DD1}) the two channels of data (L/R) are input simultaneously via (DATA L) and (DATA R), accompanied with BCK and a latch-enable input (LE). With this mode selected the data must be in offset binary.

The format of data input signals is shown in figures 3, 4 and 5.

True 16-bit performance is achieved by each channel using three 2-bit active dividers, operating on the dynamic element matching principle, in combination with a 10-bit passive current-divider, based on emitter scaling. All digital inputs are TTL compatible.

Table 1 Input data selection

$\overline{OB}$/TWC	mode	pin 1	pin 2	pin 3	pin 4
−5 V	simultaneous	LE	BCK	DATA L	DATA R
0 V	time MUX OB	WS	BCK	DATA OB	SCK
+5 V	time MUX TWC	WS	BCK	DATA TWC	SCK

Where:

LE = latch enable
WS = word select
BCK = bit clock
DATA L = data left
DATA R = data right
DATA OB = data offset binary
DATA TWC = data two's complement
MUX OB = multiplexed offset binary
MUX TWC = multiplexed two's complement

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage ranges		
pin 28	V_{DD}	0 to + 7 V
pin 26	V_{DD1}	0 to −7 V
pin 15	V_{DD2}	0 to −17 V
Crystal temperature range	T_{XTAL}	−55 to + 150 °C
Storage temperature range	T_{stg}	−55 to + 150 °C
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Electrostatic handling*	V_{es}	−1000 to + 1000 V

THERMAL RESISTANCE

From junction to ambient	$R_{th\ j\text{-}a}$	=	35 K/W

* Discharging a 250 pF capacitor through a 1 kΩ series resistor.

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CHARACTERISTICS

V_{DD} = + 5 V; V_{DD1} = −5 V; V_{DD2} = −12 V; T_{amb} = + 25 °C; measured in Fig. 1; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply					
Supply voltage ranges					
pin 28	V_{DD}	4,0	5,0	6,0	V
pin 26	$-V_{DD1}$	4,5	5,0	6,0	V
pin 15	$-V_{DD2}$	14	15	16	V
Supply currents					
pin 28	I_{DD}	–	45	tbf	mA
pin 26	$-I_{DD1}$	–	45	tbf	mA
pin 15	$-I_{DD2}$	–	25	tbf	mA
Resolution	Res	–	16	–	bits
Inputs					
Input current (pin 3 and pin 4)					
digital inputs LOW (< 0,8 V)	I_{IL}	–	–	tbf	mA
digital inputs HIGH (> 2,0 V)	I_{IH}	–	–	tbf	μA
Input frequency					
at clock input (pin 4)	f_{SCK}	–	–	12	MHz
at clock input (pin 2)	f_{BCK}	–	–	6	MHz
at data inputs (pin 3 and pin 4)	f_{DAT}	–	–	6	MHz
at word select input (pin 1)	f_{WS}	–	–	200	kHz
Input capacitance of digital inputs	C_I	–	12	–	pF
Oscillator					
Oscillator frequency with internal capacitor	f_{osc}	150	200	250	kHz
Analogue outputs (AOL; AOR)					
Output voltage compliance	V_{OC}	tbf	–	tbf	mV
Full scale current	I_{FS}	3,4	4,0	4,6	mA
Zero scale current	$\pm I_{ZS}$	–	tbf	–	nA
Full scale temperature coefficient T_{amb} = −20 to + 70 °C	TC_{FS}	–	$\pm 200 \times 10^{-6}$	–	K^{-1}
Linearity error integral					
at T_{amb} = 25 °C	E_1	–	0,5	–	LSB
at T_{amb} = −20 to + 70 °C	E_1	–	tbf	–	LSB
Linearity error differential					
at T_{amb} = 25 °C	E_{d1}	–	0,5	1	LSB
at T_{amb} = −20 to + 70 °C	E_{d1}	–	tbf	–	LSB

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parameter	symbol	min.	typ.	max.	unit
Signal-to-noise ratio + THD*	S/N	90	95	–	dB
Settling time to ± 1 LSB	t_{cs}	–	1	–	μs
Channel separation	α	80	tbf	–	dB
Unbalance between outputs	ΔI_{FS}	–	0,1	0,2	dB
Time delay between outputs	t_d	–	–	1	μs
Power supply ripple rejection**					
V_{DD} = + 5 V	RR	–	tbf	–	dB
V_{DD1} = −5 V	RR	–	tbf	–	dB
V_{DD2} = −15 V	RR	–	tbf	–	dB
Signal-to-noise ratio at bipolar zero	S/N	–	−100	–	dB
Timing (see Figs 3, 4 and 5)					
Rise time	t_r	–	–	35	ns
Fall time	t_f	–	–	35	ns
Bit clock cycle time	t_{CY}	160	–	–	ns
Bit clock HIGH time	t_{HB}	48	–	–	ns
Bit clock LOW time	t_{LB}	48	–	–	ns
Bit clock fall time to latch rise time	t_{FBRL}	0	–	–	ns
Bit clock rise time to latch fall time	t_{RBFL}	0	–	–	ns
Data set-up time to bit clock	t_{SDB}	32	–	–	ns
Data hold time to bit clock	t_{HDB}	0	–	–	ns
Data set-up time to system clock	t_{SDS}	32	–	–	ns
Word select hold time to system clock	t_{HWS}	0	–	–	ns
Word select set-up time to system clock	t_{SWS}	32	–	–	ns
Bit clock fall time to system clock rise time	t_{FBRS}	32	–	–	ns
System clock rise time to bit clock fall time	t_{RSFB}	32	–	–	ns
System clock fall time to bit clock rise time	t_{FSRB}	50	–	–	ns
Bit clock rise time to system clock fall time	t_{RBFS}	0	–	–	ns
Latch enable LOW time	t_{LLE}	20	–	–	ns
Latch enable HIGH time	t_{HLE}	32	–	–	ns

* Signal-to-noise ratio + THD with 1 kHz full scale sinewave generated at a sampling rate of 176,4 kHz.

** V_{ripple} = 1% of supply voltage and f_{ripple} = 100 Hz.

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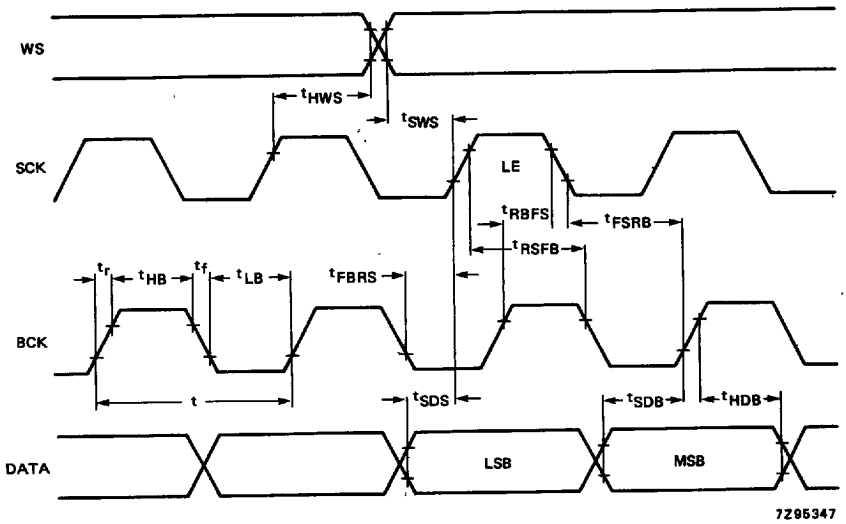

Fig. 3 Format of input signals; time multiplexed at $f_{SCK} = f_{BCK}$ (I^2S format).

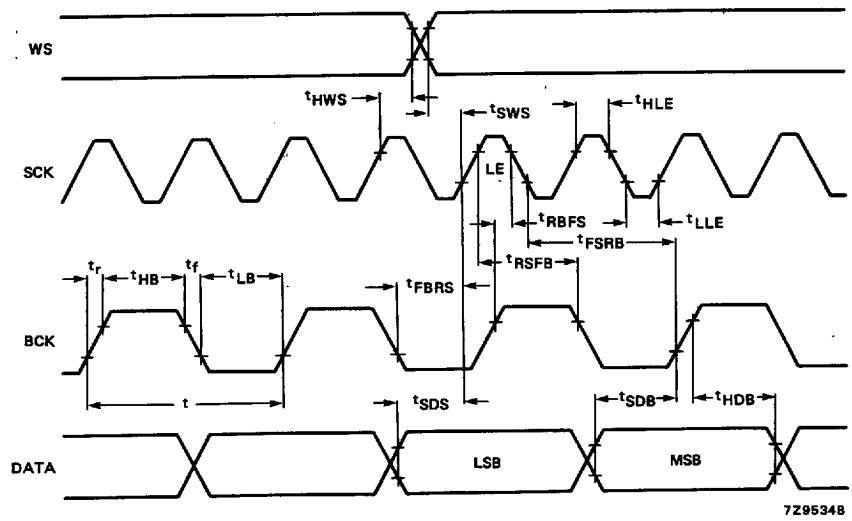

Fig. 4 Format of input signals; **time multiplexed** at $f_{SCK} = 2 \times f_{BCK}$.

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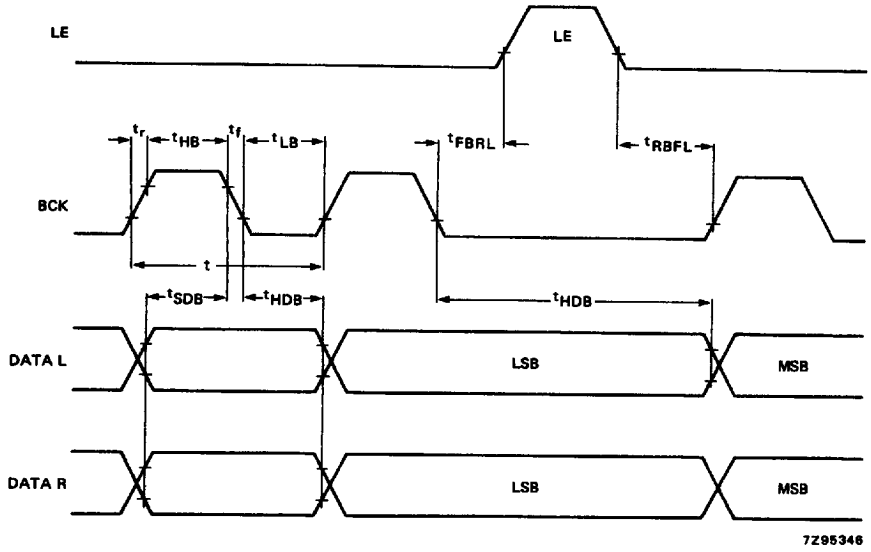

Fig. 5 Format of input signals; **simultaneous data.**

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