

# PEB 2465

## Four Channel Codec Filter



## Transceivers



Never stop thinking.

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## Four Channel Codec Filter

Transceivers



Never stop thinking.

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**PEB 2465****Revision History:**      **2000-02-08**

DS 3

Previous Version:      02.97

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| Page | Subjects (major changes since last revision) |
|------|----------------------------------------------|
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| <b>Table of Contents</b> |                                                   | <b>Page</b> |
|--------------------------|---------------------------------------------------|-------------|
| <b>1</b>                 | <b>General Description</b>                        | <b>10</b>   |
| 1.1                      | Features                                          | 11          |
| 1.2                      | Pin Configuration                                 | 12          |
| 1.3                      | Pin Definition and Functions                      | 13          |
| <b>2</b>                 | <b>Functional Description</b>                     | <b>16</b>   |
| 2.1                      | SICOFI-4 Principles                               | 16          |
| 2.2                      | IOM-2 Interface                                   | 19          |
| <b>3</b>                 | <b>Programming the SICOFI-4</b>                   | <b>23</b>   |
| 3.1                      | Types of Monitor Bytes                            | 24          |
| 3.2                      | Storage of Programming Information                | 24          |
| 3.3                      | SICOFI-4 Commands                                 | 25          |
| 3.3.1                    | SOP – Write Commands                              | 25          |
| 3.3.2                    | XOP – Write Commands                              | 26          |
| 3.3.3                    | COP – Write Commands                              | 27          |
| 3.3.4                    | SOP – Read Commands                               | 28          |
| 3.3.5                    | XOP – Read Commands                               | 29          |
| 3.3.6                    | COP – Read Commands                               | 30          |
| 3.3.7                    | Example for a Mixed Command                       | 31          |
| 3.4                      | SOP Command                                       | 33          |
| 3.4.1                    | CR1 Configuration Register 1                      | 34          |
| 3.4.2                    | CR2 Configuration Register 2                      | 35          |
| 3.4.3                    | CR3 Configuration Register 3                      | 36          |
| 3.4.4                    | CR4 Configuration Register 4                      | 38          |
| 3.5                      | How to Program the Filter Coefficients            | 40          |
| 3.6                      | XOP Command                                       | 41          |
| 3.6.1                    | XR1 Extended Register 1                           | 41          |
| 3.6.2                    | XR2 Extended Register 2                           | 42          |
| 3.6.3                    | XR3 Extended Register 3                           | 44          |
| 3.6.4                    | XR4 Extended Register 4                           | 44          |
| <b>4</b>                 | <b>SLIC Interface</b>                             | <b>45</b>   |
| 4.1                      | IOM-2 Interface Command/Indication Byte           | 45          |
| 4.2                      | Data-downstream C/I Channel Byte Format (receive) | 46          |
| 4.3                      | Data Upstream C/I Channel Byte Format (transmit)  | 46          |
| <b>5</b>                 | <b>Operating Modes</b>                            | <b>49</b>   |
| 5.1                      | RESET (Basic setting mode)                        | 50          |
| 5.2                      | Standby Mode                                      | 51          |
| 5.3                      | Operating Mode                                    | 51          |
| <b>6</b>                 | <b>Programmable Filters</b>                       | <b>52</b>   |
| 6.1                      | Impedance Matching Filter                         | 52          |

| <b>Table of Contents</b>                                                | <b>Page</b> |
|-------------------------------------------------------------------------|-------------|
| 6.2 Transhybrid Balancing (TH) Filter . . . . .                         | 52          |
| 6.3 Filters for Frequency Response Correction . . . . .                 | 53          |
| 6.4 Amplification/Attenuation-Filters AX1, AX2, AR1, AR2 . . . . .      | 54          |
| 6.5 Amplification/Attenuation Receive (AR1, AR2)-Filter . . . . .       | 54          |
| 6.6 Amplification/Attenuation Transmit (AX1, AX2)-Filter . . . . .      | 54          |
| <b>7 QSICOS Software . . . . .</b>                                      | <b>55</b>   |
| 7.1 QSICOS Supports . . . . .                                           | 56          |
| <b>8 Transmission Characteristics . . . . .</b>                         | <b>57</b>   |
| 8.1 Frequency Response . . . . .                                        | 59          |
| 8.2 Group Delay . . . . .                                               | 60          |
| 8.3 Out-of-Band Signals at Analog Input . . . . .                       | 62          |
| 8.4 Out-of-Band Signals at Analog Output . . . . .                      | 63          |
| 8.5 Out of Band Idle Channel Noise at Analog Output . . . . .           | 64          |
| 8.6 Overload Compression . . . . .                                      | 65          |
| 8.7 Gain Tracking (receive or transmit) . . . . .                       | 66          |
| 8.8 Total Distortion . . . . .                                          | 67          |
| 8.8.1 Total Distortion Measured with Sine Wave . . . . .                | 67          |
| 8.8.2 Total Distortion Measured with Noise According to CCITT . . . . . | 68          |
| 8.9 Single Frequency Distortion . . . . .                               | 69          |
| 8.10 Transhybrid Loss . . . . .                                         | 70          |
| <b>9 Electrical Characteristics . . . . .</b>                           | <b>71</b>   |
| 9.1 Absolute Maximum Ratings . . . . .                                  | 71          |
| 9.2 Operating Range . . . . .                                           | 72          |
| 9.3 Digital Interface . . . . .                                         | 73          |
| 9.4 Analog Interface . . . . .                                          | 74          |
| 9.5 Reset Timing . . . . .                                              | 74          |
| 9.5.1 IOM-2 Interface Timing . . . . .                                  | 74          |
| 9.5.2 4-MHz Operation Mode (Mode = 1) . . . . .                         | 74          |
| 9.5.3 2-MHz Operation Mode (Mode = 0) . . . . .                         | 75          |
| 9.6 IOM-2 Command/Indication Interface Timing . . . . .                 | 77          |
| 9.6.1 4-MHz Operation Mode (Mode = 1) . . . . .                         | 77          |
| 9.6.2 2-MHz Operation Mode (Mode = 0) . . . . .                         | 78          |
| 9.7 Detector Select Timing . . . . .                                    | 79          |
| <b>10 Appendix . . . . .</b>                                            | <b>80</b>   |
| 10.1 IOM-2 Interface Monitor Transfer Protocol . . . . .                | 80          |
| 10.1.1 Monitor Channel Operation . . . . .                              | 80          |
| 10.1.2 Monitor Handshake Procedure . . . . .                            | 81          |
| 10.1.3 State Diagram of the SICOFI-4 Monitor Transmitter . . . . .      | 82          |
| 10.1.4 State Diagram of the SICOFI-4 Monitor Receiver . . . . .         | 83          |
| 10.1.5 Monitor Channel Data Structure . . . . .                         | 84          |

|           |                                                    |            |
|-----------|----------------------------------------------------|------------|
| 10.2      | IOM-2 Interface Programming Procedure . . . . .    | 85         |
| 10.3      | Test Features . . . . .                            | 87         |
| 10.3.1    | Boundary Scan . . . . .                            | 87         |
| 10.3.2    | The TAP-Controller . . . . .                       | 89         |
| 10.3.3    | Level Metering Function . . . . .                  | 92         |
| 10.3.4    | Using the Level Metering Function . . . . .        | 94         |
| 10.4      | Programming the SICOFI-4 Tone Generators . . . . . | 96         |
| <b>11</b> | <b>Proposed Test Circuit . . . . .</b>             | <b>97</b>  |
| <b>12</b> | <b>Board Layout Recommendation . . . . .</b>       | <b>98</b>  |
| 12.1      | Board Layout . . . . .                             | 98         |
| 12.2      | Filter Capacitors . . . . .                        | 98         |
| <b>13</b> | <b>Package Outlines . . . . .</b>                  | <b>100</b> |

## List of Figures

## Page

|           |                                                                        |    |
|-----------|------------------------------------------------------------------------|----|
| Figure 1  | Pin Configuration . . . . .                                            | 12 |
| Figure 2  | SICOFI-4 Signal Flow Graph (for either channel) . . . . .              | 16 |
| Figure 3  | SICOFI-4 Block Diagram . . . . .                                       | 18 |
| Figure 4  | IOM-2 Interface Timing for 16 Voice Channels (per 8 kHz frame) . . . . | 19 |
| Figure 5  | IOM-2 Interface Timing (DCL=4096 kHz, MODE=1, per 8 kHz frame) . .     | 20 |
| Figure 6  | IOM-2 Interface Timing (DCL = 2048 kHz, MODE = 0) . . . . .            | 21 |
| Figure 7  | CUT OFFs and Loops . . . . .                                           | 37 |
| Figure 8  | Channel Registers . . . . .                                            | 40 |
| Figure 9  | SLICs with Multiplexed Loop/Ground Key Detect . . . . .                | 43 |
| Figure 10 | Data Flow . . . . .                                                    | 48 |
| Figure 11 | Operating Modes . . . . .                                              | 49 |
| Figure 12 | QSICOS Software . . . . .                                              | 55 |
| Figure 13 | Receive: Reference Frequency 1 kHz, Input Signal Level 0 dBm0 . . .    | 59 |
| Figure 14 | Transmit: Reference Frequency 1 kHz, Input Signal Level 0 dBm0 . .     | 59 |
| Figure 15 | Group Delay Distortion Transmit: Input Signal Level 0 dBm0 . . . . .   | 60 |
| Figure 16 | Group Delay Distortion Receive: Input Signal Level 0 dBm0. . . . .     | 61 |
| Figure 17 | $\mu$ -Law, Transmit: measured with sine wave $f = 1014$ Hz. . . . .   | 65 |
| Figure 18 | Gain Tracking: . . . . . (measured with sine wave $f = 1014$ Hz        | 66 |
| Figure 19 | Receive or Transmit: measured with sine wave $f = 1014$ Hz. . . . .    | 67 |
| Figure 20 | Receive . . . . .                                                      | 68 |
| Figure 21 | Transmit. . . . .                                                      | 68 |
| Figure 22 | Block Diagram . . . . .                                                | 93 |

**List of Tables****Page**

|         |                                                                  |    |
|---------|------------------------------------------------------------------|----|
| Table 1 | Pin Definition and Functions . . . . .                           | 13 |
| Table 2 | IOM-2 Timeslot Selection. . . . .                                | 21 |
| Table 3 | Transmission Characteristics. . . . .                            | 58 |
| Table 4 | Group Delay Absolute Values: Input signal level 0 dBm0 . . . . . | 60 |
| Table 5 | Switching Characteristics. . . . .                               | 75 |
| Table 6 | Switching Characteristics. . . . .                               | 76 |
| Table 7 | Switching Characteristics. . . . .                               | 78 |
| Table 8 | Switching Characteristics. . . . .                               | 79 |

## **1 General Description**

The four Channel CODEC Filter PEB 2465 SICOFI-4 is the logic continuation of a well-established family of SIEMENS codec-filter-ICs.

The SICOFI-4 is a fully integrated PCM CODEC and FILTER fabricated in low power 1 $\mu$  CMOS technology for applications in digital communication systems. Based on an advanced digital filter concept, the PEB 2465 provides excellent transmission performance and high flexibility. The new filter concept (second generation) lends to a maximum of independence between the different filter blocks. Each filter block can be seen like an one to one representative of the corresponding network element.

Only very few external components are needed, to complete the functionality of the SICOFI-4. The internal level accuracy is based on a very accurate bandgap reference. The frequency behavior is mainly determined by digital filters, which do not have any fluctuations. As a result of the new ADC - and DAC - concepts linearity is only limited by second order parasitic effects. Although the device works with only one single 5 V supply there is a very good dynamic range available.

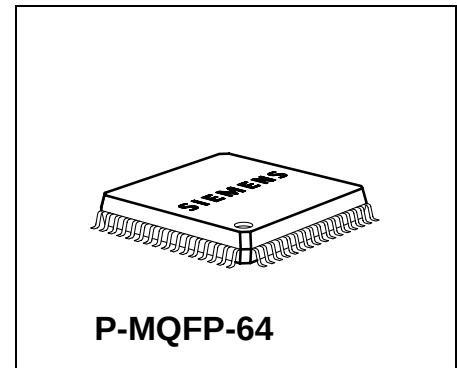
## Four Channel Codec Filter SICOFI-4

PEB 2465

### V2.3

#### 1.1 Features

- Single chip CODEC and FILTER to handle four CO- or PABX-channels
- Specification according to relevant CCITT, EIA and LSSGR recommendations
- Digital signal processing technique
- Programmable interface optimized to current feed SLICs and transformer solutions
- Four pin serial IOM-2 Interface
- Single power supply 5 V
- Advanced low power 1  $\mu$ m analog CMOS technology
- Standard 64 pin P-MQFP-64 package
- High performance Analog to Digital Conversion
- High performance Digital to Analog Conversion
- Programmable digital filters to adapt the transmission behavior especially for
  - AC impedance matching
  - transhybrid balancing
  - frequency response
  - gain
- Advanced test capabilities
  - all digital pins can be tested within a boundary scan scheme (IEEE 1149.1)
  - five digital loops
  - four analog loops
  - two programmable tone generators per channel
- Comprehensive Development Platform available
  - software for automatic filter coefficient calculation - QSICOS
  - Hardware development board - STUT 2465



| Type     | Package |
|----------|---------|
| PEB 2465 |         |

## 1.2 Pin Configuration

(top view)

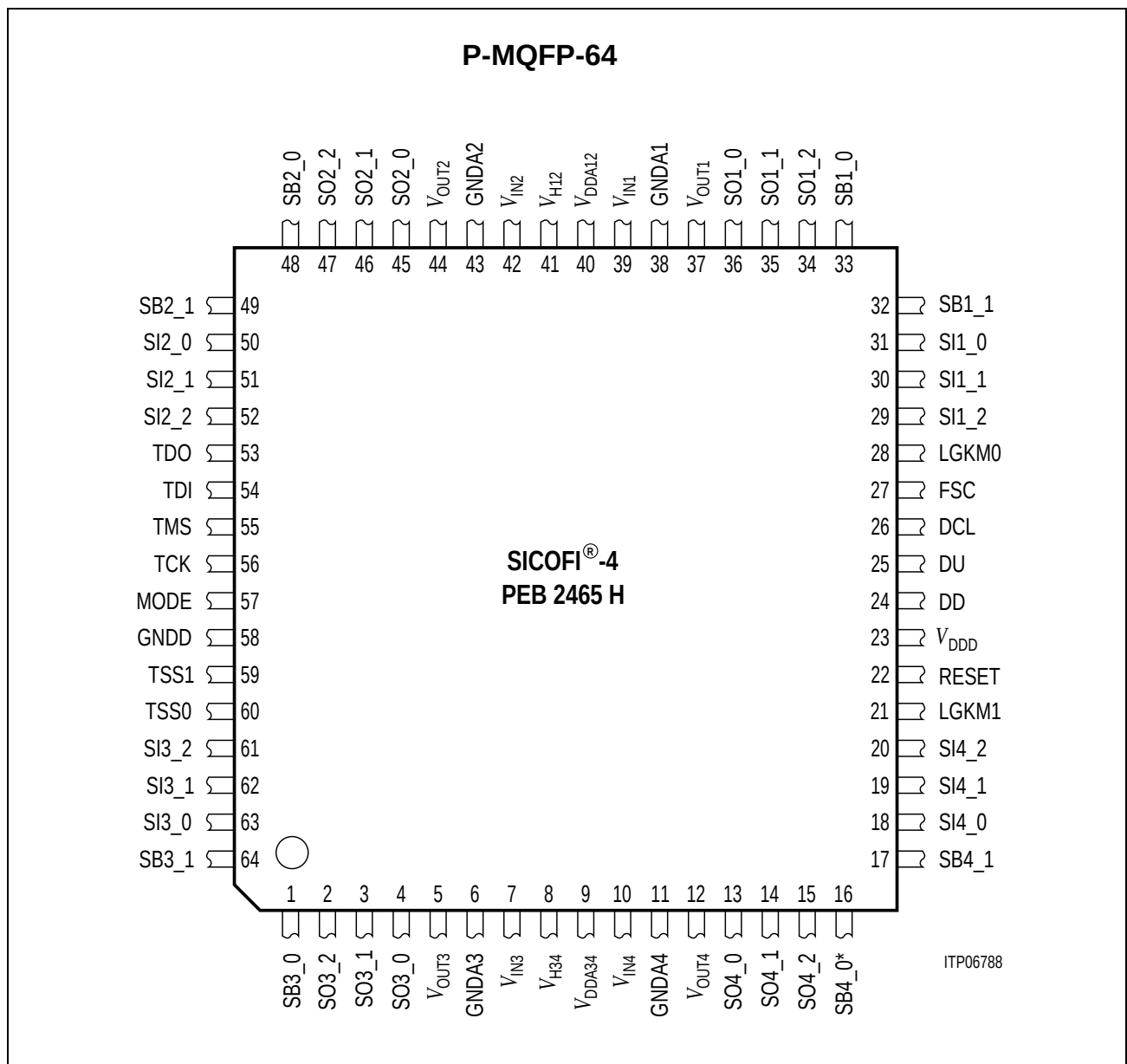


**Figure 1 Pin Configuration**

\*pin designation is corrected in 01.00

### 1.3 Pin Definition and Functions

**Table 1 Pin Definition and Functions**

| Pin No.                             | Symbol             | Input (I)<br>Output (O) | Function                                                                                                    |
|-------------------------------------|--------------------|-------------------------|-------------------------------------------------------------------------------------------------------------|
| <b>Common Pins for All Channels</b> |                    |                         |                                                                                                             |
| 23                                  | V <sub>DDD</sub>   | I                       | + 5 V supply for the digital circuitry <sup>1)</sup>                                                        |
| 58                                  | GNDD               | I                       | Ground Digital, not internally connected to GNDA 1, 2, 3, 4<br>All digital signals are referred to this pin |
| 40                                  | V <sub>DDA12</sub> | I                       | + 5 V Analog supply voltage for channel 1 and 2 <sup>1)</sup>                                               |
| 9                                   | V <sub>DDA34</sub> | I                       | + 5 V Analog supply voltage for channel 3 and 4 <sup>1)</sup>                                               |
| 27                                  | FSC                | I                       | IOM-2: Frame synchronization clock , 8 kHz                                                                  |
| 26                                  | DCL                | I                       | IOM-2: Data clock, 2048 kHz or 4096 kHz depending on MODE                                                   |
| 25                                  | DU                 | O                       | IOM-2: Data upstream, open drain output                                                                     |
| 24                                  | DD                 | I                       | IOM-2: Data downstream, input                                                                               |
| 22                                  | RESET              | I                       | Reset input - forces the device to the default mode, active high                                            |
| 57                                  | MODE               | I                       | IOM-2: Mode Selection                                                                                       |
| 60                                  | TSS0               | I                       | IOM-2: Time slot selection pin 0                                                                            |
| 59                                  | TSS1               | I                       | IOM-2: Time slot selection pin 1                                                                            |
| 56                                  | TCK                | I                       | Boundary scan: Test Clock                                                                                   |
| 55                                  | TMS                | I                       | Boundary scan: Test Mode Select                                                                             |
| 54                                  | TDI                | I                       | Boundary scan: Test Data Input                                                                              |
| 53                                  | TDO                | O                       | Boundary scan: Test Data Output                                                                             |
| 28                                  | LGKM0              | O                       | Loop/Ground Key Multiplexing output 0 for channel 1, 2                                                      |
| 21                                  | LGKM1              | O                       | Loop/Ground Key Multiplexing output 1 for channel 3, 4                                                      |
| 41                                  | V <sub>H12</sub>   | I/O                     | Reference voltage for channel 1 and 2, has to be connected via a 220 nF cap. to ground                      |
| 8                                   | V <sub>H34</sub>   | I/O                     | Reference voltage for channel 3 and 4, has to be connected via a 220 nF cap. to ground                      |

<sup>1)</sup> A 100 nF cap. should be used for blocking these pins, see also on [Page 75](#).

**General Description**
**Table 1 Pin Definition and Functions (cont'd)**

| Pin No.                            | Symbol            | Input (I)<br>Output (O) | Function                                                                      |
|------------------------------------|-------------------|-------------------------|-------------------------------------------------------------------------------|
| <b>Specific Pins for Channel 1</b> |                   |                         |                                                                               |
| 38                                 | GNDA1             | I                       | Ground Analog for channel 1, not internally connected to GNDD or GNDA 2, 3, 4 |
| 39                                 | V <sub>IN1</sub>  | I                       | Analog voice (voltage) input for channel 1                                    |
| 37                                 | V <sub>OUT1</sub> | O                       | Analog voice (voltage) output for channel 1                                   |
| 31                                 | SI1_0             | I                       | Signaling indication input pin 0 for channel 1                                |
| 30                                 | SI1_1             | I                       | Signaling indication input pin 1 for channel 1                                |
| 29                                 | SI1_2             | I                       | Signaling indication input pin 2 for channel 1                                |
| 36                                 | SO1_0             | O                       | Signaling command output pin 0 for channel 1                                  |
| 35                                 | SO1_1             | O                       | Signaling command output pin 1 for channel 1                                  |
| 34                                 | SO1_2             | O                       | Signaling command output pin 2 for channel 1                                  |
| 33                                 | SB1_0             | I/O                     | Bi-directional signal. command indication pin 0 for channel 1                 |
| 32                                 | SB1_1             | I/O                     | Bi-directional signal. command indication pin 1 for channel 1                 |
| <b>Specific Pins for Channel 2</b> |                   |                         |                                                                               |
| 43                                 | GNDA2             | I                       | Ground Analog for channel 2, not internally connected to GNDD or GNDA 1, 3, 4 |
| 42                                 | V <sub>IN2</sub>  | I                       | Analog voice (voltage) input for channel 2                                    |
| 44                                 | V <sub>OUT2</sub> | O                       | Analog voice (voltage) output for channel 2                                   |
| 50                                 | SI2_0             | I                       | Signaling indication input pin 0 for channel 2                                |
| 51                                 | SI2_1             | I                       | Signaling indication input pin 1 for channel 2                                |
| 52                                 | SI2_2             | I                       | Signaling indication input pin 2 for channel 2                                |
| 45                                 | SO2_0             | O                       | Signaling command output pin 0 for channel 2                                  |
| 46                                 | SO2_1             | O                       | Signaling command output pin 1 for channel 2                                  |
| 47                                 | SO2_2             | O                       | Signaling command output pin 2 for channel 2                                  |
| 48                                 | SB2_0             | I/O                     | Bi-directional signal. command indication pin 0 for channel 2                 |
| 49                                 | SB2_1             | I/O                     | Bi-directional signal. command indication pin 1 for channel 2                 |

**General Description**
**Table 1 Pin Definition and Functions (cont'd)**

| Pin No.                            | Symbol            | Input (I)<br>Output (O) | Function                                                                     |
|------------------------------------|-------------------|-------------------------|------------------------------------------------------------------------------|
| <b>Specific Pins for Channel 3</b> |                   |                         |                                                                              |
| 6                                  | GNDA3             | I                       | Ground Analog for channel 3, not internally connected to GNDD or GNDA1, 2, 4 |
| 7                                  | V <sub>IN3</sub>  | I                       | Analog voice (voltage) input for channel 3                                   |
| 5                                  | V <sub>OUT3</sub> | O                       | Analog voice (voltage) output for channel 3                                  |
| 63                                 | SI3_0             | I                       | Signaling indication input pin 0 for channel 3                               |
| 62                                 | SI3_1             | I                       | Signaling indication input pin 1 for channel 3                               |
| 61                                 | SI3_2             | I                       | Signaling indication input pin 2 for channel 3                               |
| 4                                  | SO3_0             | O                       | Signaling command output pin 0 for channel 3                                 |
| 3                                  | SO3_1             | O                       | Signaling command output pin 1 for channel 3                                 |
| 2                                  | SO3_2             | O                       | Signaling command output pin 2 for channel 3                                 |
| 1                                  | SB3_0             | I/O                     | Bi-directional signal. command indication pin 0 for channel 3                |
| 64                                 | SB3_1             | I/O                     | Bi-directional signal. command indication pin 1 for channel 3                |
| <b>Specific Pins for Channel 4</b> |                   |                         |                                                                              |
| 11                                 | GNDA4             | I                       | Ground Analog for channel 4, not internally connected to GNDD or GNDA1,2,3   |
| 10                                 | V <sub>IN4</sub>  | I                       | Analog voice (voltage) input for channel 4                                   |
| 12                                 | V <sub>OUT4</sub> | O                       | Analog voice (voltage) output for channel 4                                  |
| 18                                 | SI4_0             | I                       | Signaling indication input pin 0 for channel 4                               |
| 19                                 | SI4_1             | I                       | Signaling indication input pin 1 for channel 4                               |
| 20                                 | SI4_2             | I                       | Signaling indication input pin 2 for channel 4                               |
| 13                                 | SO4_0             | O                       | Signaling command output pin 0 for channel 4                                 |
| 14                                 | SO4_1             | O                       | Signaling command output pin 1 for channel 4                                 |
| 15                                 | SO4_2             | O                       | Signaling command output pin 2 for channel 4                                 |
| 16                                 | SB4_0             | I/O                     | Bi-directional signal. command indication pin 0 for channel 4                |
| 17                                 | SB4_1             | I/O                     | Bi-directional signal. command indication pin 1 for channel 4                |

## 2 Functional Description

### 2.1 SICOFI-4 Principles

The change from 2  $\mu\text{m}$  to 1  $\mu\text{m}$  CMOS process requires new concepts in the realization of the analog functions. High performance (in the terms of gain, speed, stability...) 1  $\mu\text{m}$  CMOS devices can not withstand more than 5.5 V of supply-voltage. On that account the negative supply voltage  $V_{SS}$  of the previous SICOFI<sup>®</sup>s will be omitted. This is a benefit for the user but it makes a very high demand on the analog circuitry.

ADC and DAC are changed to Sigma-Delta-concepts to fulfill the stringent requirements on the dynamic parameters.

Using 1  $\mu\text{m}$  CMOS does not only lend to problems – it is the only acceptable solution in terms of area and power consumption for the integration of more then two SICOFI channels on a single chip.

It is rather pointless to implement 4 codec-filter-channels on one chip with pure analog circuitry. The use of a DSP-concept (the SICOFI<sup>®</sup> and the SICOFI<sup>®</sup>-2-approach) for this function seems to be a must for an adequate four channel architecture.

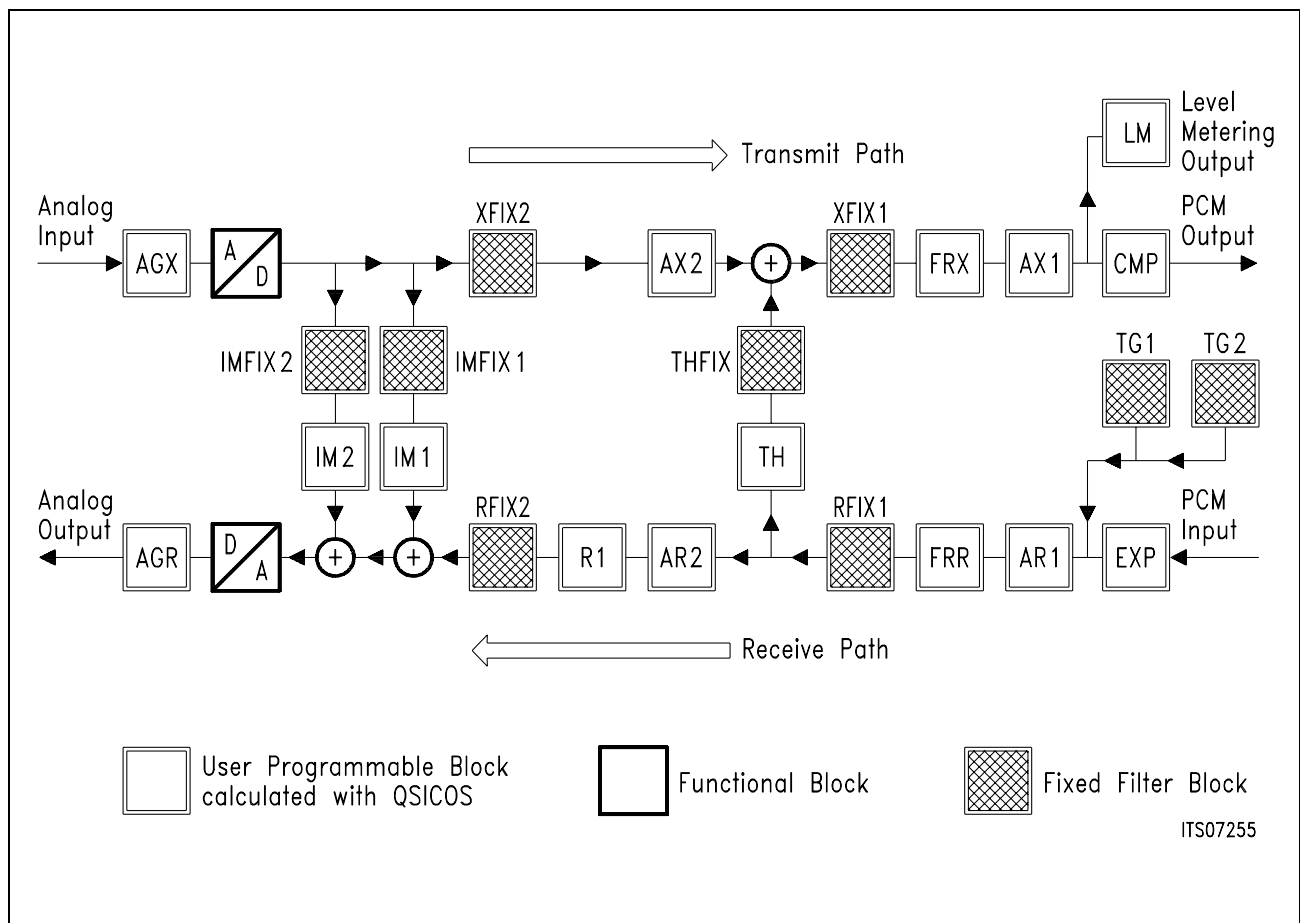


**Figure 2 SICOFI-4 Signal Flow Graph (for either channel)**

### **Transmit Path**

The analog input signal has to be DC-free connected by an external capacitor because there is an internal virtual reference ground potential. After passing a simple antialiasing prefilter (PREFI) the voice signal is converted to a 1-bit digital data stream in the Sigma-Delta-converter. The first downsampling steps are done in fast running digital hardware filters. The following steps are implemented in the micro-code which has to be executed by the central Digital Signal Processor. This DSP-machine is able to handle the workload for all four channels. At the end the fully processed signal (flexibly programmed in many parameters) is transferred to the IOM-2 interface in a PCM-compressed signal representation.

### **Receive Path**

The digital input signal is received via the IOM-2 interface. Expansion, PCM-Law-pass-filtering, gain correction and frequency response correction are the next steps which are done by the DSP-machine. The upsampling interpolation steps are again processed by fast hardware structures to reduce the DSP-workload. The upsampled 1-bit data stream is then converted to an analog equivalent which is smoothed by a POST-Filter (POFI). As the signal  $V_{OUT}$  is also referenced to an internal virtual ground potential, an external capacitor is required for DC-decoupling.

### **Loops**

There are two loops implemented. The first is to generate the AC-input impedance (IM) and the second is to perform a proper hybrid balancing (TH). A simple extra path IM2 (from the transmit to the receive path) supports the impedance matching function.

### **Test Features**

There are four analog and five digital test loops implemented in the SICOFI-4. For special tests it is possible to 'Cut Off' the receive and the transmit path at two different points.

## Functional Description

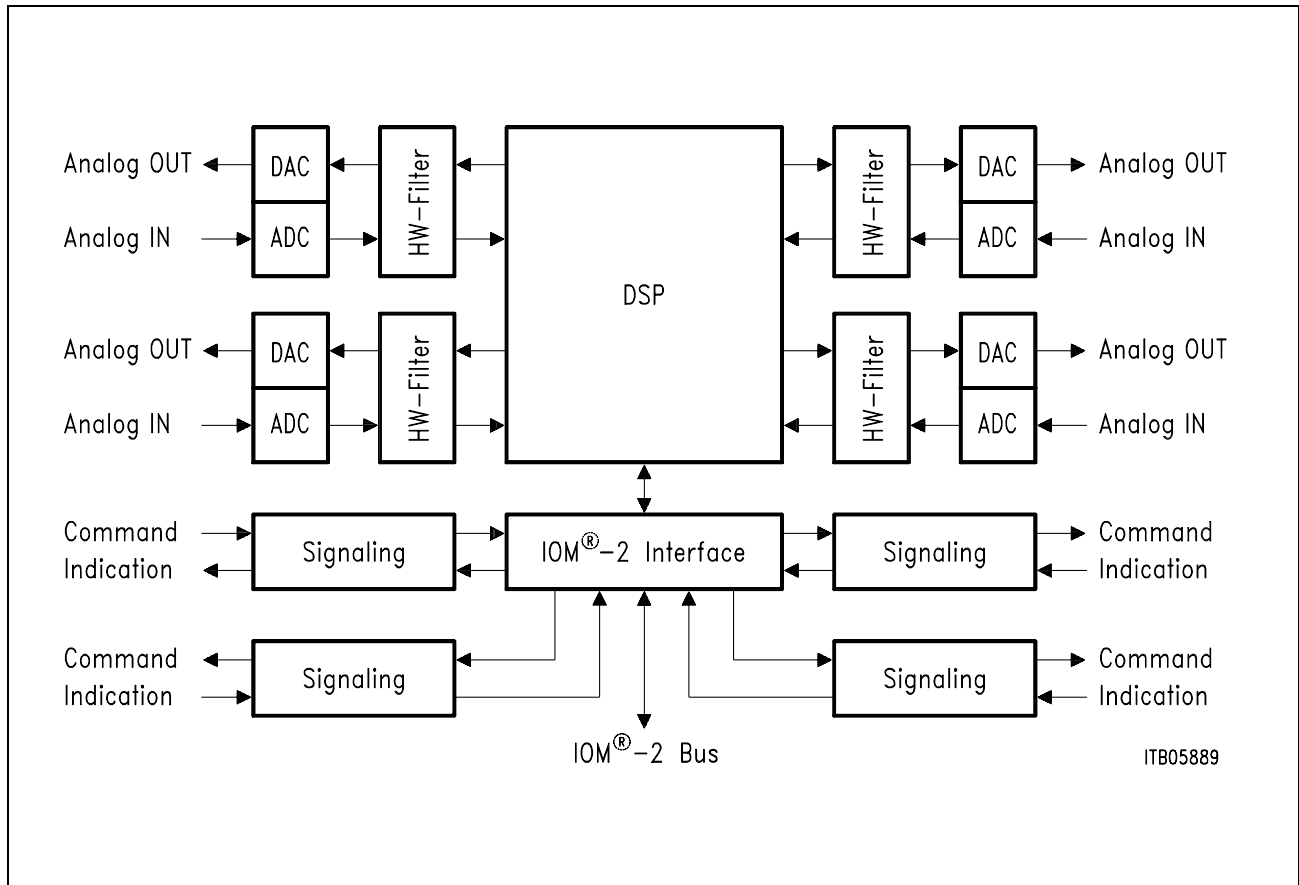


**Figure 3 SICOFI-4 Block Diagram**

The SICOFI-4 bridges the gap between analog and digital voice signal transmission in modern telecommunication systems. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) provide the required conversion accuracy. Analog antialiasing prefilters (PREFI) and smoothing postfilters (POFI) are included. The connection between the ADC and the DAC (with high sampling rate) and the DSP, is done by specific Hardware Filters, for filtering like interpolation and decimation. The dedicated Digital Signal Processor (DSP) handles all the algorithms necessary e.g. for PCM bandpass filtering, sample rate conversion and PCM companding. The IOM-2 Interface handles digital voice transmission, SICOFI-4 feature control and transparent access to the SICOFI-4 command and indication pins. To program the filters, precalculated sets of coefficients are downloaded from the system to the on chip coefficient ram (CRAM).

## 2.2 IOM-2 Interface

The IOM-2 Interface consists of two data lines and two clock lines. DU (data upstream) carries data from the SICOFI-4 to a master device. This master device performs the interface between the PCM-backplane, the  $\mu$ -controller and up to 24 SICOFI-4's. DD (data downstream) carries data from the master device to the SICOFI-4. A frame synchronization clock signal (8 kHz, FSC) as well as a data clock signal (2048 kHz or 4096 kHz DCL) has to be supplied to the SICOFI-4. The SICOFI-4 handles data as described in the IOM-2 specification for analog devices.

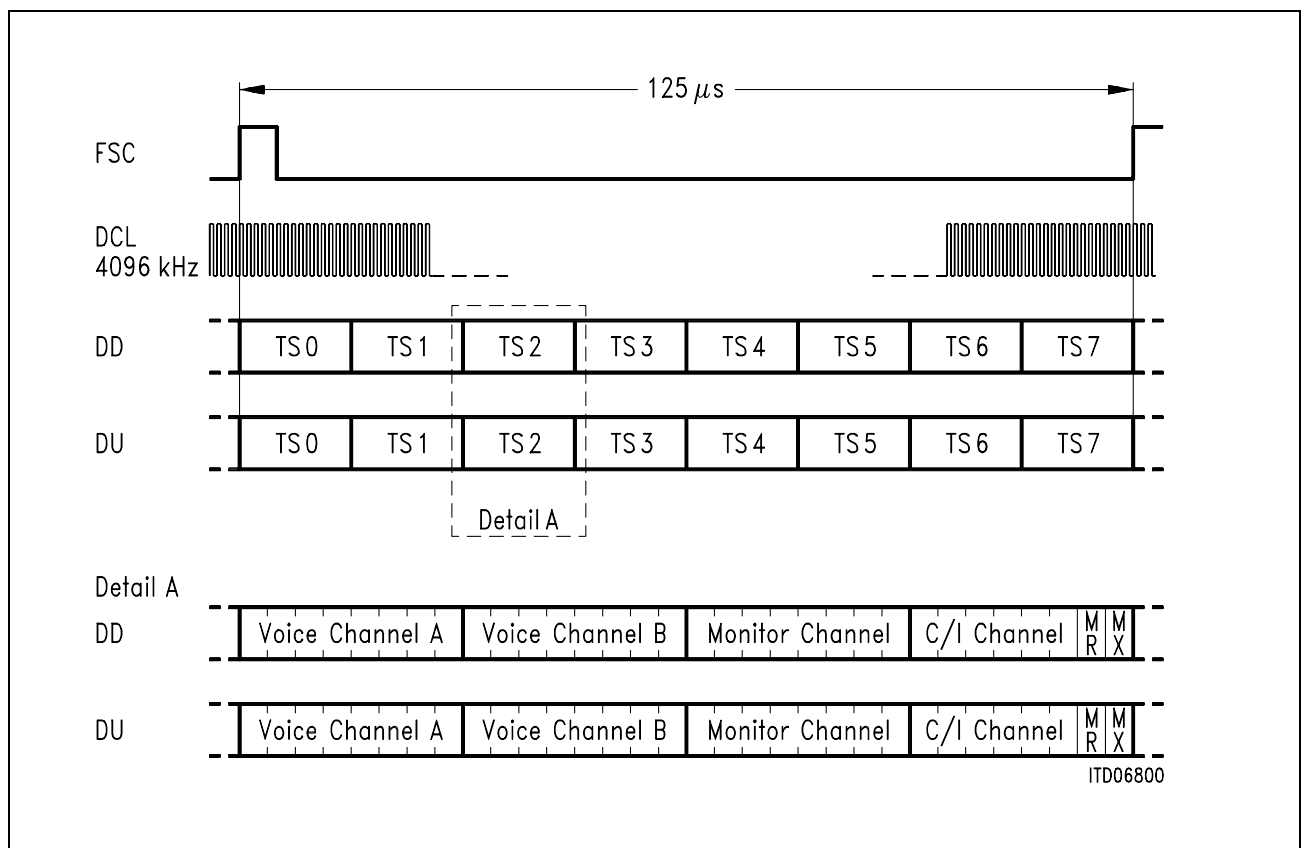


**Figure 4 IOM-2 Interface Timing for 16 Voice Channels (per 8 kHz frame)**

## Functional Description

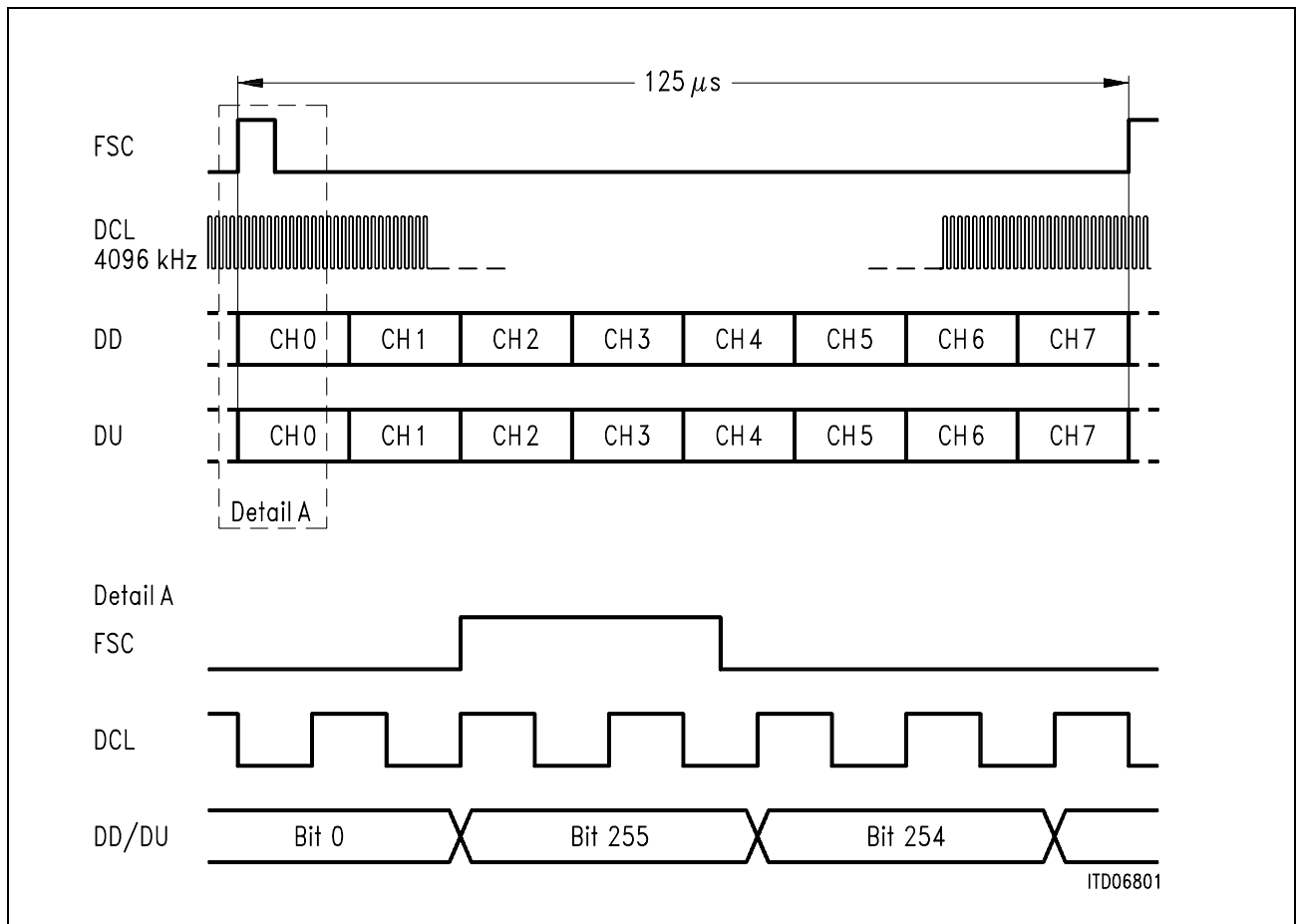


**Figure 5 IOM-2 Interface Timing (DCL=4096 kHz, MODE=1, per 8 kHz frame)**

## Functional Description

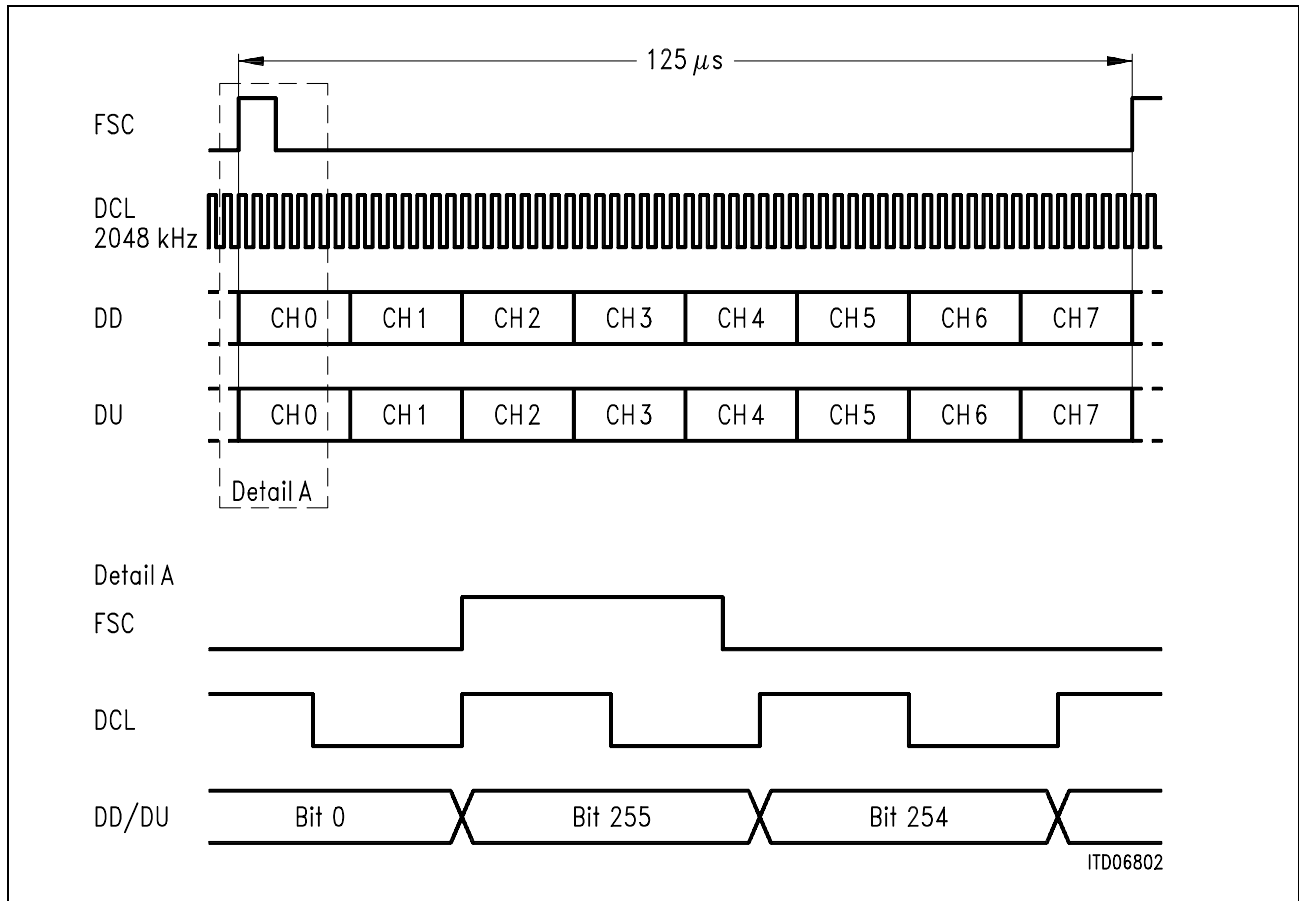


**Figure 6 IOM-2 Interface Timing (DCL = 2048 kHz, MODE = 0)**

### IOM-2 Timeslot Selection

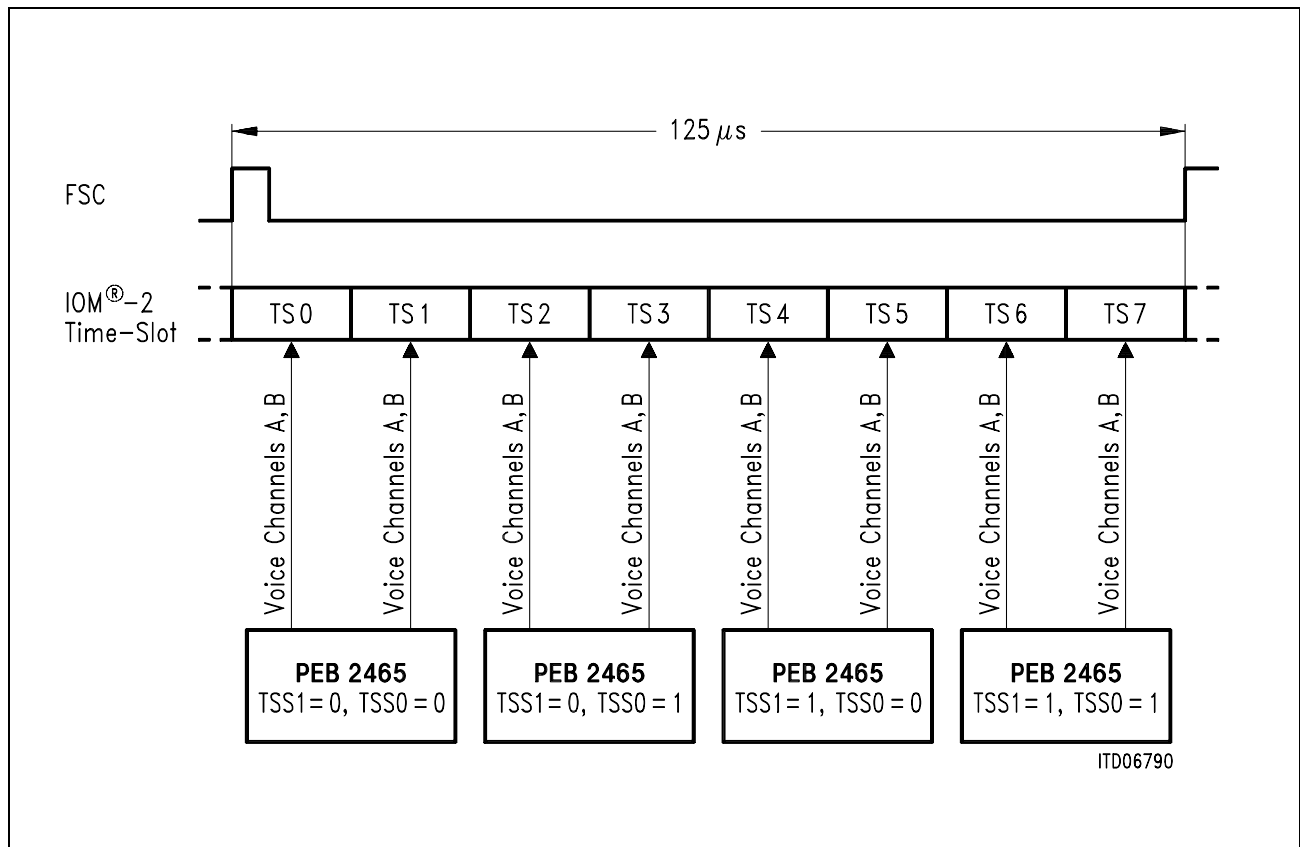
The four channels of each SICOFI-4 can be assigned to 4 pairs of timeslots by pin-strapping the pins TSS0 and TSS1. (TS0 + TS1, TS2 + TS3, TS4 + TS5, TS6 + TS7). The IOM-2 operating mode is selected by the MODE pin.

**Table 2 IOM-2 Timeslot Selection**

| TSS1 | TSS0 | MODE | IOM-2 Operating Mode           |
|------|------|------|--------------------------------|
| 0    | 0    | 1    | Timeslot 0 + 1; DCL = 4096 kHz |
| 0    | 1    | 1    | Timeslot 2 + 3; DCL = 4096 kHz |
| 1    | 0    | 1    | Timeslot 4 + 5; DCL = 4096 kHz |
| 1    | 1    | 1    | Timeslot 6 + 7; DCL = 4096 kHz |
| 0    | 0    | 0    | Timeslot 0 + 1; DCL = 2048 kHz |
| 0    | 1    | 0    | Timeslot 2 + 3; DCL = 2048 kHz |
| 1    | 0    | 0    | Timeslot 4 + 5; DCL = 2048 kHz |
| 1    | 1    | 0    | Timeslot 6 + 7; DCL = 2048 kHz |

## Functional Description

Each IOM-timeslot contains 2 voice channels (A and B). Those two voice channels share a common IOM-Monitor-byte as well as a common C/I-byte. The AD-bit in the Monitor command defines which of the two voice channels should be affected (programmed). (For more information on IOM-2 specific Monitor Channel Data Structure see appendix, [Page 64](#)).



| SICOFI-4 Channels | TSS1 = 0, TSS0 = 0 |               | TSS1 = 0, TSS0 = 1 |               | TSS1 = 1, TSS0 = 0 |               | TSS1 = 1, TSS0 = 1 |               |
|-------------------|--------------------|---------------|--------------------|---------------|--------------------|---------------|--------------------|---------------|
|                   | TS                 | Voice Channel | TS                 | Voice Channel | TS                 | Voice Channel | TS                 | Voice Channel |
| 1                 | TS0                | A             | TS2                | A             | TS4                | A             | TS6                | A             |
| 2                 | TS0                | B             | TS2                | B             | TS4                | B             | TS6                | B             |
| 3                 | TS1                | A             | TS3                | A             | TS5                | A             | TS7                | A             |
| 4                 | TS1                | B             | TS3                | B             | TS5                | B             | TS7                | B             |

In the following sections, only SICOFI-4 channels 1 and 2 are discussed. Channel 3 and channel 4 behave accordingly.

### 3 Programming the SICOFI-4

With the appropriate commands, the SICOFI-4 can be programmed and verified very flexibly via the IOM-2 Interface monitor channel.

Data transfer to the SICOFI-4 starts with a SICOFI-specific address byte (81<sub>H</sub>).

With the second byte one of 3 different types of commands (SOP, XOP and COP) is selected. Each of those can be used as a write or read command. Due to the extended SICOFI-4 feature control facilities, SOP, COP and XOP commands contain additional information (e.g. number of subsequent bytes) for programming (write) and verifying (read) the SICOFI-4 status.

A write command is followed by up to 8 bytes of data. The SICOFI-4 responds to a read command with its IOM-2 specific address and the requested information, that is up to 8 bytes of data (see Programming Procedure, [Page 66](#)).

**Attention:** Each byte on the monitor channel, has to be sent twice at least, according to the IOM-2 Monitor handshake procedure. (For more information on IOM-2 specific Monitor Channel Data Structure see appendix, [Page 64](#)).

### 3.1 Types of Monitor Bytes

The 8-bit Monitor bytes have to be interpreted as either commands or status information stored in Configuration Registers or the Coefficient Ram. There are three different types of SICOFI-4 commands which are selected by bit 3 and 4 as shown below.

**SOP**                      **STATUS OPERATION:**                      **SICOFI-4** status setting/monitoring

|     |   |   |   |   |   |   |   |   |
|-----|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|     |   |   |   | 1 | 0 |   |   |   |

**XOP**                      **EXTENDED OPERATION:**                      C/I channel configuration/evaluation

|     |   |   |   |   |   |   |   |   |
|-----|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|     | X |   |   | 1 | 1 |   |   |   |

**COP**                      **COEFFICIENT OPERATION:**                      filter coefficient setting/monitoring

|     |   |   |   |   |   |   |   |   |
|-----|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|     |   |   |   | 0 |   |   |   |   |

### 3.2 Storage of Programming Information

4 configuration registers per channel:CR1, CR2, CR3, CR4 accessed by SOP commands

4 common configuration registers:XR1, XR2, XR3 and XR4 accessed by XOP commands (the contents are valid for two voice channels i.e. 1 IOM-2 timeslot)

1 Coefficient RAM per channel:CRAM accessed by COP commands

### 3.3 SICOFI-4 Commands

#### 3.3.1 SOP – Write Commands

| DD               | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|------------------|------|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----|
| Address          | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |    |
| SOP-Write 1 Byte |      | 0 |   | 1 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |    |
| CR1              | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |

| DD                | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|-------------------|------|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----|
| Address           | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |    |
| SOP-Write 2 Bytes |      | 0 |   | 1 | 0 | 0 | 1 | 0 |     | Idle |   |   |   |   |   |   |   |    |
| CR2               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| CR1               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |

| DD                | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|-------------------|------|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----|
| Address           | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |    |
| SOP-Write 3 Bytes |      | 0 |   | 1 | 0 | 0 | 1 | 1 |     | Idle |   |   |   |   |   |   |   |    |
| CR3               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| CR2               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| CR1               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |

| DD                | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|-------------------|------|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----|
| Address           | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |    |
| SOP-Write 4 Bytes |      | 0 |   | 1 | 0 | 1 | 0 | 0 |     | Idle |   |   |   |   |   |   |   |    |
| CR4               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| CR3               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| CR2               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| CR1               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |

### 3.3.2 XOP – Write Commands

| DD                | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|-------------------|------|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----|
| Address           | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |    |
| XOP-Write 2 Bytes |      | 0 |   | 1 | 1 | 0 | 1 | 0 |     | Idle |   |   |   |   |   |   |   |    |
| XR2               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| XR1               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |

| DD                | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|-------------------|------|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----|
| Address           | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |    |
| XOP-Write 3 Bytes |      | 0 |   | 1 | 1 | 0 | 1 | 0 |     | Idle |   |   |   |   |   |   |   |    |
| XR3               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| XR2               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| XR1               | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |

### 3.3.3 COP – Write Commands

| DD                | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|-------------------|------|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----|
| Address           | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |    |
| COP-Write 4 Bytes |      | 0 |   | 0 | 1 |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 4          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 3          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 2          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 1          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |

| DD                | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU |
|-------------------|------|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----|
| Address           | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |    |
| COP-Write 8 Bytes |      | 0 |   | 0 | 0 |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 8          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 7          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 6          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 5          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 4          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 3          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 2          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |
| Coeff. 1          | Data |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |    |

### 3.3.4 SOP – Read Commands

| DD              | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU      |
|-----------------|---|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|---------|
| Address         | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |         |
| SOP-Read 1 Byte |   | 1 |   | 1 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |         |
|                 |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                 |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                 |   |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
|                 |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR1     |

| DD               | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU      |
|------------------|---|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|---------|
| Address          | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |         |
| SOP-Read 2 Bytes |   | 1 |   | 1 | 0 | 0 | 1 | 0 |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR2     |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR1     |

| DD               | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU      |
|------------------|---|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|---------|
| Address          | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |         |
| SOP-Read 3 Bytes |   | 1 |   | 1 | 0 | 0 | 1 | 1 |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR3     |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR2     |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR1     |

| DD               | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU      |
|------------------|---|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|---------|
| Address          | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |         |
| SOP-Read 4 Bytes |   | 1 |   | 1 | 0 | 1 | 0 | 0 |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR4     |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR3     |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR2     |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR1     |

### 3.3.5 XOP – Read Commands

| DD              | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU      |
|-----------------|---|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|---------|
| Address         | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |         |
| XOP-Read 1 Byte |   | 1 |   | 1 | 1 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |         |
|                 |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                 |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                 |   |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
|                 |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | XR1     |

| DD               | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU      |
|------------------|---|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|---------|
| Address          | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |         |
| XOP-Read 2 Bytes |   | 1 |   | 1 | 1 | 0 | 1 | 0 |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | XR2     |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | XR1     |

| DD               | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU      |
|------------------|---|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|---------|
| Address          | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |         |
| XOP-Read 3 Bytes |   | 1 |   | 1 | 1 | 0 | 1 | 1 |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |         |
|                  |   |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | XR3     |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | XR2     |
|                  |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | XR1     |

### 3.3.6 COP – Read Commands

| DD               | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU       |         |
|------------------|------|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----------|---------|
| Address          | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |          |         |
| COP-Read 4 Bytes |      | 1 |   | 0 | 1 |   |   |   |     | Idle |   |   |   |   |   |   |   |          |         |
|                  | Idle |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1        | Address |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 4 |         |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 3 |         |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 2 |         |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 1 |         |

| DD               | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU       |         |
|------------------|------|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----------|---------|
| Address          | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |          |         |
| COP-Read 8 Bytes |      | 1 |   | 0 | 0 |   |   |   |     | Idle |   |   |   |   |   |   |   |          |         |
|                  | Idle |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1        | Address |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 8 |         |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 7 |         |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 6 |         |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 5 |         |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 4 |         |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 3 |         |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 2 |         |
|                  | Idle |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 1 |         |

### 3.3.7 Example for a Mixed Command

| DD                | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Bit | 7    | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DU       |
|-------------------|---|---|---|---|---|---|---|---|-----|------|---|---|---|---|---|---|---|----------|
| Address           | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |          |
| SOP-Write 4 Bytes |   | 0 |   | 1 | 0 | 1 | 0 | 0 |     | Idle |   |   |   |   |   |   |   |          |
| CR4               |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| CR3               |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| CR2               |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| CR1               |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| XOP-Write 2 Bytes |   | 0 |   | 1 | 1 | 0 | 1 | 0 |     | Idle |   |   |   |   |   |   |   |          |
| XR2               |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| XR1               |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| COP-Write 4 Bytes |   | 0 |   | 0 | 1 |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| Coeff. 4          |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| Coeff. 3          |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| Coeff. 2          |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| Coeff. 1          |   |   |   |   |   |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
| SOP-Read 3 Bytes  |   | 1 |   | 1 | 0 | 0 | 1 | 1 |     | Idle |   |   |   |   |   |   |   |          |
|                   |   |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address  |
|                   |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR3      |
|                   |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR2      |
|                   |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | CR1      |
| Address           | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |     | Idle |   |   |   |   |   |   |   |          |
| COP-Read 4 Bytes  |   | 1 |   | 0 | 1 |   |   |   |     | Idle |   |   |   |   |   |   |   |          |
|                   |   |   |   |   |   |   |   |   |     | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address  |
|                   |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 4 |
|                   |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 3 |
|                   |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 2 |
|                   |   |   |   |   |   |   |   |   |     | Data |   |   |   |   |   |   |   | Coeff. 1 |

**Programming the SICOFI-4**

|                 |      |   |   |   |   |   |   |   |
|-----------------|------|---|---|---|---|---|---|---|
| Address         | 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| XOP-Read 1 Byte |      | 1 |   | 1 | 1 | 0 | 0 | 1 |
|                 | Idle |   |   |   |   |   |   |   |
|                 | Idle |   |   |   |   |   |   |   |

|      |   |   |   |   |   |   |   |         |
|------|---|---|---|---|---|---|---|---------|
| Idle |   |   |   |   |   |   |   |         |
| Idle |   |   |   |   |   |   |   |         |
| 1    | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Address |
| Data |   |   |   |   |   |   |   | XR1     |

### 3.4 SOP Command

To modify or evaluate the SICOFI-4 status, the contents of up to four configuration registers CR1, CR2, CR3 and CR4 may be transferred to or from the SICOFI-4. This is started by a SOP-Command (status operation command).

| Bit | 7  | 6  | 5     | 4 | 3 | 2     | 1     | 0     |
|-----|----|----|-------|---|---|-------|-------|-------|
|     | AD | RW | PWRUP | 1 | 0 | LSEL2 | LSEL1 | LSEL0 |

**AD** Address Information

AD = 0 SICOFI-4 channel 1(3) is addressed with this command

AD = 1 SICOFI-4 channel 2(4) is addressed with this command

**RW** Read/Write Information: Enables reading from the SICOFI-4 or writing information to the SICOFI-4

RW = 0 Write to SICOFI-4

RW = 1 Read from SICOFI-4

**PWRUP** Power Up / Power Down

PWRUP = 1 sets the assigned channel (see bit AD) of SICOFI-4 to power-up (operating mode)

PWRUP = 0 resets the assigned channel of SICOFI-4 to power-down (standby mode)

**LSEL** Length select information (see also Programming Procedure, [Page 66](#))

This field identifies the number of subsequent data bytes

LSEL = 000 0 bytes of data are following

LSEL = 001 1 byte of data is following (CR1)

LSEL = 010 2 bytes of data are following (CR2, CR1)

LSEL = 011 3 bytes of data are following (CR3, CR2, CR1)

LSEL = 100 4 bytes of data are following (CR4, CR3, CR2, CR1)

All other codes are reserved for future use!

It is possible to program each Configuration register separately, just by putting only one byte into the FIFO of the upstream master device (e.g. EPIC), and aborting after transmission of one (or n) byte.

### 3.4.1 CR1 Configuration Register 1

Configuration register CR1 defines the basic SICOFI-4 settings, which are: enabling/disabling the programmable digital filters and tone generators.

| Bit | 7  | 6     | 5   | 4   | 3  | 2  | 1    | 0    |
|-----|----|-------|-----|-----|----|----|------|------|
|     | TH | IM/R1 | FRX | FRR | AX | AR | ETG2 | ETG1 |

|              |                                                                                                                                                                  |
|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>TH</b>    | Enable TH- (TransHybrid Balancing) Filter<br>TH = 0: TH-filter disabled<br>TH = 1: TH-filter enabled                                                             |
| <b>IM/R1</b> | Enable IM-(Impedance Matching) Filter and R1-Filter<br>IM/R1 = 0: IM-filter and R1-filter disabled<br>IM/R1 = 1: IM-filter and R1-filter enabled                 |
| <b>FRX</b>   | Enable FRX (Frequency Response Transmit)-Filter<br>FRX = 0: FRX-filter disabled<br>FRX = 1: FRX-filter enabled                                                   |
| <b>FRR</b>   | Enable FRR (Frequency Response Receive)-Filter<br>FRR = 0: FRR-filter disabled<br>FRR = 1: FRR-filter enabled                                                    |
| <b>AX</b>    | Enable AX-(Amplification/Attenuation Transmit) Filter<br>AX = 0: AX-filter disabled<br>AX = 1: AX-filter enabled                                                 |
| <b>AR</b>    | Enable AR-(Amplification/Attenuation Receive) Filter<br>AR = 0: AR-filter disabled<br>AR = 1: AR-filter enabled                                                  |
| <b>ETG2</b>  | Enable programmable tone generator 2 <sup>1)</sup><br>ETG2 = 0 : programmable tone generator 2 is disabled<br>ETG2 = 1: programmable tone generator 2 is enabled |
| <b>ETG1</b>  | Enable programmable tone generator 1<br>ETG1 = 0 : programmable tone generator 1 is disabled<br>ETG1 = 1: programmable tone generator 1 is enabled               |

<sup>1)</sup> Tone generator 2 is not available if Level Metering Function is enabled!

### 3.4.2 CR2 Configuration Register 2

| Bit | 7      | 6 | 5  | 4   | 3   | 2   | 1    | 0    |
|-----|--------|---|----|-----|-----|-----|------|------|
|     | TH-Sel |   | LM | LMR | LAW | LIN | PTG2 | PTG1 |

**TH-Sel** 2 bit field to select one of four programmed TH-filter coefficient sets

TH-Sel = 0 0: TH-filter coefficient set 1 is selected

TH-Sel = 0 1: TH-filter coefficient set 2 is selected

TH-Sel = 1 0: TH-filter coefficient set 3 is selected

TH-Sel = 1 1: TH-filter coefficient set 4 is selected

**LM** Level Metering function<sup>1)</sup>

LM = 0 : level metering function is disabled

LM = 1: level metering function is enabled

**LMR** Result of Level Metering function (this bit can not be written)

LMR = 0: level detected was lower than the reference

LMR = 1: level detected was higher than the reference

**LAW** PCM - law selection

LAW = 0: A-Law is selected

LAW = 1:  $\mu$ -Law ( $\mu$ 255 PCM) is selected

**LIN** Linear mode selection

LIN = 0: PCM-mode is selected

LIN = 1: linear mode is selected<sup>2)</sup>

**PTG2** User programmed frequency or fixed frequency is selected

PTG2 = 0: fixed frequency for tone generator 2 is selected (1 kHz)

PTG2 = 1: programmed frequency for tone generator 2 is selected

**PTG1** User programmed frequency or fixed frequency is selected

PTG1 = 0: fixed frequency for tone generator 1 is selected (1 kHz)

PTG1 = 1: programmed frequency for tone generator 1 is selected

<sup>1)</sup> Explanation of the level metering function:

A signal fed to A/ $\mu$ -Law compression via AX- and HPX-filters (from a digital loop, or externally via  $V_{IN}$ ), is rectified, and the power is measured. If the power exceeds a certain value, loaded to XR4, bit LMR is set to '1'. The power of the incoming signal can be adjusted by AX-filters.

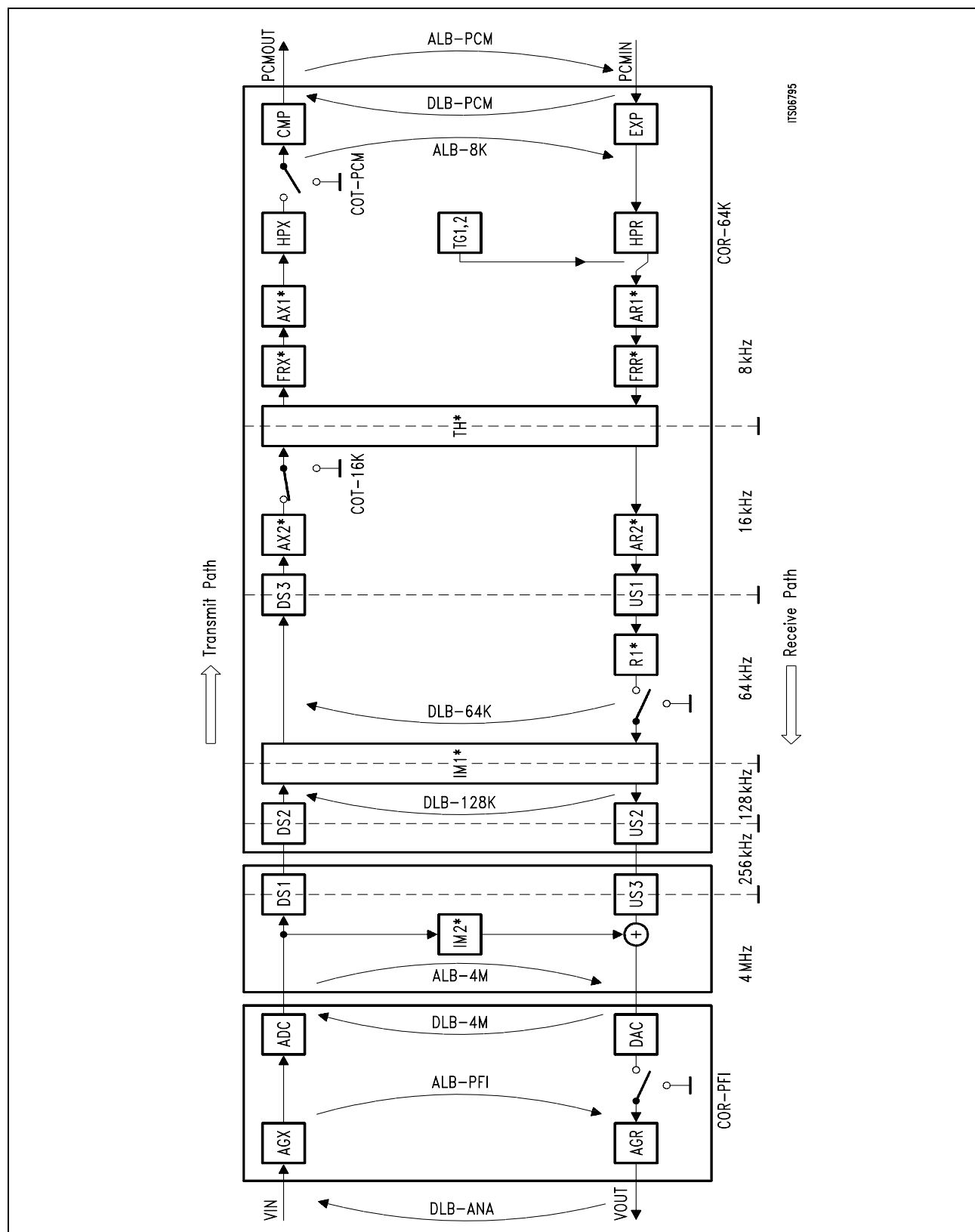
<sup>2)</sup> During Linear operation only one 16 bit voice channel, is available per timeslot. Depending on the address bit (AD) the voice-data of channel 1 or 2 is transmitted. The other voice channel is not available during this time.

### 3.4.3 CR3 Configuration Register 3

| Bit | 7     | 6 | 5 | 4 | 3   | 2       | 1 | 0 |
|-----|-------|---|---|---|-----|---------|---|---|
|     | COT/R |   |   | 0 | IDR | Version |   |   |

|                |                                                                |  |  |  |  |  |  |  |
|----------------|----------------------------------------------------------------|--|--|--|--|--|--|--|
| <b>COT/R</b>   | Selection of Cut of Transmit/Receive Paths                     |  |  |  |  |  |  |  |
|                | 0 0 0: Normal Operation                                        |  |  |  |  |  |  |  |
| Filter)        | 0 0 1: COT_16KCut Off Transmit Path at 16 kHz (input of TH-    |  |  |  |  |  |  |  |
|                | 0 1 0: COT_PCMLCut Off Transmit Path at 8 kHz (input of        |  |  |  |  |  |  |  |
|                | compression) (output is zero for $\mu$ -law                    |  |  |  |  |  |  |  |
|                | and linear mode, 1 LSB for A-law)                              |  |  |  |  |  |  |  |
|                | 1 0 1: COR_PFI Cut Off Receive Path at 4 MHz (POFI-output)     |  |  |  |  |  |  |  |
|                | 1 1 0: COR_64KCut Off Receive Path at 64 kHz (IM-filter input) |  |  |  |  |  |  |  |
| <b>IDR</b>     | Initialize Data RAM                                            |  |  |  |  |  |  |  |
|                | IDR = 0: normal operation is selected                          |  |  |  |  |  |  |  |
|                | IDR = 1: contents of Data RAM is set to 0                      |  |  |  |  |  |  |  |
|                | (used for production test purposes)                            |  |  |  |  |  |  |  |
| <b>Version</b> | The Version number shows the actual design version of SICOFI-4 |  |  |  |  |  |  |  |
|                | (                                                              |  |  |  |  |  |  |  |
|                | 001 for PEB 2465 V1.1                                          |  |  |  |  |  |  |  |
|                | 010 for PEB 2465 V1.2                                          |  |  |  |  |  |  |  |
|                | 011 for PEB 2465 V2.1                                          |  |  |  |  |  |  |  |
|                | 100 for PEB 2465 V2.2 and V2.3)                                |  |  |  |  |  |  |  |

## CUT OFFs' and Loops'



### Figure 7 CUT OFFs and Loops

### 3.4.4 CR4 Configuration Register 4

| Bit | 7          | 6 | 5 | 4 | 3   | 2   | 1     | 0     |
|-----|------------|---|---|---|-----|-----|-------|-------|
|     | Test-Loops |   |   |   | AGX | AGR | D-HPX | D-HPR |

**Test-Loops** 4 bit field for selection of Analog and Digital Loop Backs

|          |          |                                                 |
|----------|----------|-------------------------------------------------|
| 0 0 0 0: |          | no loop back is selected (normal operation)     |
| 0 0 0 1: | ALB-PFI  | analog loop back via PREFI-POFI is selected     |
| 0 0 1 1: | ALB-4M   | analog loop back via 4 MHz is selected          |
| 0 1 0 0: | ALB-PCM  | analog loop back via 8 kHz (PCM) is selected    |
| 0 1 0 1: | ALB-8K   | analog loop back via 8 kHz (linear) is selected |
| 1 0 0 0: | DLB-ANA  | digital loop back via analog port is selected   |
| 1 0 0 1: | DLB-4M   | digital loop back via 4 MHz is selected         |
| 1 1 0 0: | DLB-128K | digital loop back via 128 kHz is selected       |
| 1 1 0 1: | DLB-64K  | digital loop back via 64 kHz is selected        |
| 1 1 1 1: | DLB-PCM  | digital loop back via PCM-registers is selected |

**AGX** Analog gain in transmit direction  
 AGX = 0: analog gain is disabled  
 AGX = 1: analog gain is enabled (6.02 dB amplification)

**AGR** Analog gain in receive direction  
 AGR = 0: analog gain is disabled  
 AGR = 1: analog gain is enabled (6.02 dB attenuation)

**D-HPX** Disable highpass in transmit direction  
 D-HPX = 0: transmit high pass is enabled  
 D-HPX = 1: transmit high pass is disabled<sup>1)</sup>

**D-HPR** Disable highpass in receive direction  
 D-HPR = 0: receive high pass is enabled  
 D-HPR = 1: receive high pass is disabled<sup>2)</sup>

<sup>1)</sup> In this case the transmit-path signal is attenuated 0.06 dB

<sup>2)</sup> In this case the receive-path signal is attenuated 0.12 dB

### 3.5 COP Command

With a COP Command coefficients for the programmable filters can be written to the SICOFI-4 Coefficient RAM or read from the Coefficient RAM via the IOM-2 interface for verification.

|     |    |    |     |   |       |       |       |       |
|-----|----|----|-----|---|-------|-------|-------|-------|
| Bit | 7  | 6  | 5   | 4 | 3     | 2     | 1     | 0     |
|     | AD | RW | RST | 0 | CODE3 | CODE2 | CODE1 | CODE0 |

#### **AD** Address

AD = 0 SICOFI-4 channel 1 (3) is addressed  
AD = 1 SICOFI-4 channel 2 (4) is addressed

#### **RW** Read/Write

RW = 0 Subsequent data is written to the SICOFI-4  
RW = 1 Read data from SICOFI-4

#### **RST** Reset

RST = 1 Reset SICOFI-4  
(same as RESET-pin, valid for all four channels)

#### **CODE** includes number of following bytes and filter-address

|      |                                 |                               |
|------|---------------------------------|-------------------------------|
| 0000 | TH-Filter coefficients (part 1) | (followed by 8 bytes of data) |
| 0001 | TH-Filter coefficients (part 2) | (followed by 8 bytes of data) |
| 0010 | TH-Filter coefficients (part3)  | (followed by 8 bytes of data) |
| 0100 | IM-Filter coefficients (part1)  | (followed by 8 bytes of data) |
| 0101 | IM-Filter coefficients (part2)  | (followed by 8 bytes of data) |
| 0110 | FRX-Filter coefficients         | (followed by 8 bytes of data) |
| 0111 | FRR-Filter coefficients         | (followed by 8 bytes of data) |
| 1000 | AX-Filter coefficients          | (followed by 4 bytes of data) |
| 1001 | AR-Filter coefficients          | (followed by 4 bytes of data) |
| 1100 | TG1-Filter coefficients         | (followed by 4 bytes of data) |
| 1101 | TG2-Filter coefficients         | (followed by 4 bytes of data) |

### 3.6 How to Program the Filter Coefficients

**TH-Filter:** Four sets of TH-filter coefficients can be loaded to the SICOFI-4. Each of the four sets can be selected for any of the four SICOFI-4 channels, by setting the value of TH-Sel in configuration register CR2. Coefficient set 1 is loaded to the SICOFI-4 via channel 1, set 2 is loaded via channel 2 and so on.

**AX, AR, IM,**

**FRX, FRR-Filter:** An individual coefficient set is available for each of the four channels

**Tone-generators:** An individual coefficient set is available for each of the four channels

An **independent set** of coefficients is available for all the four channels, for all the filters and Tone-Generators. So AX, AR, FRR, FRX, IM and TG1 and TG2 behave like AX and AR-filters in Version V1.\*.

The programming flexibility for the **TH-filter was not changed** from Version V1.\* to Version V2.\*. Four sets of TH-filter coefficients can be loaded to the SICOFI-4. Each of the four sets can be selected for any of the four SICOFI-4 channels, by setting the value of TH-SEL in configuration register CR2. Coefficients set #1 is loaded to the SICOFI-4 via channel 1, set #2 is loaded via channel 2 and so on.

*Note: After RESET coefficient set #1 is used for all of the four channels, as all bits in configuration register CR2 are set to '0'.*

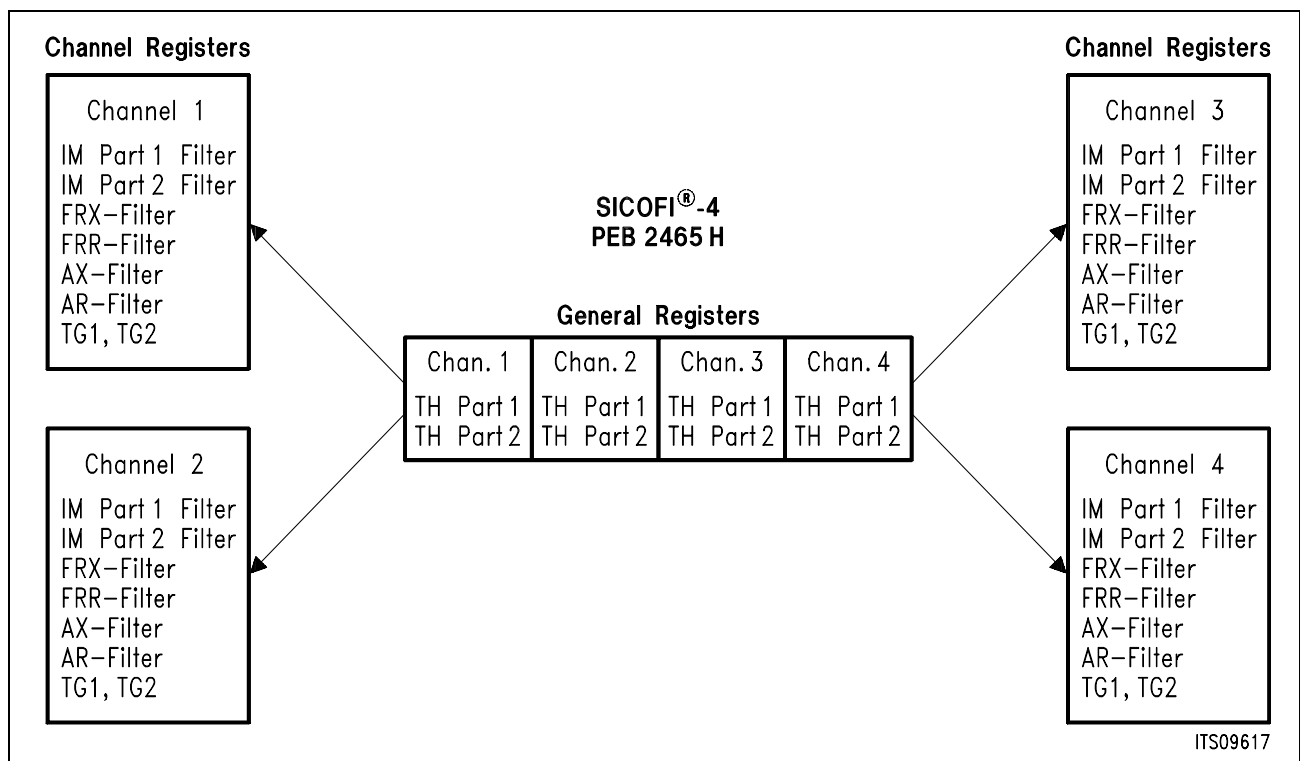


**Figure 8 Channel Registers**

### 3.7 XOP Command

With the XOP command the SICOFI-4 C/I channel is configured and evaluated. The XR registers are valid for two voice channels 1, 2 or 3, 4, depending on the selected IOM-2 timeslot<sup>1)</sup> (i.e. TS0+TS1: channel 1, 2 in TS0, channel 3, 4 in TS1).

| Bit | 7 | 6  | 5 | 4 | 3 | 2     | 1     | 0     |
|-----|---|----|---|---|---|-------|-------|-------|
|     | 0 | RW | 0 | 1 | 1 | LSEL2 | LSEL1 | LSEL0 |

**RW** Read / Write Information: Enables reading from the SICOFI-4 or writing information to the SICOFI-4

RW = 0 Write to SICOFI-4

RW = 1 Read from SICOFI-4

**LSEL** Length select information, for setting the number of subsequent data bytes

LSEL = 000 0 bytes of data are following

LSEL = 001 1 byte of data is following (XR1)

LSEL = 010 2 bytes of data are following (XR2, XR1)

LSEL = 011 3 bytes of data are following (XR3, XR2, XR1)

LSEL = 100 4 bytes of data are following (XR4, XR3, XR2, XR1)

#### 3.7.1 XR1 Extended Register 1<sup>2)</sup>

| Bit | 7        | 6        | 5                           | 4              | 3        | 2        | 1              | 0              |
|-----|----------|----------|-----------------------------|----------------|----------|----------|----------------|----------------|
|     | SB2[4]_1 | SB2[4]_0 | SI2[4]_0<br>3 <sup>3)</sup> | SI2[4]_0<br>3) | SB1[3]_1 | SB1[3]_0 | SI1[3]_0<br>3) | SI1[3]_0<br>3) |

**SB2[4]\_1** status of pin SB2[4]\_1 is transferred to the upstream master device

**SB2[4]\_0** status of pin SB2[4]\_0 is transferred to the upstream master device

**SI2[4]\_0** status of pin SI2[4]\_0 is transferred to the upstream master device

**SB1[3]\_1** status of pin SB1[3]\_1 is transferred to the upstream master device

**SB1[3]\_0** status of pin SB1[3]\_0 is transferred to the upstream master device

**SI1[3]\_0** status of pin SI1[3]\_0 is transferred to the upstream master device

<sup>1)</sup> IOM-2 timeslots TS0+TS1, TS2+TS3, TS4+TS5 or TS6+TS7, by pin-strapping the pins TSS0 and TSS1 (see pages <Fett>17 and <Fett>18)

<sup>2)</sup> Register XR1 can be read only.

<sup>3)</sup> Bits SI1[3]\_0 and SI2[4]\_0 have special meaning depending on contents of XR2 (see Page 35).

### 3.7.2 XR2 Extended Register 2

Register XR2 configures the data-upstream command/indication channel.

|     |   |   |   |   |   |   |   |   |
|-----|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|     | N |   |   |   | T |   |   |   |

#### Upstream Update Interval N

To restrict the rate of upstream C/I-bit changes, deglitching (persistence checking) of the status information from the SLIC may be applied. New status information will be transmitted upstream, after it has been stable for N milliseconds. N is programmable in the range of 1 to 15 ms in steps of 1 ms, with N = 0 the deglitching is disabled.

| Field N |   |   |   | Update Interval Time              |
|---------|---|---|---|-----------------------------------|
| 0       | 0 | 0 | 0 | Deglitching is disabled           |
| 0       | 0 | 0 | 1 | Upstream transmission after 1 ms  |
| 0       | 0 | 1 | 0 | Upstream transmission after 2 ms  |
| .       | . | . | . | .                                 |
| .       | . | . | . | .                                 |
| 1       | 1 | 1 | 0 | Upstream transmission after 14 ms |
| 1       | 1 | 1 | 1 | Upstream transmission after 15 ms |

#### Detector Select Sampling Interval T

SLICs with multiplexed loop- and ground-key-status, which have a single status output pin for carrying the loop- and ground-key-status information, need a special detector select input.

| Field T |   |   |   | Time Interval T between Detector Selected High States       |
|---------|---|---|---|-------------------------------------------------------------|
| 0       | 0 | 0 | 0 | Detector select output LGKM0,1 program. to 0 permanently    |
| 0       | 0 | 0 | 1 | Time interval T is 1 ms                                     |
| 0       | 0 | 1 | 0 | Time interval T is 2 ms                                     |
| .       | . | . | . | .                                                           |
| .       | . | . | . | .                                                           |
| 1       | 1 | 1 | 0 | Time interval T is 14 ms                                    |
| 1       | 1 | 1 | 1 | Detector select output LGKM0,1 is program. to 1 permanently |

LGKM0[1] is detector select output for channel 1[3] and 2[4]

## SLICs with Multiplexed Loop/Ground Key Detect

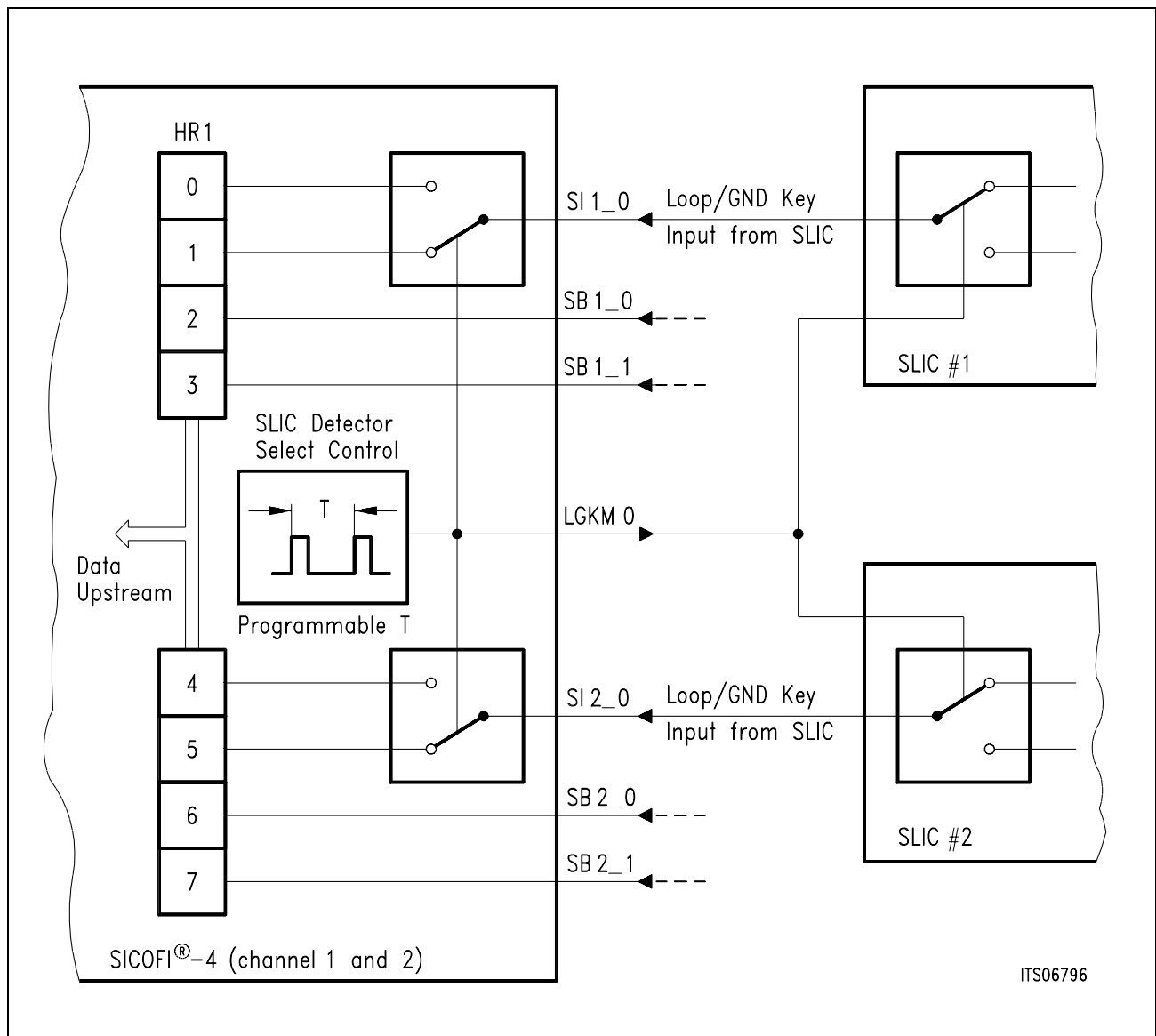


**Figure 9 SLICs with Multiplexed Loop/Ground Key Detect**

SICOFI-4 pins LGKM0,[1] are detector select outputs. These command output pins are normally set to logical '0', such that the SLIC outputs loop status, which is passed to XR1 - bits 0 and 4 via indication pins SI1\_0 and SI2\_0.

Every T milliseconds, the detector select outputs change to logical '1' for a time of 125  $\mu$ s (Period FSC). During this time the ground key status is read from the SLIC and transferred upstream using XR1 - bits 1 and 5 via indication pins SIx\_0 and SIy\_0.

The time interval T is programmable from 1 ms to 14 ms in 1 ms steps. It is possible to program the output to be permanently logical '0' or '1'.

### 3.7.3 XR3 Extended Register 3

This register controls the direction of the programmable C/I pins.

| Bit | 7             | 6             | 5 | 4 | 3             | 2             | 1 | 0 |
|-----|---------------|---------------|---|---|---------------|---------------|---|---|
|     | PSB2[4]<br>_1 | PSB2[4]<br>_0 | 0 | 0 | PSB1[3]<br>_1 | PSB1[3]<br>_0 | 0 | 0 |

**PSB2[4]\_1** Programmable bi-directional C/I pin SB2[4]\_1 is programmed

PSB2[4]\_1 = 0: pin SB2[4]\_1 is indication input

PSB2[4]\_1 = 1: pin SB2[4]\_1 is command output

**PSB2[4]\_0** Programmable bi-directional C/I pin SB2[4]\_0 is programmed

PSB2[4]\_0 = 0: pin SB2[4]\_0 is indication input

PSB2[4]\_0 = 1: pin SB2[4]\_0 is command output

**PSB1[3]\_1** Programmable bi-directional C/I pin SB1[3]\_1 is programmed

PSB1[3]\_1 = 0: pin SB1[3]\_1 is indication input

PSB1[3]\_1 = 1: pin SB1[3]\_1 is command output

**PSB1[3]\_0** Programmable bi-directional C/I pin SB1[3]\_0 is programmed

PSB1[3]\_0 = 0: pin SB1[3]\_0 is indication input

PSB1[3]\_0 = 1: pin SB1[3]\_0 is command output

### 3.7.4 XR4 Extended Register 4

This register holds the offset value for the level metering function. It is only available via the first used timeslot.

| Bit | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     | OF7 | OF6 | OF5 | OF4 | OF3 | OF2 | OF1 | OF0 |

## **4 SLIC Interface**

The signaling connection between SICOFI-4 and a SLIC is performed by the SICOFI-4 command/indication pins. Data received from the downstream C/I byte are inverted and transferred to command output pins (SB, SO). Data on input pins (SI, SB) are inverted and transferred to the upstream C/I-byte.

### **4.1 IOM-2 Interface Command/Indication Byte**

The SICOFI-4 offers a 8 pin parallel command/indication SLIC interface per channel

**Indication input pins:** Slx\_0, Slx\_1 Slx\_2

**Command output pins:** SOx\_0, SOx\_1, SOx\_2

**Program. command/indication pins:** SBx\_0, SBx\_1 (with x: 1 ... 4)

Data present at Slx\_0, Slx\_1, Slx\_2 and SBx\_0, SBx\_1 (if programmed as input) are sampled, inverted and transferred upstream. Data received downstream from IOM-2 interface are latched, inverted and fed to SOx\_0, SOx\_1, SOx\_2 and SBx\_0, SBx\_1 (if output).

## 4.2 Data-downstream C/I Channel Byte Format (receive)

The IOM-2 channel contains 6 bits (for two voice channels) in both directions for analog devices like the SICOFI-4. As the SICOFI-4 has up to five command output pins per channel (depending on XR3) it is not possible to send commands to all pins at a time. So C/I-channel bit 5 is used as an address bit to select the channel for the command data on C/I-channel bits 4 ... 0.

General Case:

| Bit | 5  | 4     | 3     | 2     | 1     | 0     |
|-----|----|-------|-------|-------|-------|-------|
|     | AD | SBx_1 | SBx_0 | SOx_2 | SOx_1 | SOx_0 |

Example for SICOFI-4 channels 1 and 2 (IOM-2 timeslot 0):

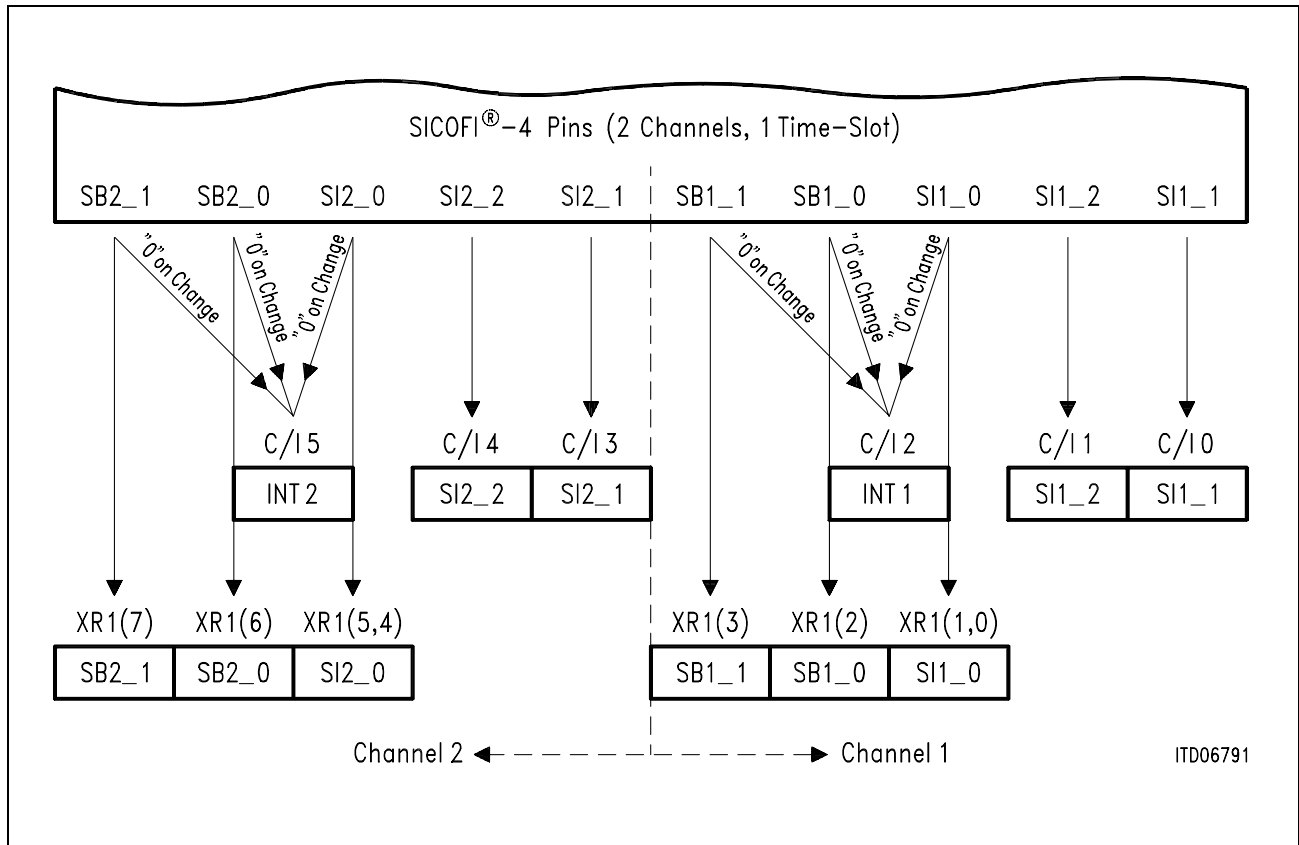
## 4.3 Data Upstream C/I Channel Byte Format (transmit)

| Bit | 5 | 4                   | 3                   | 2     | 1     | 0     |
|-----|---|---------------------|---------------------|-------|-------|-------|
|     | 1 | SB1_1 <sup>1)</sup> | SB1_0 <sup>1)</sup> | SO1_2 | SO1_1 | SO1_0 |

| Bit | 5 | 4                   | 3                   | 2     | 1     | 0     |
|-----|---|---------------------|---------------------|-------|-------|-------|
|     | 0 | SB2_1 <sup>1)</sup> | SB2_0 <sup>1)</sup> | SO2_2 | SO2_1 | SO2_0 |

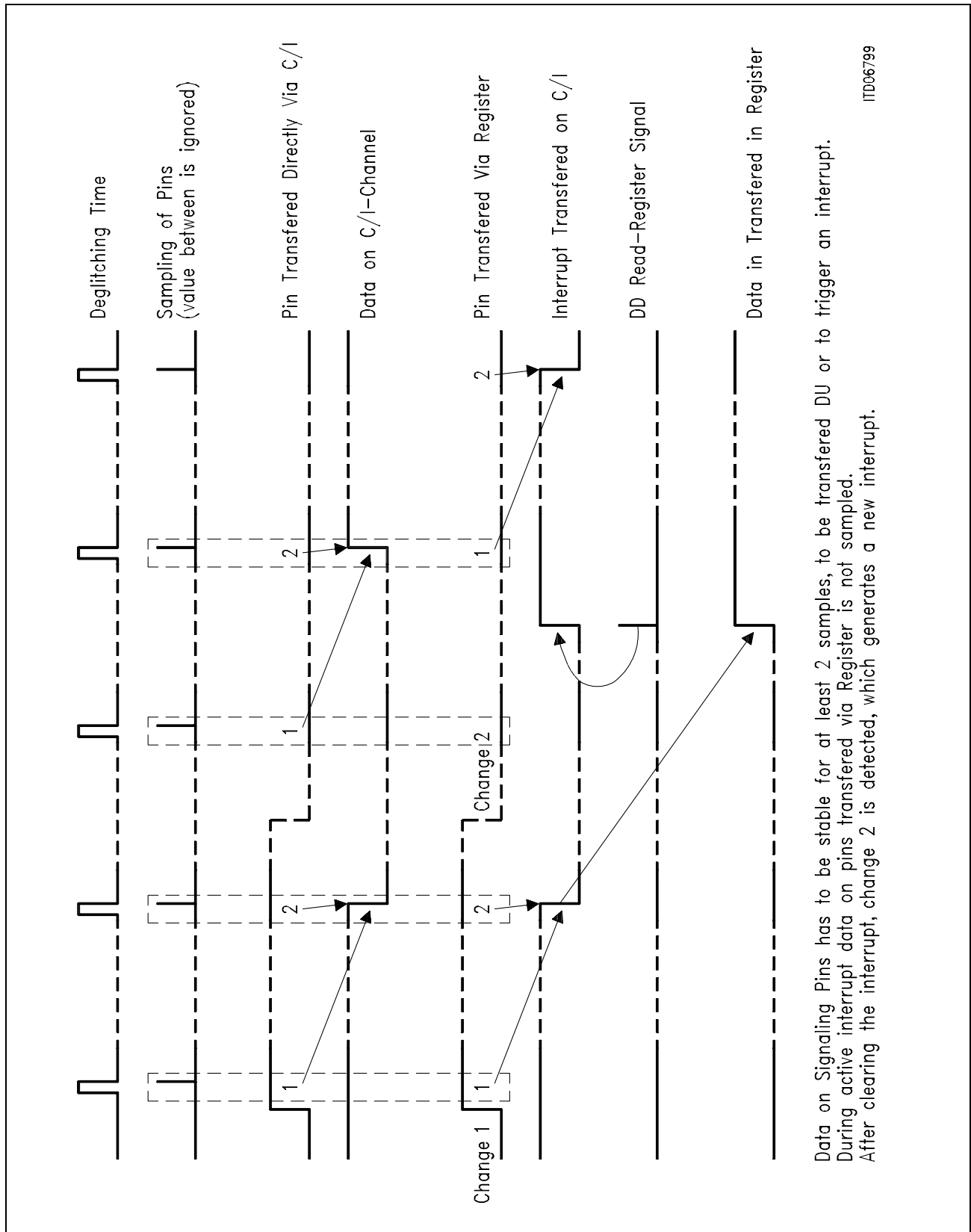
<sup>1)</sup> If SBx\_y is programmed as command output.

As the C/I-channel holds only 6 bits for two voice channels and the SICOFI-4 has up to five indication pins per voice channel, only pins SI1\_1 and SI1\_2 for voice channel 1, and pins SI2\_1 and SI2\_2 for voice channel 2 are fed directly to the C/I-channel. Any change at one of the other indication pins (SIx\_0, SBx\_0 and SBx\_1) will generate an interrupt per channel, which is transmitted upstream immediately (C/I-channel bits 2 and 5). Data on those pins is fed to register XR1 and can be evaluated with a XOP-read command.



There was a functional connection between two neighboring channels sharing the same C/I-channel of an IOM-2 interface in V1.\*. When an interrupt occurred in the C/I-channel, changes on all signaling input pins of this channel and of the neighboring channel were ignored, until the interrupt was cleared.

In Version V2.\* this **functional connection no longer exists**. If an interrupt occurs in one channel, changes in the neighboring channel will also generate an interrupt.



### Figure 10 Data Flow

## 5 Operating Modes

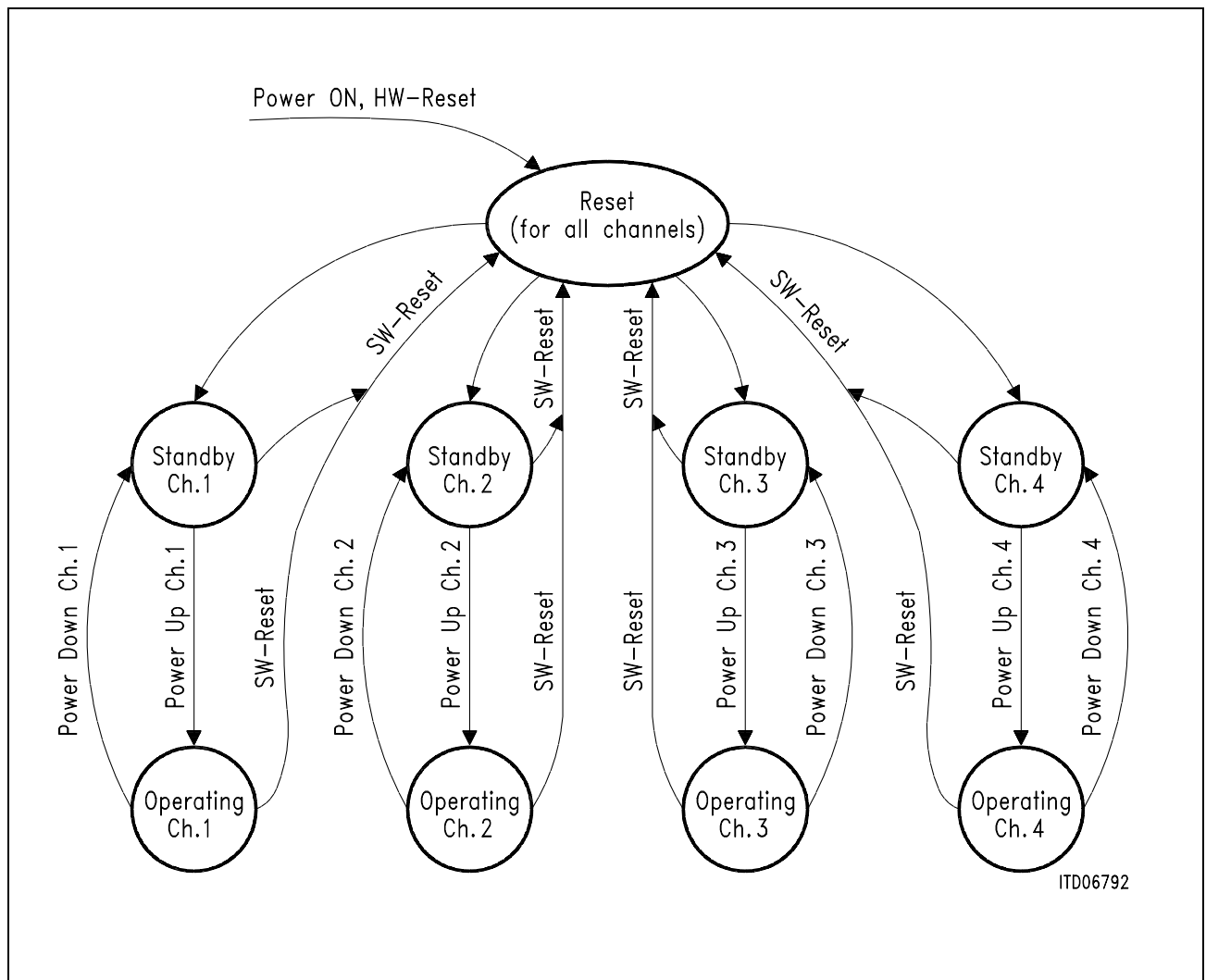


**Figure 11** Operating Modes

## 5.1 RESET (Basic setting mode)

Upon initial application of  $V_{DD}$  or resetting pin RESET to '1' during operation, or by software-reset (see COP command, [Page 31](#)), the SICOFI-4 enters a basic setting mode. Basic setting means, that the SICOFI-4 configuration registers CR1 ... CR4 and XR1 ... XR3 are initialized to '0' for all channels.

All programmable filters are disabled, A-law is chosen, all programmable command/indication pins are inputs. The two tone generators as well as any testmodes are disabled. There is no persistence checking. Receive signaling registers are cleared. DU-pin is in high impedance state, the analog outputs and the signaling outputs are forced to ground.

|                     |                |
|---------------------|----------------|
| CR1 ... CR4         | 00 Hex         |
| XR1 ... XR4         | 00 Hex         |
| Coefficient RAM     | not defined    |
| Command Stack       | cleared        |
| DD-input            | ignored        |
| DU-output           | high impedance |
| $V_{OUT1, 2, 3, 4}$ | GNDA1, 2, 3, 4 |
| SBx_y               | Input          |
| SOx_y               | GNDD           |

If any voltage is applied to any input-pin before initial application of  $V_{DD}$ , the SICOFI-4 may not enter the basic setting mode. In this case it is necessary to reset the SICOFI-4 or to initialize the SICOFI-4 configuration registers to '0'.

The SICOFI-4 leaves this mode automatically with the beginning of the next 8 kHz frame (RESET-pin is released).

## **5.2 Standby Mode**

After releasing the RESET-pin, (RESET-state), beginning with the next 8 kHz frame, the SICOFI-4 will enter the Standby mode. The SICOFI-4 is forced to standby mode with the PWRUP bit set to '0' in the SOP command (POWERDOWN). All 4 channels must be programmed separately. During standby mode the serial SICOFI-4 IOM-2 interface is ready to receive and transmit commands and data. Received voice data on DD-pin will be ignored. SICOFI-4 configuration registers and coefficient ram can be loaded and read back in this mode. Data downstream C/I-channel data is fed to appropriate Command pins. Data on indication pins is transmitted Data upstream.

|                      |                   |
|----------------------|-------------------|
| IOM-2 Voice Channels | '11111111' (idle) |
| $V_{OUT1, 2, 3, 4}$  | GNDA1, 2, 3, 4    |

## **5.3 Operating Mode**

The operating mode for any of the four channels is entered upon recognition of a PWRUP bit set to '1' in a SOP command for the specific channel.

## **6 Programmable Filters**

Based on an advanced digital filter concept, the PEB 2465 provides excellent transmission performance and high flexibility. The new filter concept leads to a maximum independence between the different filter blocks.

### **6.1 Impedance Matching Filter**

- Realization by 3 different loops
  - 4 MHz: Multiplication by a constant (12 bit)
  - 128 kHz: Wave Digital Filter (IIR) (60 bit)  
(improves low frequency response)
  - 64 kHz: FIR-Filter (48 bit)  
(for fine-tuning)
- Improved stability behavior of feedback loops
- Real part of termination impedance positive under all conditions
- Improved overflow performance for transients
- Return loss better 30 dB

### **6.2 Transhybrid Balancing (TH) Filter**

- New concept: 2 loops at 16 kHz
- Flexible realization allows optimization of wide impedance range
- Consists of a fixed and a programmable part
  - 2<sup>nd</sup> order Wave Digital Filter (IIR) (106 bit)  
(improves low frequency response)
  - 7-TAP FIR-Filter (84 bit)  
(for fine-tuning)
- Trans-Hybrid-Loss better 30 dB (typically better 40 dB, device only)
- Adaptation to different lines by:
  - Easy selection between four different downloaded coefficient sets

### **6.3 Filters for Frequency Response Correction**

- For line equalization and compensation of attenuation distortion
- Improvement of Group-Delay-Distortion by using minimum phase filters (instead of linear phase filters)
- FRR filter for correction of receive path distortion  
5 TAP programmable FIR filter operating at 8 kHz (60 bit)
- FRX filter for correction of transmit path distortion  
5 TAP programmable FIR filter operating at 8 kHz (60 bit)
- Frequency response better 0.1 dB

## 6.4 Amplification/Attenuation-Filters AX1, AX2, AR1, AR2

- Improved level adjustment for transmit and receive
- Two separate filters at each direction for
  - Improved trans-hybrid balancing
  - Optimal adjustment of digital dynamic range
  - Gain adjustments independent of TH-filter

## 6.5 Amplification/Attenuation Receive (AR1, AR2)-Filter

|                         |                         |                            |
|-------------------------|-------------------------|----------------------------|
| Step size for AR-Filter | range 3 ... – 14 dB:    | step size 0.02 ... 0.05 dB |
|                         | range – 14 ... – 24 dB: | step size 0.5 dB           |

## 6.6 Amplification/Attenuation Transmit (AX1, AX2)-Filter

|                         |                      |                            |
|-------------------------|----------------------|----------------------------|
| Step size for AX-Filter | range – 3 ... 14 dB: | step size 0.02 ... 0.05 dB |
|                         | range 14 ... 24 dB:  | step size 0.5 dB           |

## 7 QSICOS Software

The QSICOS-software has been developed to help to obtain an optimized set of coefficients both quickly and easily. The QSICOS program runs on any PC with at least 575 Kbytes of memory. This also requires MS-DOS Version 5.0 or higher, as well as extended memory.

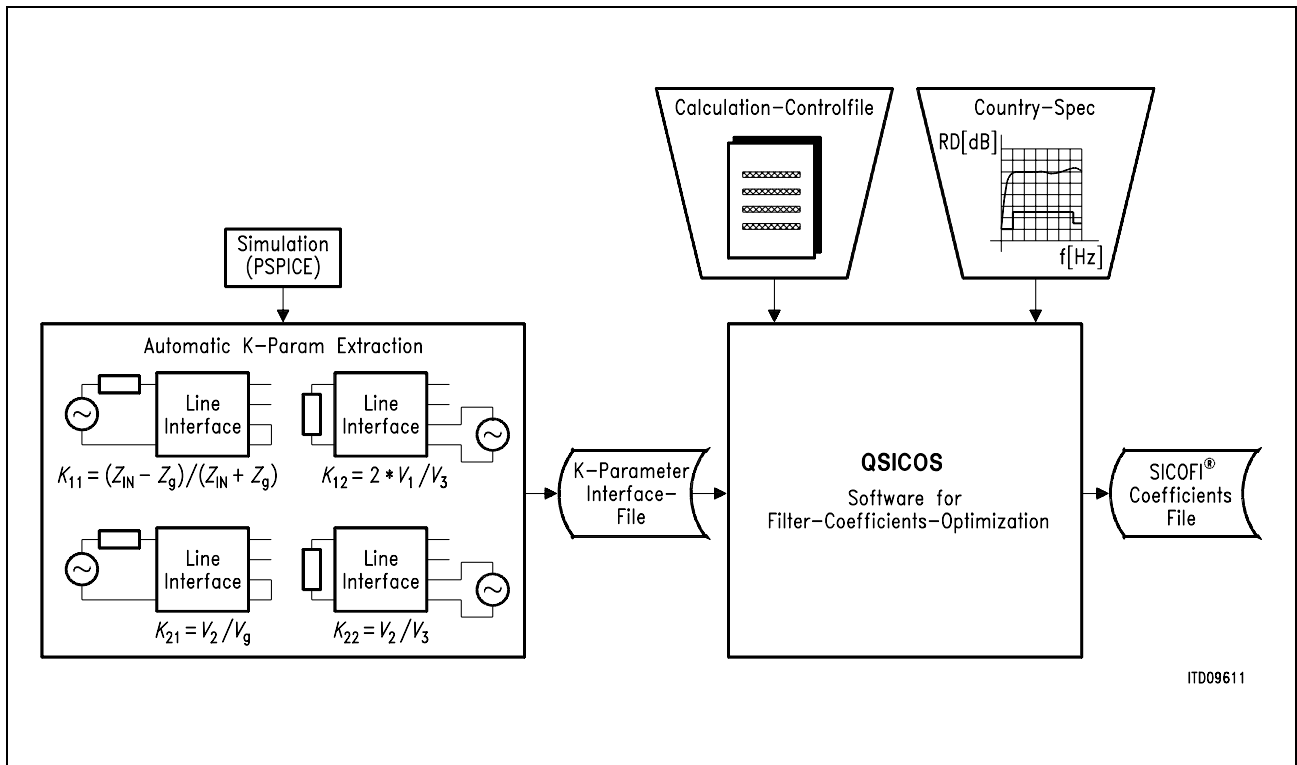


Figure 12 QSICOS Software

## 7.1 QSICOS Supports

- **Calculation of coefficients for the**

Impedance Filter (IM) for return loss calculation

FRR and FRX-Filters for frequency response in receive and transmit path

AR1, AR2 and AX1, AX2-Filter for level adjustment in receive and transmit path

Trans-Hybrid Balancing Filter (TH) and

two programmable tone generators (TG 1 and TG 2)

- **Simulation of the PEB 2465 and SLIC system** with fixed filter coefficients allows simulations of tolerances which may be caused e.g. by discrete external components.

- **Graphical output of transfer functions to the screen** for

Return Loss

Frequency responses in receive and transmit path

Transhybrid Loss

- **Calculation of the PEB 2465 and SLIC system stability.** The IM-Filter of the PEB 2465 adjust the total system impedance by making a feedback loop. Because the line is also a part of the total system, a very robust method has to be used to avoid oscillations and to ensure system stability. The input impedance of the PEB 2465 and SLIC combination is calculated. If the real part of the system input impedance is positive, the total system stability can be guaranteed.

## 8 Transmission Characteristics

The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) needs a complete knowledge of the SICOFI-4's analog environment, and it is suggested to use the QSICOS-program for calculating the propriate coefficients. Unless otherwise stated, the transmission characteristics are guaranteed within the test conditions.

### Test Conditions

$T_A = 0\text{ }^{\circ}\text{C}$  to  $70\text{ }^{\circ}\text{C}$ ;  $V_{DD} = 5\text{ V} \pm 5\%$ ;  $\text{GNDA1} \dots 4 = \text{GNDD} = 0\text{ V}$ ;  
 $R_L^{1)} > 20\text{ k}\Omega$ ;  $C_L < 20\text{ pF}$ ;

$H(\text{IM}) = H(\text{TH}) = 0$ ;  $H(\text{R1}) = H(\text{FRX}) = H(\text{FRR}) = 1$ ;  
HPR and HPX enabled;

$\text{AR}^{2)} =$  0 to  $-13\text{ dB}$  for sine-wave-, and  
0 to  $-11\text{ dB}$  for CCITT-noise-measurements

$\text{AX}^{3)} =$  0 to  $13\text{ dB}$  for sine-wave-, and  
0 to  $11\text{ dB}$  for CCITT-noise-measurements

$f = 1014\text{ Hz}$ ;  $0\text{ dBm0}$ ; A-Law or  $\mu$ -Law;

$\text{AGX} = 0\text{ dB}$ ,  $6.02\text{ dB}$ ,  $\text{AGR} = 0\text{ dB}$ ,  $-6.02\text{ dB}$ ;

In Transmit direction for  $\mu$ -law an additional gain of  $1.94\text{ dB}$  is implemented automatically, in the companding block (CMP). This additional gain has to be considered at all gain calculations, and reduces possible AX-gain.

A  $0\text{ dBm0}^{4)}$  signal is equivalent to  $1.095\text{ [1.0906] Vrms}$ . A  $+3.14\text{ [3.17] dBm0}$  signal is equivalent to  $1.57\text{ Vrms}$  which corresponds to the overload point of  $2.223\text{ V}$  (A-law,  $[\mu$ -law]).

When the gain in the receive path is set at  $0\text{ dB}$ , an  $1014\text{ Hz}$  PCM sinewave input with a level  $0\text{ dBm0}$  will correspond to a voltage of  $1.095\text{ Vrms}$  at A-Law ( $1.0906\text{ V}$   $\mu$ -Law) at the analog output.

When the gain in the transmit path is set at  $0\text{ dB}$ , an  $1014\text{ Hz}$  sine wave signal with a voltage of  $1.095\text{ Vrms}$  A-Law ( $1.0906\text{ V}$   $\mu$ -Law) will correspond to a level of  $0\text{ dBm0}$  at the PCM output.

<sup>1)</sup>  $R_L$ ,  $C_L$  forms the load on  $V_{OUT}$

<sup>2)</sup> Consider, in a complete System,  $\text{AR} = \text{AR1} + \text{AR2} + \text{FRR} + \text{R1}$

<sup>3)</sup> Consider, in a complete System,  $\text{AX} = \text{AX1} + \text{AX2} + \text{FRX}$

<sup>4)</sup> The absolute power level in decibels referred to the PCM interface levels.

**Transmission Characteristics**
**Table 3 Transmission Characteristics**

| Parameter                                                                                                                                                                                                                         | Symbol                                       | Limit Values     |            |                                  | Unit                           |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------|------------------|------------|----------------------------------|--------------------------------|
|                                                                                                                                                                                                                                   |                                              | min.             | typ.       | max.                             |                                |
| Gain absolute (AGX = AGR = 0)<br>$T_A = 25\text{ °C}; V_{DD} = 5\text{ V}$<br>$T_A = 0 - 70\text{ °C}; V_{DD} = 5\text{ V} \pm 5\%$                                                                                               | $G$                                          | - 0.15<br>- 0.25 | $\pm 0.10$ | + 0.15<br>+ 0.25                 | dB<br>dB                       |
| Gain absolute (AGX = 6.02 dB,<br>AGR = - 6.02 dB)<br>$T_A = 25\text{ °C}; V_{DD} = 5\text{ V}$<br>$T_A = 0 - 70\text{ °C}; V_{DD} = 5\text{ V} \pm 5\%$                                                                           | $G$                                          | - 0.15<br>- 0.25 | $\pm 0.10$ | + 0.15<br>+ 0.25                 | dB<br>dB                       |
| Harmonic distortion, 0 dBm0;<br>$f = 1000\text{ Hz}; 2^{\text{nd}}, 3^{\text{rd}}$ order                                                                                                                                          | HD                                           |                  | - 50       | - 44                             | dB                             |
| Intermodulation <sup>1)</sup> R2                                                                                                                                                                                                  | IMD                                          |                  | - 46       |                                  | dB                             |
| R3                                                                                                                                                                                                                                | IMD                                          |                  | - 56       |                                  | dB                             |
| Crosstalk 0 dBm0; $f = 200\text{ Hz}$ to $3400\text{ Hz}$<br>any combination of direction and channel                                                                                                                             | CT                                           |                  | - 85       | - 80                             | dB                             |
| Idle channel noise,<br>transmit, A-law, psophometric $V_{IN} = 0\text{ V}$<br>transmit, $\mu$ -law, C-message $V_{IN} = 0\text{ V}$<br>receive, A-law, psophometric idle code + 0<br>receive, $\mu$ -law, C-message idle code + 0 | $N_{TP}$<br>$N_{TC}$<br>$N_{RP}$<br>$N_{RC}$ |                  | - 85<br>5  | - 67.4<br>17.5<br>- 78.0<br>12.0 | dBm0p<br>dBmc<br>dBm0p<br>dBmc |

<sup>1)</sup> Using equal-level, 4-tone method (EIA) at a composite level of - 13 dBm0 with frequencies in the range between 300 Hz and 3400 Hz.

## 8.1 Frequency Response

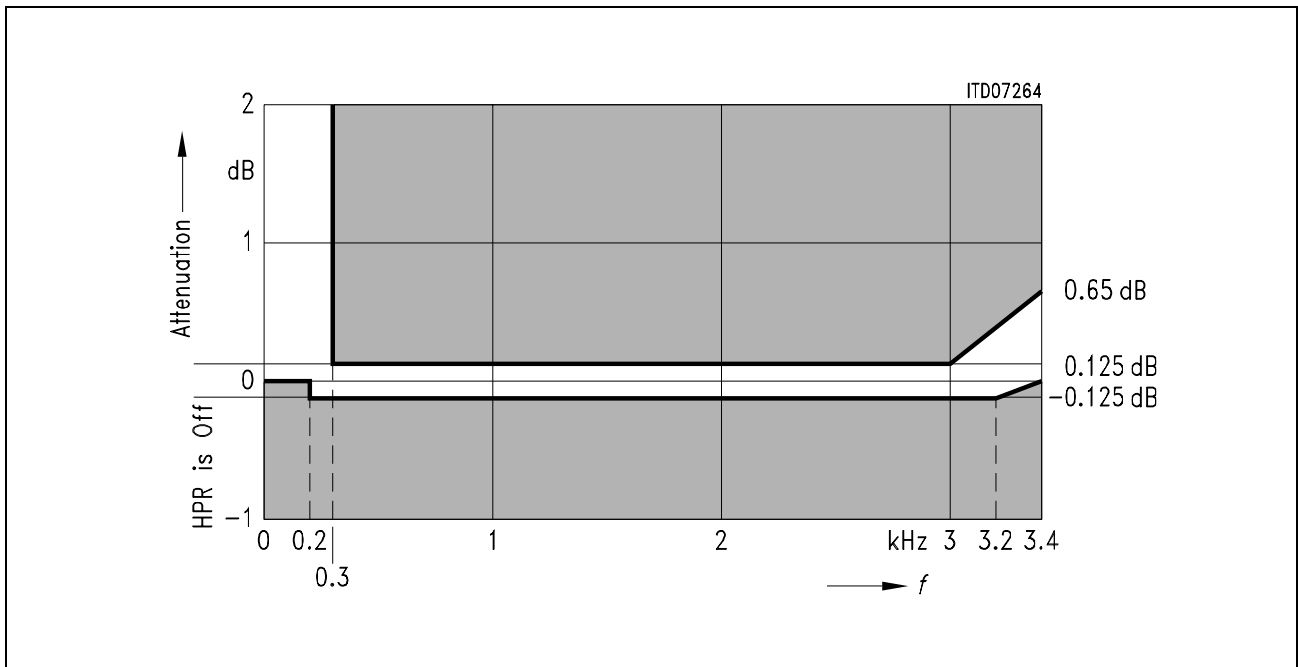


**Figure 13** Receive: Reference Frequency 1 kHz, Input Signal Level 0 dBm0

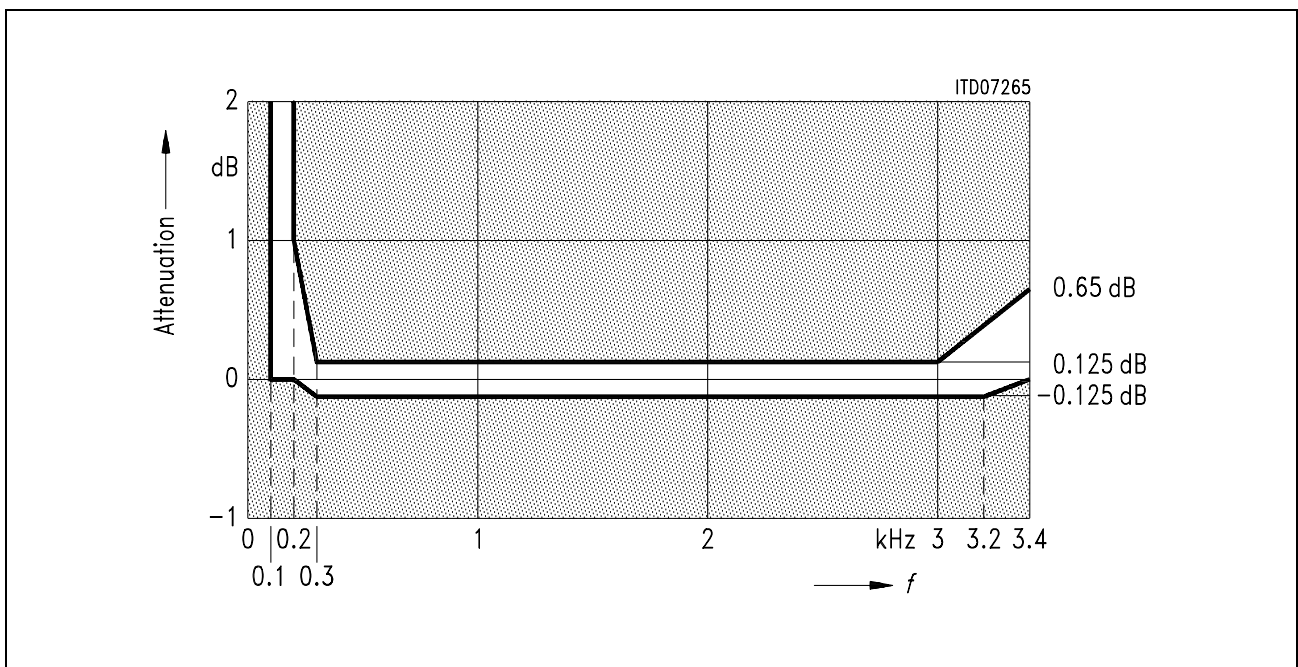


**Figure 14** Transmit: Reference Frequency 1 kHz, Input Signal Level 0 dBm0

## 8.2 Group Delay

Maximum delays when the SICOFI-4 is operating with  $H(\text{TH}) = H(\text{IM}) = 0$  and  $H(\text{FRR}) = H(\text{FRX}) = 1$  including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group Delay deviations stay within the limits in the figures below.

**Table 4 Group Delay Absolute Values: Input signal level 0 dBm0**

| Parameter      | Symbol          | Limit Values |      |      | Unit          | Reference |
|----------------|-----------------|--------------|------|------|---------------|-----------|
|                |                 | min.         | typ. | max. |               |           |
| Transmit delay | $D_{\text{XA}}$ |              |      | 300. | $\mu\text{s}$ |           |
| Receive delay  | $D_{\text{RA}}$ |              |      | 250  | $\mu\text{s}$ |           |

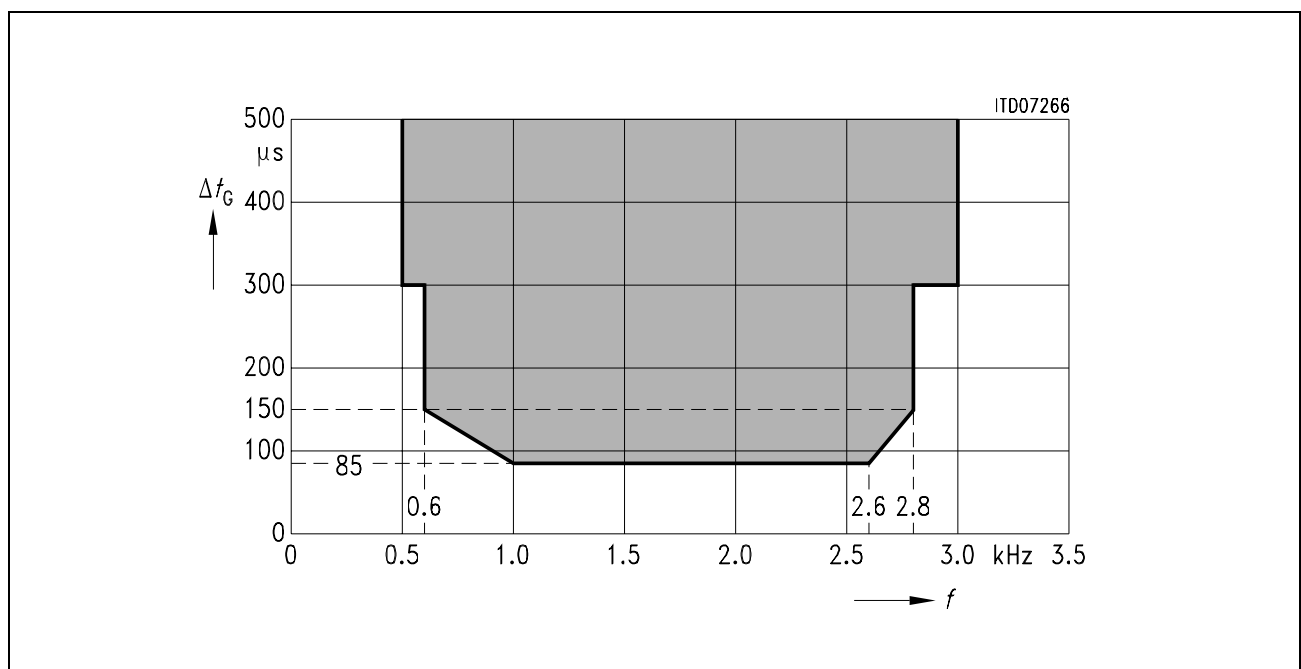


**Figure 15 Group Delay Distortion Transmit: Input Signal Level 0 dBm0**

## Transmission Characteristics

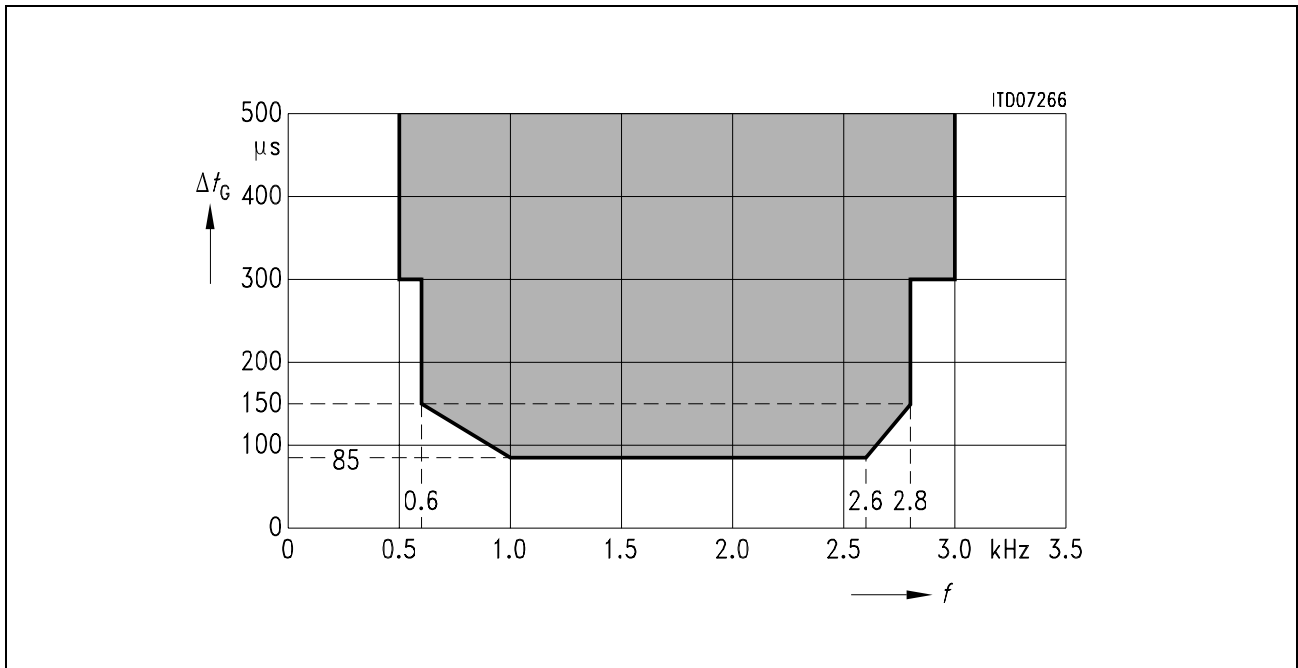
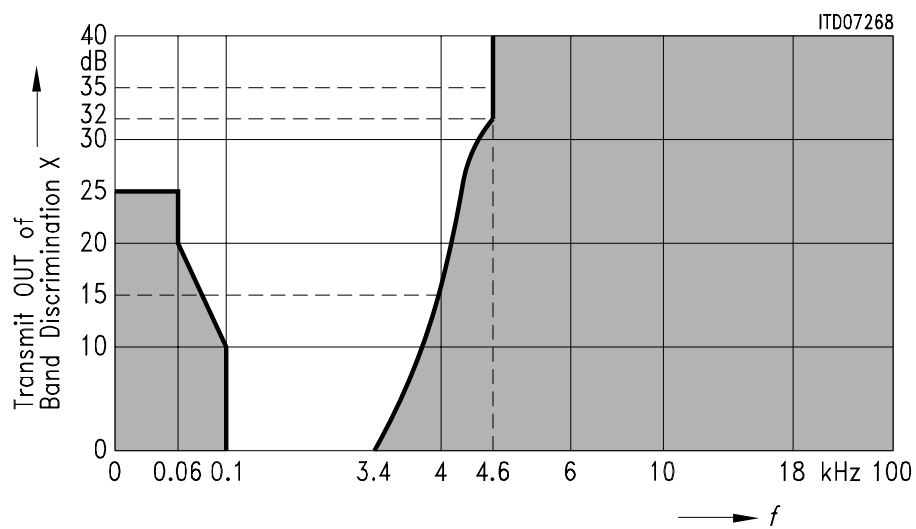


**Figure 16 Group Delay Distortion Receive: Input Signal Level 0 dBm<sup>1)</sup>**

<sup>1)</sup> HPR is switched on: reference point is at  $t_{Gmin}$   
HPR is switched off: reference is at 1.5 kHz

### 8.3 Out-of-Band Signals at Analog Input

With an 0 dBm0 out-of-band sine wave signal with frequency  $f$  ( $\ll 100$  Hz or 3.4 kHz to 100 kHz) applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog input<sup>1)</sup>.



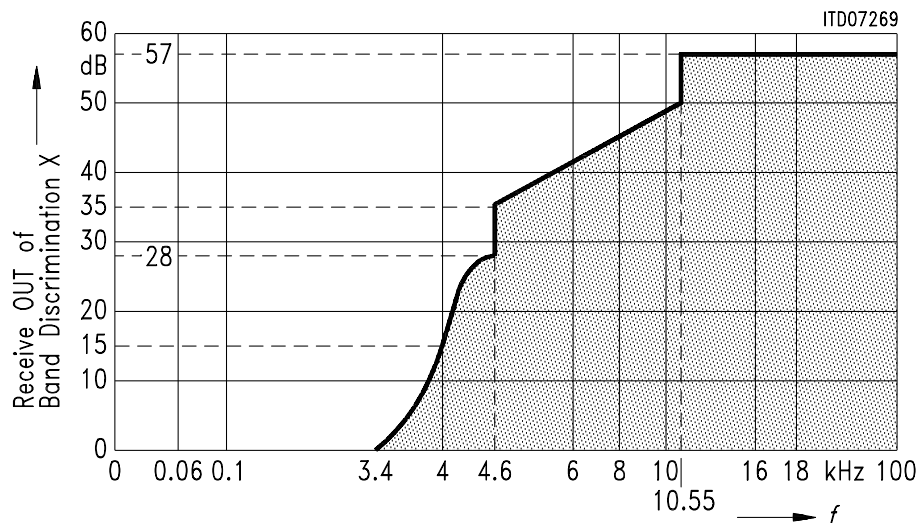
$$3.4 \dots 4.0 \text{ kHz: } X = -14 \left( \sin \left( \pi \frac{4000-f}{1200} \right) - 1 \right)$$

$$4.0 \dots 4.6 \text{ kHz: } X = -18 \left( \sin \left( \pi \frac{4000-f}{1200} \right) - \frac{7}{9} \right)$$

<sup>1)</sup> Poles at 12 kHz  $\pm$  150 Hz and 16 kHz  $\pm$  150 Hz are provided

## 8.4 Out-of-Band Signals at Analog Output

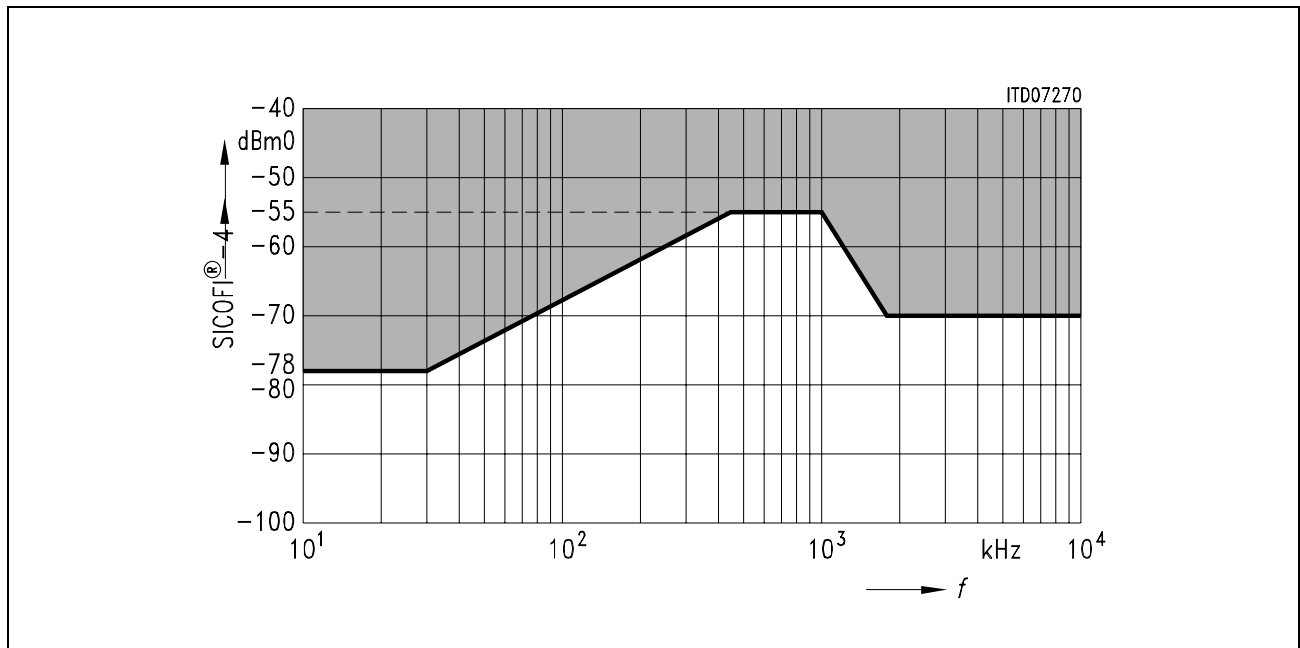
With a 0 dBm0 sine wave with frequency  $f$  (300 Hz to 3.99 kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.



$$3.4 \dots 4.6 \text{ kHz: } X = -14 \left( \sin \left( \pi \frac{4000-f}{1200} \right) - 1 \right)$$

## 8.5 Out of Band Idle Channel Noise at Analog Output

With an idle code applied to the digital input, the level of any resulting out-of-band power spectral density (measured with 3 kHz bandwidth) at the analog output, will be not greater than the limit curve shown in the figure below.



## 8.6 Overload Compression

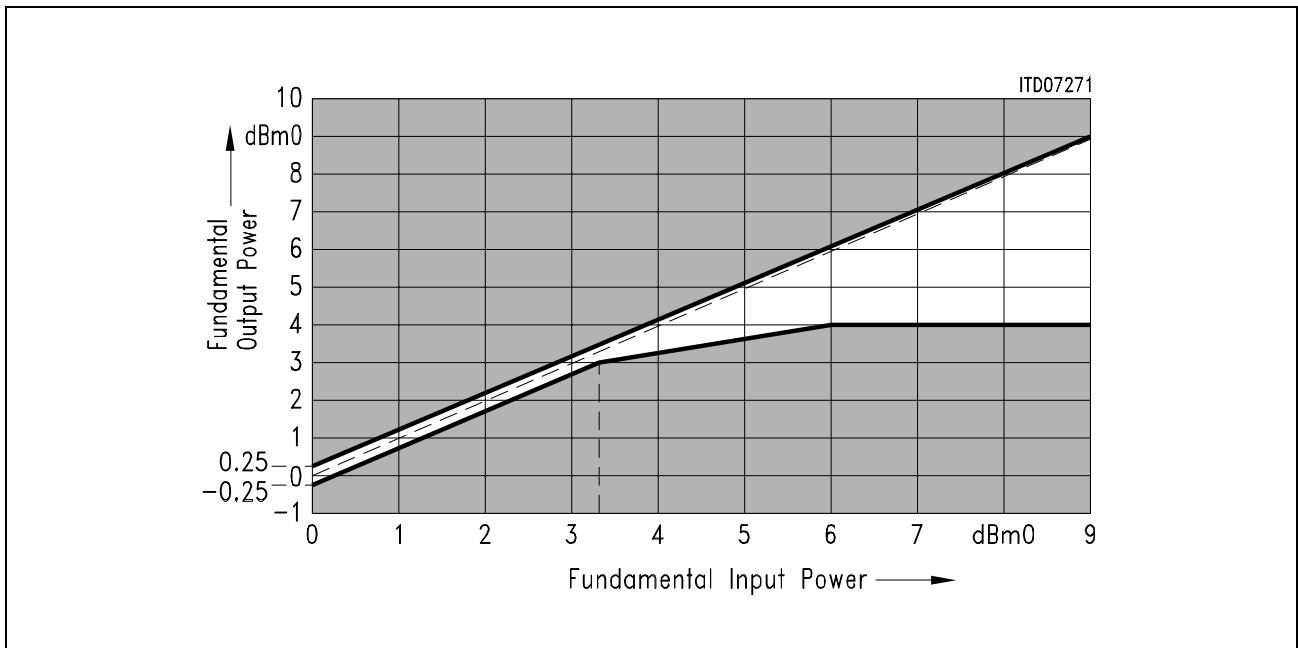


Figure 17  $\mu$ -Law, Transmit: measured with sine wave  $f = 1014$  Hz.

## 8.7 Gain Tracking (receive or transmit)

The gain deviations stay within the limits in the figures below.

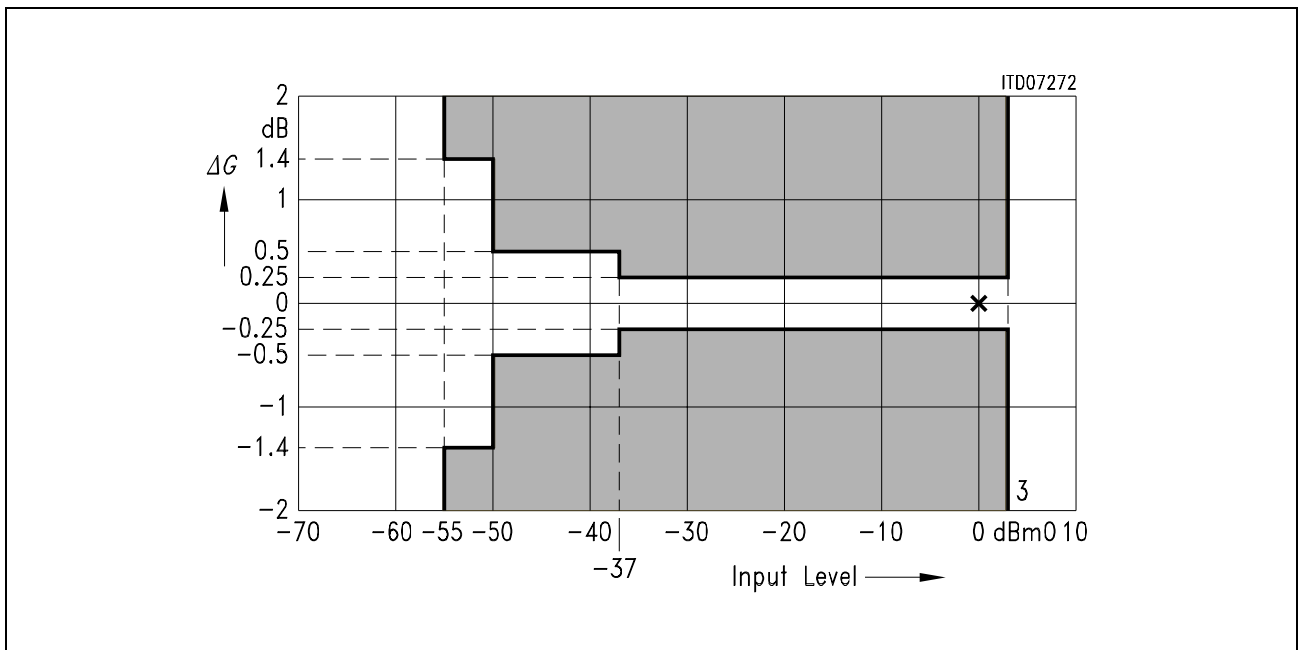


**Figure 18** Gain Tracking: (measured with sine wave  $f = 1014$  Hz  
(reference level is 0 dBm0))

## 8.8 Total Distortion

The signal to distortion ratio exceeds the limits in the following figure.

### 8.8.1 Total Distortion Measured with Sine Wave

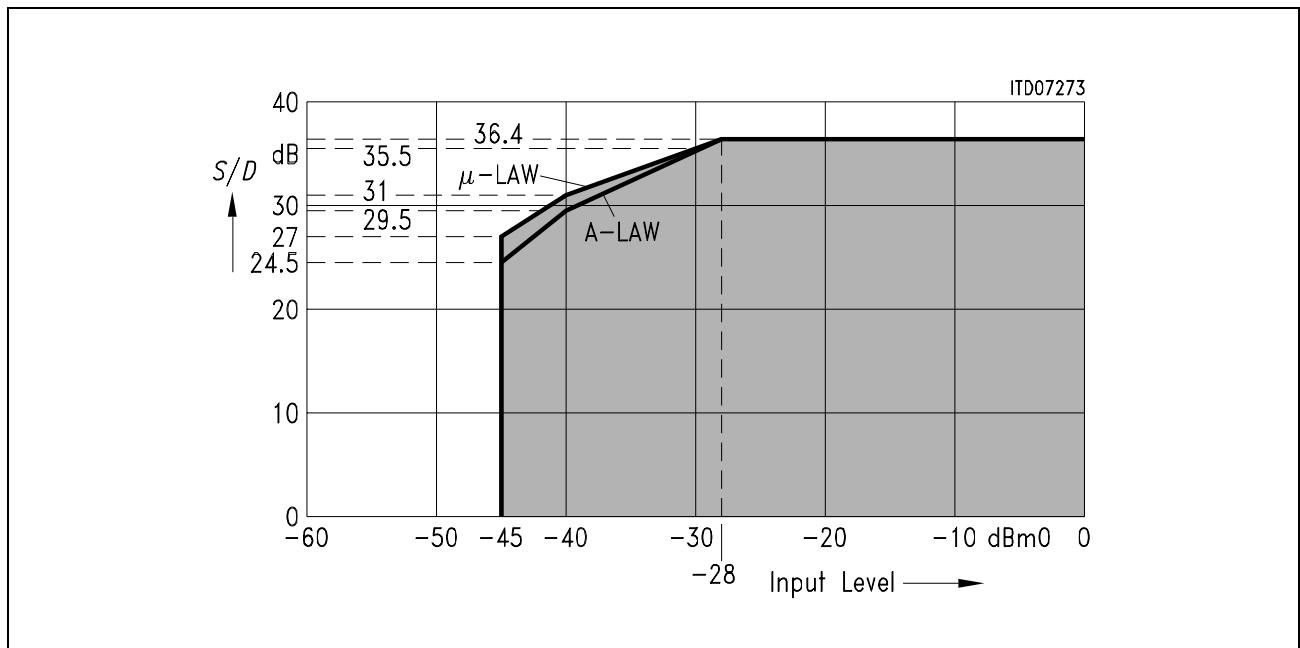


**Figure 19 Receive or Transmit: measured with sine wave  $f = 1014$  Hz**  
(C-message weighted for  $\mu$ -law, psophometrically weighted for A-law)

## 8.8.2 Total Distortion Measured with Noise According to CCITT

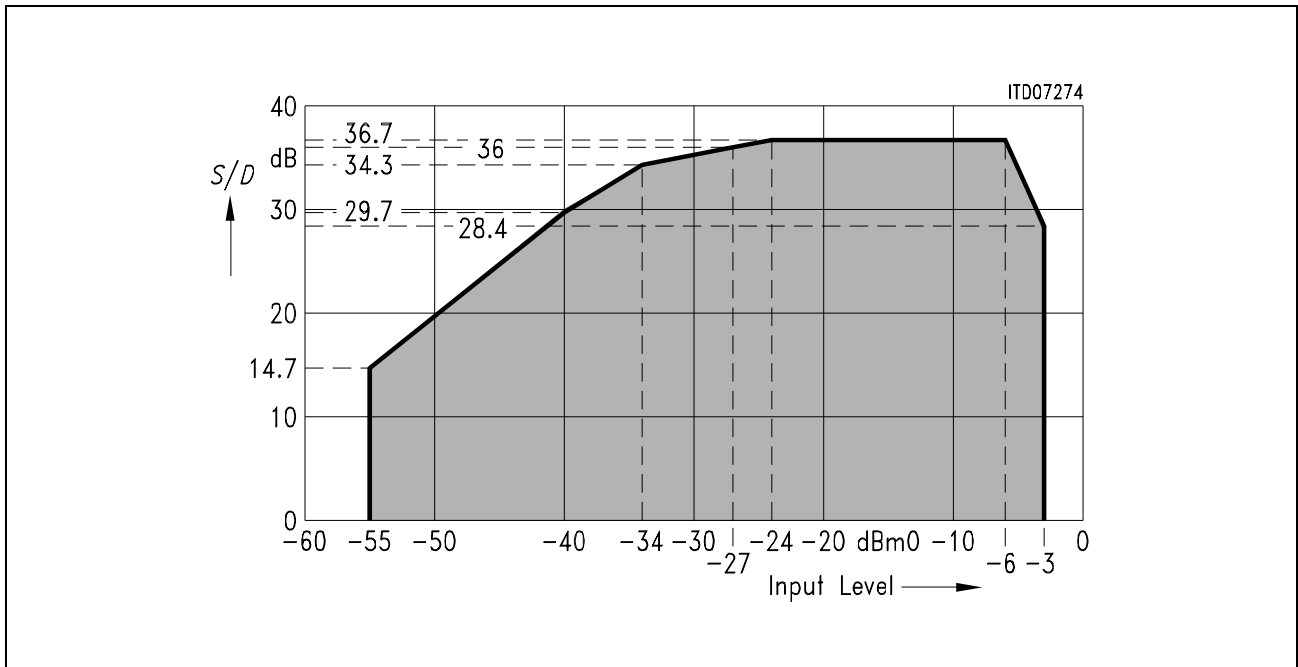


Figure 20 Receive

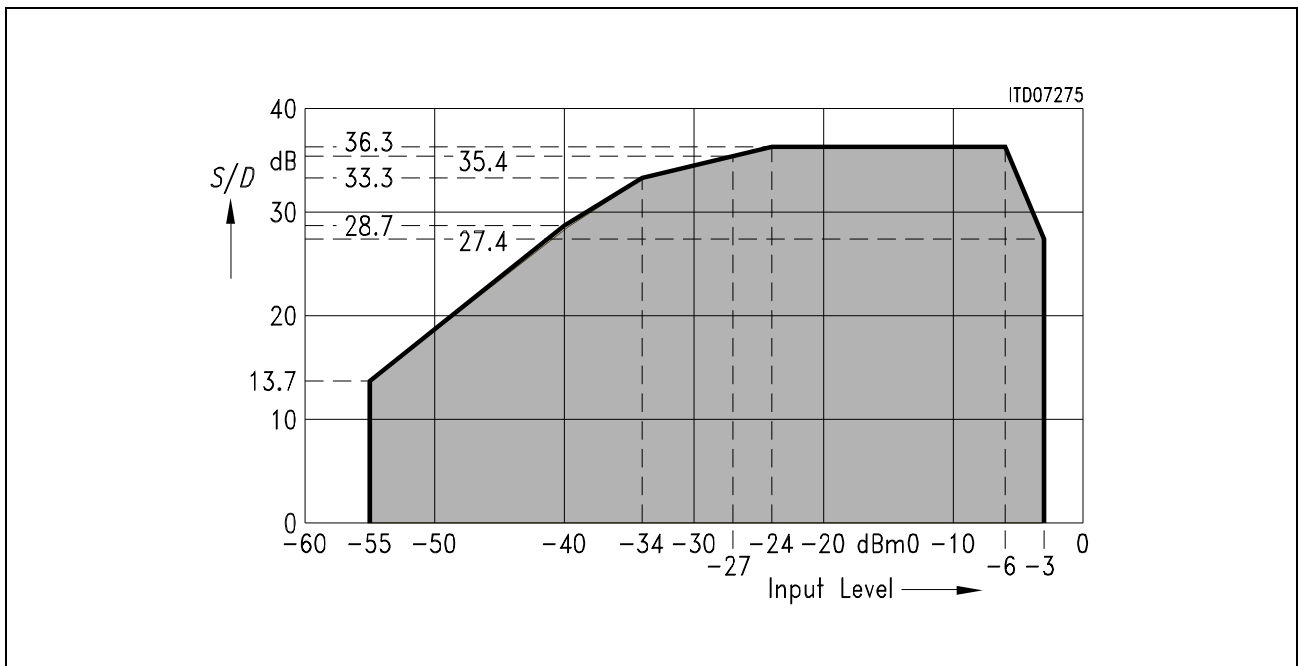


Figure 21 Transmit

## 8.9 Single Frequency Distortion

An input signal with its frequency swept between 0.3 to 3 kHz for the receive path, or 0 to 12 kHz for the transmit path, any generated output signal with other frequency than the input frequency will stay 28 dB below the maximum input level of 0 dBm0.

| Receive           |                  | Transmit    |                  |
|-------------------|------------------|-------------|------------------|
| Frequency         | max. Input Level | Frequency   | max. Input Level |
| 300 Hz to 3.4 kHz | 0 dBm0           | 0 to 12 kHz | 0 dBm 0          |

## 8.10 Transhybrid Loss

The quality of Transhybrid-Balancing is very sensitive to deviations in gain and group delay - deviations inherent to the SICOFI-4 A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP's etc.)

Measurement of SICOFI-4 Transhybrid-Loss: A 0 dBm0 sine wave signal and a frequency in the range between 300 - 3400 Hz is applied to the digital input. The resulting analog output signal at pin  $V_{OUT}$  is directly connected to  $V_{IN}$ , e.g. with the SICOFI-4 testmode "Digital Loop Back via Analog Port". The programmable filters FRR, AR, FRX, AX and IM are disabled, the balancing filter TH is enabled with coefficients optimized for this configuration ( $V_{OUT} = V_{IN}$ ).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below. (Filter coefficients will be provided)

| Parameter                   | Symbol              | Limit Values |      | Unit | Test Condition                                          |
|-----------------------------|---------------------|--------------|------|------|---------------------------------------------------------|
|                             |                     | min.         | typ. |      |                                                         |
| Transhybrid Loss at 300 Hz  | THL <sub>300</sub>  | 27           | 40   | dB   | $T_A = 25\text{ }^{\circ}\text{C}; V_{DD} = 5\text{ V}$ |
| Transhybrid Loss at 500 Hz  | THL <sub>500</sub>  | 33           | 45   | dB   | $T_A = 25\text{ }^{\circ}\text{C}; V_{DD} = 5\text{ V}$ |
| Transhybrid Loss at 2500 Hz | THL <sub>2500</sub> | 29           | 40   | dB   | $T_A = 25\text{ }^{\circ}\text{C}; V_{DD} = 5\text{ V}$ |
| Transhybrid Loss at 3000 Hz | THL <sub>3000</sub> | 27           | 35   | dB   | $T_A = 25\text{ }^{\circ}\text{C}; V_{DD} = 5\text{ V}$ |
| Transhybrid Loss at 3400 Hz | THL <sub>3400</sub> | 27           | 35   | dB   | $T_A = 25\text{ }^{\circ}\text{C}; V_{DD} = 5\text{ V}$ |

The listed values for THL correspond to a typical variation of the signal amplitude and -delay in the analog blocks.

$\Delta$  amplitude = typ  $\pm$  0.15 dB

$\Delta$  delay = typ  $\pm$  0.5  $\mu$ s

## 9 Electrical Characteristics

### 9.1 Absolute Maximum Ratings

| Parameter                                                                                                                              | Symbol    | Limit Values   |            | Unit   | Test Condition |
|----------------------------------------------------------------------------------------------------------------------------------------|-----------|----------------|------------|--------|----------------|
|                                                                                                                                        |           | min.           | max.       |        |                |
| $V_{DD}$ referred to GNDD                                                                                                              |           | – 0.3          | 7.0        | V      |                |
| GNDA to GNDD                                                                                                                           |           | – 0.6          | 0.6        | V      |                |
| Analog input and output voltage referred to $V_{DD} = 5\text{ V}$ ;<br>referred to GNDA = 0 V                                          |           | – 5.3<br>– 0.3 | 0.3<br>5.3 | V<br>V |                |
| All digital input voltages referred to GNDD = 0 V;<br>( $V_{DD} = 5\text{ V}$ )<br>referred to $V_{DD} = 5\text{ V}$ ;<br>(GNDD = 0 V) |           | – 0.3<br>– 5.3 | 5.3<br>0.3 | V<br>V |                |
| DC input and output current at any input or output pin (free from latch-up)                                                            |           |                | 10         | mA     |                |
| Storage temperature                                                                                                                    | $T_{STG}$ | – 60           | 125        | °C     |                |
| Ambient temperature under bias                                                                                                         | $T_A$     | – 10           | 80         | °C     |                |
| Power dissipation (package)                                                                                                            | $P_D$     |                | 1          | W      |                |

*Note: Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.*

*The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25^\circ\text{C}$  and the given supply voltage.*

## 9.2 Operating Range

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ;  $V_{DD} = 5 \text{ V} \pm 5 \%$ ;  $GNDD = 0 \text{ V}$ ;  $GNDA = 0 \text{ V}$

| Parameter                                                                                                                    | Symbol    | Limit Values       |           |           | Unit                   | Test Condition                                                                                              |
|------------------------------------------------------------------------------------------------------------------------------|-----------|--------------------|-----------|-----------|------------------------|-------------------------------------------------------------------------------------------------------------|
|                                                                                                                              |           | min.               | typ.      | max.      |                        |                                                                                                             |
| $V_{DD}$ supply current<br>standby<br>operating (4 channels)                                                                 | $I_{DD}$  |                    | 1.2<br>27 | 1.5<br>40 | mA<br>mA               |                                                                                                             |
| Power supply rejection<br><br>of either supply/direction<br><br>receive $V_{DD}$ guaranteed<br>receive $V_{DD}$ target value | $P_{SRR}$ | 30<br><br>14<br>30 |           |           | <br><br>dB<br>dB<br>dB | ripple: 0 to 150 kHz,<br>70 mVrms<br>measured: 300 Hz to<br>3.4 kHz<br>measured: at $f$ : 3.4 to<br>150 kHz |
| Power dissipation standby                                                                                                    | $P_{DS}$  |                    | 15        | 20        | mW                     |                                                                                                             |
| Power dissipation operating                                                                                                  | $P_{D01}$ |                    | 75        | 110       | mW                     | 1 channel operating                                                                                         |
| Power dissipation operating                                                                                                  | $P_{D02}$ |                    | 100       | 140       | mW                     | 2 channels operating                                                                                        |
| Power dissipation operating                                                                                                  | $P_{D03}$ |                    | 120       | 175       | mW                     | 3 channels operating                                                                                        |
| Power dissipation operating                                                                                                  | $P_{D04}$ |                    | 140       | 210       | mW                     | 4 channels operating                                                                                        |

*Note: In the operating range the functions given in the circuit description are fulfilled.*

### 9.3 Digital Interface

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ;  $V_{DD} = 5 \text{ V} \pm 5 \%$ ;  $GNDD = 0 \text{ V}$ ;  $GNDA = 0 \text{ V}$

All input-pins, with exception of the RESET-pin, have a TTL-input characteristic.

| Parameter                 | Symbol   | Limit Values |         | Unit          | Test Condition                                        |
|---------------------------|----------|--------------|---------|---------------|-------------------------------------------------------|
|                           |          | min.         | max.    |               |                                                       |
| Low-input voltage         | $V_{IL}$ | - 0.3        | 0.8     | V             |                                                       |
| High-input voltage        | $V_{IH}$ | 2.0          |         | V             |                                                       |
| Low-output voltage        | $V_{OL}$ |              | 0.45    | V             | $I_O = - 5 \text{ mA}$                                |
| Low-output voltage DU-pin | $V_{OL}$ |              | 0.45    | V             | $I_O = - 7 \text{ mA}$ ,<br>$R_L = 1 \text{ k}\Omega$ |
| High-output voltage       | $V_{OH}$ | 4.4          |         | V             | $I_O = 5 \text{ mA}$                                  |
| Input leakage current     | $I_{IL}$ |              | $\pm 1$ | $\mu\text{A}$ | $- 0.3 \leq V_{IN} \leq V_{DD}$                       |

## 9.4 Analog Interface

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ;  $V_{DD} = 5 \text{ V} \pm 5 \%$ ;  $GNDD = 0 \text{ V}$ ;  $GNDA = 0 \text{ V}$

| Parameter                | Symbol   | Limit Values |           |             | Unit             | Test Condition              |
|--------------------------|----------|--------------|-----------|-------------|------------------|-----------------------------|
|                          |          | min.         | typ.      | max.        |                  |                             |
| Analog input resistance  | $R_i$    | 160          | 270       | 480         | $\text{k}\Omega$ |                             |
| Analog output resistance | $R_o$    |              |           | 10          | $\Omega$         |                             |
| Analog output load       | $R_L$    | 20           |           |             | $\text{k}\Omega$ |                             |
|                          | $C_L$    |              |           | 20          | $\text{pF}$      |                             |
| Input leakage current    | $I_{IL}$ |              | $\pm 0.1$ | $\pm 1.0$   | $\mu\text{A}$    | $0 \leq V_{IN} \leq V_{DD}$ |
| Input voltage range (AC) | $V_{IR}$ |              |           | $\pm 2.223$ | $\text{V}$       |                             |

## 9.5 Reset Timing

To reset the SICOFI-4 to basic setting mode, positive pulses applied to pin RS have to be higher than 2.4 V (CMOS-Schmitt-Trigger Input) and longer than 3  $\mu\text{s}$ . Signals shorter than 1  $\mu\text{s}$  will be ignored.

### 9.5.1 IOM-2 Interface Timing

### 9.5.2 4-MHz Operation Mode (Mode = 1)

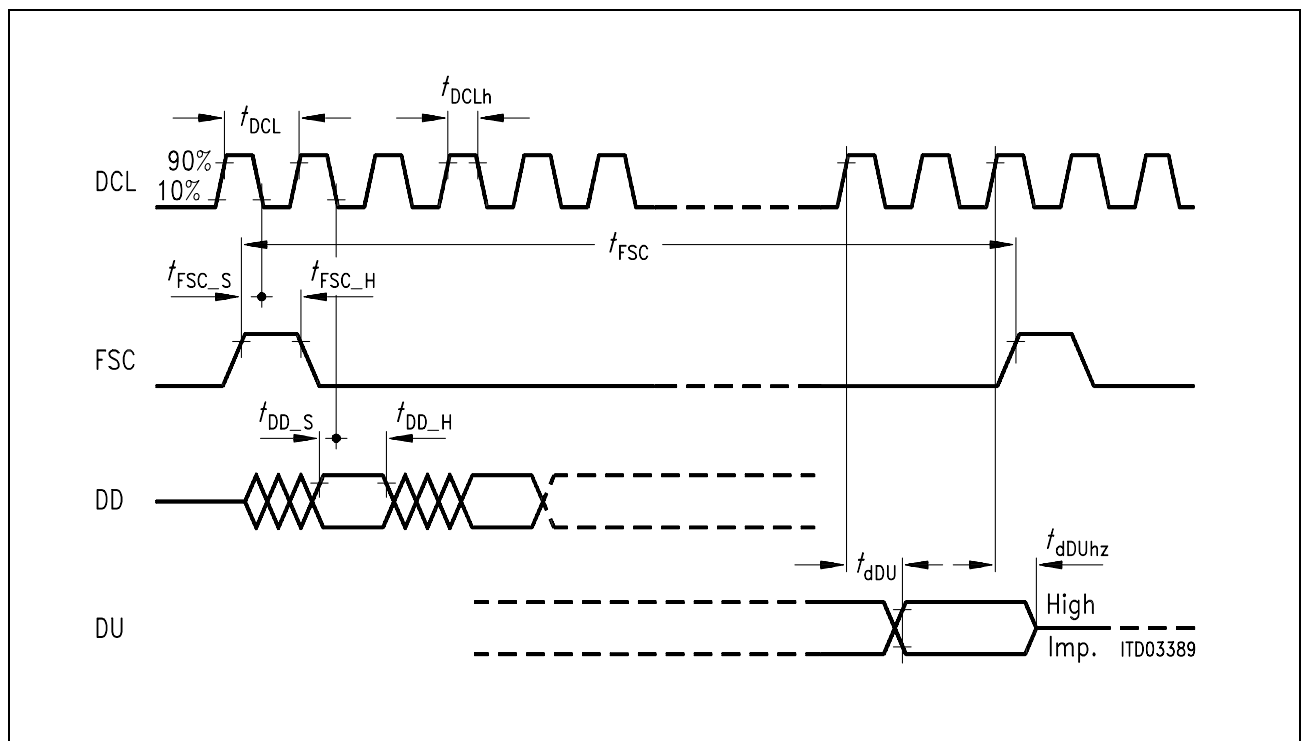


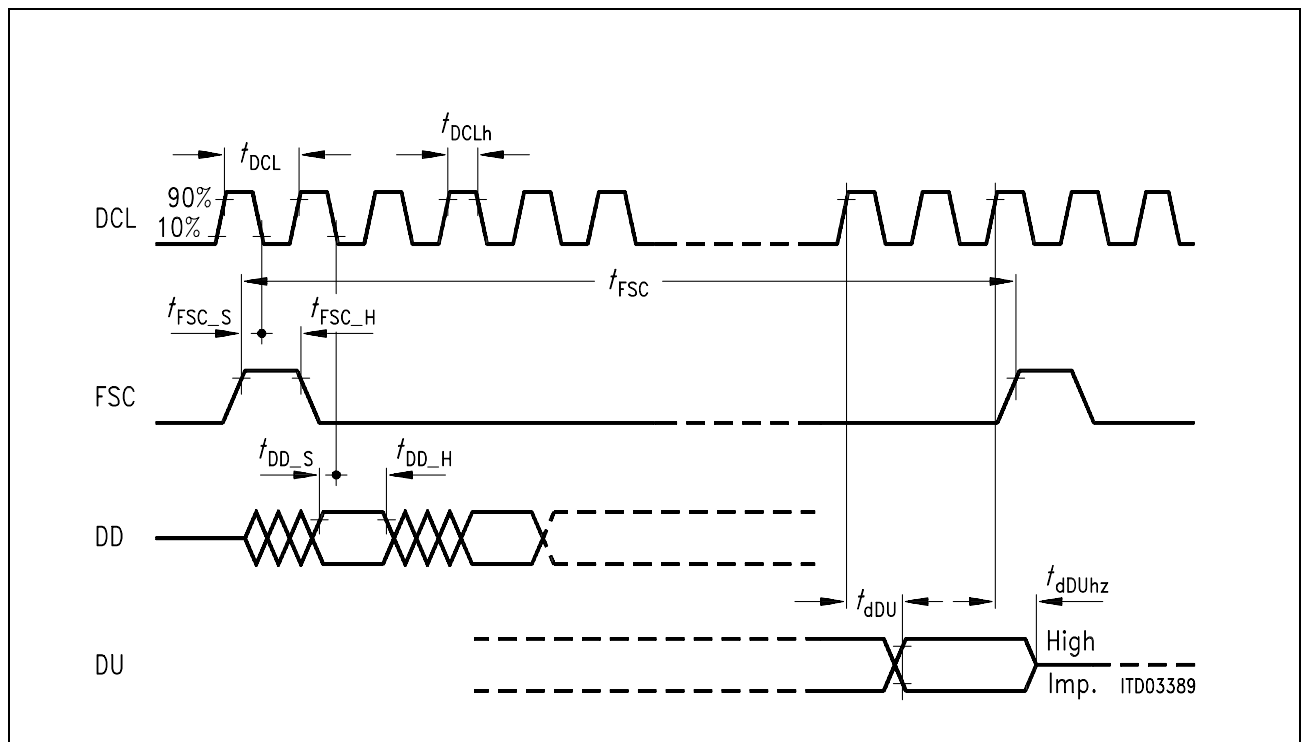
**Table 5 Switching Characteristics**

| Parameter                            | Symbol       | Limit Values |            |      | Unit    |
|--------------------------------------|--------------|--------------|------------|------|---------|
|                                      |              | min.         | typ.       | max. |         |
| Period DCL 'fast' mode <sup>1)</sup> | $t_{DCL}$    |              | 1/4096 kHz |      |         |
| DCL Duty Cycle                       |              | 40           |            | 60   | %       |
| Period FSC <sup>1)</sup>             | $t_{FSC}$    |              | 125        |      | $\mu$ s |
| FSC setup time                       | $t_{FSC\_S}$ | 70           | $t_{DCLh}$ |      | ns      |
| FSC hold time                        | $t_{FSC\_H}$ | 40           |            |      | ns      |
| DD data in setup time                | $t_{DD\_S}$  | 20           |            |      | ns      |
| DD data in hold time                 | $t_{DD\_H}$  | 50           |            |      | ns      |
| DU data out delay <sup>2)</sup>      | $t_{dDU}$    |              | 150        | 320  | ns      |

<sup>1)</sup> DCL = 4096 kHz:  $t_{FSC} = 512 \times t_{DCL}$

<sup>2)</sup> Depending on Pull up resistor (typical 1 k $\Omega$ ), DU and DD are "open drain"-lines.

### 9.5.3 2-MHz Operation Mode (Mode = 0)



**Electrical Characteristics**
**Table 6      Switching Characteristics**

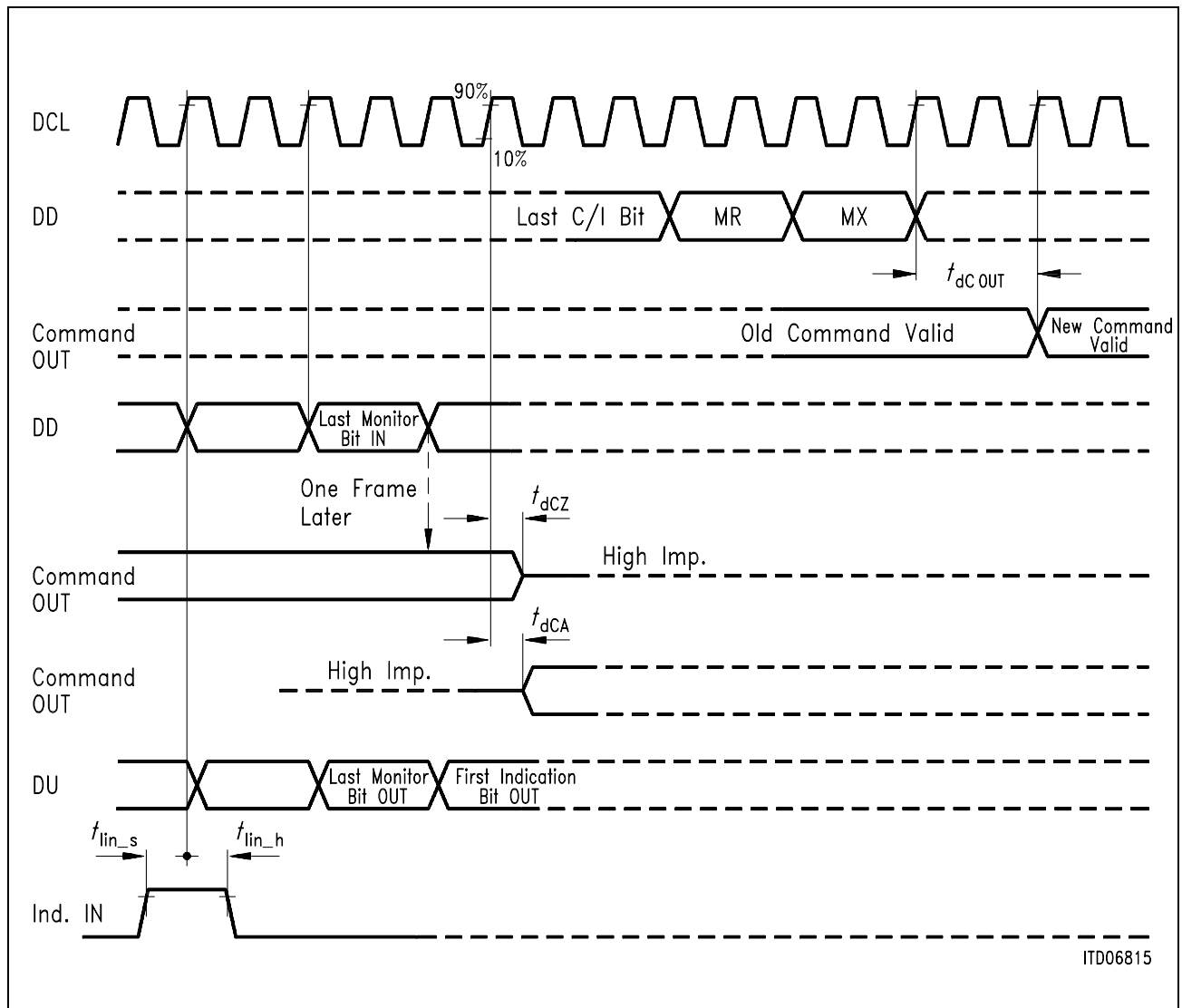
| Parameter                            | Symbol       | Limit Values |            |      | Unit    |
|--------------------------------------|--------------|--------------|------------|------|---------|
|                                      |              | min.         | typ.       | max. |         |
| Period DCL 'slow' mode <sup>1)</sup> | $t_{DCL}$    |              | 1/2048 kHz |      |         |
| DCL Duty Cycle                       |              | 40           |            | 60   | %       |
| Period FSC <sup>1)</sup>             | $t_{FSC}$    |              | 125        |      | $\mu$ s |
| FSC setup time                       | $t_{FSC\_S}$ | 70           | $t_{DCLh}$ |      | ns      |
| FSC hold time                        | $t_{FSC\_H}$ | 40           |            |      | ns      |
| DD data in setup time                | $t_{DD\_S}$  | 20           |            |      | ns      |
| DD data in hold time                 | $t_{DD\_H}$  | 50           |            |      | ns      |
| DU data out delay <sup>2)</sup>      | $t_{dDU}$    |              | 150        | 175  | ns      |

<sup>1)</sup> DCL = 2048 kHz:  $t_{FSC} = 256 \times t_{DCL}$

<sup>2)</sup> Depending on Pull up resistor (typical 1 k $\Omega$ ), DU and DD are "open drain"-lines.

## 9.6 IOM-2 Command/Indication Interface Timing

### 9.6.1 4-MHz Operation Mode (Mode = 1)



### 9.6.2 2-MHz Operation Mode (Mode = 0)

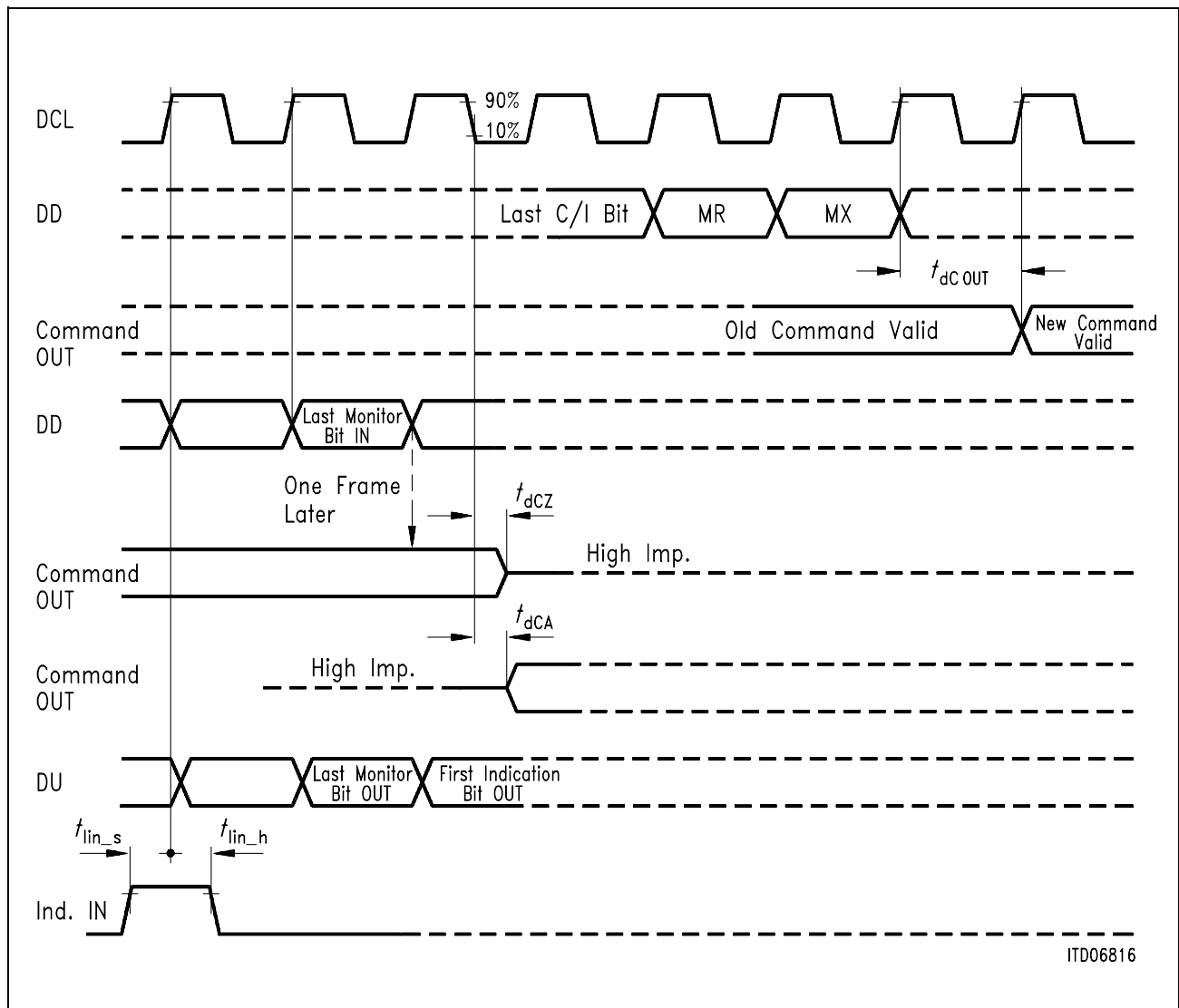


**Table 7 Switching Characteristics**

| Parameter                  | Symbol       | Limit Values |      |      | Unit |
|----------------------------|--------------|--------------|------|------|------|
|                            |              | min.         | typ. | max. |      |
| Command out delay          | $t_{dCout}$  |              | 150  | 250  | ns   |
| Command out high impedance | $t_{dCZ}$    |              | 150  | 250  | ns   |
| Command out active         | $t_{dCA}$    |              | 150  | 250  | ns   |
| Indication in setup time   | $t_{lin\_s}$ | 50           |      |      | ns   |
| Indication in hold time    | $t_{lin\_h}$ | 100          |      |      | ns   |

## 9.7 Detector Select Timing

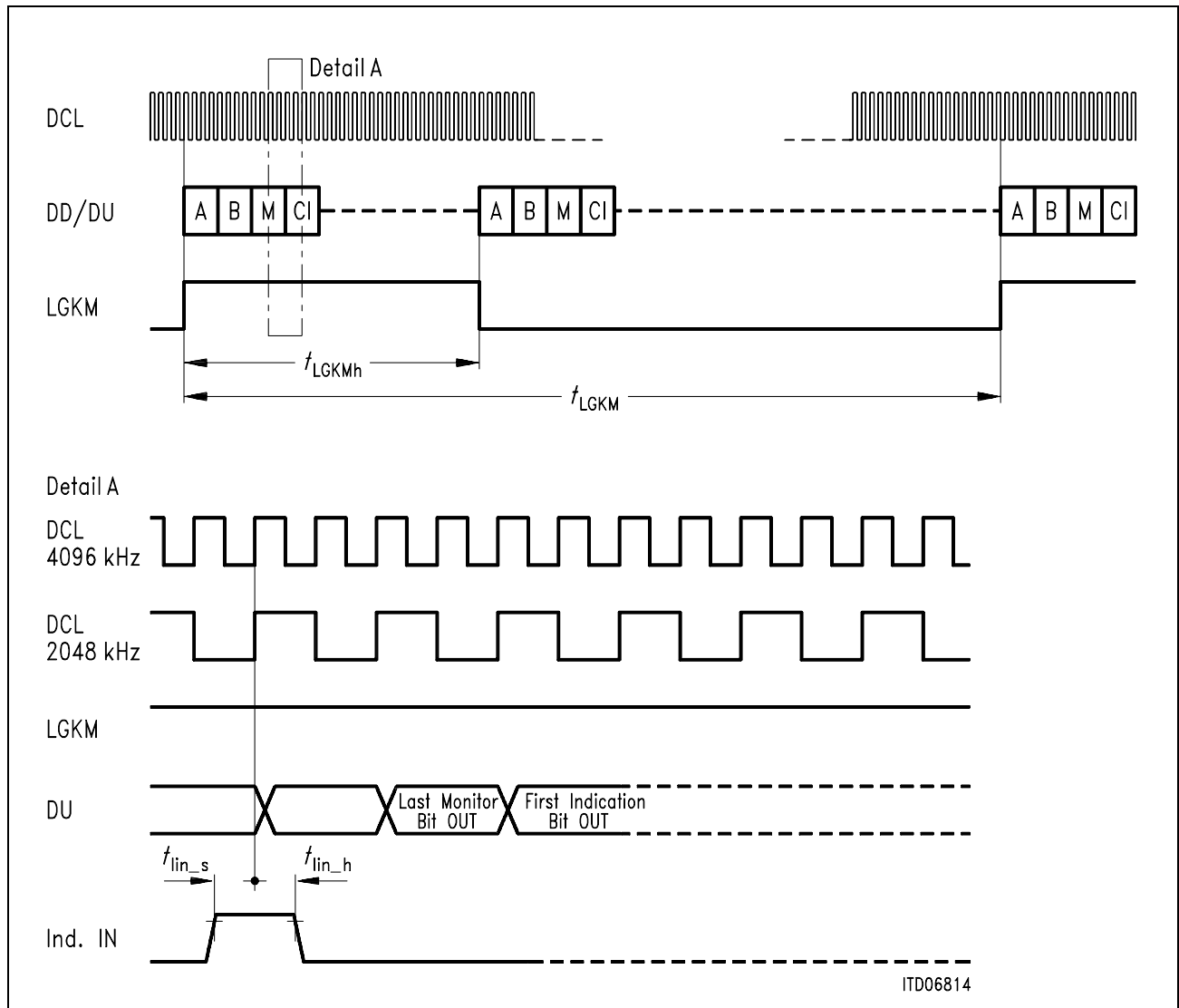


**Table 8 Switching Characteristics**

| Parameter                 | Symbol       | Limit Values |          |      | Unit    |
|---------------------------|--------------|--------------|----------|------|---------|
|                           |              | min.         | typ.     | max. |         |
| Detector select high time | $t_{LGKMh}$  |              | 125      |      | $\mu$ s |
| Detector select repeat    | $t_{LGKM}$   |              | 1 ... 14 |      | ms      |
| Indication in setup time  | $t_{lin\_s}$ | 50           |          |      | ns      |
| Indication in hold time   | $t_{lin\_h}$ | 100          |          |      | ns      |

## 10 Appendix

### 10.1 IOM-2 Interface Monitor Transfer Protocol

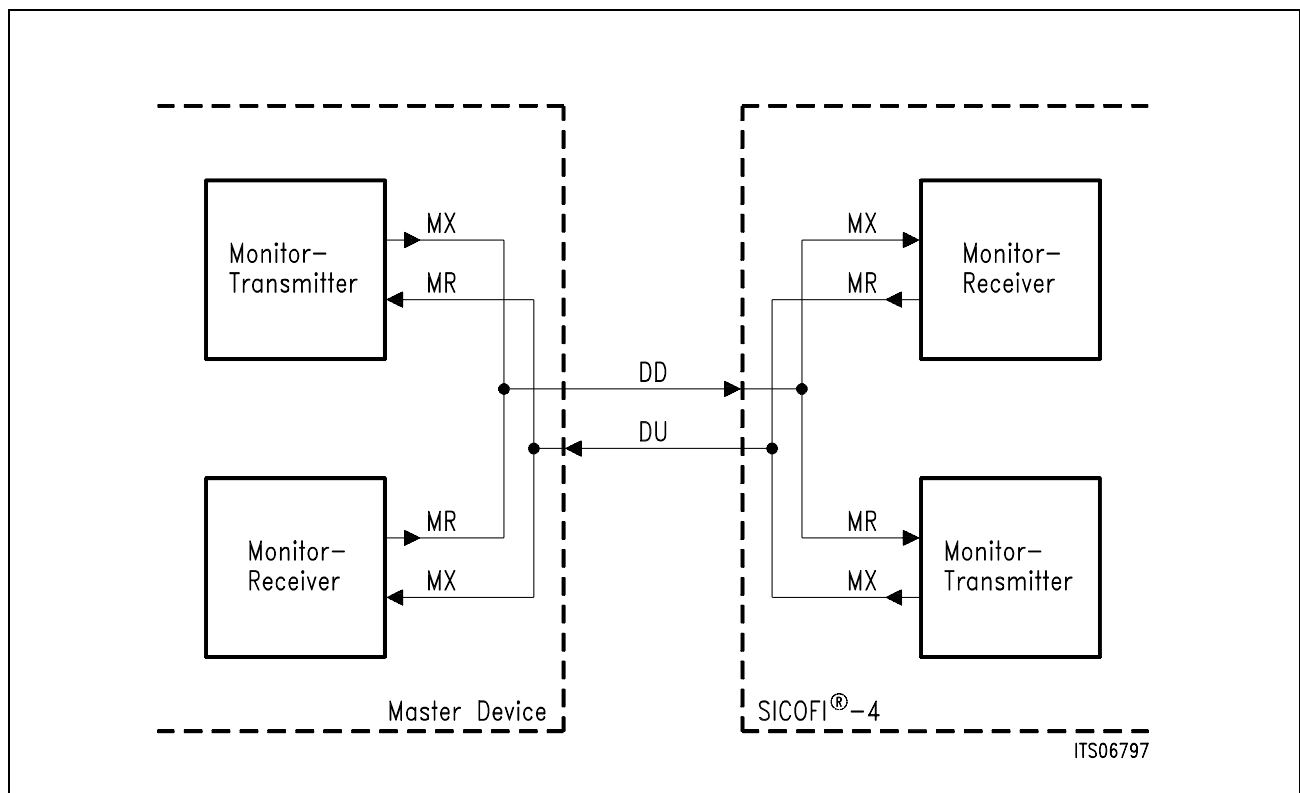
#### 10.1.1 Monitor Channel Operation

The monitor channel is used for the transfer of maintenance information between two functional blocks. Using two monitor control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure. The MR and MX bits in the fourth octet (C/I channel) of the IOM-2 frame are used for the handshake procedure of the monitor channel.

The monitor channel transmission operates on a pseudo-asynchronous basis:

- Data transfer (bits) on the bus is synchronized to Frame Sync FSC
- Data flow (bytes) are asynchronously controlled by the handshake procedure.

For example: Data is placed onto the DD-Monitor-Channel by the Monitor-transmitter of the master device (DD-MX-Bit is activated i.e. set to '0'). This data transfer will be repeated within each frame (125  $\mu$ s rate) until it is acknowledged by the SICOFI-4 Monitor-receiver by setting the DU-MR-bit to '0', which is checked by the Monitor-transmitter of the master device. Thus, the data rate is not 8-kbytes/sec.



### 10.1.2 Monitor Handshake Procedure

The monitor channel works in 3 states

- idle state: A pair of inactive (set to '1') MR- and MX-bits during two or more consecutive frames: End of Message (EOM)
- sending state: MX-bit is activated (set to '0') by the Monitor-transmitter, together with data-bytes (can be changed) on the Monitor-channel
- acknowledging: MR-bit is set to active (set to '0') by the Monitor-receiver, together with a data-byte remaining in the Monitor-channel.

A start of transmission is initiated by a Monitor-transmitter in sending out an active MX-bit together with the first byte of data (the address of the receiver) to be transmitted in the Monitor-channel.

This state remains until the addressed Monitor-Receiver acknowledges the received data by sending out an active MR-bit, which means that the data-transmission is repeated each 125  $\mu$ s frame (minimum is one repetition). During this time the Monitor-transmitter evaluates the MR-bit.

Flow control, means in the form of transmission delay, can only take place when the transmitters MX and the receivers MR bit are in active state.

Since the receiver is able to receive the monitor data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received the receiver will wait for the receipt of two identical successive bytes (last look function).

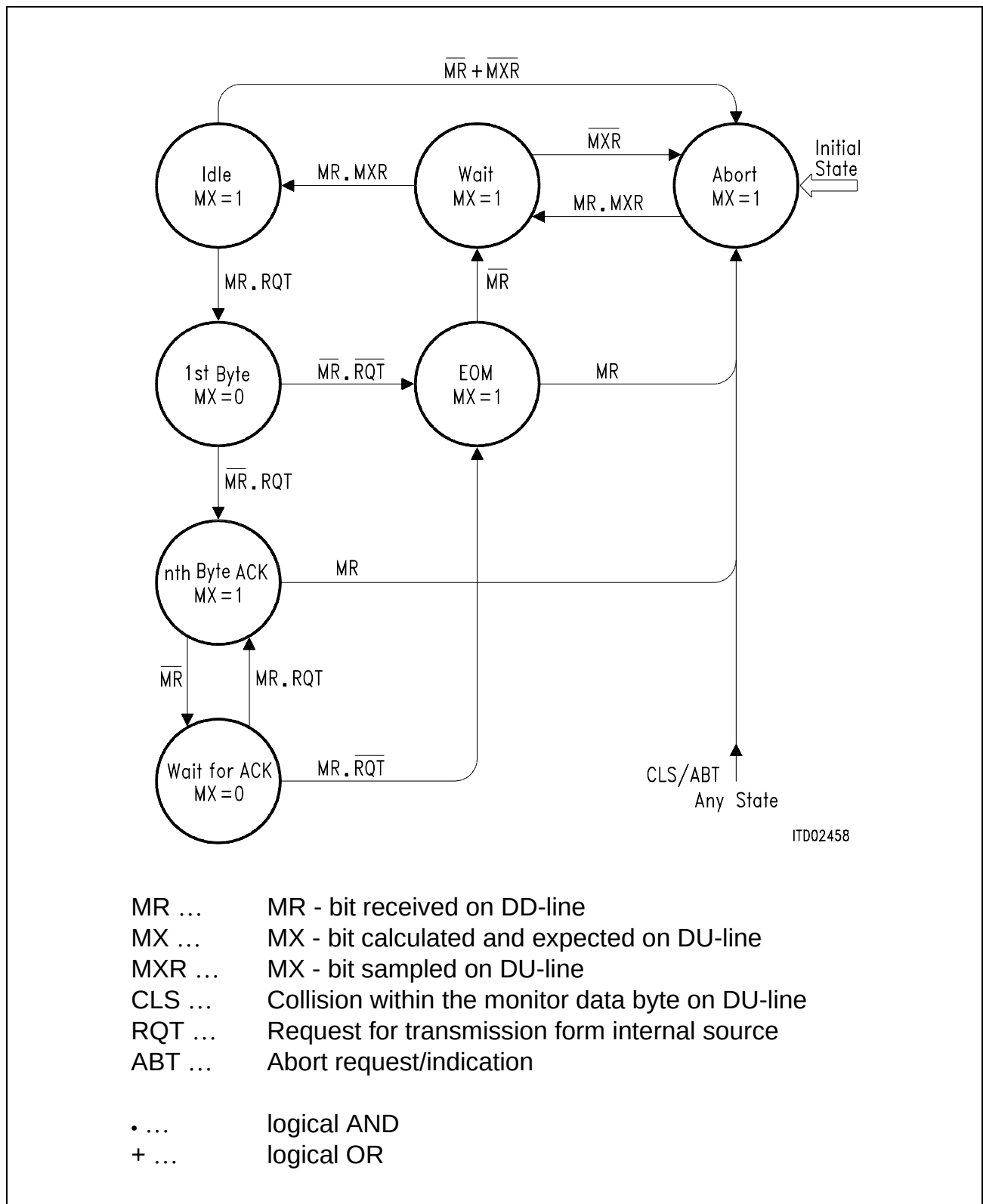
A collision resolution mechanism (check if another device is trying to send data during the same time) is implemented in the transmitter. This is done by looking for the inactive ('1') phase of the MX-bit and making a per bit collision check on the transmitted monitor data (check if transmitted '1's are on DU/DD-line; DU/DD-line are open-drain lines).

Any abort leads to a reset of the SICOFI-4 command stack, the device is ready to receive new commands.

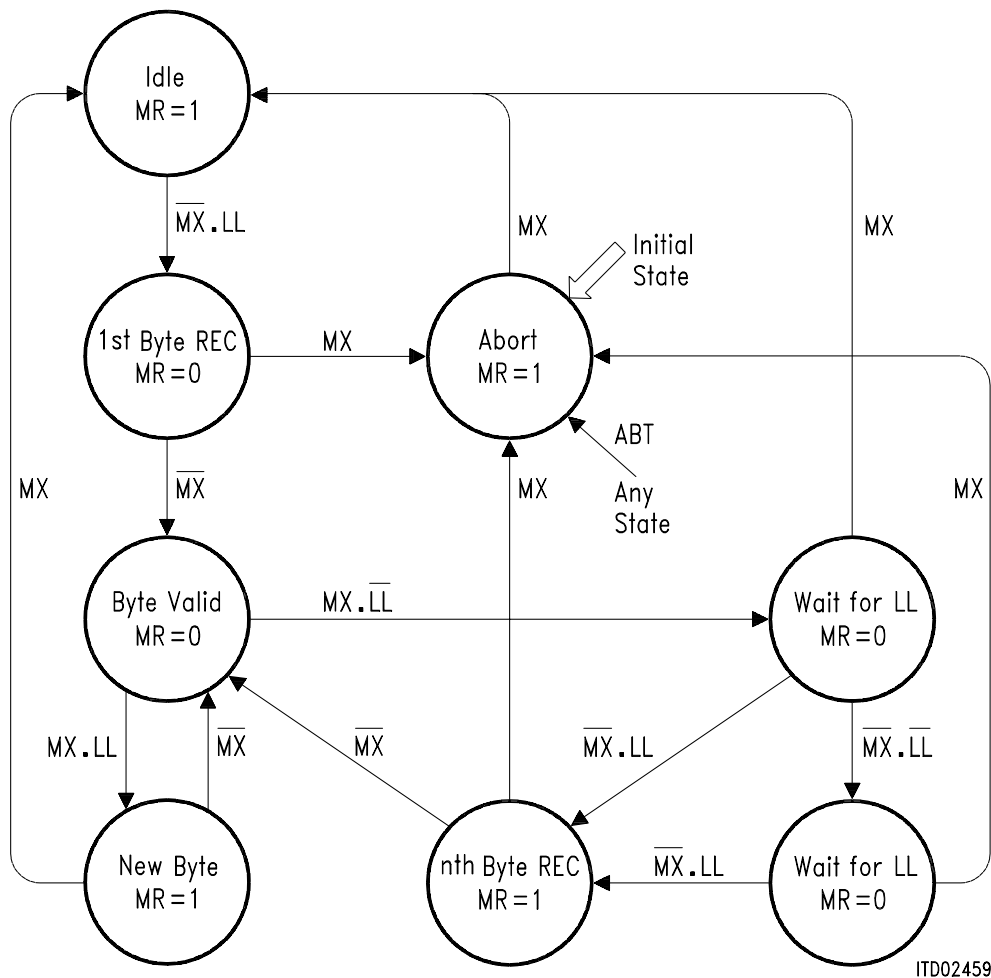
To obtain a maximum speed data transfer, the transmitter anticipates the falling edge of the receivers acknowledgment.

Due to the inherent programming structure, duplex operation is not possible. It is **not allowed** to send any data to the SICOFI-4, while transmission is active.

### 10.1.3 State Diagram of the SICOFI-4 Monitor Transmitter



### 10.1.4 State Diagram of the SICOFI-4 Monitor Receiver



MR ... MR - bit calculated and transmitted on DU-line  
 MX ... MX - bit received data downstream (DD-line)  
 LL ... Last lock of monitor byte received on DD-line  
 ABT ... Abort indication to internal source

• ... logical AND  
 + ... logical OR

### 10.1.5 Monitor Channel Data Structure

The monitor channel is used for the transfer of maintenance information between two functional blocks. By use of two monitor control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure.

#### Address Byte

Messages to and from the SICOFI-4 are started with the following Monitor byte:

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|---|---|---|---|---|---|---|---|
|     | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Thus providing information for two voice channels, the SICOFI-4 is one device on one IOM-2 timeslot. Monitor data for a specific voice channel is selected by the SICOFI-4 specific command (SOP or COP).

#### Identification Command

In order to be able to unambiguously identify different devices by software, a two byte identification command is defined for analog lines IOM-2 devices.

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Each device will then respond with its specific identification code. For the SICOFI-4 this two byte identification code is:

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Each byte is transferred at least twice (in two consecutive frames).

## 10.2 IOM-2 Interface Programming Procedure

Example for a typical IOM-2 Interface programming procedure, consisting of identification request and answer, a SOP Write command with three byte following, and SOP Read to verify the programming.

| Frame | Data down                   |       | Data up                     |       |
|-------|-----------------------------|-------|-----------------------------|-------|
|       | Monitor                     | MR/MX | Monitor                     | MR/MX |
| 1     | 11111111                    | 11    | 11111111                    | 11    |
| 2     | IDRQT. 1 <sup>st</sup> byte | 10    | 11111111                    | 11    |
| 3     | IDRQT. 1 <sup>st</sup> byte | 10    | 11111111                    | 01    |
| 4     | IDRQT. 2 <sup>nd</sup> byte | 11    | 11111111                    | 01    |
| 5     | IDRQT. 2 <sup>nd</sup> byte | 10    | 11111111                    | 11    |
| 6     | 11111111                    | 11    | 11111111                    | 01    |
| 7     | 11111111                    | 11    | IDANS. 1 <sup>st</sup> byte | 10    |
| 8     | 11111111                    | 01    | IDANS. 1 <sup>st</sup> byte | 10    |
| 9     | 11111111                    | 01    | IDANS. 2 <sup>nd</sup> byte | 11    |
| 10    | 11111111                    | 11    | IDANS. 2 <sup>nd</sup> byte | 10    |
| 11    | 11111111                    | 01    | 11111111                    | 11    |
| 12    | Address                     | 10    | 11111111                    | 11    |
| 13    | Address                     | 10    | 11111111                    | 01    |
| 14    | SOP Write                   | 11    | 11111111                    | 01    |
| 15    | SOP Write                   | 10    | 11111111                    | 11    |
| 16    | CR3                         | 11    | 11111111                    | 01    |
| 17    | CR3                         | 10    | 11111111                    | 11    |
| 18    | CR2                         | 11    | 11111111                    | 01    |
| 19    | CR2                         | 10    | 11111111                    | 11    |
| 20    | CR1                         | 11    | 11111111                    | 01    |
| 21    | CR1                         | 10    | 11111111                    | 11    |
| 22    | SOP Read                    | 11    | 11111111                    | 01    |
| 23    | SOP Read                    | 10    | 11111111                    | 11    |
| 24    | 11111111                    | 11    | 11111111                    | 01    |
| 25    | 11111111                    | 11    | Address                     | 10    |
| 26    | 11111111                    | 01    | Address                     | 10    |

| Frame | Data down |       | Data up  |       |
|-------|-----------|-------|----------|-------|
|       | Monitor   | MR/MX | Monitor  | MR/MX |
| 27    | 11111111  | 01    | CR3      | 11    |
| 28    | 11111111  | 11    | CR3      | 10    |
| 29    | 11111111  | 01    | CR2      | 11    |
| 30    | 11111111  | 11    | CR2      | 10    |
| 31    | 11111111  | 01    | CR1      | 11    |
| 32    | 11111111  | 11    | CR1      | 10    |
| 33    | 11111111  | 01    | 11111111 | 11    |

IDRQT ... identification request (80<sub>H</sub>, 00<sub>H</sub>)

IDANS ... answer to identification request (80<sub>H</sub>, 82<sub>H</sub>)

Address ... SICOFI-4 specific address byte (81<sub>H</sub>)

CRx ... Data for/from configuration register x.

## **10.3 Test Features**

### **10.3.1 Boundary Scan**

#### **General**

The SICOFI-4 provides fully IEEE Std. 1149.1 compatible boundary scan support consisting of:

- a complete boundary scan (digital pins)
- a test access port controller (TAP)
- four dedicated pins (TCK, TMS, TDI, TDO)
- a 32 bit ICODE register

All SICOFI-4 digital pins expect power supply VDDD and ground GNDD are included in the boundary scan. Depending on the pin functionality one, two or three boundary cells are provided.

| <b>Pin Type</b> | <b>Number of Boundary Scan Cells</b> | <b>Usage</b>          |
|-----------------|--------------------------------------|-----------------------|
| Input           | 1                                    | Input                 |
| Output          | 2                                    | Output, enable        |
| I/O             | 3                                    | Input, output, enable |

When the TAP controller is in the appropriate mode, data is shifted into/out of the boundary scan via the pins TDI/TDO controlled by the clock applied to pin TCK.

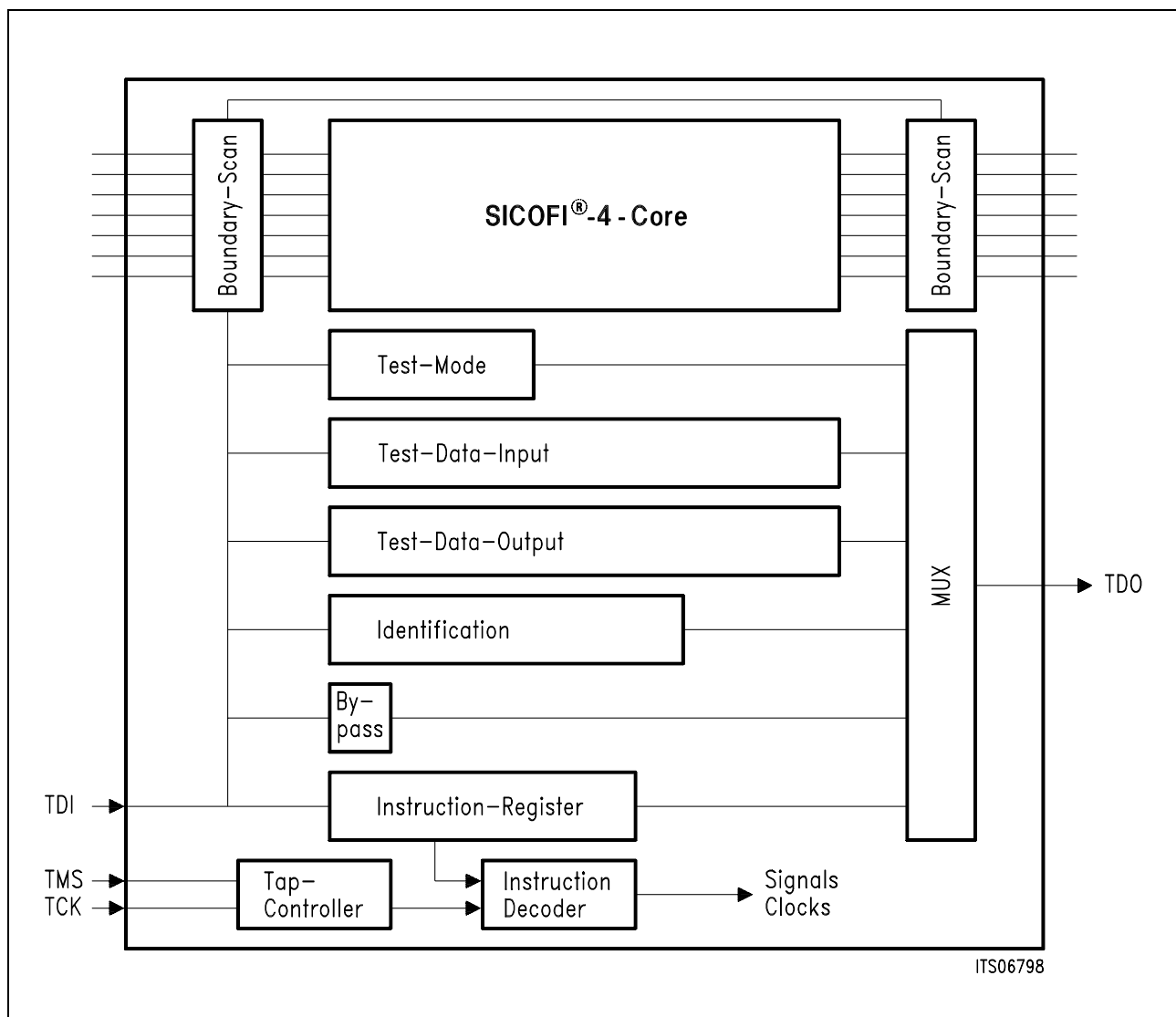
The SICOFI-4 pins are included in the following sequence in the boundary scan:

| Pin No. | Pin Name | Type           |
|---------|----------|----------------|
| 57      | MODE     | I              |
| 59      | TSS1     | I              |
| 60      | TSS0     | I              |
| 61      | SI3_2    | I              |
| 62      | SI3_1    | I              |
| 63      | SI3_0    | I              |
| 64      | SB3_1    | I/O            |
| 1       | SB3_0    | I/O            |
| 2       | SO3_2    | O              |
| 3       | SO3_1    | O              |
| 4       | SO3_0    | O              |
| 13      | SO4_0    | O              |
| 14      | SO4_1    | O              |
| 15      | SO4_2    | O              |
| 16      | SB4_0    | I/O            |
| 17      | SB4_1    | I/O            |
| 18      | SI4_0    | I              |
| 19      | SI4_1    | I              |
| 20      | SI4_2    | I              |
| 21      | LGKM1    | O              |
| 22      | RESET    | I              |
| 24      | DD       | I              |
| 25      | DU       | O (open drain) |
| 26      | DCL      | I              |
| 27      | FSC      | I              |
| 28      | LGKM0    | O              |
| 29      | SI1_2    | I              |
| 30      | SI1_1    | I              |
| 31      | SI1_0    | I              |
| 32      | SB1_1    | I/O            |
| 33      | SB1_0    | I/O            |

| Pin No. | Pin Name | Type |
|---------|----------|------|
| 34      | SO1_2    | O    |
| 35      | SO1_1    | O    |
| 36      | SO1_0    | O    |
| 45      | SO2_0    | O    |
| 46      | SO2_1    | O    |
| 47      | SO2_2    | O    |
| 48      | SB2_0    | I/O  |
| 49      | SB2_1    | I/O  |
| 50      | SI2_0    | I    |
| 51      | SI2_1    | I    |
| 52      | SI2_0    | I    |

### 10.3.2 The TAP-Controller

The Test Access Port (TAP) controller implements the state machine defined in the JTAG standard IEEE Std. 1149.1. Transitions on pin TMS (Test Mode Select) cause the TAP controller to perform a state change. According to the standard definition five instructions are executable:



| Code | Instruction        | Function                                        |
|------|--------------------|-------------------------------------------------|
| 0000 | EXTEST             | External testing                                |
| 0001 | INTEST             | Internal testing                                |
| 0010 | SAMPLE/<br>PRELOAD | Snap-shot testing                               |
| 0011 | ICODE              | Reading ID code                                 |
| 0100 | Tap_Test 1         | Configuration for Level Metering                |
| 0101 | Tap_Test 2         | Wait for result                                 |
| 1000 | Tap_Test 5         | Serial testdata output (Level Metering Results) |
| 0111 | Tap_Test 4         | Switch off Test                                 |
| 11xx | BYPASS             | Bypass operation                                |

|                        |                                                                                                                                                                                                                                                                                       |
|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>EXTEST:</b>         | Is used to examine the board interconnections.                                                                                                                                                                                                                                        |
| <b>INTEST:</b>         | Supports internal chip testing (is the default value of the instruction register)                                                                                                                                                                                                     |
| <b>SAMPLE/PRELOAD:</b> | Provides a snap-shot of the pin level during normal operation, or<br>is used to preload the boundary scan with a test vector                                                                                                                                                          |
| <b>ICODE:</b>          | The 32 bit identification register is serially read out via TDO. It contains a version number (4 bit), a device code (16 bit) and the manufacture code (11bit). The LSB is fixed to '1'.<br>For the SICOFI-4 V2.2 and V2.3 the Code is:<br>'0011 0000 0000 0001 0101 0000 1000 001 1' |
| <b>TAP_TEST1</b>       | 39 bit field for selecting operation<br>(Level Metering Offset, Loops, Tone Generator...)                                                                                                                                                                                             |
| <b>TAP_TEST2:</b>      | Wait for Level Metering result ready (should be > t.b.d. mS)                                                                                                                                                                                                                          |
| <b>TAP_TEST5:</b>      | Level Metering Data output (1 bit result of Level Metering per channel)                                                                                                                                                                                                               |
| <b>TAP_TEST4:</b>      | Level Metering Operation is switched off                                                                                                                                                                                                                                              |
| <b>BYPASS:</b>         | A bit entering TDI is shifted to TDO after one TCK clock cycle                                                                                                                                                                                                                        |

### 10.3.3 Level Metering Function

The Level Metering Function is a functional selftest (available per channel), which allows selftest of the chip (digital, or digital and analogue), and also selftest of the board (including the SLIC).

An external or internally generated sine-wave signal is fed to the receive path. After switching a loop (internal or external via the SLIC) to the Transmit-path the return level is measured and compared to a programmable offset value. The result of this operation (greater or smaller than offset) can be read out via the IOM-2 interface (bit LMR in configuration register CR2).

There is a single 8 bit Offset-Register available for all the 4 channels. This offset register can be accessed as XR4 with a XOP-Command (Field LSEL = 100)

This register contains the 2's complement offset value for the level metering function.

|     |     |     |     |     |     |     |     |     |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Bit | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|     | OF7 | OF6 | OF5 | OF4 | OF3 | OF2 | OF1 | OF0 |

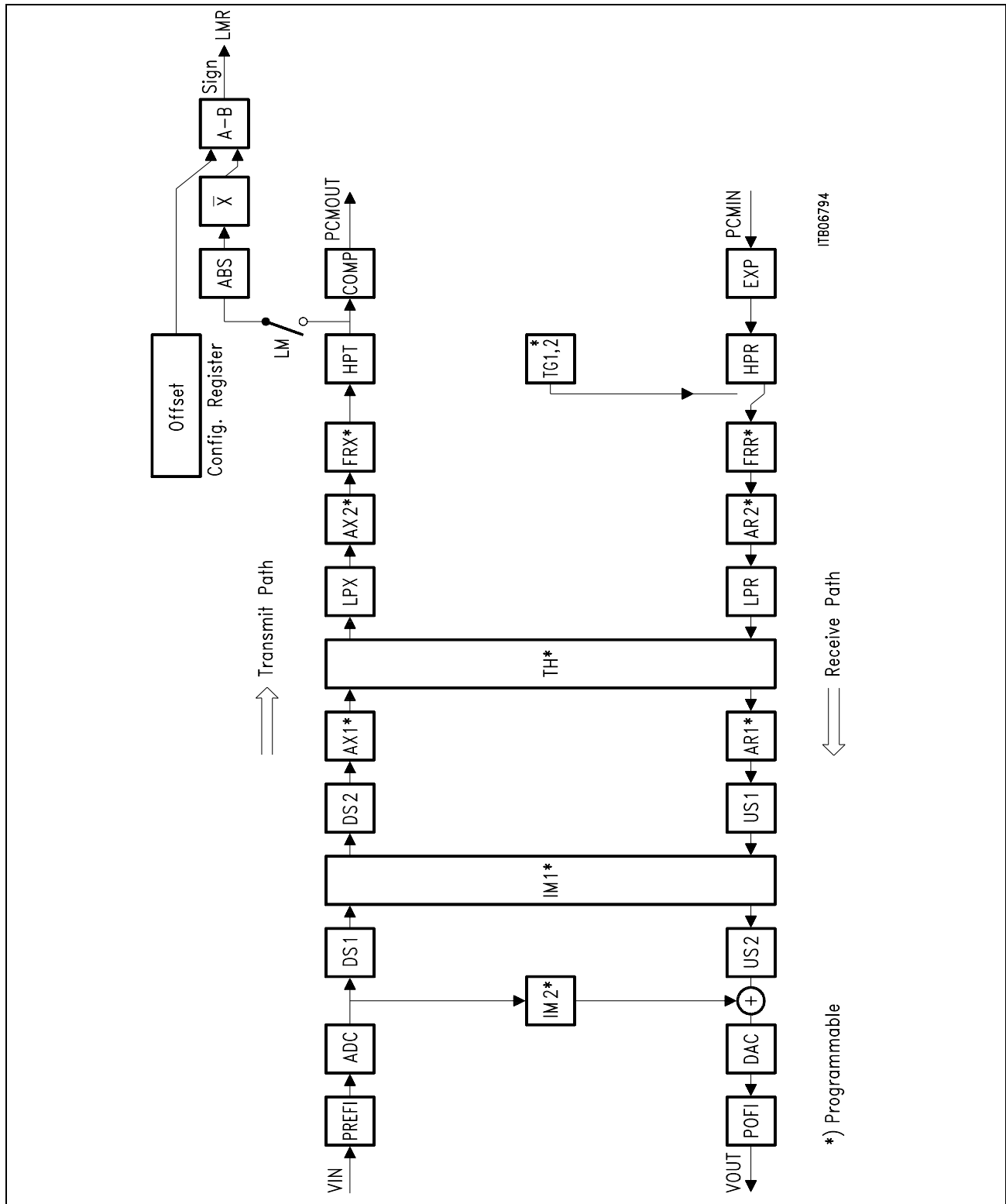


**Figure 22 Block Diagram**

(For further information, an application-note describing the calculation of the offset value and the sensitivity, is available)

### 10.3.4 Using the Level Metering Function

#### Task

An external sine wave (applied to the analog input pin  $V_{IN}$ ) or an internally generated sine wave signal (via tone generator TG1 or via test loops) is sent to the SICOFI-4 transmit path. This signal will be rectified and the power of this signal will be compared to the programmable offset value of the level metering function. If the measured power exceeds a certain value the LMR bit of the register CR2 is set to '1'.

In the appendix you will find a printout of the Track file to test the SICOFI-4 level metering function.

The following steps show how to detect a sine wave with a frequency of 2 kHz and a PCM level  $L = 0$  dB (like measured with the PCM4 in the A/D measurement).

#### Step 1

The SICOFI-4 extended register XR4 holds the offset value for the level metering function. With the QSICOS utility program 'Calculation of Level Metering Function' the programming byte for this register XR4 can be calculated. In our case the Level  $L$  will be 0 dB.

Bytes for Level Metering Register XR4: 71

#### Step 2

The level metering function is always used together with a bandpass filter. The programming of this bandpass filter has to be done by programming the tone-generator coefficients of the tone generator TG2. (During Level Metering Function enabled, TG2 is not available). For this example the coefficients of the TG2 for a frequency of  $f = 2000$  Hz have to be calculated using the QSICOS utility program 'Calculate Tone Generator Coefficients':

Bytes for Tone Generator 2 (0D): 00, 80, 40, 09

#### Step 3

The SICOFI-4 extended register XR4 has to be programmed.

#### Step 4

In the SICOFI-4 configuration register CR2 the level metering bit LM has to be set to '1' and the programmed frequency for the tone generator 2 has to be chosen by setting the PTG2 bit to '1'.

Example for writing the CR2 register: 0 0 1 0 0 0 1 0 =  $22_{\text{H}}$  (A-Law is selected)

**Step 5**

After sending the sine wave in the SICOFI-4 transmit path the result of the Level Metering function will be present in the LMR bit of the configuration register CR2.

Examples for reading back the CR2 register:

0 0 1 0 0 0 1 0 = 22<sub>H</sub> Level was lower than reference

0 0 1 1 0 0 1 0 = 32<sub>H</sub> Level was higher than reference

**Step 6**

By programming different levels for the level metering function the actual PCM coded level can be found. Also a change of the AX1 gain filter will change the PCM level in the transmit path.

If an analog signal is applied to the SICOFI-4 analog input, the level of this analog signal can be calculated. To calculate the analog level, the gain setting of the SICOFI-4 filters together with the 0 dBm0 reference voltage have to be taken into account.

## 10.4 Programming the SICOFI-4 Tone Generators

Two independent Tone Generators are available per channel. When one or both tone-generators are switched on, the voice signal is switched off automatically for the selected voice channel. To make the generated signal sufficient for DTMF, a programmable bandpass-filter is included. The default frequency for both tone generators is 1000 Hz.

The QSICOS-program contains a program for generating coefficients for variable frequencies.

Byte sequences for programming both the tone generators and the bandpass-filters:

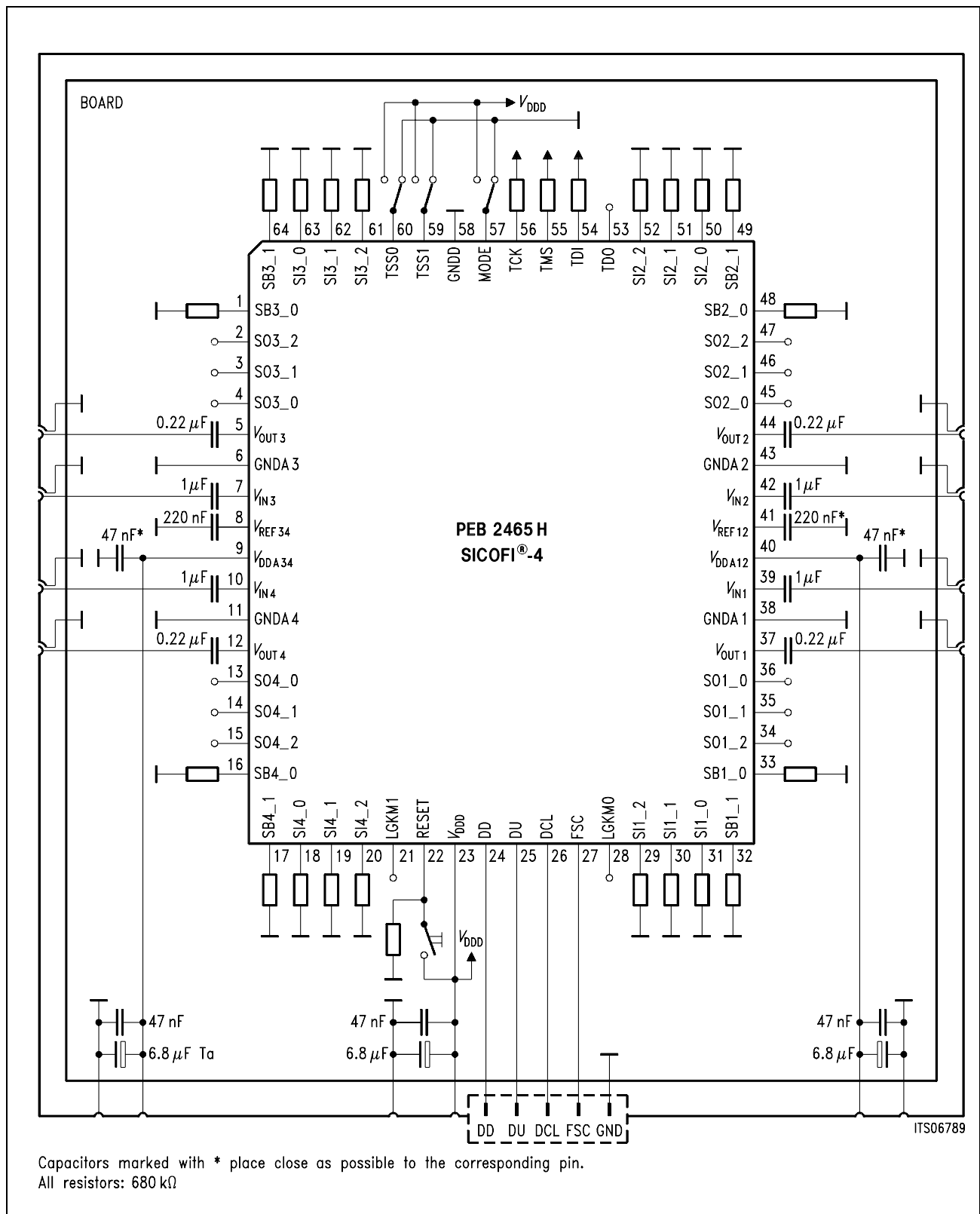
| Frequency | Command             | Byte 1 | Byte 2 | Byte 3 | Byte 4 |
|-----------|---------------------|--------|--------|--------|--------|
| 697 Hz    | 0C/0D <sup>1)</sup> | 0A     | 33     | 5A     | 2C     |
| 770 Hz    | 0C/0D <sup>1)</sup> | 12     | 33     | 5A     | C3     |
| 852 Hz    | 0C/0D <sup>1)</sup> | 13     | 3C     | 5B     | 32     |
| 941 Hz    | 0C/0D <sup>1)</sup> | 1D     | 1B     | 5C     | CC     |
| 1209 Hz   | 0C/0D <sup>1)</sup> | 32     | 32     | 52     | B3     |
| 1336 Hz   | 0C/0D <sup>1)</sup> | EC     | 1D     | 52     | 22     |
| 1477 Hz   | 0C/0D <sup>1)</sup> | AA     | AC     | 51     | D2     |
| 800 Hz    | 0C/0D <sup>1)</sup> | 12     | D6     | 5A     | C0     |
| 950 Hz    | 0C/0D <sup>1)</sup> | 1C     | F0     | 5C     | C0     |
| 1008 Hz   | 0C/0D <sup>1)</sup> | 1A     | AE     | 57     | 70     |
| 2000 Hz   | 0C/0D <sup>1)</sup> | 00     | 80     | 50     | 09     |

<sup>1)</sup> 0C is used for programming Tone Generator 1, in channel 1(3).

0D is used for programming Tone Generator 2, in channel 1(3).

The resulting signal amplitude can be set by transmitting the AR1 and AR2 filters. By switching a 'digital loop' the generated sine-wave signal can be fed to the transmit path.

## 11 Proposed Test Circuit



## 12 Board Layout Recommendation

### 12.1 Board Layout

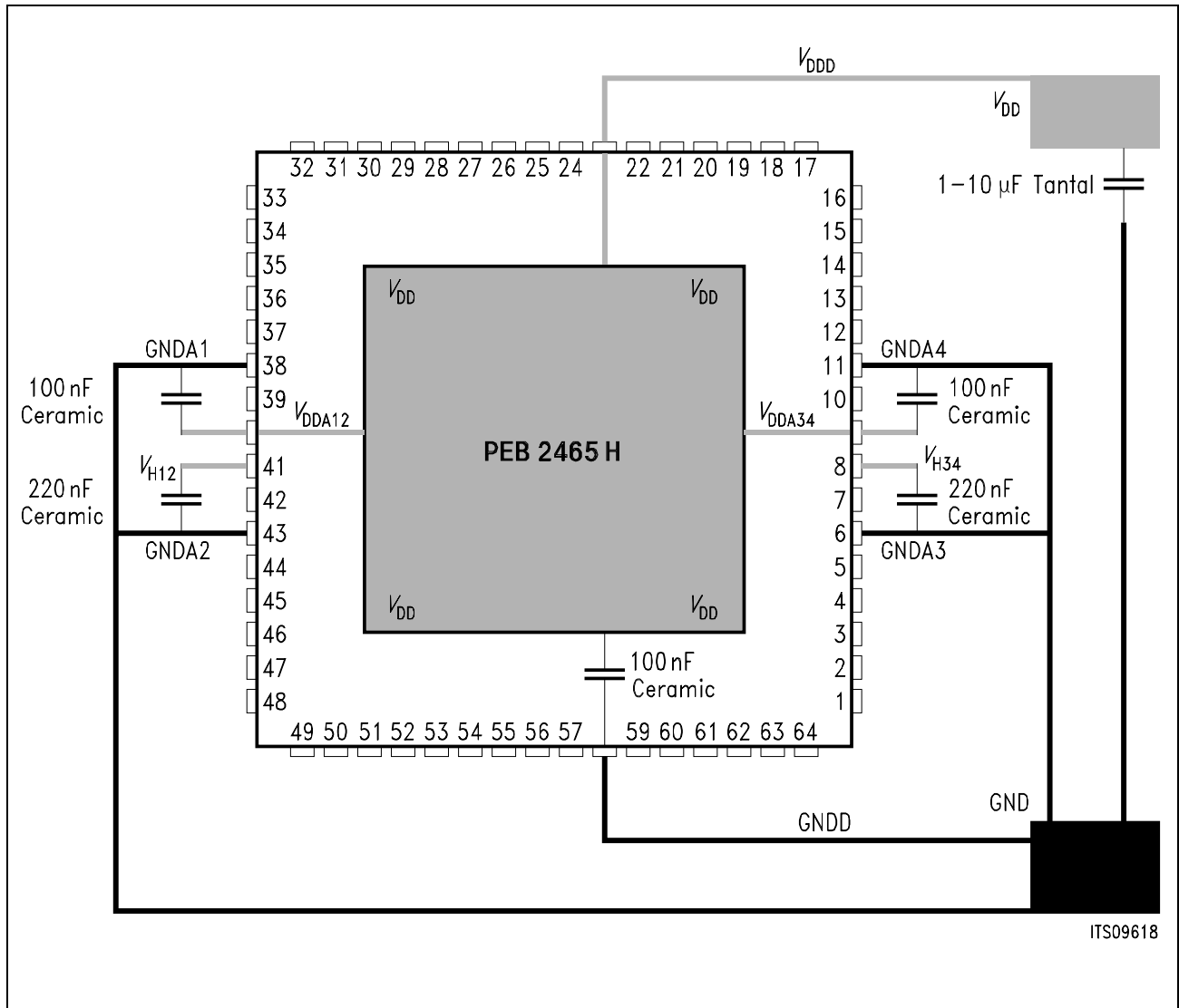
Keep in mind that inside the SICOFI-4 all the different  $V_{DD}$ -supplies are connected via the substrate of the chip, and the areas connected to different grounds are separated on chip.

- a) Separate all digital supply lines from analog supply lines as long as possible.
- b) Use a separate GND-connection for the capacitors which are filtering the Reference voltage (220 nF ceramic-capacitor at  $V_{H12}/V_{H34}$ ).
- c) Don't use a common ground-plane under the SICOFI-4.
- d) Use a large ground-plane (distant from the SICOFI-4) and use different ground lines for connecting the SICOFI-4: one common analog ground and a separate digital ground.

### 12.2 Filter Capacitors

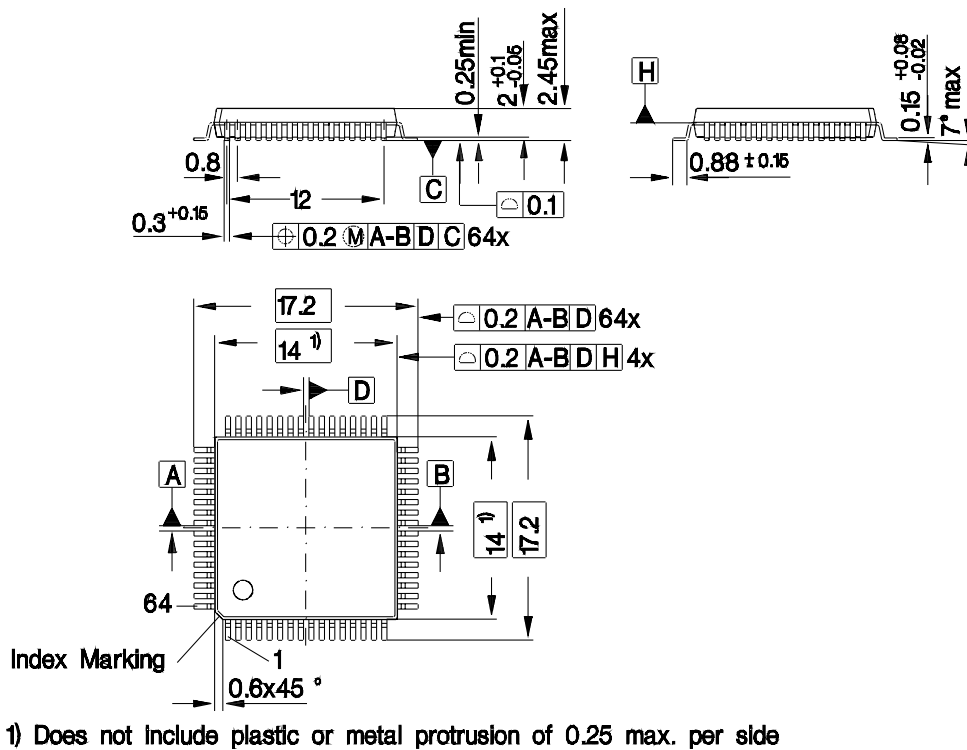
- a) To achieve a good filtering for the high frequency band, place SMD ceramic-capacitors with 100 nF from  $V_{DDA12}$  and  $V_{DDA34}$  to GNDA.
- b) One 100 nF SMD ceramic-capacitor is needed to filter the digital supply ( $V_{DDD}$  to GNDD).
- c) Use 220 nF ceramic-capacitors to connect  $V_{H12}$  and  $V_{H34}$  to analog ground.
- d) Place all filter capacitors as close as possible to the SICOFI-4 (most important!!!).
- e) Use one central Tantalum-capacitor with about 1  $\mu$ F to 10  $\mu$ F to block  $V_{DD}$  to GND.

## Board Layout Recommendation



## 13 Package Outlines

**Plastic Package, P-MQFP-64 (SMD)**  
(Plastic Metric Quad Flat Package)



GPM0525

## Sorts of Packing

Package outlines for tubes, trays etc. are contained in our

SMD = Surface Mounted Device

Dimensions in mm





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Dr. Ulrich Schumacher

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