

FMM5051VU

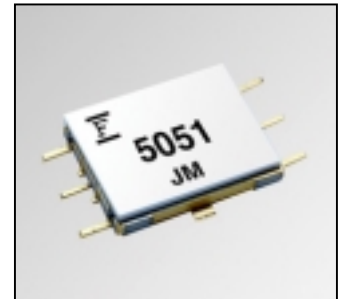
Ku band Power Amplifier MMIC

FEATURES

- High Output Power: 31.5dBm(typ.)
- High Linear Gain: 31.5dB(typ.)
- Low Input VSWR
- Broad Band: 13.75~14.5GHz
- Impedance Matched $Z_{in}/Z_{out} = 50\Omega$
- Small Hermetic Metal-Ceramic SMT Package(VU)

DESCRIPTION

The FMM5051VU is a MMIC amplifier that contains a three-stage amplifier, internally matched, for standard communications in the 13.75 to 14.5GHz frequency range. This product is well suited for VSAT applications as it offers high power, high gain, and low VSWR.



Eudyna's stringent Quality Assurance Program assures the highest reliability and consistent performance.

ABSOLUTE MAXIMUM RATING

Item	Symbol	Rating	Unit
Drain-Source Voltage	VDD	+8	V
Gate-Source Voltage	VGG	-3	V
Input Power	P _{in}	+8	dBm
Storage Temperature	T _{stg}	-55 to +125	°C

RECOMMENDED OPERATING CONDITION

Item	Symbol	Condition	Unit
DC Input Voltage	VDD	+5	V
DC Input Voltage	VGG	0	V
Operating Case Temperature	T _c	-40 to +85	°C

ELECTRICAL CHARACTERISTICS (Case Temperature T_c=25°C)

Item	Symbol	Condition	Limit			Unit
			Min.	Typ.	Max.	
Output Power	P _{out}	VDD=5V VGG=0V f=13.75~14.50GHz P _{in} =+3dBm	30.8	31.5	-	dBm
Linear Gain (Note 1)	GL		30.0	31.5	-	dB
Total Drain Current	I _{ddt}		-	800	1000	mA
Power Added Efficiency	η_{add}		-	35.0	-	%
Gain Flatness (Note 1)	ΔG		-	1.5	2.0	dB
Input Return Loss (Note 1)	RL _{in}		-	-9	-6	dB
Output Return Loss (Note 1)	RL _{out}		-	-9	-6	dB

Note 1 : P_{in}=-10dBm

ESD	Class 0	~ 199V
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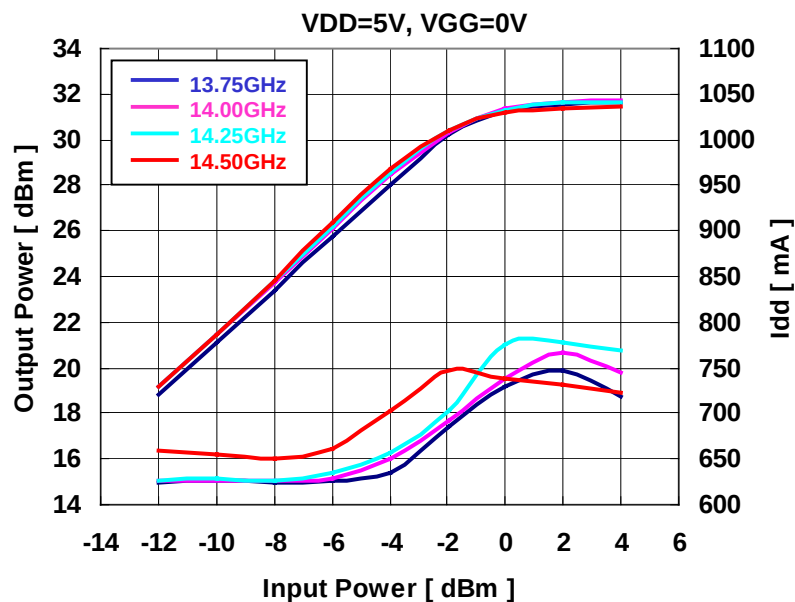
Note : Based on EIAJ ED-4701 C-111A(C=100pF, R=1.5k Ω)

CASE STYLE : VU

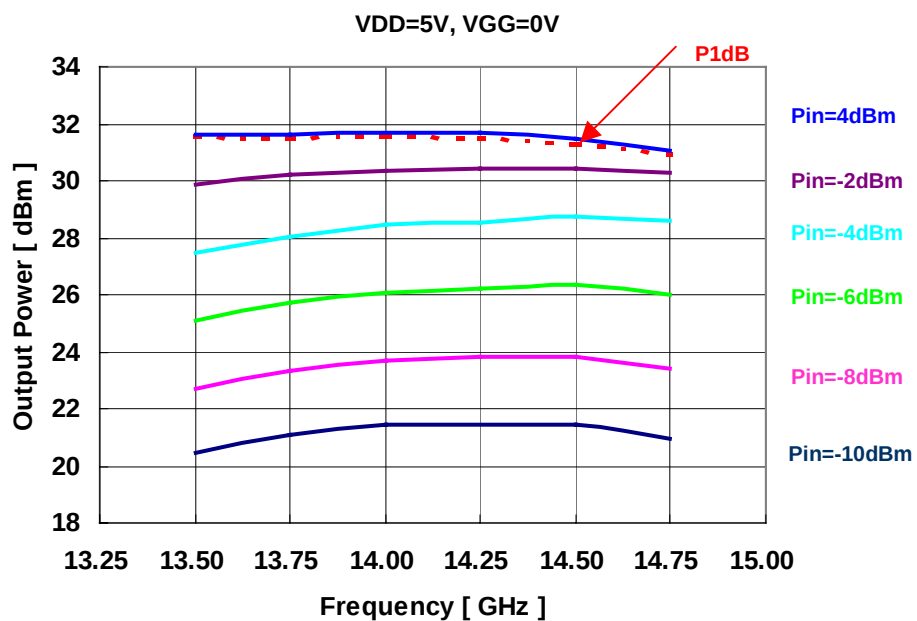
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OUTPUT POWER, DRAIN CURRENT vs. INPUT POWER



OUTPUT POWER vs. FREQUENCY

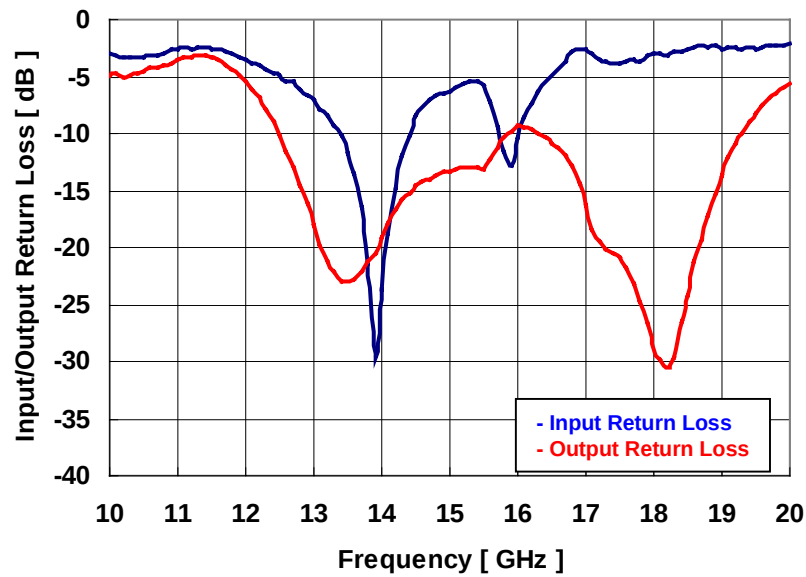


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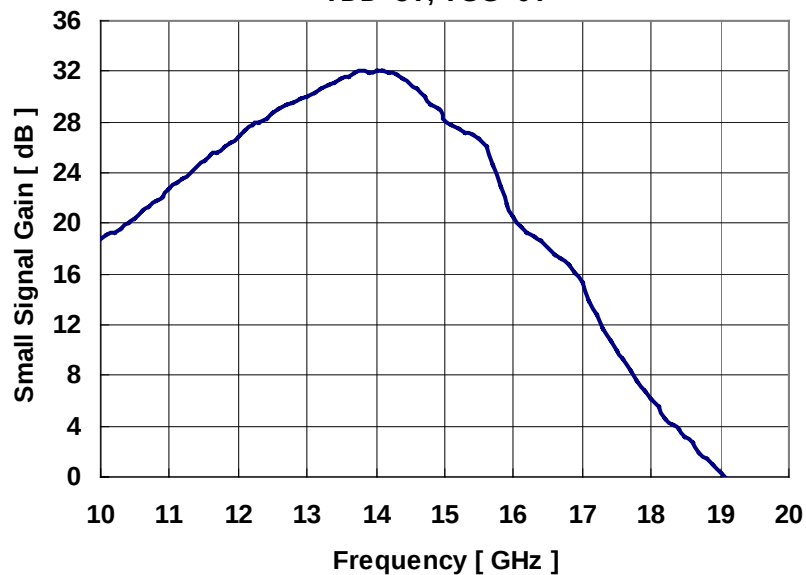
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■ S-PARAMETERS

Input/Output Return Loss vs. Frequency
VDD=5V, VGG=0V



Small Signal Gain vs. Frequency
VDD=5V, VGG=0V



※ S-parameter was taken with PCB in Page 6.

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■ S-PARAMETERS

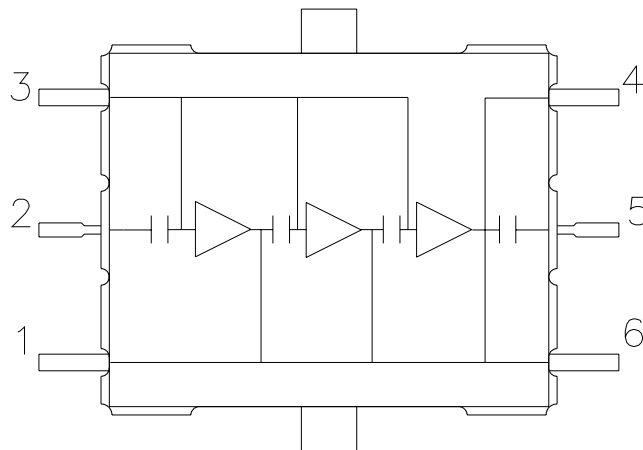
VDD=5V, VGG=0V

Frequency [GHz]	S 11		S 21		S 12		S 22	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
1.0	0.960	-38.0	0.013	149.0	0.001	55.0	0.989	-41.3
2.0	0.901	-66.1	0.062	95.7	0.001	-14.1	0.946	-72.2
3.0	0.858	-102.0	0.348	-110.1	0.001	-146.8	0.924	-111.4
4.0	0.793	-154.0	0.331	28.3	0.001	58.5	0.904	-167.9
5.0	0.810	163.4	0.478	-96.4	0.002	-84.5	0.869	148.6
6.0	0.778	134.7	2.534	96.5	0.002	40.1	0.789	103.0
7.0	0.763	87.0	5.072	-143.2	0.001	-72.2	0.641	33.3
8.0	0.822	51.4	5.596	14.9	0.001	-174.4	0.385	-34.3
9.0	0.826	40.2	6.908	178.9	0.001	42.3	0.343	132.0
10.0	0.708	10.6	8.722	-8.2	0.002	-52.4	0.565	67.1
11.0	0.732	-21.7	13.732	160.4	0.005	110.3	0.669	-0.4
12.0	0.661	-53.9	22.054	-47.9	0.002	-69.9	0.533	-73.7
13.0	0.442	-94.4	31.712	88.9	0.001	-139.0	0.126	-139.0
13.1	0.405	-100.5	32.711	66.2	0.001	-161.2	0.103	-146.3
13.2	0.376	-106.0	33.863	43.3	0.001	-167.5	0.087	-153.7
13.3	0.345	-111.4	35.530	20.2	0.001	175.1	0.079	-162.4
13.4	0.307	-119.6	35.695	-3.1	0.001	-176.6	0.071	-170.6
13.5	0.260	-126.5	36.939	-26.7	0.001	154.4	0.071	-175.8
13.6	0.213	-137.3	38.118	-50.7	0.001	155.3	0.072	178.6
13.7	0.149	-145.7	39.215	-75.8	0.002	127.7	0.079	173.5
13.8	0.085	-165.3	40.315	-100.6	0.002	129.6	0.086	166.3
13.9	0.033	150.1	39.596	-125.1	0.002	110.5	0.094	161.3
14.0	0.066	67.7	40.096	-151.1	0.002	89.6	0.111	155.4
14.1	0.116	31.5	39.888	-176.7	0.002	83.9	0.127	146.8
14.2	0.184	20.6	39.321	157.8	0.002	67.9	0.147	137.5
14.3	0.252	11.1	38.610	132.0	0.002	57.4	0.161	128.1
14.4	0.310	2.4	37.032	106.6	0.002	40.5	0.172	119.1
14.5	0.376	-3.0	35.438	81.2	0.002	25.8	0.187	109.2
14.6	0.413	-10.0	33.702	55.7	0.001	23.9	0.196	99.9
14.7	0.449	-18.7	31.595	30.9	0.001	5.4	0.200	91.2
14.8	0.468	-24.2	29.637	6.0	0.001	15.6	0.207	82.2
14.9	0.473	-29.1	28.136	-17.8	0.002	-0.8	0.214	74.0
15.0	0.482	-33.5	25.564	-40.4	0.002	0.4	0.214	67.2
16.0	0.301	-45.9	10.535	82.7	0.006	-151.0	0.340	17.2
17.0	0.739	-116.6	5.781	-135.9	0.010	-14.0	0.153	-32.8
18.0	0.707	-134.3	2.027	21.5	0.004	57.8	0.036	-40.5
19.0	0.738	-146.4	1.038	175.2	0.006	-111.7	0.207	8.5
20.0	0.780	152.4	0.381	-66.2	0.005	67.2	0.520	-7.9

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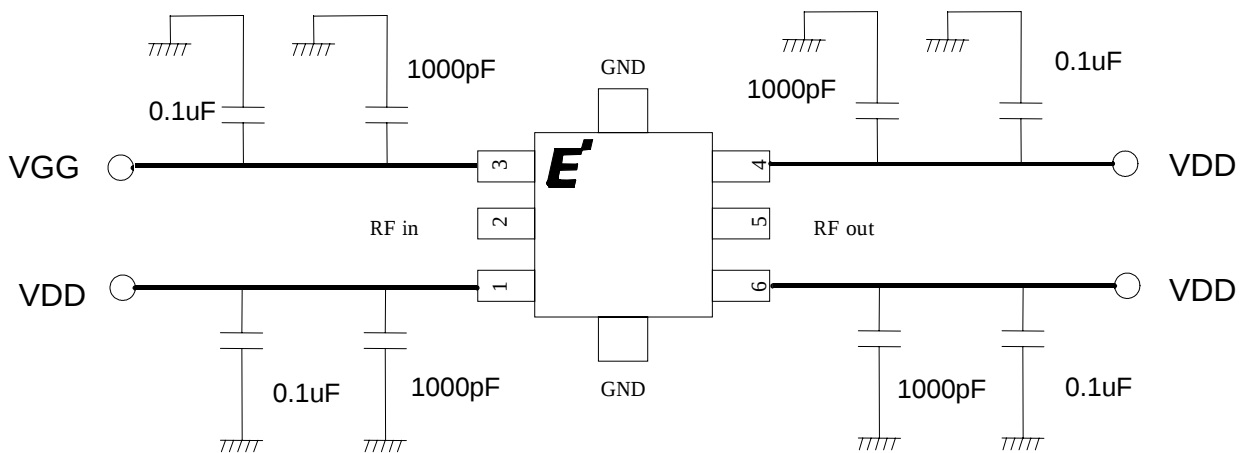
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■ Block diagram



PIN ASSIGNMENT
1 : VDD
2 : RF in
3 : VGG
4 : VDD
5 : RF out
6 : VDD

■ Recommended Bias Circuit

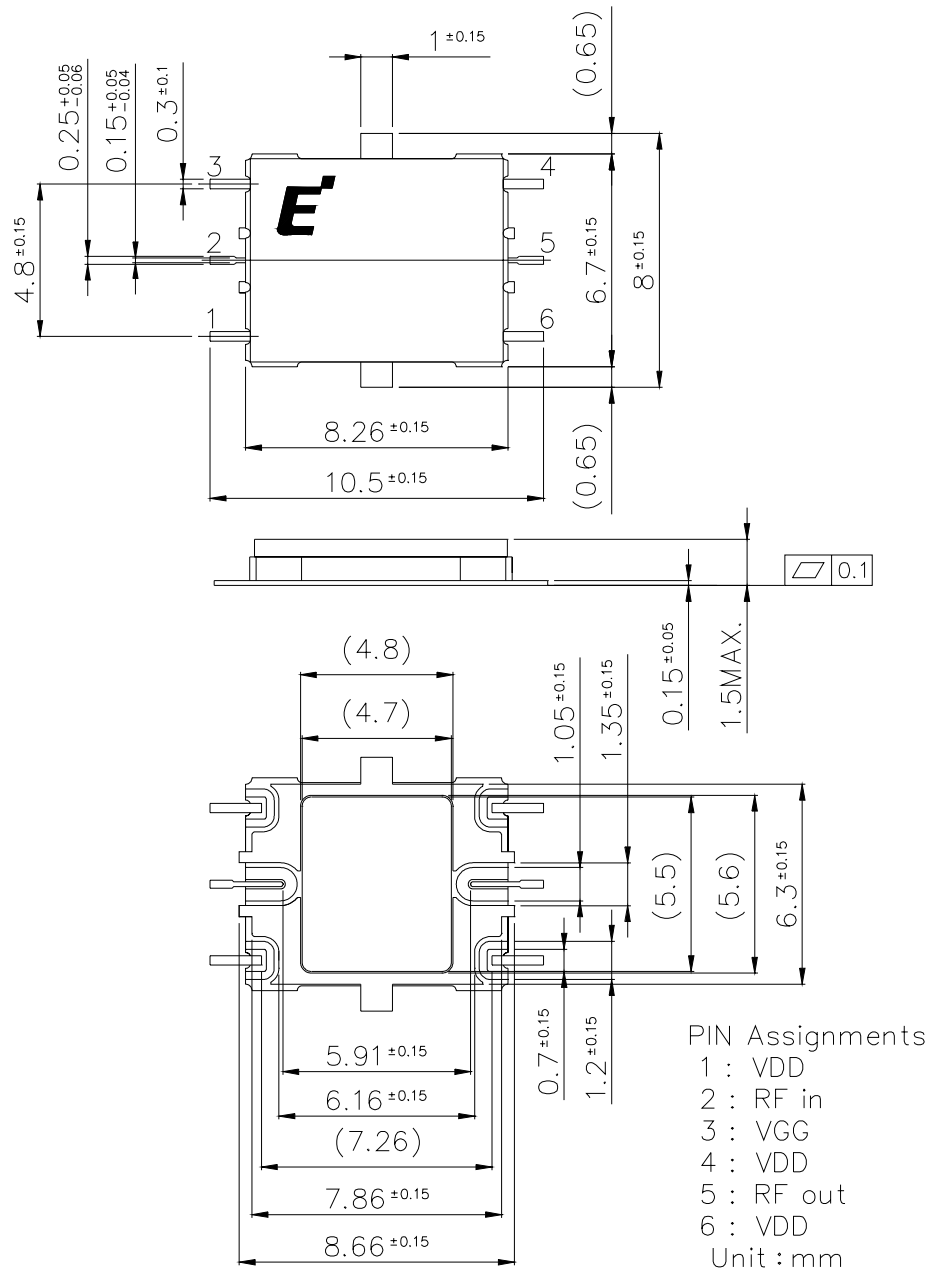


Note 1: The capacitors are recommended on the bias supply line, close to the package, in order to prevent video oscillations which could damage the module.
Note 2: Three pins named VDD are internally connected.

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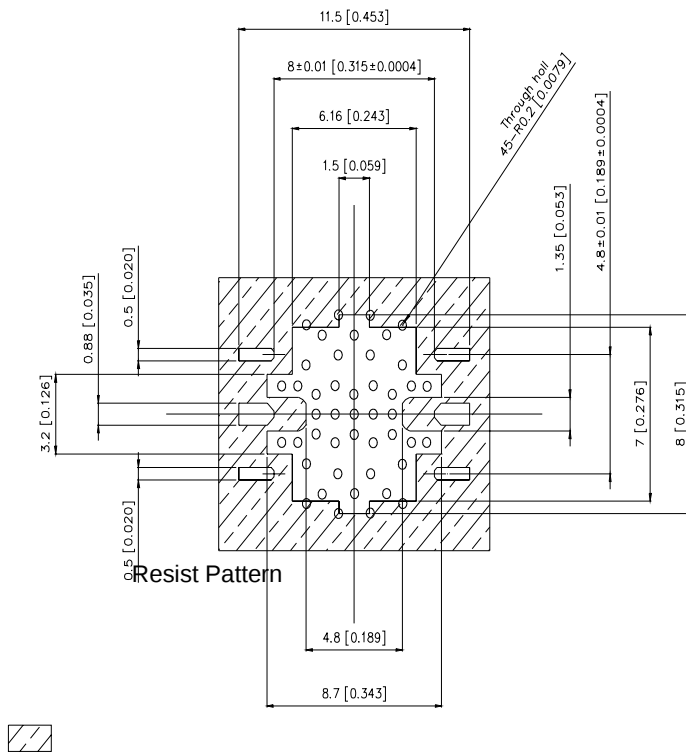
■ Package Outline



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■ PCB Pads and Solder-resist Pattern



Unit: mm [inches]
 PCB: Diclad-522
 Under plating: Cu
 : Nickel (Ni) 1 ~ 4 μ m
 Top plating: Gold (Au)
 (Flash plating 0.1 μ m or less)

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