

N-channel 500 V, 0.40 Ω typ., 8.5 A MDmesh™ II Power MOSFET in a TO-220FP package

Datasheet - production data

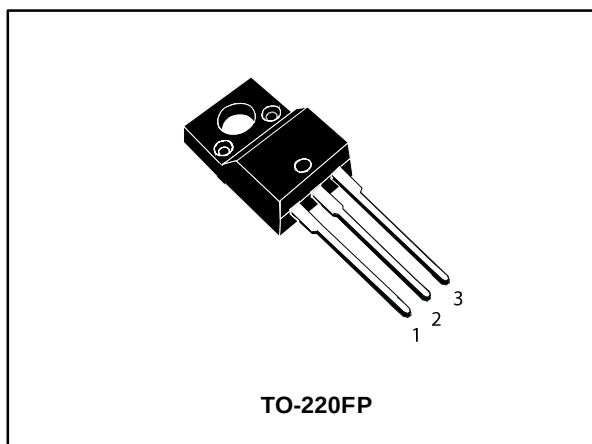
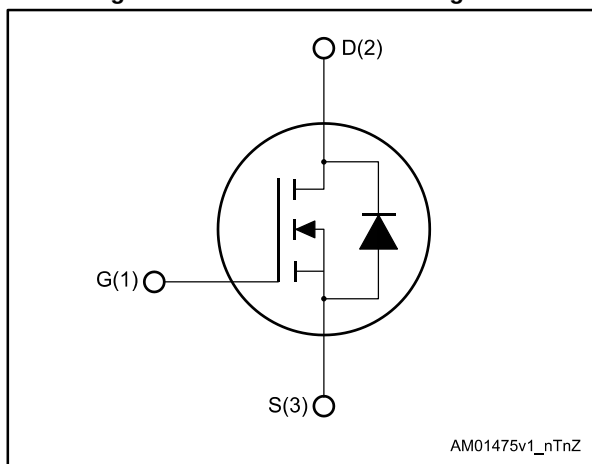


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} @ T _J max	R _{DS(on)} max	I _D
STF11NM50N	550 V	0.47 Ω	8.5 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF11NM50N	11NM50N	TO-220FP	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	8.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	6	A
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	34	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	25	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^\circ\text{C}$)	2500	V
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:⁽¹⁾Limited by maximum junction temperature⁽²⁾Pulse width limited by safe operating area.⁽³⁾ $I_{SD} \leq 8.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} \leq V_{(BR)DSS}$, $V_{DD} \leq 80\% V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{jmax})	3	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	150	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	500			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 500 V			1	μA
		V _{GS} = 0 V, V _{DS} = 500 V, T _C = 125 °C ⁽¹⁾			100	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 4.5 A		0.40	0.47	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	547	-	pF
C _{oss}	Output capacitance		-	42	-	pF
C _{rss}	Reverse transfer capacitance		-	2	-	pF
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{GS} = 0 V, V _{DS} = 0 to 400 V	-	210	-	pF
Q _g	Total gate charge	V _{DD} = 400 V, I _D = 8.5 A,	-	19	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V (see Figure 14: "Test circuit for gate charge behavior")	-	3.7	-	nC
Q _{gd}	Gate-drain charge		-	10	-	nC
R _G	Gate input resistance	f = 1 MHz, I _D = 0 A	-	5.8	-	Ω

Notes:

⁽¹⁾C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 250 V, I _D = 4.25 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	8	-	ns
t _r	Rise time		-	10	-	ns
t _{d(off)}	Turn-off delay time		-	33	-	ns
t _f	Fall time		-	10	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		8.5	A
I_{SDM}	Source-drain current (pulsed)		-		34	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 8.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 8.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	230		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	2.1		μC
I_{RRM}	Reverse recovery current		-	18		A
t_{rr}	Reverse recovery time	$I_{SD} = 8.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	275		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	2.5		μC
I_{RRM}	Reverse recovery current		-	18		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

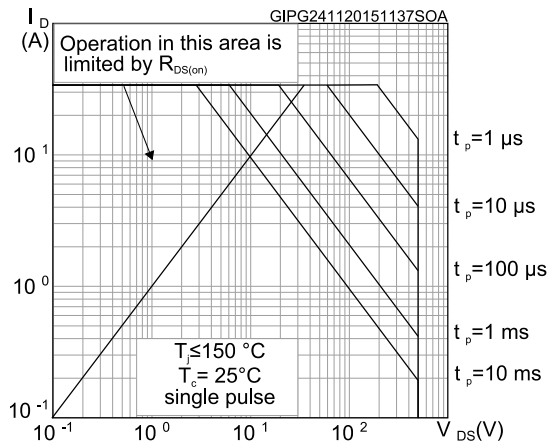


Figure 3: Thermal impedance

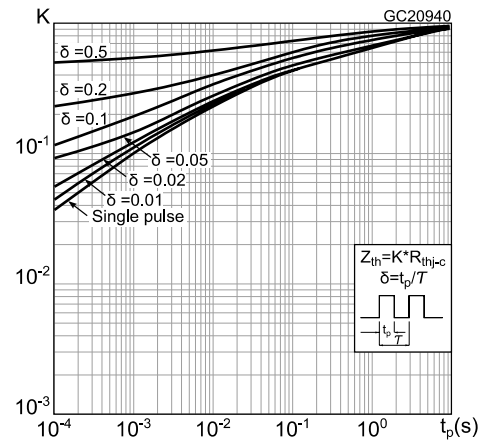


Figure 4: Output characteristics

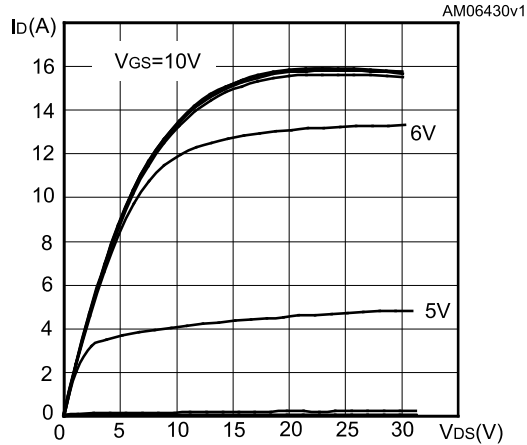


Figure 5: Transfer characteristics

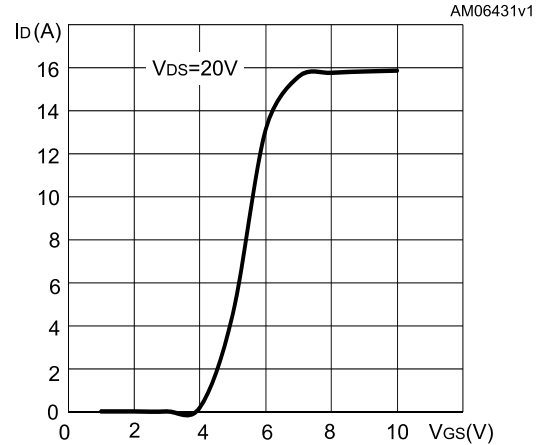


Figure 6: Gate charge vs gate-source voltage

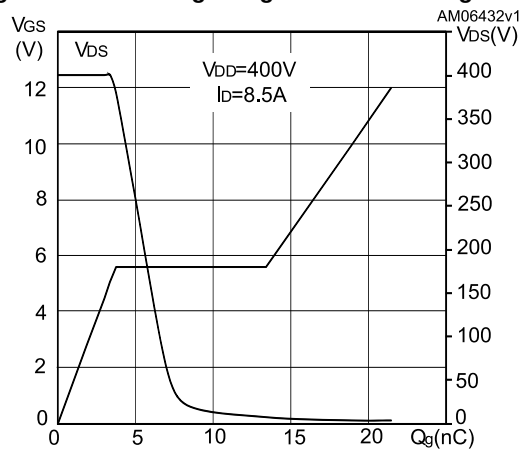


Figure 7: Static drain-source on resistance

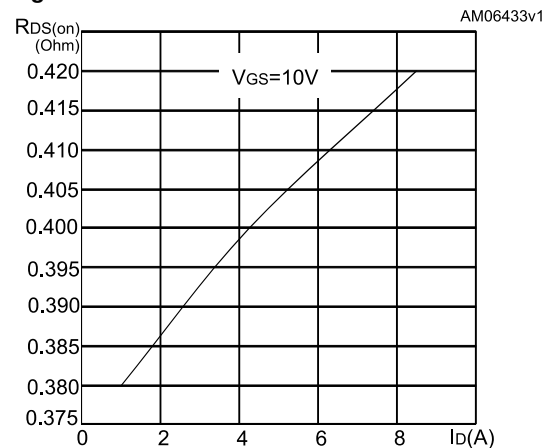


Figure 8: Capacitance variations

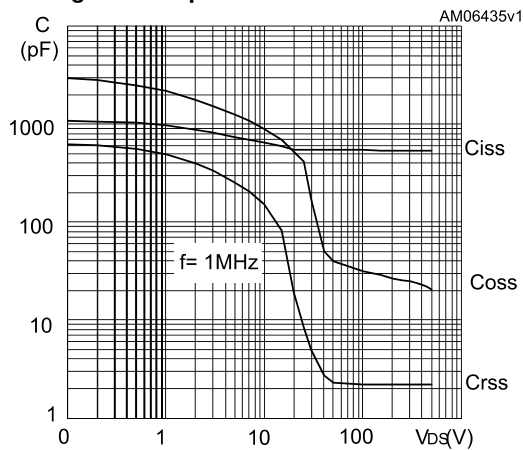


Figure 9: Output capacitance stored energy

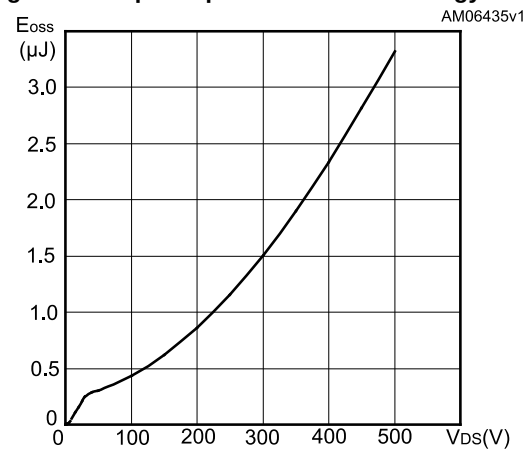


Figure 10: Normalized gate threshold voltage vs temperature

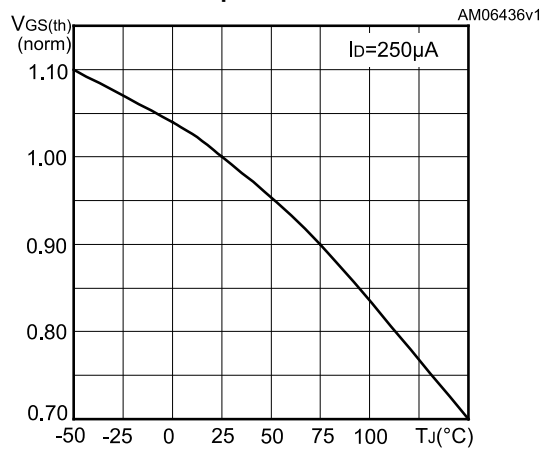


Figure 11: Normalized on-resistance vs temperature

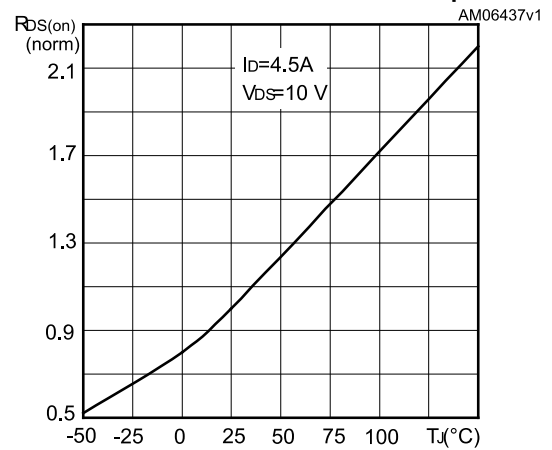
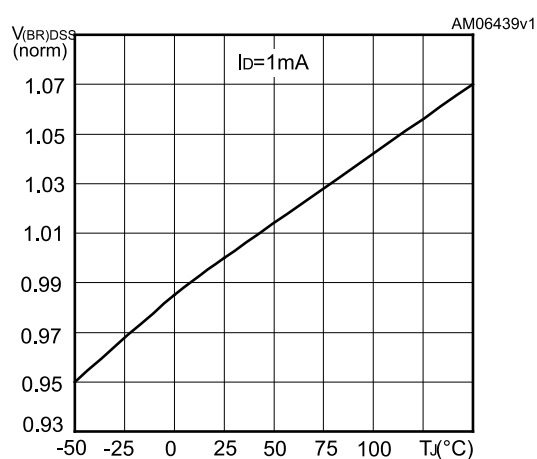
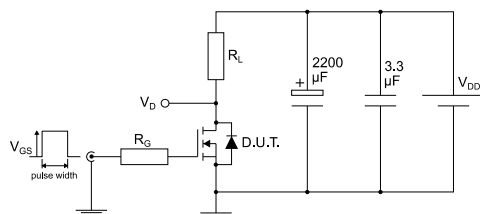


Figure 12: Normalized V(BR)DSS vs temperature



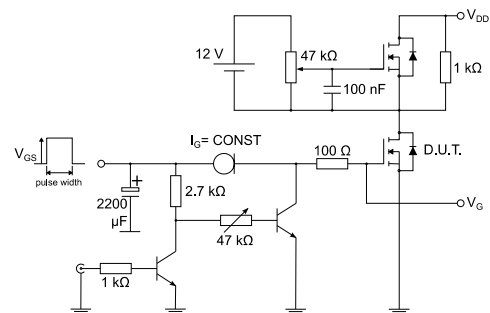
3 Test circuits

Figure 13: Test circuit for resistive load switching times



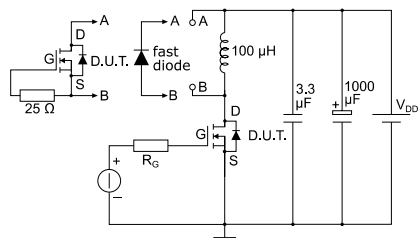
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Figure 14: Test circuit for gate charge behavior



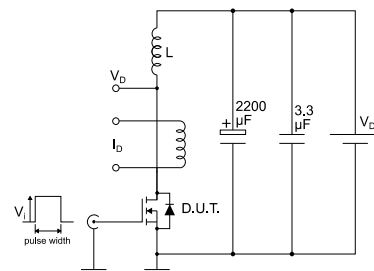
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Figure 15: Test circuit for inductive load switching and diode recovery times



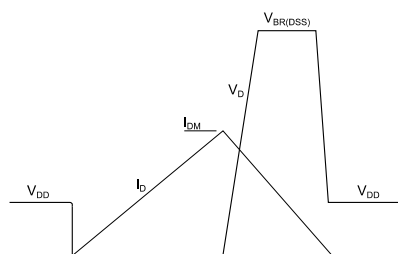
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Figure 16: Unclamped inductive load test circuit



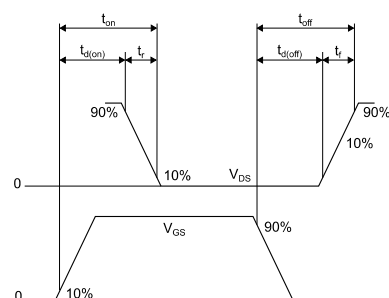
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 19: TO-220FP package outline

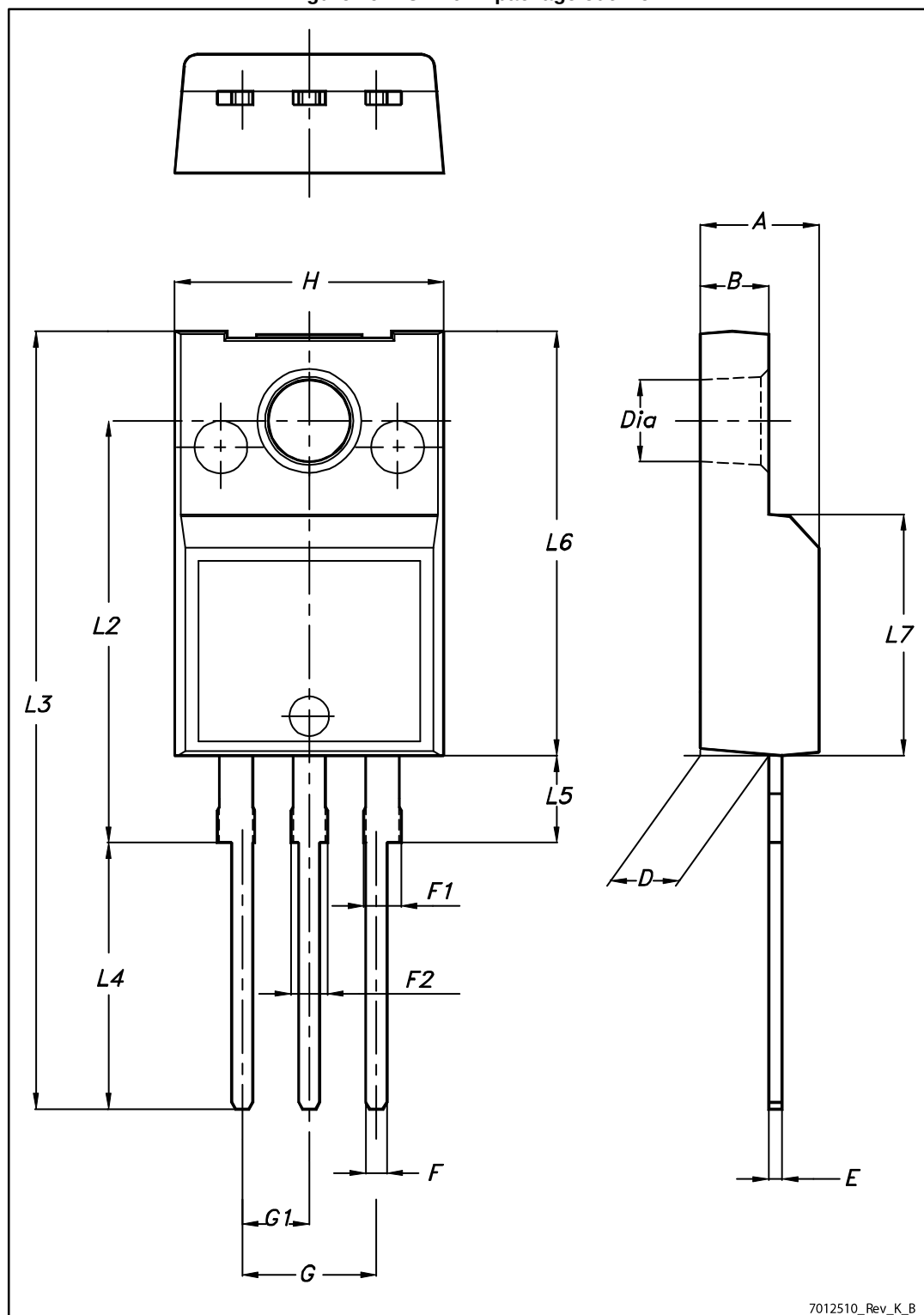


Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
25-Nov-2015	1	First release. Part number previously included in datasheet DocID17156.
09-Jun-2016	2	Updated I_{GSS} unit from μA to nA in Table 5: "On/off states" . Updated Table 7: "Switching times" modifying references in test conditions. Document reformatted with the current standard with minor text changes to improve readability.

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