PSMN050-80BS

N-channel 80 V 46 mΩ standard level MOSFET in D2PAK

Rev. 1 — 2 March 2012 **Product data sheet**

1. Product profile

1.1 General description

Standard level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

1.3 Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

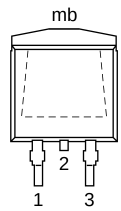
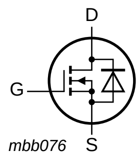
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	80	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 10$ V; see Figure 1	-	-	22	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	56	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 10$ A; $T_j = 25$ °C	-	37	46	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10$ V; $I_D = 25$ A; $V_{DS} = 40$ V; see Figure 14; see Figure 15	-	2.3	-	nC
$Q_{G(tot)}$	total gate charge		-	11	-	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $I_D = 22$ A; $V_{sup} \leq 80$ V; $R_{GS} = 50$ Ω; unclamped	-	-	18	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT404 (D2PAK)	
2	D	drain[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make connection to pin 2.

3. Ordering information

Table 3. Ordering information

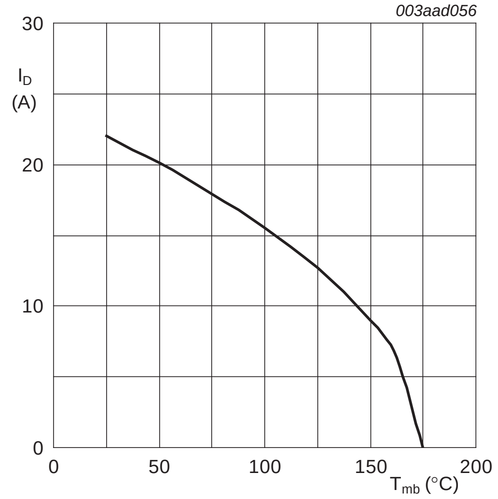
Type number	Package		
	Name	Description	Version
PSMN050-80BS	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

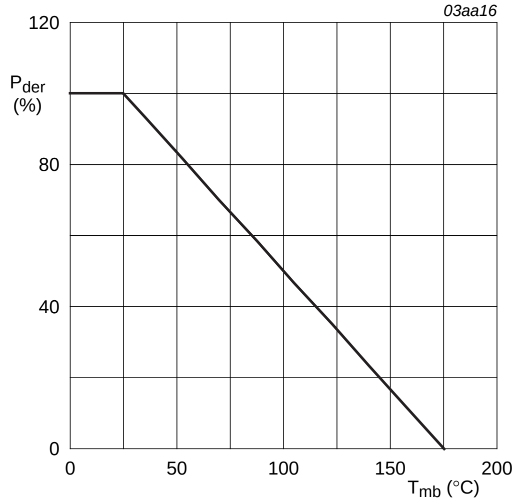
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T_j ≥ 25 °C; T_j ≤ 175 °C	-	80	V
V_{DGR}	drain-gate voltage	T_j ≥ 25 °C; T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	80	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 100 °C; see Figure 1	-	16	A
		V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1	-	22	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; see Figure 3	-	88	A
P_{tot}	total power dissipation	T_{mb} = 25 °C;see Figure 2	-	56	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	22	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C	-	88	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; I_D = 22 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; unclamped	-	18	mJ



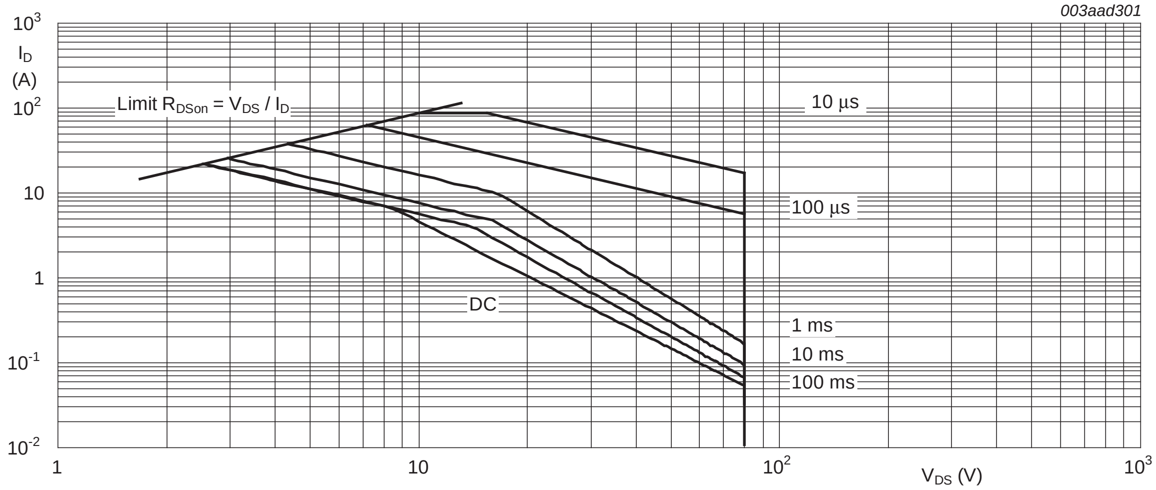
$$V_{GS} \geq 10\,V$$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25°C$; I_{DM} is a single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	2.2	2.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W

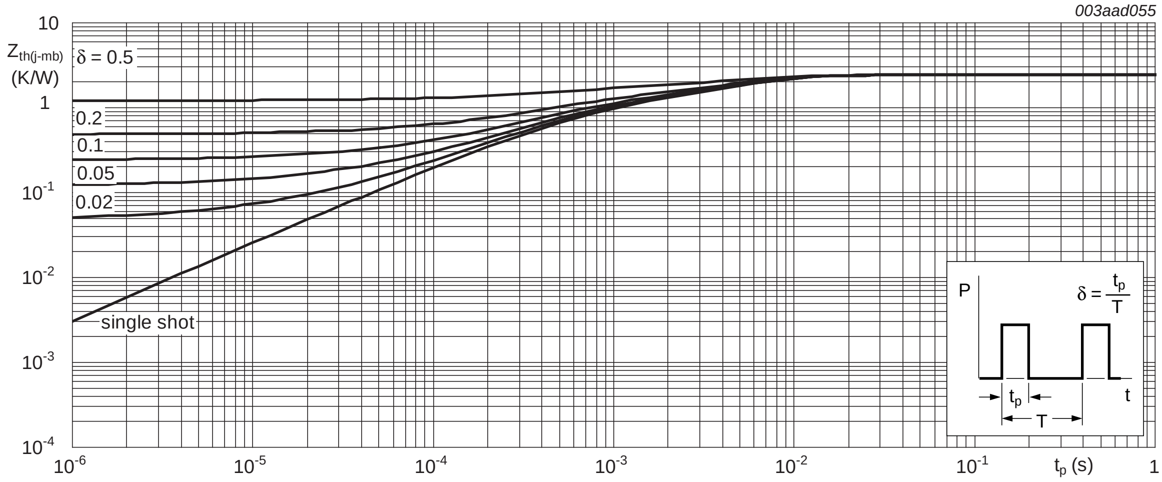


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

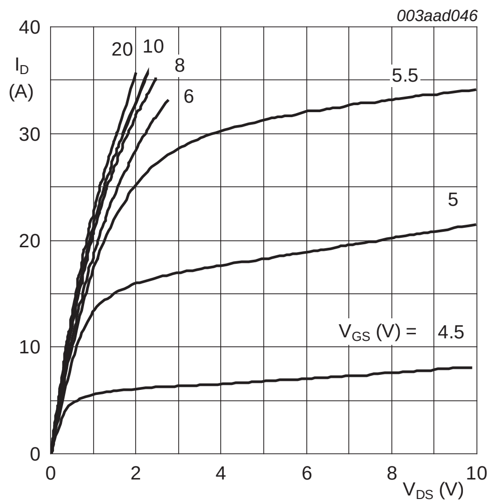
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C	73	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C	80	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 11; see Figure 12	1	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 11; see Figure 12	-	-	4.6	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 11; see Figure 12	2	3	4	V
I_{DSS}	drain leakage current	V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 °C	-	-	1	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 °C	-	-	15	µA
I_{GSS}	gate leakage current	V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
		V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C	-	-	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 100 °C; see Figure 13	-	-	74	mΩ
		V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C	-	37	46	mΩ
R_G	internal gate resistance (AC)	f = 1 MHz	-	2	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V	-	9	-	nC
		I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; see Figure 14; see Figure 15	-	11	-	nC
Q_{GS}	gate-source charge		-	3.8	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; see Figure 14	-	1.9	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	1.9	-	nC
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; see Figure 14; see Figure 15	-	2.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	V_{DS} = 40 V	-	5.2	-	V
C_{iss}	input capacitance	V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; see Figure 17	-	633	-	pF
C_{oss}	output capacitance		-	100	-	pF
C_{rss}	reverse transfer capacitance		-	50	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 12 V; R_L = 0.5 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 4.7 Ω	-	9.2	-	ns
t_r	rise time		-	1	-	ns
$t_{d(off)}$	turn-off delay time		-	16	-	ns
t_f	fall time		-	2.4	-	ns

Table 6. Characteristics *…continued*

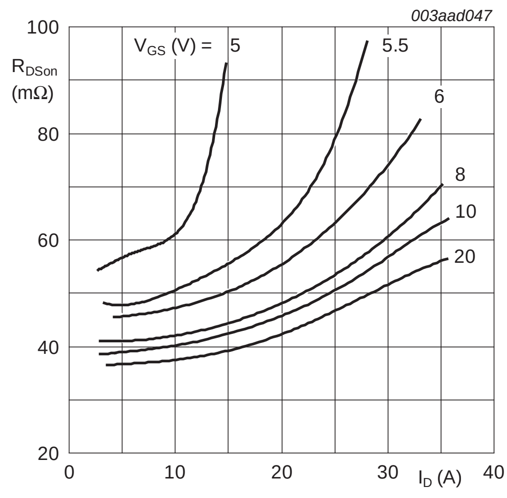
Tested to JEDEC standards where applicable.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 15 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 16	-	0.86	1.2	V
t_{rr}	reverse recovery time	I_S = 50 A; dI_S/dt = 100 A/µs; V_{GS} = 0 V; V_{DS} = 40 V	-	32	-	ns
Q_r	recovered charge		-	28	-	nC



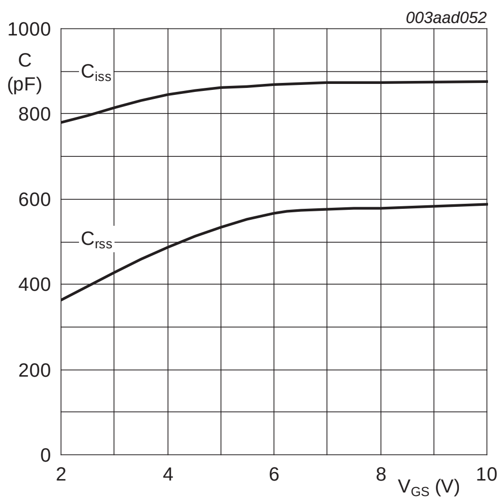
$T_j = 25\,°C; t_p = 300\mu s$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



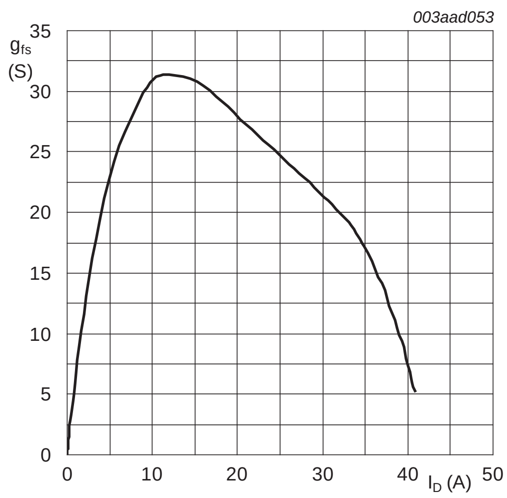
$T_j = 25\,°C; t_p = 300\mu s$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



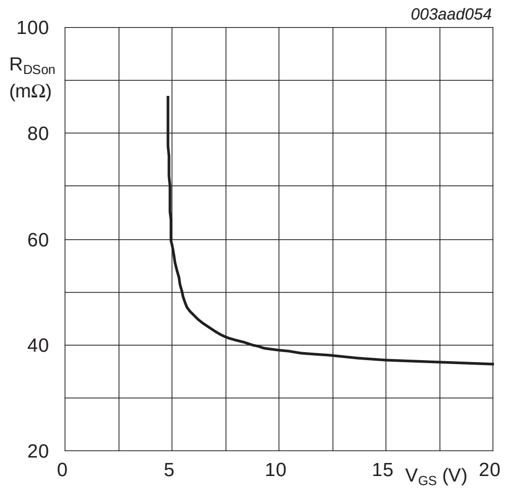
$V_{DS} = 0\,V; f = 1\,MHz$

Fig 7. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



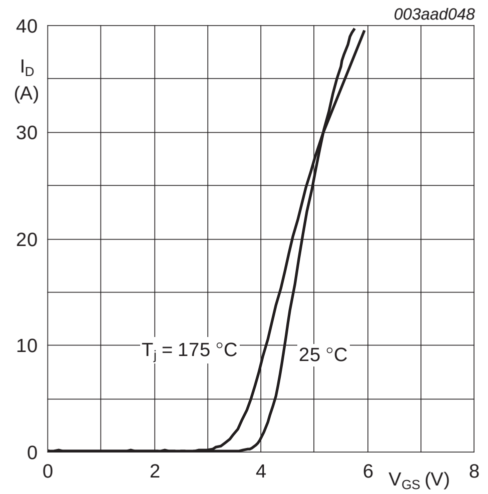
$T_j = 25\,°C; V_{DS} = 15\,V$

Fig 8. Forward transconductance as a function of drain current; typical values



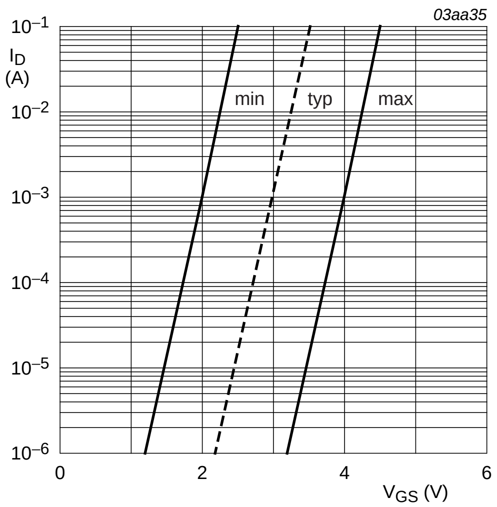
$T_j = 25\,°C; I_D = 10\,A$

Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



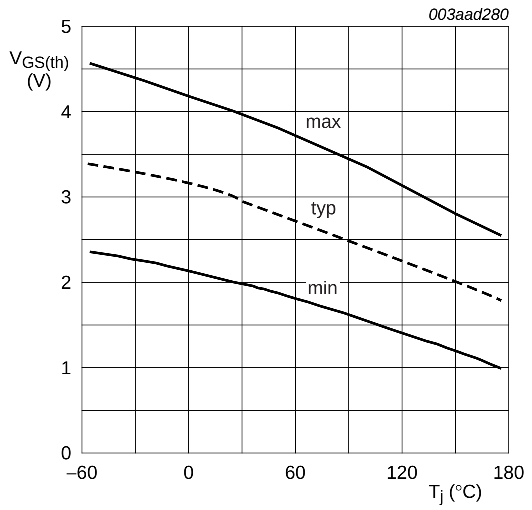
$V_{DS} = 15\,V$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



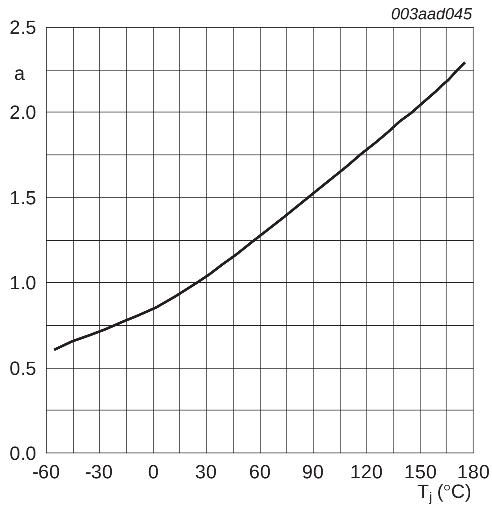
$T_j = 25\,°C; V_{DS} = 5\,V$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 12. Gate-source threshold voltage as a function of junction temperature



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

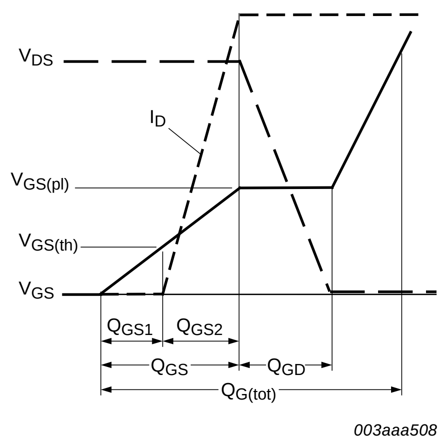
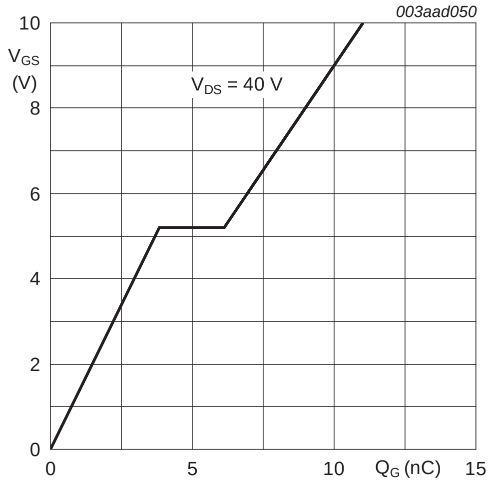
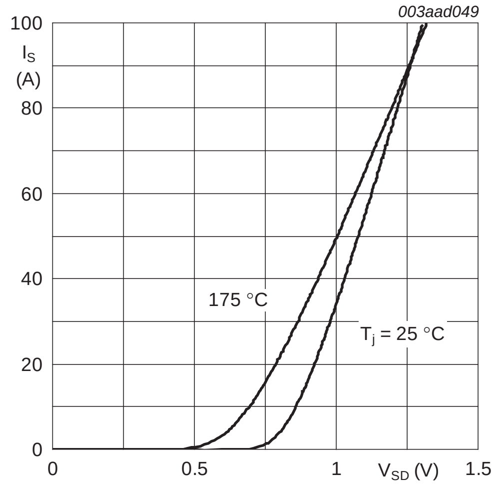


Fig 14. Gate charge waveform definitions



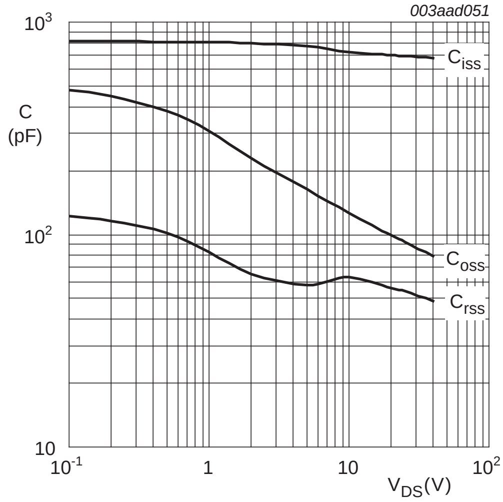
$$T_j = 25°C; I_D = 25A$$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$$V_{GS} = 0V$$

Fig 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

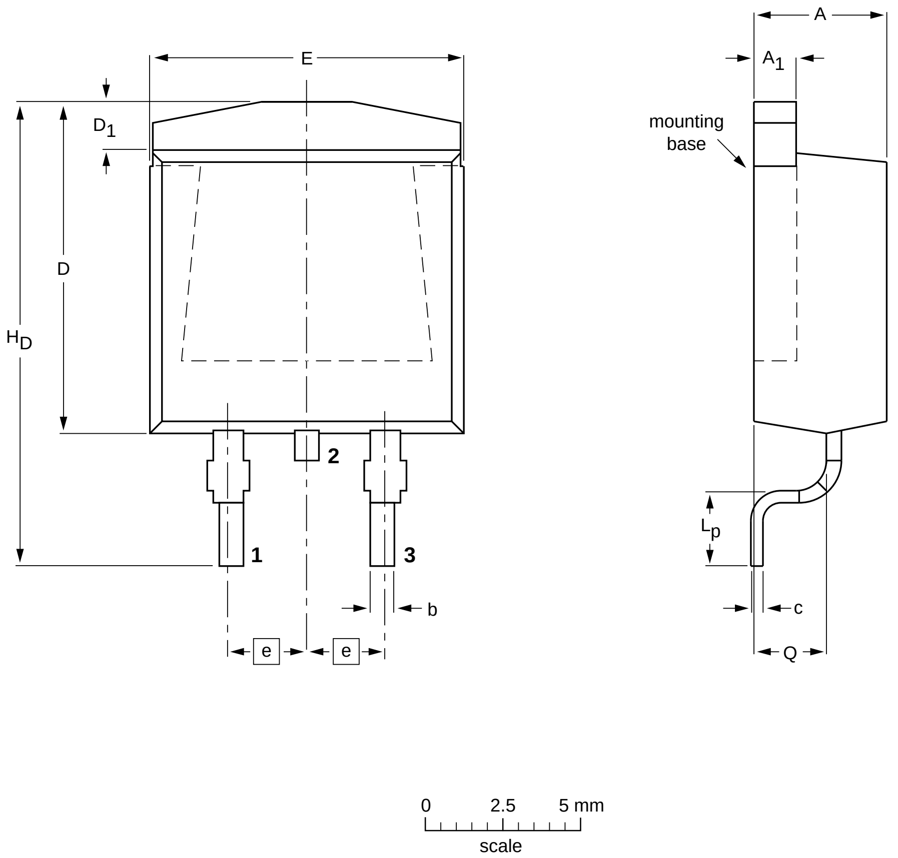


$V_{GS} = 0V; f = 1MHz$

Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig 18. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN050-80BS v.1	20120302	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URLhttp://www.nxp.com.

9.2 Definitions

Preview— The document is a preview version only. The document is still subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Draft— The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet— A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification— The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

9.3 Disclaimers

Limited warranty and liability— Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the*Terms and conditions of commercial sale*of NXP Semiconductors.

Right to make changes— NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use— NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data— The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications— Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values— Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale— NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published athttp://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license— Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control— This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products— Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations— A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

9.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Adelante,**Bitport**,**Bitsound**,**CoolFlux**,**CoReUse**,**DESFire**,**EZ-HV**,**FabKey**,**GreenChip**,**HiPerSmart**,**HITAG**,**I²C-bus**logo,**ICODE**,**I-CODE**,**ITEC**,**Labelution**,**MIFARE**,**MIFARE Plus**,**MIFARE Ultralight**,**MoReUse**,**QLPAK**,**Silicon Tuner**,**SiliconMAX**,**SmartXA**,**STARplug**,**TOPFET**,**TrenchMOS**,**TriMedia**and **UCODE**— are trademarks of NXP B.V.

HD Radioand**HD Radio**logo — are trademarks of iBiquity Digital Corporation.

10. Contact information

For more information, please visit:http://www.nxp.com

For sales office addresses, please send an email to:salesaddresses@nxp.com

11. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 2 March 2012
Document identifier: PSMN050-80BS