

# N0118GA

## SCR

Rev. 1 — 11 July 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Planar passivated ultra sensitive gate Silicon Controlled Rectifier in a SOT54 (T0-92) plastic package.

### 1.2 Features and benefits

- High voltage capability
- Ultra sensitive gate
- Planar passivated for voltage ruggedness and reliability

### 1.3 Applications

- Electronic ballasts
- Sensing circuits
- Safety shut down and protection circuits
- Smoke detectors
- Switched Mode Power Supplies

### 1.4 Quick reference data

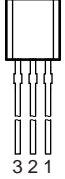

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	600	V
$V_{RRM}$	repetitive peak reverse voltage		-	-	600	V
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; see <a href="#">Figure 4</a> ; see <a href="#">Figure 5</a>	-	-	8	A
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 67\text{ °C}$ ; see <a href="#">Figure 3</a>	-	-	0.51	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 67\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 2</a>	-	-	0.8	A
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 10\text{ mA}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 7</a>	0.5	-	7	$\mu\text{A}$



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 <p>SOT54 (TO-92)</p>	
2	G	gate		
3	K	cathode		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
N0118GA	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{\text{DRM}}$	repetitive peak off-state voltage		-	600	V
$V_{\text{RRM}}$	repetitive peak reverse voltage		-	600	V
$I_{\text{T(AV)}}$	average on-state current	half sine wave; $T_{\text{lead}} \leq 67\text{ }^{\circ}\text{C}$ ; see <a href="#">Figure 3</a>	-	0.51	A
$I_{\text{T(RMS)}}$	RMS on-state current	half sine wave; $T_{\text{lead}} \leq 67\text{ }^{\circ}\text{C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 2</a>	-	0.8	A
$I_{\text{TSM}}$	non-repetitive peak on-state current	half sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$ ; $t_{\text{p}} = 10\text{ ms}$ ; see <a href="#">Figure 4</a> ; see <a href="#">Figure 5</a>	-	8	A
		half sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$ ; $t_{\text{p}} = 8.3\text{ ms}$	-	9	A
$I^2t$	$I^2t$ for fusing	$t_{\text{p}} = 10\text{ ms}$ ; sine-wave pulse	-	0.32	$\text{A}^2\text{s}$
$dl_T/dt$	rate of rise of on-state current	$I_{\text{T}} = 0.8\text{ A}$ ; $I_{\text{G}} = 10\text{ mA}$ ; $dl_{\text{G}}/dt = 0.1\text{ A}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
$I_{\text{GM}}$	peak gate current		-	1	A
$V_{\text{RGM}}$	peak reverse gate voltage		-	5	V
$P_{\text{GM}}$	peak gate power		-	2	W
$P_{\text{G(AV)}}$	average gate power	over any 20 ms period	-	0.1	W
$T_{\text{stg}}$	storage temperature		-40	150	$^{\circ}\text{C}$
$T_{\text{j}}$	junction temperature		-	125	$^{\circ}\text{C}$

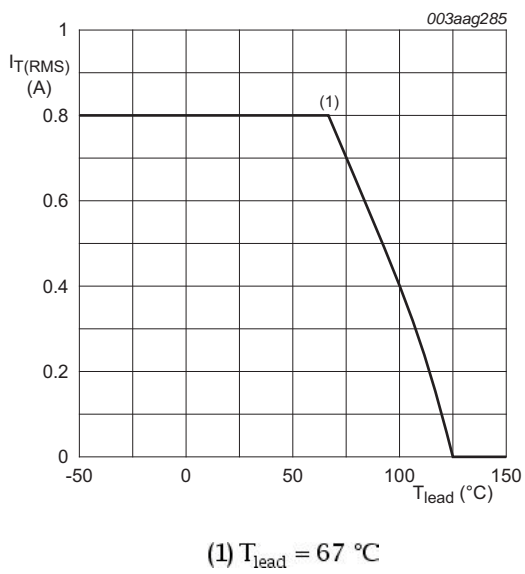


Fig 1. RMS on-state current as a function of lead temperature; maximum values

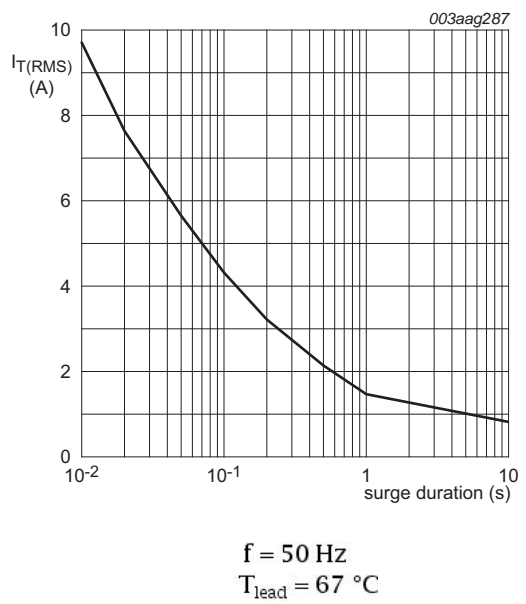


Fig 2. RMS on-state current as a function of surge duration; maximum values

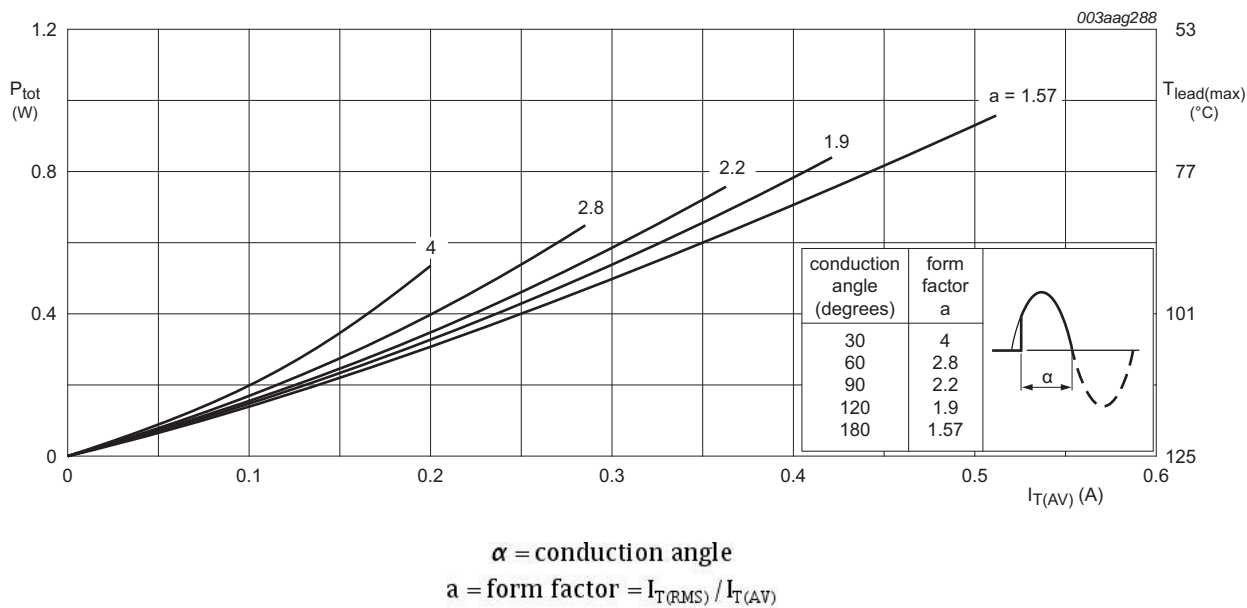
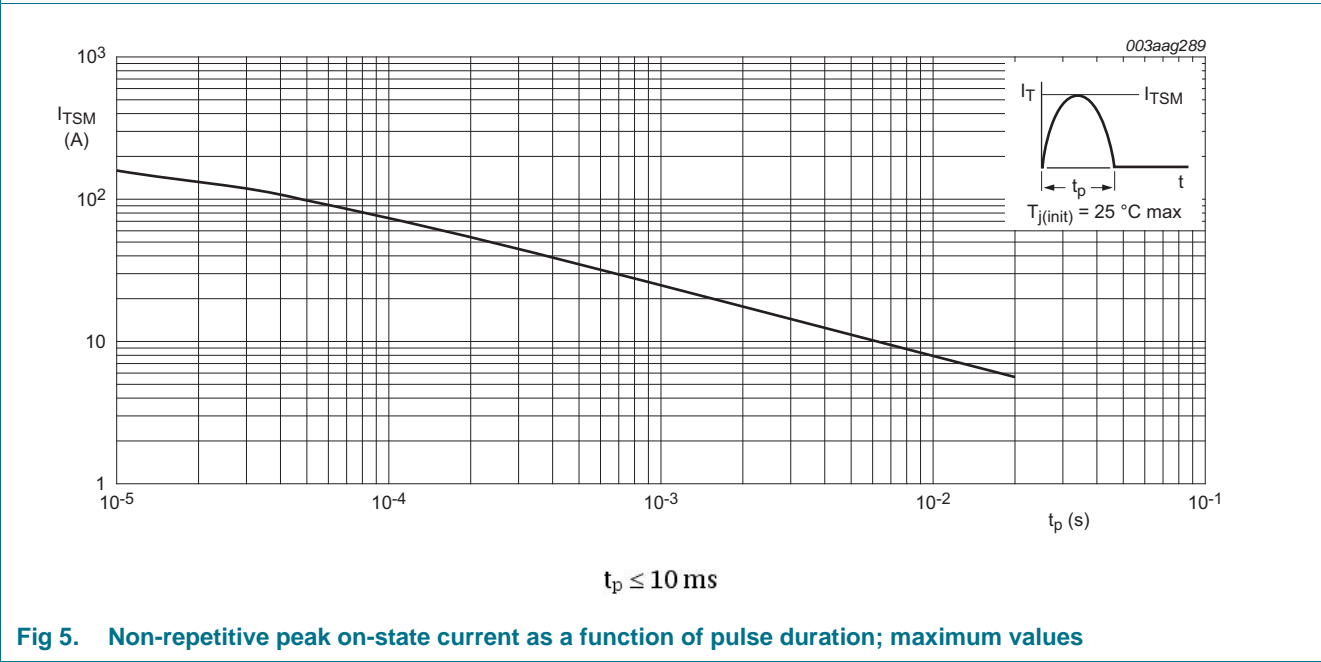
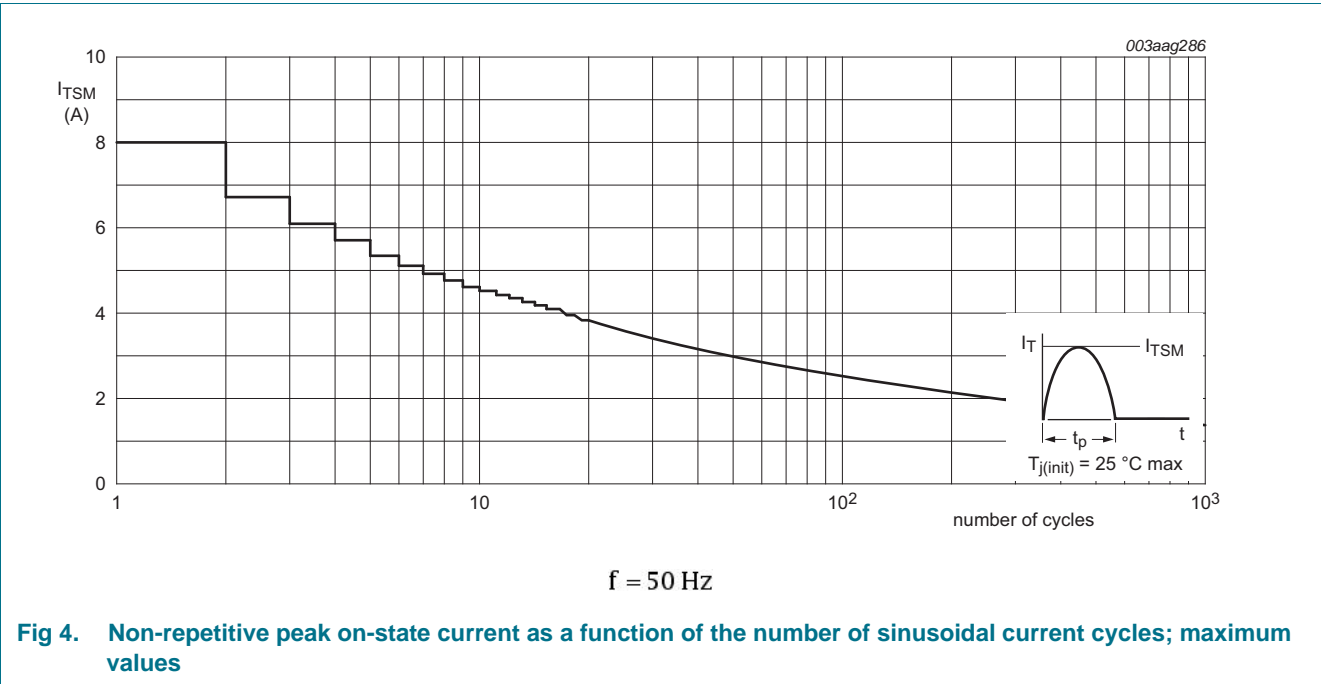


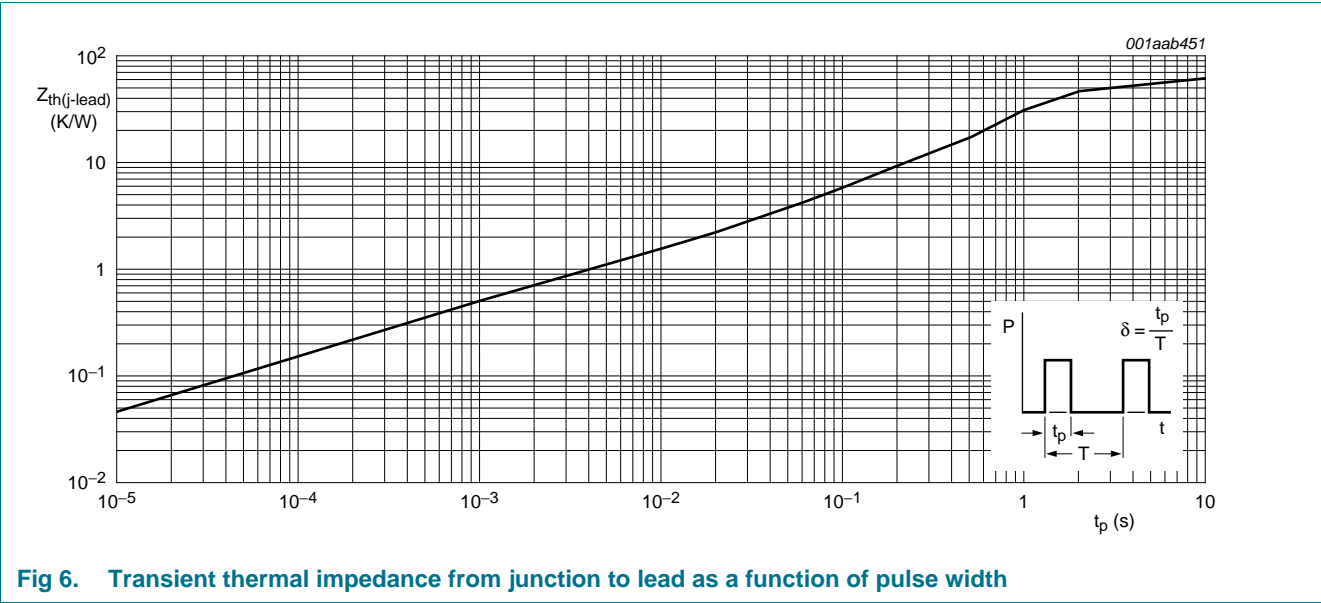
Fig 3. Total power dissipation as a function of average on-state current; maximum values



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	see <a href="#">Figure 6</a>	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W



## 6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 10 mA; T <sub>j</sub> = 25 °C; see <a href="#">Figure 7</a>	0.5	-	7	μA
I <sub>L</sub>	latching current	V <sub>D</sub> = 12 V; I <sub>G</sub> = 0.1 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 8</a>	-	-	6	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; see <a href="#">Figure 9</a> ; see <a href="#">Figure 10</a>	-	-	5	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 1.6 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 11</a>	-	1.4	1.95	V
V <sub>GT</sub>	gate trigger voltage	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	-	0.8	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 600 V; T <sub>j</sub> = 25 °C; R <sub>GK</sub> = 1 kΩ	-	-	10	μA
		V <sub>D</sub> = 600 V; T <sub>j</sub> = 125 °C; R <sub>GK</sub> = 1 kΩ	-	-	100	μA
I <sub>R</sub>	reverse current	T <sub>j</sub> = 25 °C; R <sub>GK</sub> = 1 kΩ; V <sub>R</sub> = 600 V	-	-	10	μA
		T <sub>j</sub> = 125 °C; R <sub>GK</sub> = 1 kΩ; V <sub>R</sub> = 600 V	-	-	100	μA
Dynamic characteristics						
dV <sub>D</sub> /dt	rate of rise of off-state voltage	V <sub>DM</sub> = 402 V; T <sub>j</sub> = 125 °C; R <sub>GK</sub> = 1 kΩ; exponential waveform; see <a href="#">Figure 13</a> ; see <a href="#">Figure 14</a>	75	-	-	V/μs

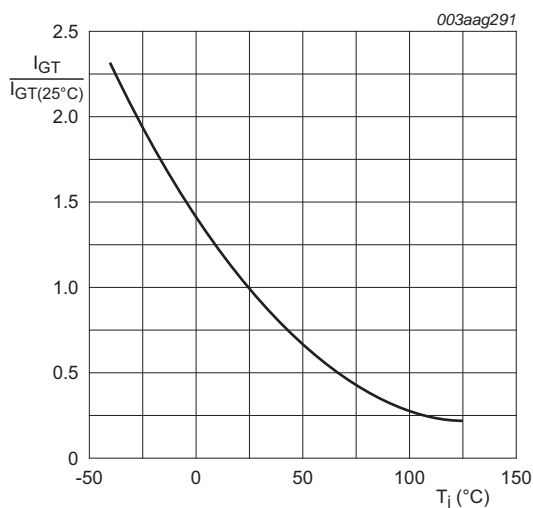


Fig 7. Normalized gate trigger current as a function of junction temperature

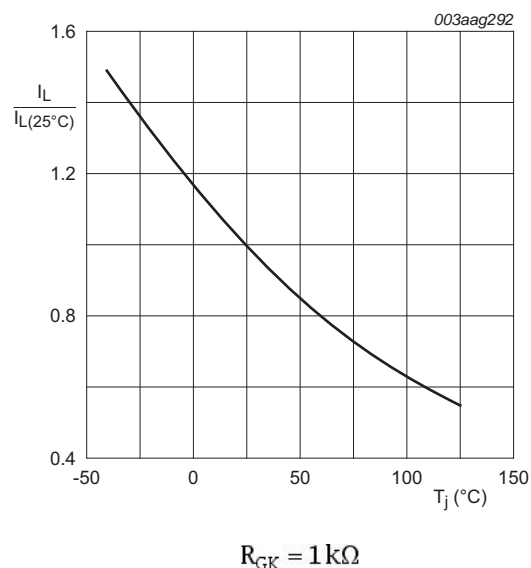


Fig 8. Normalized latching current as a function of junction temperature

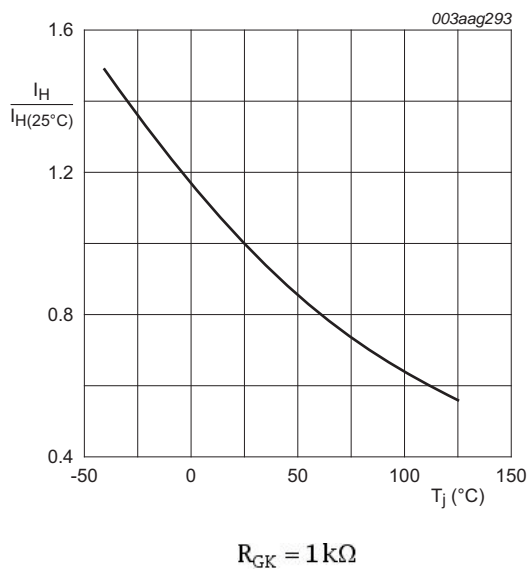


Fig 9. Normalized holding current as a function of junction temperature

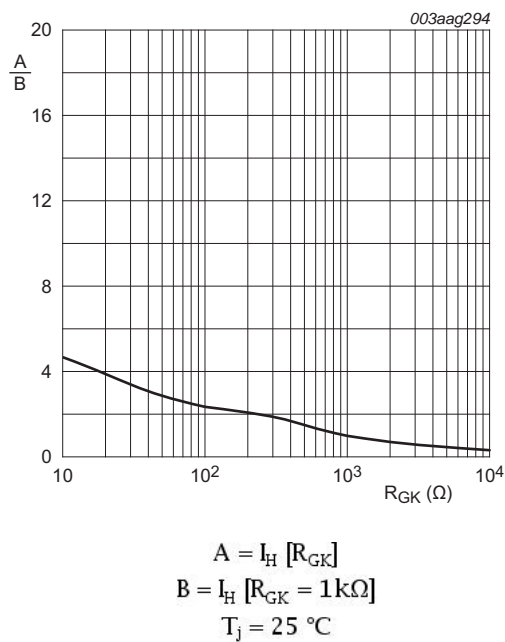


Fig 10. Normalized holding current as a function of gate-cathode resistance (typical values)

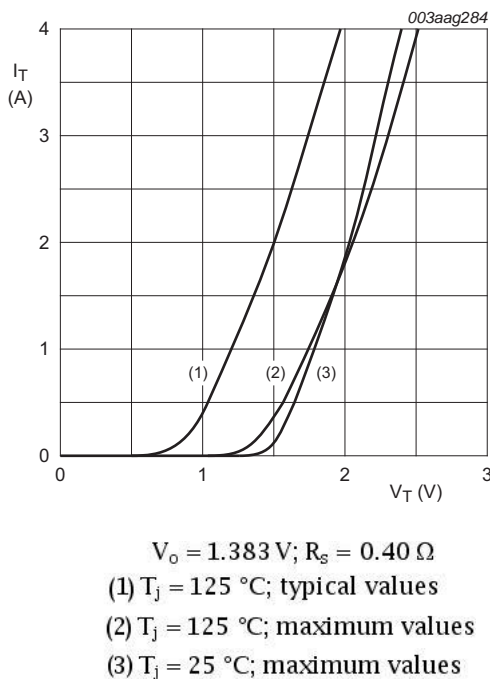


Fig 11. On-state current as a function of on-state voltage

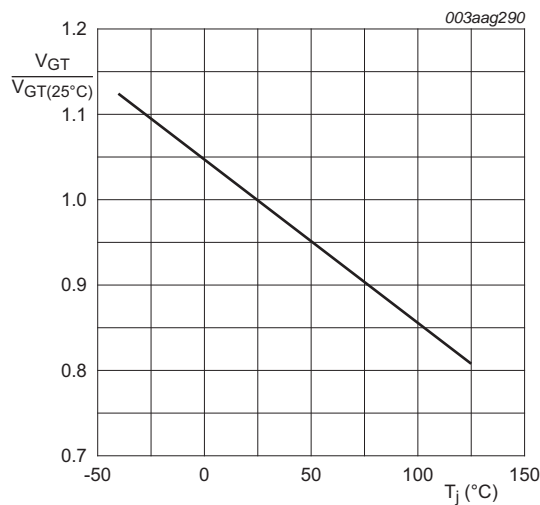
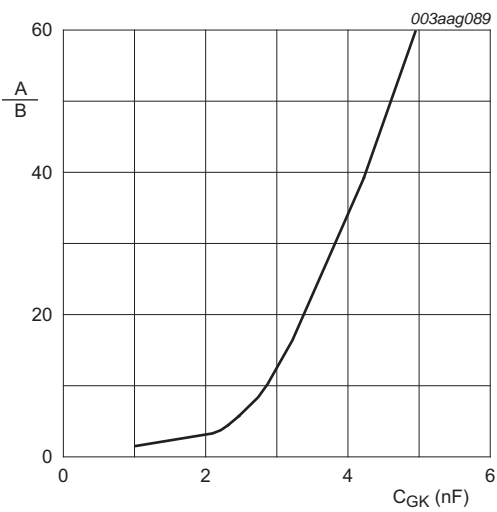


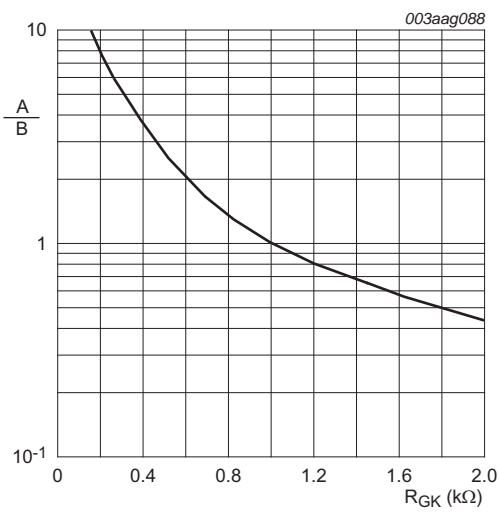
Fig 12. Normalized gate trigger voltage as a function of junction temperature



$$A = \frac{dV}{dt} [C_{GK}]$$
$$B = \frac{dV}{dt} [R_{GK} = 1\text{ k}\Omega]$$

$T_j = 125\text{ }^{\circ}\text{C}; R_{GK} = 1\text{ k}\Omega; V_{DM} = 402\text{ V}$

Fig 13. Normalized dVd/dt immunity as a function of gate-cathode capacitance (typical values)



$$A = \frac{dV}{dt} [R_{GK}]$$
$$B = \frac{dV}{dt} [R_{GK} = 1\text{ k}\Omega]$$

$T_j = 125\text{ }^{\circ}\text{C}; V_{DM} = 402\text{ V}$

Fig 14. Normalized dVd/dt immunity as a function of gate-cathode resistance (typical values)

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

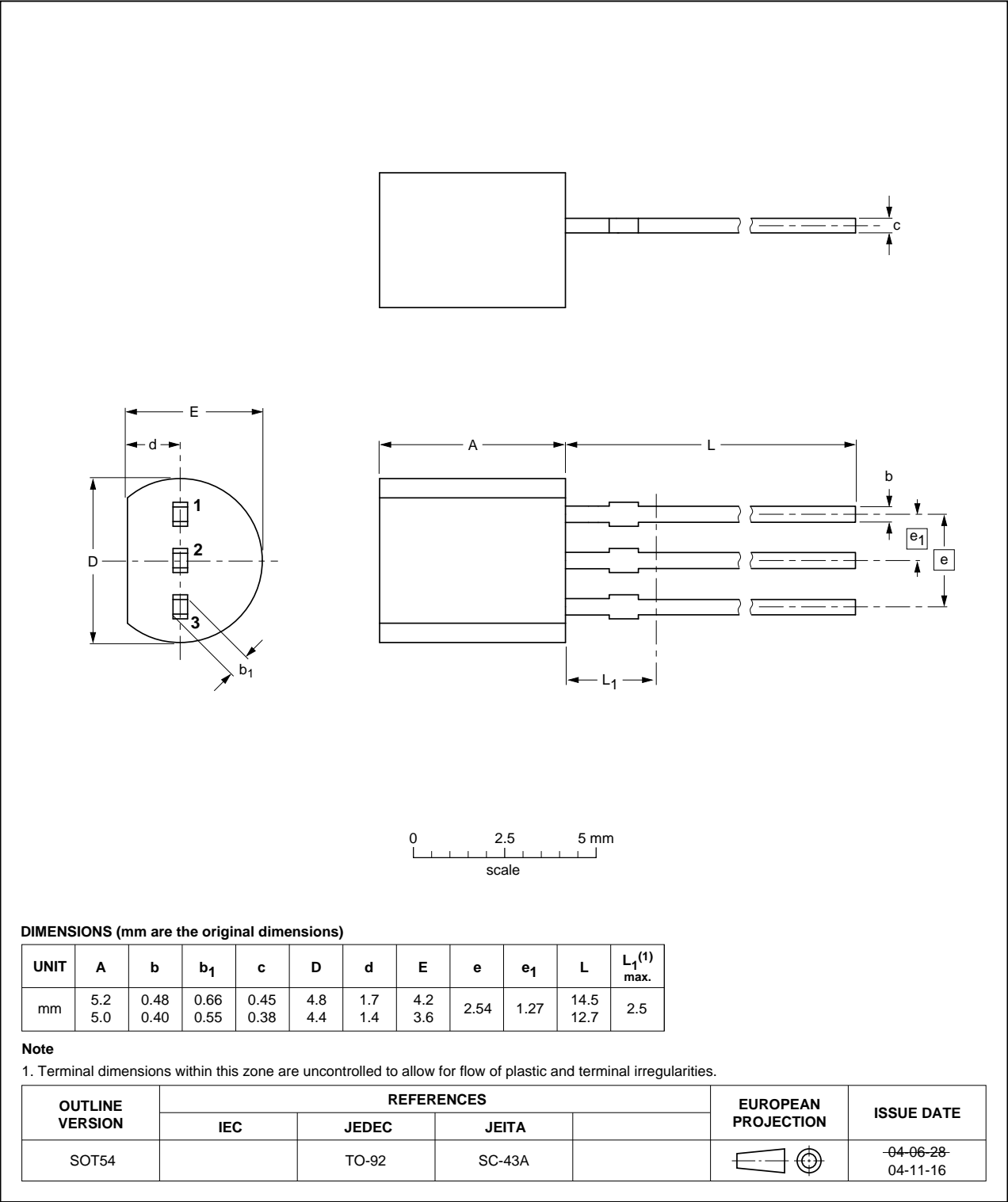


Fig 15. Package outline SOT54 (TO-92)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
N0118GA v.1	20110711	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1] [2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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