IES5431
Electronic Dual Blanket Controller with Timing

1 FEATURES

- Low external component count
- Duty cycle power control, set by potentiometer
- Triac switched control of blanket power
- Master and slave control from a single control IC
- No DC component in the AC supply current
- On chip circuit protection against triac gate spikes
- Low supply current
- Boost time capability. Wide set range by external R or C components
- Run time set to a wide range by external R or C components
- Negative triac gate drive (avoids insensitive quadrant operation)

2 GENERAL DESCRIPTION

The IES5431 is a monolithic bipolar circuit for duty cycle control of an electric blanket. It offers control of both a Master and a Slave blanket with independent control and burst mode drive to each resistive blanket load.

The full control circuit for both loads (Master and Slave) is incorporated in the IES5431 with 3 wire connection to a remote Slave control (containing only the potentiometer, switch and indicator LED). The master control can also be used alone, with the Slave control features not connected.

ON/OFF control is via separate push-button switches on the master and slave controls, with boost and run times preset by capacitors and resistors external to the IES5431 IC. LED indicators show when it is in the boost mode, or the normal run mode with the duty cycle power control set by the control potentiometers.

The triac drive circuits provide zero-crossing firing of the triacs in a manner designed to minimise rfi. The IES5431 requires a minimum of external components while providing accurate power control with minimum heat dissipation in the control unit.

3 BLOCK DIAGRAM

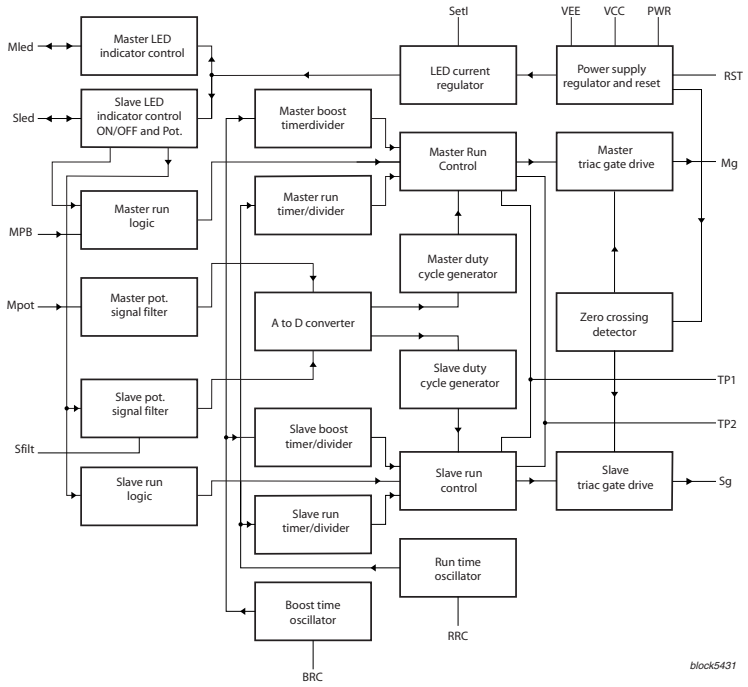

Fig.1 Block diagram

Contents are subject to the Disclaimer

4 PINNING INFORMATION

4.1 Pin description (16 pin)

SYMBOL	PIN	DESCRIPTION
Mled	1	LED drive Master
Sfilt	2	Slave pot input filter
Mpot	3	Master pot wiper
MPB	4	Master ON/OFF Switch
BRC	5	Boost RC oscillator
RRC	6	Run RC oscillator
TP1	7	Test point 1
TP2	8	Test point 2
RST	9	Reset
VCC	10	Positive Common
Mg	11	Gate drive: Master triac
Sg	12	Gate drive: Slave triac
VEE	13	Negative, substrate
PWR	14	AC resistor to Active
Sled	15	LED drive Slave
SetI	16	Set LED current

4.2 Pinning layout (16 pin)

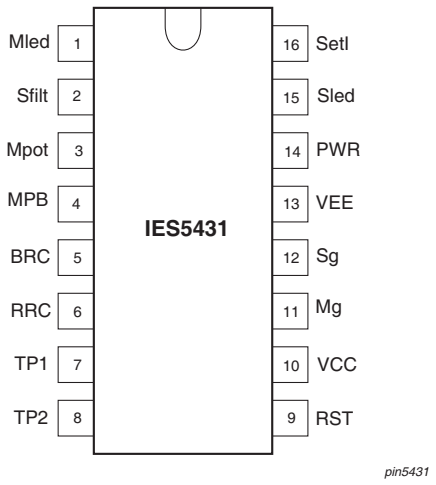

Fig.2 Pin configuration (16 pin)

4.3 Pin description (20 pin)

SYMBOL	PIN	DESCRIPTION
Mled	1	LED drive Master
Sfilt	2	Slave pot input filter
Mpot	3	Master pot wiper
n.c.	4	not connected
MPB	5	Master ON/OFF Switch
BRC	6	Boost RC oscillator
n.c.	7	not connected
RRC	8	Run RC oscillator
TP1	9	Test point 1
TP2	10	Test point 2
RST	11	Reset
VCC	12	Positive Common
Mg	13	Gate drive: Triac 1, Master
n.c.	14	not connected
Sg	15	Gate drive: Triac 2, Slave
VEE	16	Negative, substrate
n.c.	17	not connected
PWR	18	AC resistor to Active
Sled	19	LED drive Slave
SetI	20	Set LED current

4.4 Pinning layout (20 pin)

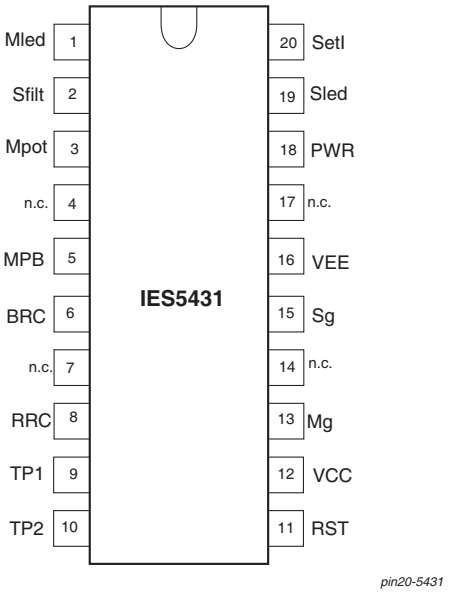

Fig.3 Pin configuration (20 pin)

5 FUNCTIONAL DESCRIPTION

5.1 IES5431

The IES5431 is a bipolar Integrated Circuit intended to be used to control an electric blanket. It features independent control of two sections of the blanket from one control IC, with the major part of the control function arising from the IES5431 built into a Master control box. Only a minimum number of components are required in the second Slave control box, which controls its section of the blanket via the circuitry in the Master. There is a 3 wire connection between the master and slave, and also from the Master to the blanket. There is no direct connection from the Slave controller to the blanket or to the mains supply.

The IES5431 contains the necessary logic and timing functions to provide automatic switching of the function of the blanket under the control of the users through ON/OFF push buttons on the Master and the Slave controllers.

For a single bed control the master alone is used, with only 2 wires needed to connect to the blanket.

See figure 4 for a typical outline of the connections between the mains supply, the Master control, the Slave, and the blanket.

The blanket must include the heating elements, together with some form of over-temperature protection. This may be by the use of an inherently safe heating wire, or by means of a screened heating element using a diode and resistor current-steering mechanism to heat a fusible link or some other similar kind of protection circuit.

5.2 PWR - Power supply input

The power supply and mains synchronisation for the IES5431 is obtained from a resistor connected from the mains active to the PWR pin as is shown in figure 5.

This resistor conducts during the positive and negative half wave voltages of the mains cycle, with the controller using the currents in each polarities for different functions. The current flowing during the positive half cycle is used to drive the LED indicators in both the master and the slave control. During the negative half cycle the current drives the negative power supply that powers the electronic control and timing circuit.

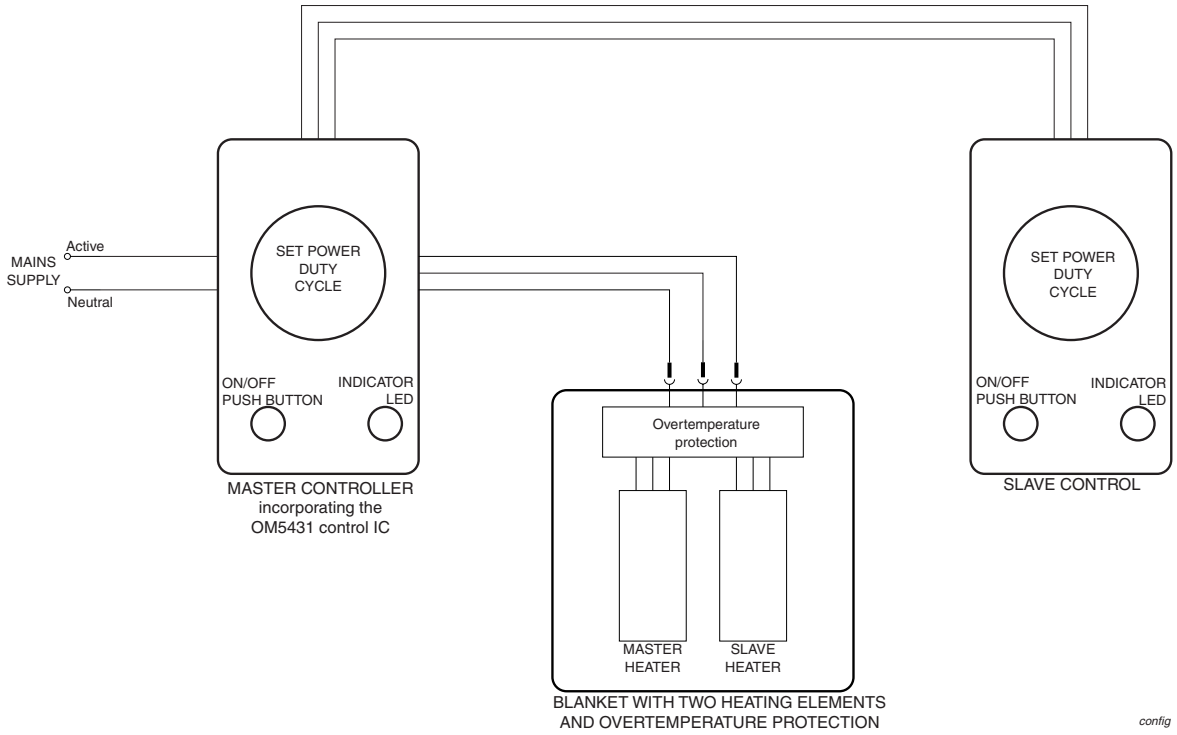

Fig.4 Blanket Circuit Configuration

A zero crossing synchronisation signal is also obtained from the time when the mains signal crosses through zero volts each half cycle.

The current is flowing in this resistor whenever the mains supply is switched on to the control. Therefore the choice of resistance value will set the ongoing power dissipation, contributing to a small amount of heat being generated in the control box.

While this heat generated is not so significant on 110V supply, on 240V it is four times greater, and steps may need to be taken to ensure that the circuit is designed to ensure a minimal supply current requirement.

The power supply current needed by the IES5431 control circuit has been designed to be minimal. However the required minimum brightness of the indicator Light Emitting Diodes (LEDs) will typically be the predominant factor in setting the power supply current. Therefore the LED brightness will set the typical power dissipation of this resistor. It needs to be remembered that the LED indicators will usually be observed in a dark room.

To keep this power to an acceptable minimum, the master and slave LEDs are connected in series, so that the same current that lights the Master LED(s) is also use to drive the LED(s) in the Slave.

If the forward voltage of the LED when it is ON is not too high, two LEDs may be used in series in both the Master and the Slave. Otherwise when dual indicators are needed, the pairs of Master and Slave LEDs will need to be run in parallel to keep within the voltage drive capability available from the IES5431 (4.5V total for the single LED, parallel LEDs, or two series LEDs, and leakage blocking diode). If the typical LED forward voltage is no greater than 2 Volts, then they may be connected in series.

The voltage present on the PWR pin is also used to provide zero-crossing information to synchronise the triac drive. As the thresholds are at VEE and VCC, an additional external resistor is required between VCC and VEE to force symmetry of the threshold detection voltage around the zero volts level.

Figure 5 also shows the current source which regulates the current drive to the Master and the Slave LEDs in series. It has an external current setting resistor to set the LED brightness making it independent of mains voltage variations.

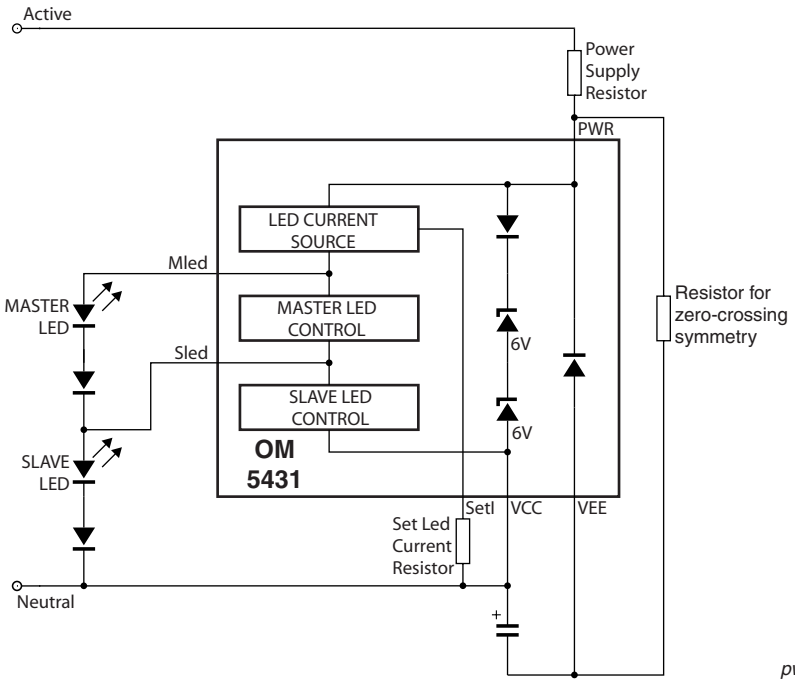

Fig.5 Power Supply and LED drive circuit

5.3 VCC - Neutral, and positive DC supply

The Neutral side of the mains supply is connected to the VCC line. That is to the positive side of the DC power supply needed to operate the IES5431. This is because triacs required a negative gate drive for their best sensitivity and performance. This is important when it is considered that modern triacs are now available which no longer operate in the firing quadrant which requires a positive gate drive to applied during the negative half cycle of the mains supply. With most triacs it is much to be preferred to use negative gate pulse drive during both the positive and negative mains half cycles.

5.4 VEE - Negative DC supply

This pin connects to the internally generated and regulated negative DC supply, and should be bypassed to VCC (common) by a capacitor of typically 100 µF 16V. The capacitor needs to be sufficiently large to maintain the operating voltage during the half cycle when it is not being charged. In addition to the current requirements of the control circuit, it must also maintain a sufficient supply voltage to provide the required minimum gate current to drive the triac gate during both the negative and positive mains half cycles.

This capacitor is charged by the current flowing in the power supply resistor during the negative mains half cycle.

Internal DC supply voltage sensing prevents the commencement of an ON cycle while the voltage is too low for reliable circuit operation. If during an ON cycle the supply voltage falls below this level the ON period will terminate at the first opportunity consistent with the cycle algorithm for gate drive.

5.5 RST - Reset signal

The Reset signal is held high by a current source from power on until the power supply has reached its normal regulated level. It then switches to a low state with a pull-down current.

The reset signal is available to reset a microcontroller, external latches or counters, so that at power up the complete system starts in a known state.

If the mains voltage drops (brownout?) and the supply voltage rail falls below the level needed to provide an adequate gate drive current for the triacs, then the reset is again pulled high and the IES5431 disables the triac gate output drives to minimise current consumption. Timing and logic functions will not be reset unless supply voltage level falls below 3.2V typically. The output drives resumes normal operation when the supply voltage reaches its normal regulated level.

The current sources pulling RST HIGH or LOW are switched to enable two IES5431 to operate from a common power supply. Thus a large current source pulls RST HIGH until the power supply voltage reaches the minimum operating voltage, and once it has reached this minimum operating voltage the current falls to a much lower maintenance value (still pulling high).

When it reaches the peak supply voltage point the shunt regulator starts to conduct, and the reset signal is switched to pull LOW (towards VEE). This is pulled low with a high current for a short time as the RST voltage falls, before dropping back to the much lower maintenance value.

If the power supply falls to below the minimum operating value for safe gate drive, the reset signal is again pulled HIGH with the large current source, dropping back to the maintenance value (still pulled HIGH) as it passes the minimum safe operating value, and only falling to LOW when the shunt regulator again reaches its regulating value.

5.6 SetI - Set LED current source

A resistor is connected from the SetI pin to VCC to set the constant current which is switched to drive the LEDs.

A single transistor VBE (+700mV) is used as the voltage reference, and a resistor current of 111µA sets the regulated LED current to 1mA. Therefore for 2mA LED current a resistor of (0.7/0.222) = 3.15kΩ is required.

The VBE reference is temperature sensitive, increasing or decreasing the LED current by 0.3% per degree C below or above room temperature respectively.

This circuit (together with all the LED drive circuit) is only active during the positive mains half cycle when positive current is available at the PWR pin.

5.7 Mled - Master LED drive

The current source set by the SetI resistor drives the Master and Slave LEDs in series so that the LED brightness will not vary with supply voltage. Whenever the available power supply current exceeds this set value for the current source drive (that is the current in the resistor driving the PWR pin), then any excess current is bypasses to VCC via a shunt regulator.

The circuit is not filtered, with the regulating current shunt operating only during the positive half cycle when current greater than the preset constant current figure is available from the power source.

The Master LED is controlled by the IES5431 circuit, and is held off by

providing an alternative current path for the constant current drive within the chip. Depending on the indicator output function required the LED is OFF, continuously ON, or flashing.

During the negative half cycle when the Slave control function is used, the Master LEDs will be reverse biased, and their leakage current may upset the high impedance duty cycle setting signal being received from the Slave. Therefore an external small signal diode (e.g. 1N4148) is required in series with the LED(s). This is not needed in a single blanket application, because the Slave LED drive is held OFF, and no signal input is derived from the unused Sled pin.

5.8 Sled - Slave LED drive

In series with the Master LED, with the LED current returning to the VCC supply rail, is the Slave LED control pin. The three connections to the Slave controller are SLED, VCC and VEE. Therefore the SLED pin must not only drive the LED in the Slave controller, it must also communicate back to the IES5431 the position of the Slave potentiometer, and whether the Slave ON/OFF switch has been pressed.

when the slave LED is on, the constant current from the current source which drives the Master LED also flows through the Slave LED. When the LEDs are switched OFF the LED drive current source is switched into a low voltage bypass path. Being a regulated current source, both Master and Slave LEDs carry the same current from the regulated supply, and their brightness does not vary with supply voltage.

During the negative half cycle the LEDs are reverse biased, and diodes are included in the circuit in series with the Maser and the Slave LEDs to prevent significant leakage current flowing.

5.9 Mg & Sg - Triac gate drive outputs

The triac gate output drives the gates of the triacs via current setting resistors. These triacs control the Master and Slave heating elements. The output drive has in-built protection to withstand transient voltage signals which may be induced on the gate of the triac by the mains supply voltage during firing of the triacs. The gate drive current should be set to a value suited to the gate sensitivity of the triac used, taking into account any additional drive which may be needed to compensate for low ambient temperatures. The firing pulse width must be wide enough to ensure that the gate drive is present before the current falls below the holding current, or the level at which for the triac will turn OFF, and then remains on until the rising current of the following half cycle has increased to a value greater than the latching current. See the triac data sheet for typical, and maximum values of holding and latching current.

The zero crossing synchronisation signals to provide the gate drive are derived from the voltage on the PWR pin. The thresholds are at VCC and VEE, and the gate pulse timing (pulse width) can be calculated from these threshold voltages together with the resistance values used in the resistor network connected to the PWR pin.

The triac is fired at all times with a signal applied to the gate during the zero-crossing of the mains, minimising rfi generation.

5.10 BRC & RRC - Boost and Run time setting

Both the Master and the Slave have independent timers which count the signals derived from boost and run oscillators the frequencies of which are independently set by external capacitor and a resistor networks connected to VEE in parallel from pins BRC & RRC giving the Boost and Run oscillator base frequencies of:

$$F_{osc} \approx \frac{1}{1.4 \times R \times C} \quad (Hz)$$

The Boost and Run time functions are nominally set to 10 minutes and 10 hours with capacitors of 100nF and a resistor value of 470kΩ. These times can be fine tuned by selecting different R or C values to provide other time constants to give different typical boost and run times.

The oscillators are stable with temperature, although there will be spread of the overall time between different controllers depending on the tolerance of the resistors and capacitors used. Amongst typical components, resistors are available to a good tolerance, but capacitors with a reasonably large capacitance are generally only available at 10% tolerance, and very occasionally are as accurate as 5% unless a significant cost penalty is incurred.

The typical values have been chosen to give a larger values of RC time constant to permit other possible applications which are more likely to require a very fast Boost time, and a moderate Run time. For example, in a food warmer.

It is possible to use a very short Boost time for some applications: if the time is shortened to less than one minute and the load temperature does not overshoot and become particularly noticeable within this time, the boost function may be seen as a quick preheat feature.

Note that the boost timer is used to provide the flashing LED to indicate the boost function is active. If the boost is set to a period different to 10 minutes, it will proportionally change the LED double flash rate as well.

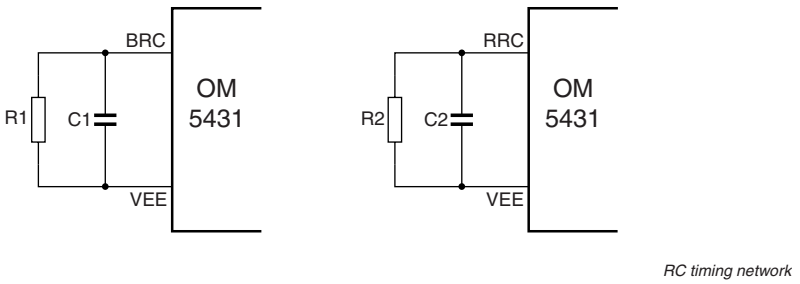

Fig.6 BRC and RRC set timing components

5.11 ON/OFF Push button control function

Both the Master and Slave heaters are independently controlled from their respective control buttons. They are switched ON and OFF using push button switches.

The function for both control switches is the same, although for the Master a pin (MPB) is switched to VEE, while for the Slave, because its controller is remote, and only connected by three wires, the switch signal is combined (multiplexed) with the LED drive and potentiometer position signal on the Sled pin.

Figure 7 shows the flow chart for the push button control function.

When the mains supply to the controller is switched on the timers are reset, and the control is in stand-by without power being applied to the blanket, and with the LEDs not illuminated.

When a push button is pressed the timed heating cycle starts. This begins 10 minutes of boost heating when power is applied to the blanket for 100% of the time. After 10 minutes the boost cycle ends, and the power in the blanket falls back to the duty cycle set by the control potentiometer for a total run time of about 10 hours.

Boost heating is indicated by a double flashing of the LED in a 4 second cycle. When the boost time has elapsed the LED remains on continuously with steady light output to indicate the normal power controlled running condition. See figure 8 for a graphical picture of the LED flashing modes.

During these times while the blanket is heating (either during the boost time, or in the subsequent power regulated run time) if the button is pressed again the controller switches into a control input mode for 5 seconds waiting for a possible further push button signal. If there is no further signal it switches off, and ends that power cycle immediately at the end of the 5 second period. This 5 second control time is indicated by the LED flashing in a single pulse mode (50% duty cycle).

If it pressed again during the 5 second control input mode it changes the active function (from boost to the normal power controlled run condition, or vice versa). That is, if it is functioning in the boost state, then pressing the button a second time within the five seconds will end the boost cycle and allow the normal run cycle to continue. If the boost cycle has ended, and it is in the normal power controlled run mode, then a new boost cycle is initiated without changing the current state of the 10 hour run timer.

This means that if a user has no wish to have the initial high power Boost cycle for the full 10 minutes, the Boost condition can be cancelled by pressing the ON/OFF push button twice within 5 seconds so that it immediately enters the Run condition.

This 5 second time period is derived from a mains divider, and will be about 4 seconds on a 60 Hz supply.

5.12 MPB - Master ON/OFF push-button switch

Shown in figure 9 is the connection of the push button switch which is used to start and stop operation of the master blanket heater.

If the ON/OFF switch contacts can become dirty, and contact is intermittent, it may be desirable to connect a capacitor across the contacts to suppress possible contact bounce.

5.13 Slave ON/OFF control

Also included in figure 9 is a typical slave circuit showing how the push button switch is connected across the LED indicator, and the series diode.

In this circuit the LED indicators are shown in parallel. Depending on the forward voltage drop of the LEDs used, it may be possible to connect them in series.

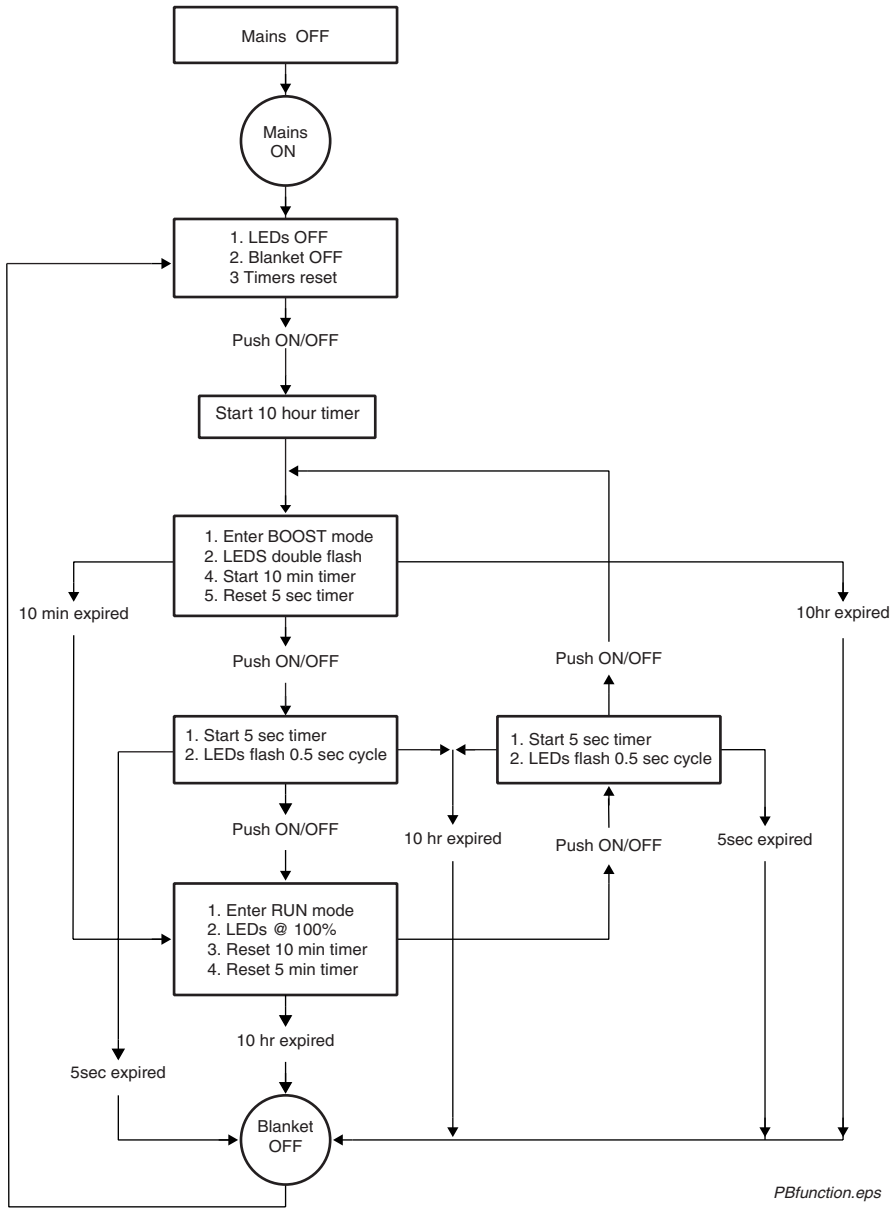

Fig.7 Push button control function flow chart

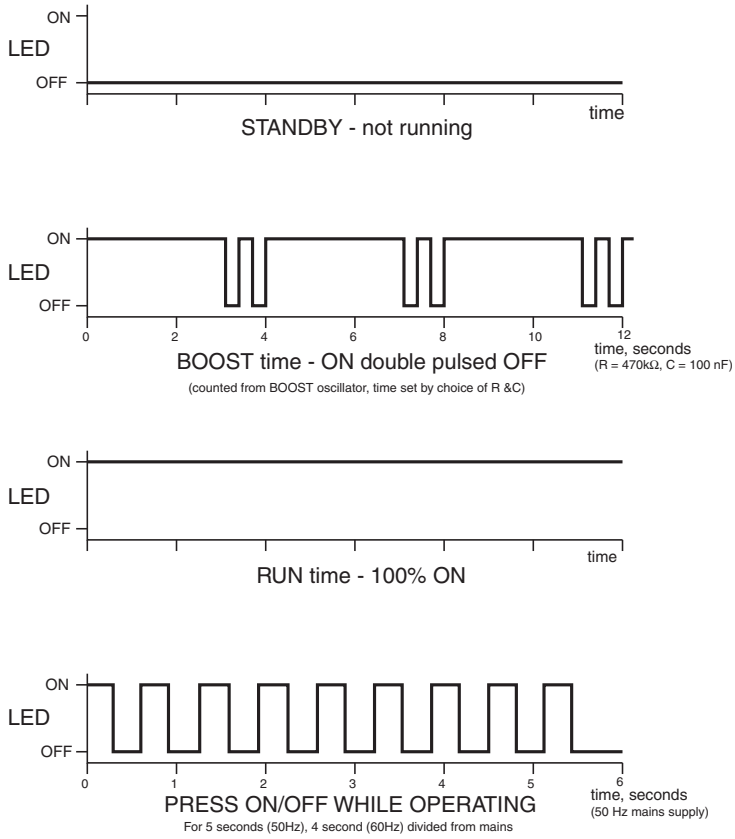

Fig.8 LED function indicating modes

5.14 Sfilt - Slave pot signal filter pin

The slave control module has three wires to connect it to the Master module. These connections are VCC, VEE, and the LED drive wire which is also used for communication (ON/OFF push button) and the potentiometer position sensing. These connections, and the circuit of the Slave module are shown in figure 9.

This communication and drive wire fulfils three functions.

During the positive half cycle of the mains supply the signal on this wire is positive, and it drives the LED (if the LED is ON). When the LED is not ON, a positive voltage that is less than the LED knee voltage is present so that the IES5431 can detect when the Slave ON/OFF push button has been pressed.

The push button shorts the LED/signal wire to VCC, and therefore while it is pressed, shorts out the LED (and the potentiometer). This is detected by the IES5431, and appropriate action is taken when the push button is released. While the button is being pressed the LED is extinguished.

During the negative half cycle the LED is reverse biased, and any leakage current is blocked by a diode, so the voltage from the Slave duty cycle setting potentiometer wiper contact (the potentiometer is bridged between VCC and VEE) is transmitted back to the IES5431 via an isolating resistor.

Some filtering is applied to this signal path by applying a capacitor (recommended 1 nF, and 2.2 nF maximum) from SLED to VCC. Because the duty cycle voltage is only present during negative half cycles further filtering is supplied by a capacitor (typically 100 nF) connected to the Sfilt pin. This is part of a sample and hold circuit which charges the capacitor during the negative half cycle, and holds this voltage during the positive half cycle when the Slave LEDs are being driven.

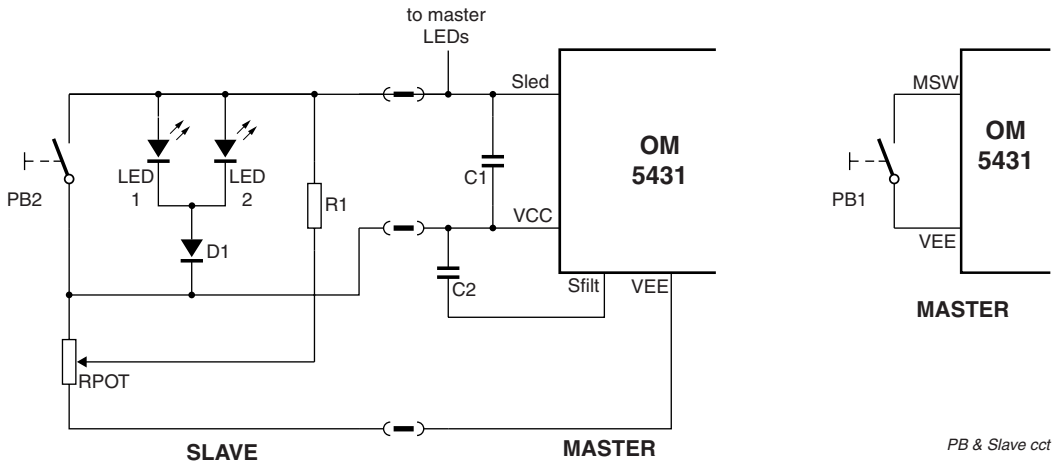

Fig.9 Slave circuit and Master push button control

5.15 Mpot - Master potentiometer input

The Master potentiometer input drives a linear analogue-to-digital duty cycle converter.

When Mpot is at the voltage VCC, the output duty cycle in the run mode is 100%. This decreases linearly from 100% to zero as the voltage on Vpot is reduced from VCC to a voltage of (VEE+1.4) V (note that VEE is a negative voltage with respect to VCC). If VEE = –8.0 V, then for a voltage on Mpot of below –6.8 V the output will be OFF.

Figure 10 shows the simplest way to provide the control signal for the Mpot voltage. As the Mpot input offers very little loading on the voltage source, a simple voltage divider from VEE to VCC can provide the input signal. The 1.4 volt dead band at the zero output, VEE end of the divider range is to allow a secure mechanical OFF position to be made available on the potentiometer, possibly with a mechanical indent location for OFF.

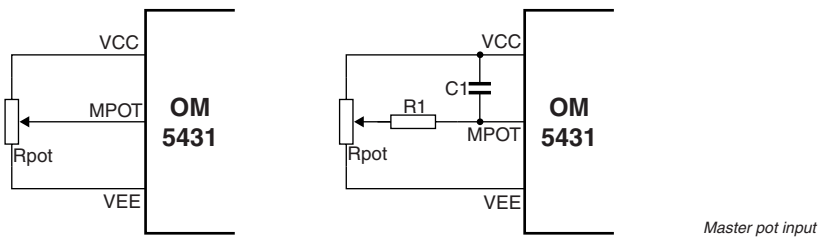

Fig.10 Master potentiometer input circuit, without and with filter

Between 0% and 100% the duty cycle increases in steps of 4%, giving a total of about 25 duty cycle steps. Because the mains power can only be set in increments of whole cycles, it is not possible to have a continuously variable duty cycle, and the stepped control characteristic is a natural consequence of controlling the mains powered load with zero crossing firing of the triac so as to not generate rfi.

This is shown in figure 11.

A filter network (capacitor and series resistor) from Mpot to VCC may be required to suppress noise on this input pin, although with good printed board layout it should not be necessary.

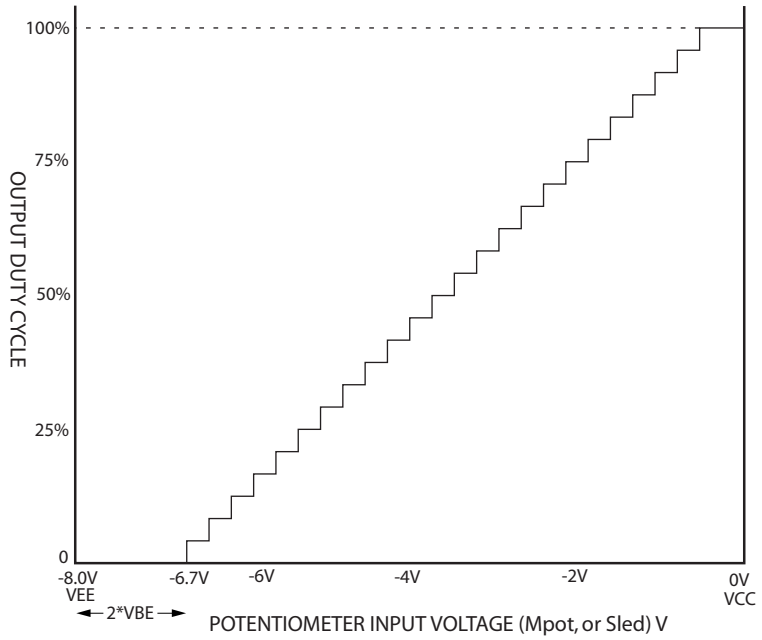

Fig.11 Master (Mpot) and Slave (Sled) input voltage versus duty cycle characteristic

5.16 TP1 & TP2 function

The IES5431 incorporates timers to perform the various timing functions. For example, boost time, run time, and the five second time-out timers for both the Master and Slave functions. These boost and run timers contain 19 and 13 divider stages respectively. Although these can be run at faster rates than their normal oscillator clock frequency, a lot of the time taken to test the device is still used in testing these timers. So test point 1 (TP1) and test point 2 (TP2) were introduce to speed up the test time for both the master and slave run timers.

When TP1 and TP2 are not connected then both switches SW1 and SW2 in figure 12 will be open, allowing all 19 stages of the run time divider to count normally. If TP1 is connected to VEE and TP2 is unconnected, then SW1 will activate which allows stages 2, 3, and 4 to be tested while stage 1 is bypassed (see figure 12 for the stage blocks). If TP1 is unconnected and TP2 is connected to VEE, then SW2 will activate which allows stages 1, 2, and 4 to be tested while stage 3 is ignored. If both TP1 and TP2 are connected to VEE, then both switches SW1 and SW2 will activate which allows stages 2 and 4 to be tested. The table shows the possible combinations, and the function for the possible connections of TP1 and TP2.

The intermediate stage 2 is necessary to provide a continuous signal flow through the run time divider to ensure all stages are tested and working correctly.

TP1	TP2	SW1	SW2	FUNCTION
o/c	o/c	open	open	default - all available stages used
s/c to VEE	o/c	closed	open	test stages 2, 3, and 4 (12 stages)
o/c	s/c to VEE	open	closed	test stages 1, 2, and 4 (12 stages)
s/c to VEE	s/c to VEE	closed	closed	test stages 2, and 4 (4 stages)

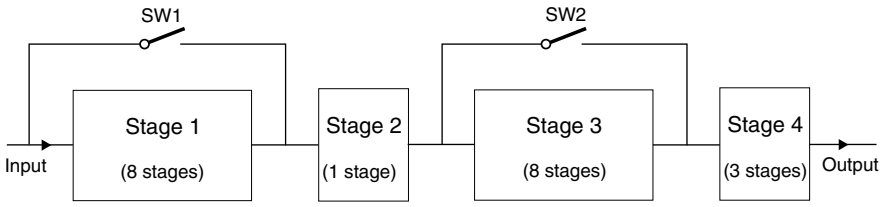

Fig.12 TP1 and TP2 Test pin function

6 IMPORTANT: ELECTRICAL SAFETY WARNING

The IES5431 circuit is connected to the mains electrical supply and operates at voltages which need to be protected by proper enclosure and protective covering. Application circuits for IES5431 should be designed to conform to relevant standards (such as IEC 65, or Australian Standards AS3100, AS3250 and AS3300), and should only be used in a manner that ensures the appliance in which they are used complies with all relevant national safety and other Standards.

It is recommended that a printed circuit board using this integrated circuit be mounted with non-conductive clips, and positioned such that the minimum creepage distances from the assembly to accessible metal parts, and between high voltage points cannot be transgressed.

It should be noted that as there are Mains Voltages on the circuit board adequate labelling should be attached to warn service personnel, and others, that this danger exists.

A control board assembly should be mounted with sufficient air flow across its surface to prevent the heat dissipated in various components from causing an unacceptable rise in the ambient temperature. In particular the triacs need to have an adequate heatsink, as exceeding its rated maximum junction temperature can result in loss of control.

The board should be mounted in a place that is clean and dry at all times, not subject to condensation or the accumulation of dust and other contaminants.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I	DC current (any pin except VEE, Mg and Sg)		–	20	mA
I	DC current (pin VEE)		–	150	mA
I	DC current (pins Mg and Sg)		–	70	mA
V_{PWR}	Voltage range PWR		VEE–0.8	+12	V
V_{SetI}	Voltage range SetI		VCC–0.8	+0.8	V
V_{RRC}	Voltage range RRC		VEE–0.8	VCC+0.8	V
V_{BRC}	Voltage range BRC		VEE–0.8	VCC+0.8	V
V_{Mg}	Voltage range Mg, transient		VEE–30	+50	V
V_{Sg}	Voltage range Sg, transient		VEE–30	+50	V
V_{Mpot}	Voltage range Mpot		VEE–0.8	VCC+0.8	V
V_{MPB}	Voltage range MPB		–0.8	+0.8	V
V_{Mled}	Voltage range Mled		VEE–0.8	VCC+10	V
V_{Sled}	Voltage range Sled		VEE–0.8	VCC+10	V
P_{tot}	total power dissipation		–	300	mW
T_{stg}	storage temperature		–40	+150	°C
T_{amb}	operating ambient temperature		0	+85	°C

8 CHARACTERISTICS

At T_{amb} = 25°C; Voltages are specified with respect to V_{CC}

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power supply						
–VEE	supply voltage (operating)	I_{CC} = 1 mA	7.4	8.0	8.6	V
–IEE	quiescent current	with pin TRG open circuit	–	530	600	µA
RST pin Reset						
I_{RST}(pwr up)	initial reset active pull up signal during power-up time	V_{EE} = 0 to –6.5V	–	50	–	µA
I_{RST}(pwr up)	initial active reset pull up signal during power-up time	V_{EE} = –6.5 to –8.0V	–	6	–	µA
I_{RST}(initial low)	initial reset pull down signal after power-up	V_{EE} = –8.0 to –6.5V	–	–50	–	µA
$t_{reset\ low}$	initial high current reset pull down time (reset OFF)	while RST voltage falls from V_{CC} to V_{EE}	–	5	–	µs
I_{RST}(low)	reset pull down signal during normal run time	V_{EE} = –8.0 to –6.5V	–	–6	–	µA
I_{RST}(active – low V_{EE})	reset pull up signal while V_{EE} is low	$\|V_{EE}\|$ < 6.5V	–	50	–	µA
$I_{RST(recover\ from\ brownout)}$	reset pull up signal during recovery from V_{EE} low	V_{EE} = –6.5 to –8.5V	–	6	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Gate drive pins Mg and Sg						
I_G	gate current (triac T1 to V_{CC})	set by R_G connected from Mg or Sg to gate	–	–	50	mA
V_{Gsat}	gate drive saturation voltage, pins Mg or Sg to VEE	at I_G = 50 mA	–	600	–	mV
V_{Gsat}	gate drive saturation voltage, pins Mg or Sg to VEE	at I_G = 15 mA	–	–	250	mV
Power sensing thresholds for zero crossing on PWR						
V_{UT}	upper threshold		–	0	–	mV
$-V_{LT}$	lower threshold		–	VEE	–	V
LED Drive pins Mled and Sled						
V_{SetI}	voltage to set LED current source	I_{LED} = 9 times setting resistor current to VCC	–	650	–	mV
V_{Mled}ON	voltage across Master LED when ON	at 2 mA LED current	2	–	5	V
V_{Mled}OFF	voltage across Master LED when OFF	VPWR positive	–	1.6	–	V
V_{Sled}ON	voltage across Slave LED when ON	at 2 mA LED current	2	–	5	V
V_{Sled}OFF	voltage across Slave LED when OFF	VPWR positive	–	1.6	–	V
$V_{S\text{-}PB}$	voltage threshold for Slave push button	VPWR positive	–	–	0.65	V
MPB pin Master control push button input						
V_{MPB}	no load voltage		–	V_{EE} + 600	–	mV
I_{MPB}	input current when switched		–	3	–	µA
t_{MPB}	pulse width to detect as low	minimum press button closed time	60	–	–	ms
Timing networks for Boost and Run times (BRC and RRC)						
$V_{threshold}$High	oscillator upper threshold	= 4 * V_{BE} above V_{EE}	–	V_{EE} + 2.8	–	V
$V_{threshold}$Low	oscillator lower threshold	= one V_{BE} above V_{EE}	–	V_{EE} + 0.7	–	V
I_{pullup}	charge current	charge C from the lower to the upper threshold	–	210	–	µA
$I_{osc\ leakage}$	discharge leakage current	V_{RC} = 1.5 V	–1	–	+1	µA
f_{osc}	oscillator frequency	R = 470 kΩ, C = 100 nF	–	15	–	Hz
Boost timing						
t_{boost}	total boost time	divider = 13 stages, R = 470 kΩ, C = 100 nF	–	9.0	–	minutes
$t_{LED\ dbl\ flash}$	ON/OFF clock pulse width: during boost period with double OFF pulse	Step pulse width: (ON 13 steps, OFF, ON, OFF, repeat)	–	250	–	ms

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LED\ dbl\ flash}$	boost flash period (ON with double OFF pulse)	divided from boost oscillator = 6 stages	–	4	–	s
Run timing						
t_{run}	total run time	divider = 19 stages, R = 470 kΩ, C = 100 nF	–	9.6	–	hours
ON/OFF push button indicator timing (wait time to press button again)						
t_{flash}	total wait time: divided from mains, 8 stage divider	mains freq. = 50 Hz mains freq = 60 Hz	–	5 4	–	s s
f_{flash}	flash frequency during the wait time, 5 stage divider	mains freq = 50 Hz mains freq = 60 Hz	–	1.56 1.87	–	Hz Hz
δ	duty cycle		–	50	–	%
Slave filter						
I_{Scap}Hold	leakage in hold condition	V_{PWR} positive	–1	–	+1	µA
IScapsample	charge current to sample pot voltage on capacitor	V_{PWR} negative	–	210	–	µA
IScapsample	discharge current to sample pot voltage on capacitor	V_{PWR} negative	–	500	–	µA
Pot inputs to A to D duty cycle converters						
I_{Mpot}input	input current to A to D converter	V_{Mpot} = -4 V.	–1	+0.1	+1	µA
V_{pot}OFF	input voltage range for fully OFF condition		–VEE	–	–VEE +1.3	V
V_{pot}ON	input voltage range for duty cycle output	linear increase from 0% to 100% over range	–VEE +1.3	–	VCC – 0.2	V

9 APPLICATION INFORMATION

9.1 Design considerations

Resistors connected directly to the AC supply rail should be specified to reliably withstand this voltage. Transient voltages carried on the mains can cause failure of resistors that are not designed to withstand such voltages well in excess of the typical mains peak value.

9.2 Double blanket circuit

Figure 13 shows an application circuit using the IES5431 to control a double blanket. It shows two LED indicators in series. The maximum voltage across the LED and diode in series must be less than 5 V.

The potentiometer circuit shown provides 0 to 100% duty cycle control of the power to the loads.

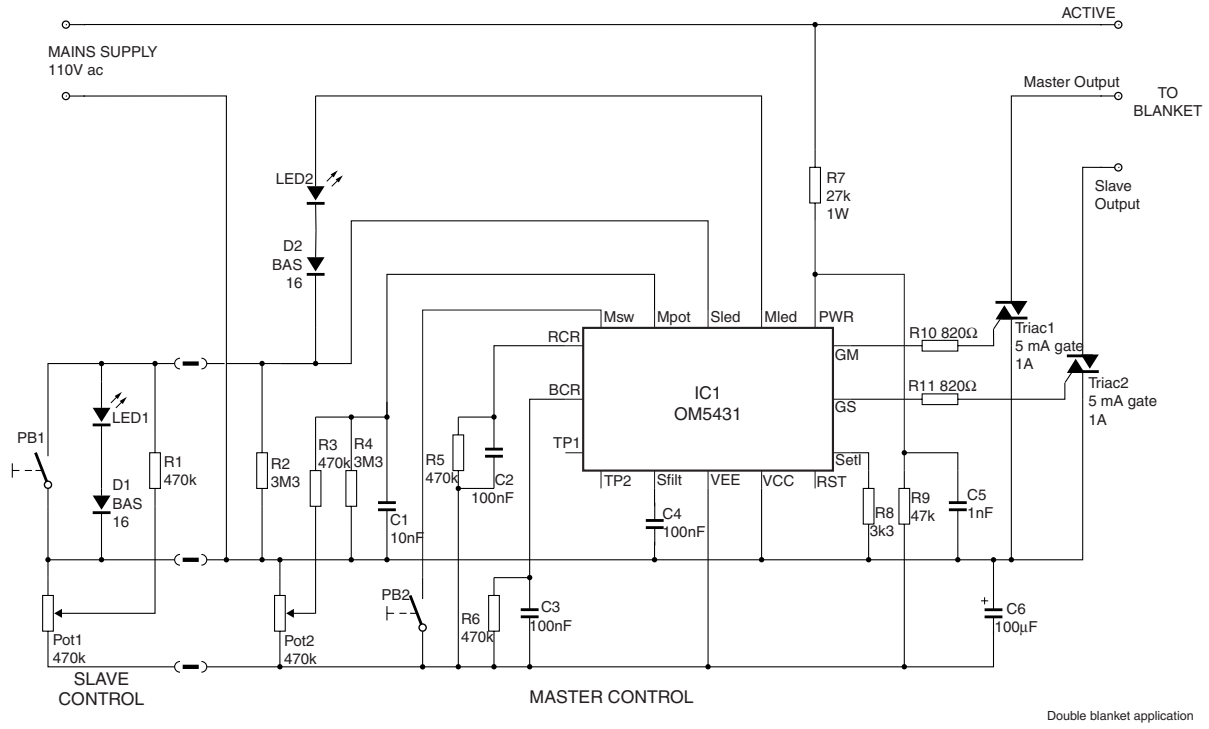

Fig.13 Application circuit: double blanket control using IES5431

9.3 Single blanket circuit

Figure 14 shows a single blanket circuit.

In this circuit a single LED indicator is shown. There is no need to include a series diode as LED leakage currents would only upset operation of the unused Slave circuit.

9.4 Power supply requirements

The DC power supply current available for the operation of the circuit is derived from the resistor connected to the PWR terminal. The average current in this resistor during the negative half cycle of the AC signals provides charge for the 100 µF power supply capacitor connected between VCC and VEE.

Amongst the current requirements of the IES5431 circuit, the triac gate drive presents a significant DC current load for the circuit power supply. As the gate pulse must be wide enough for the load current to reach the triac's specified holding current while the gate pulse is still being applied to the gate it may be necessary to calculate the required worst case DC supply and ensure that on low mains supply voltage there is adequate current available.

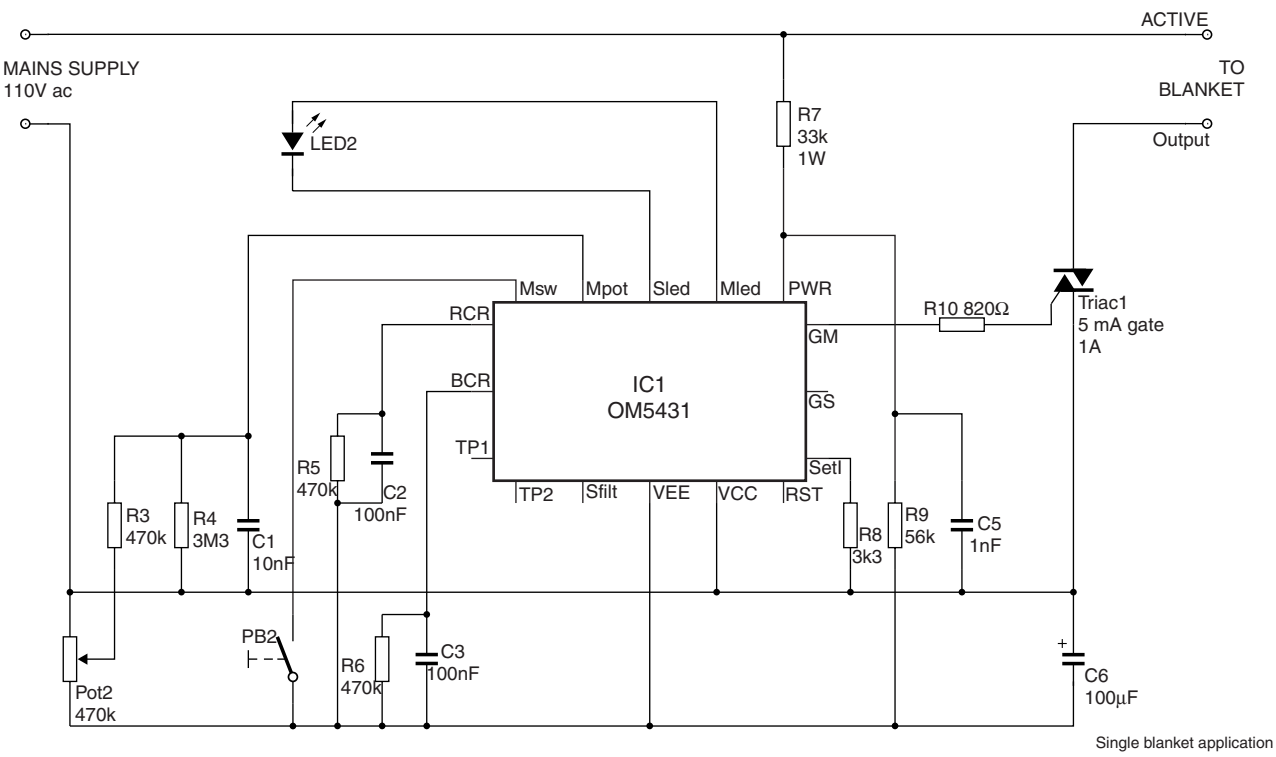

Fig.14 Application diagram: Single blanket control using IES5431

As the sine-wave load current falls below the holding current, the triac can turn off if there is no gate drive present. This can present a small transient voltage across the load, creating rfi which may exceed standards limits. As the supply voltage rises after crossing through zero, if the gate pulse ends before the current in the triac has reached the triac holding current, then the triac can turn off when the gate pulse ends too soon, and not conduct during that following half cycle.

In the level sensing circuit of the PWR terminal, the voltage thresholds are at the mains zero reference (VCC), and the negative regulated power supply voltage, (VEE). Therefore a second resistor, equal to the main power supply resistor (R4) from active to PWR, is used from PWR to VEE (R6). With this resistor the positive threshold is reached on the PWR pin when the positive mains voltage is equal in magnitude to VEE, while the negative mains voltage threshold is equal to –VEE. Thus by the divider action of the two resistors connected to PWR, the mains voltage at the positive threshold is equal to the mains voltage as the PWR pin crosses the negative threshold of –VEE.

By connecting a resistor from PWR to VCC (in addition to the resistor from PWR to VEE) the gate pulse can be further widened to ensure that both the holding current and the latching current of the triac fall within the normal worst case pulse width.

Adding this resistor to VCC from PWR requires calculation of both the negative and positive thresholds switching points to ensure that at both voltage polarities (at the start and end points of the gate pulse) the load current is greater than the holding and latching currents at the switching thresholds.

9.5 Potentiometer circuits for limiting the power range

In figure 15 a circuit is shown in which resistors can be added to the simple voltage divider between VCC and VEE to limit the range of the input voltage to the Mpot (and the Slave input via Sled), and in this way limit the control range covered by the potentiometer to a range that does

not cover the full zero to 100% range capability of the IES5431.

If there is no significant impedance, or current input loading on the wiper tap on the potentiometer, then by using the potentiometer as a voltage divider between VCC and VEE the resistance tolerance of the potentiometer does not influence the divided voltage. For the IES5431 the Mpot and Sled pins present very little loading to the potentiometer divider. But even if they did present a load impedance at the IC input pin, it would not effect the duty cycle at each end of the potentiometer travel. Such a load impedance would result in curvature of the potentiometer control characteristic, and any spread from the tolerance of the potentiometer resistance would apply only to the curvature the IC loading presented.

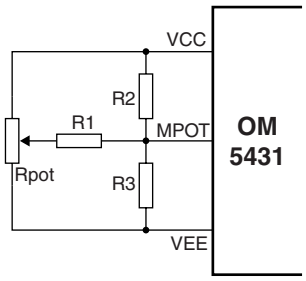

Fig.15 Potentiometer circuit to set a control range of less than 0 to 100%

As is shown in figure 15 adding the extra resistors R1, R2 and/or R3 adapts the range covered by the voltage applied to Mpot to a range that corresponds to the required reduced duty cycle span.

From the graph in figure 11 the required upper and lower (minimum and maximum) duty cycle readings can be read off the horizontal scale in terms of voltage. The input resistor network can then be analysed to find resistor values which provide these voltages when the potentiometer is at the extremes of its range.

The choice of potentiometer resistance is limited by the loading which can be applied to the -VEE power supply. Choice of 470k will load the 8 V power supply with a current of 17 μA. The current in the resistor network loads the wiper tap on the potentiometer, the current flowing in R1 needing to be small compared to the current in the potentiometer.

As an example, a circuit together with a control graph is shown in figure 16. This includes fixed resistors (R2 & R3) to restrict the duty cycle range covered by the full potentiometer rotation. The characteristic control graph of setting (knob rotation angle) against duty cycle is shown together with the required circuit values (linear potentiometer, and resistors R1, R2 and R3) giving control over the range of 40% to 80%.

This has been calculated on a spreadsheet which also includes a calculation of the error in the linearity caused by the resistor loading on the potentiometer. (Note that the maximum error may be near the mid point on the potentiometer if only R2 or R3 are used alone, while if both R2 and R3 are used the error curve is S shaped with an accurate point around the mid-range of the potentiometer. The equivalent circuit load of the potentiometer at its mid point is one quarter of the total resistance Rpot, or 117.5 kΩ. At each end of its travel the potentiometer impedance is zero ohms.

Because the accuracy of the voltage on Vpot depends on the divided voltage on the potentiometer wiper, and accurate resistors chosen to set the required range, then potentiometer and resistor tolerance variance will have negligible effect on the actual duty cycles achieved.

The Excel spreadsheet potcalc.xls automatically calculates the control range for different resistor values in the input network. It shows graphically the duty cycle stepped characteristic that will be provided by the IES5431 controller.

In addition another graph in the spreadsheet shows the ideal characteristic (by ignoring the resistance of the potentiometer and giving a straight line) and the real curve which deviates from the straight line depending on the loading offered

by the resistor network R1 to R3. This error may be curved above or below the ideal line or S shaped, depending on whether the R2 or R3 resistors are used, or both.

The final spreadsheet graph shows the error as a deviation from the ideal curve in percentage terms, ignoring the stepped characteristic of the input circuit of the IES5431. It needs to be recognised that one step is about 4%, and that an error of less than 4% can be ignored, especially considering that it is accurate anyway when the pot is fully clockwise or anti-clockwise. As can be shown in the calculated spreadsheet values, changing the pot resistance only changes the error, the end points are not dependent on pot tolerance.

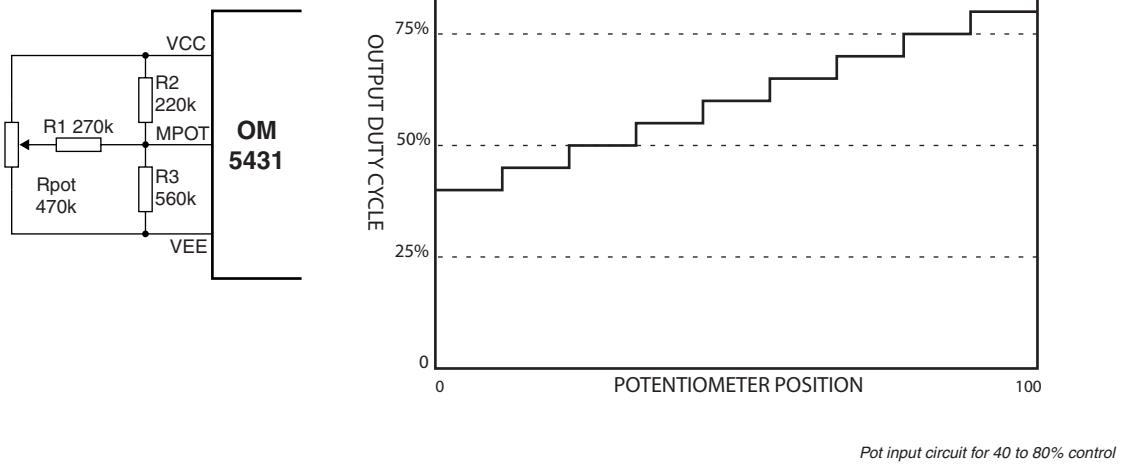

Fig.16 Potentiometer characteristic and circuit to set a control range of 40 to 80%

9.6 Gate drive

The 820 Ω gate resistor shown in the application circuits gives a gate drive figure with an appropriate tolerance margin over 5 mA, giving the current needed to drive a 5 mA triac at temperatures below 25 degrees. Thus for the circuit shown a triac would need to be specified that is suitable for 5 mA triggering with negative triggering signal for both positive and negative voltage on T2. From the threshold levels determined from the resistive networks on PWR and the AC supply, the gate pulse-width can be calculated assuming a sine wave supply. The specification of the triac will indicate the holding current and the latching current for switch-on, and knowing the minimum load with which the circuit is to operate, then proper design will ensure that the gate pulse is present before the triac switches off at the end of each half cycle, and also continues until after the triac current has reached the latching current figure.

10 ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	NAME	DESCRIPTION	VERSION	ROHS
IES5431T	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1	Yes
IES5431D	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4mm	TSSOP16	Yes

Note

1. The preferred package is the IES5431T (test capability reasons).
2. With forward notice the IES5431M can be provided in production quantities.
3. An equivalent part, OM5431P (DIP-16), is available in sample quantities for bench prototype work.

Other package options are available - contact Hendon Semiconductors for details. For more information on packages, please refer to the document “Integrated Circuit Packaging and Soldering Information” on the Hendon Semiconductors web site.

11 ESD CAUTION

Electrostatic Discharge (ESD) sensitive device. ESD can cause permanent damage or degradation in the performance of this device. This device contains ESD protection structures aimed at minimising the impact of ESD. However, it is the users responsibility to ensure that proper ESD precautions are observed during the handling, placement and operation of this device.

12 DOCUMENT HISTORY

REVISION	DATE	DESCRIPTION
1.0	20070606	Adapted from OM5431 datasheet dated 08 July 2003

13 DEFINITIONS

Data sheet status	
Engineering sample information	This contains draft information describing an engineering sample provided to demonstrate possible function and feasibility.Engineering samples have no guarantee that they will perform as described in all details.
Objective specification	This data sheet contains target or goal specifications for product development. Engineering samples have no guarantee that they will function as described in all details.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later. Products to this data may not yet have been fully tested, and their performance fully documented.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

14 COMPANY INFORMATION

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