MOTOROLA

MCM4027A

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4027A is a 4096 x 1 bit high-speed dynamic Random Access Memory. It has smaller die size than the MCM4027 providing improved speed selections. The MCM4027A is fabricated using Motorola's highly reliable N-channel silicon-gate technology.

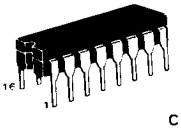
By multiplexing row and column address inputs, the MCM4027A requires only six address lines and permits packaging in Motorola's standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM4027A incorporates a one-transistor cell design and dynamic storage techniques, with each of the 64 row addresses requiring a refresh cycle every 2.0 milliseconds.

- Maximum Access Time = 120 ns – MCM4027AC1
  150 ns – MCM4027AC2
  200 ns – MCM4027AC3
  250 ns – MCM4027AC4
- Maximum Read and Write Cycle Time =
  320 ns – MCM4027AC1, C2
  375 ns – MCM4027AC3, C4
- Low Power Dissipation – 470 mW Max (Active)
  27 mW Max (Standby)
- 3-State Output for OR-Ties
- On-Chip Latches for Address, Chip Select, and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Industry Standard 16-Pin Package
- Page-Mode Capability
- Compatible with the Popular 2104/MK4096/MCM6604
- Second Source for MK4027

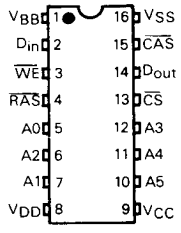
MOS
(N-CHANNEL, SILICON-GATE)

4096-BIT DYNAMIC RANDOM ACCESS MEMORY



C SUFFIX
FRIT-SEAL CERAMIC PACKAGE
CASE 620

PIN ASSIGNMENT

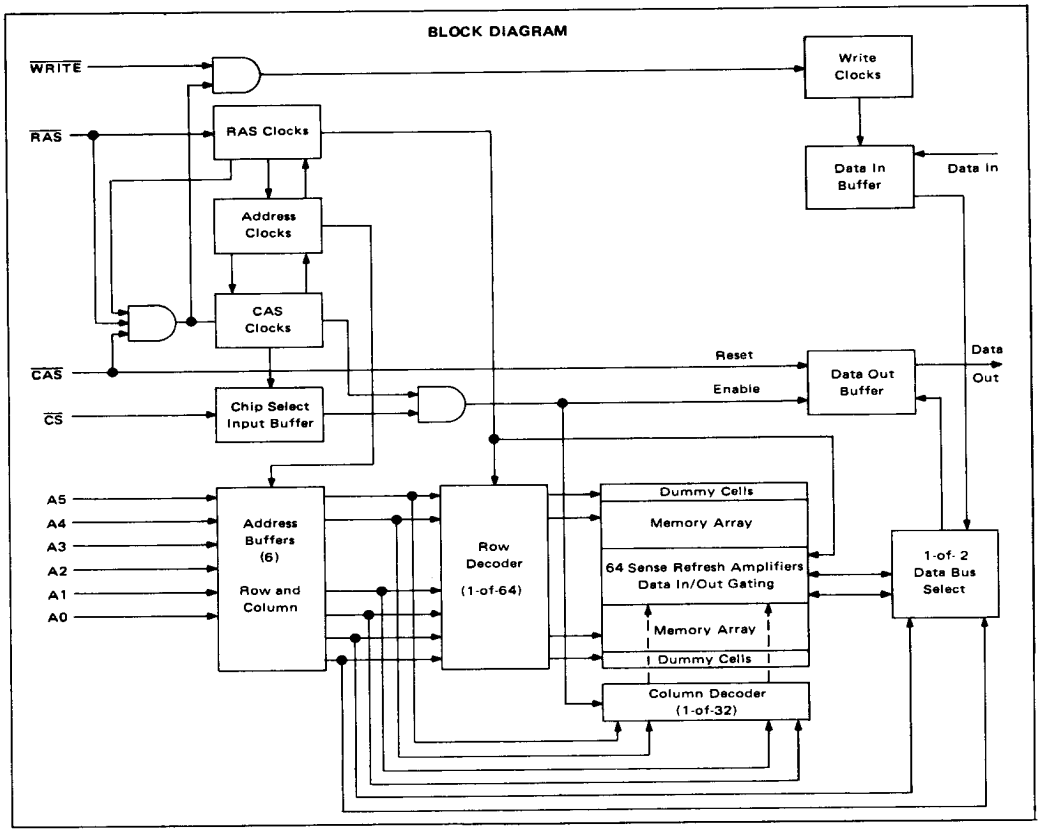


TRUTH TABLE

Inputs				Data Out			Cycle Power	Ref	Function
RAS	CAS	CS	WE	Previous	Interim	Present			
L	L	L	L	Valid data	High Imp.	Input data	Full-operating	Yes	Write cycle
L	L	L	H	Valid data	High Imp.	Valid data (cell)	Full-operating	Yes	Read cycle
L	L	H	X	Valid data	High Imp.	High Imp.	Full-operating	Yes	Deselected-refresh
L	H	X	X	Valid data	Valid data	Valid data	Reduced operating	Yes	RAS only-refresh
H	L	X	X	Valid data	High Imp.	High Imp.	Standby	No	Standby-output disabled
H	H	X	X	Valid data	Valid data	Valid data	Standby	No	Standby-output valid

H = High, L = Low, X = Don't Care

DS9464R1/11-78



OPERATING CHARACTERISTICS

ADDRESSING

The MCM4027A has six address inputs (A0–A5) and two clock signals designated Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). At the beginning of a memory cycle, the six low order address bits A0 through A5 are strobed into the chip with $\overline{RAS}$ to select one of the 64 rows. The row address strobe also initiates the timing that will enable the 64 column sense amplifiers. After a specified hold time, the row address is removed and the six high order address bits (A6–A11) are placed on the address pins. This address is then strobed into the chip with $\overline{CAS}$. Two of the 64 column sense amplifiers are selected by A1 through A5. A one of two data bus select is accomplished by A0 to complete the data selection. The Chip Select ($\overline{CS}$) is latched into the port along with the column addresses.

DATA OUTPUT

In order to simplify the memory system designed and reduce the total package count, the MCM4027A contains an input data latch and a buffered output data latch. The state of the output latch and buffer at the end of a memory cycle will depend on the type of memory cycle performed and whether the chip is selected or unselected for that memory cycle.

A chip will be unselected during a memory cycle if:

(1) The chip receives both $\overline{RAS}$ and $\overline{CAS}$ signals, but no $\overline{Chip\ Select}$ signal.

(2) The chip receives a $\overline{CAS}$ signal but no $\overline{RAS}$ signal. With this condition, the chip will be unselected regardless of the state of $\overline{Chip\ Select}$ input.

If, during a read, write, or read-modify-write cycle,

the chip is unselected, the output buffer will be in the high impedance state at the end of the memory cycle. The output buffer will remain in the high impedance state until the chip is selected for a memory cycle.

For a chip to be selected during a memory cycle, it must receive the following signals: $\overline{RAS}$, $\overline{CAS}$, and $\overline{Chip\ Select}$. The state of the output latch and buffer of a selected chip during the following type of memory cycles would be:

(1) Read Cycle – On the negative edge of $\overline{CAS}$, the output buffer will unconditionally go to a high impedance state. It will remain in this state until access time. At this time, the output latch and buffer will assume the logic state of the data read from the selected cell. This output state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(2) Write Cycle – If the $\overline{WE}$ input is switched to a logic 0 before the $\overline{CAS}$ transition, the output latch and buffer will be switched to the state of the data input at the end of the access time. This logic state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(3) Read-Modify-Write – Same as read cycle.

DATA INPUT

Data to be written into a selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of the $\overline{WE}$ and $\overline{CAS}$ signals. The last of these signals to make a negative transition will strobe the data into the latch. If the $\overline{WE}$ input is switching to a logic 0 in the beginning of a write cycle, the falling edge of $\overline{CAS}$ strobes the data into the latch. The data setup and hold times are then referenced to the negative edge of $\overline{CAS}$.

If a read-modify-write cycle is being performed, the $\overline{WE}$ input would not make its negative transistion until after the $\overline{CAS}$ signal was enabled. Thus, the data would not be strobed into the latch until the negative transistion of $\overline{WE}$. The data setup and hold times would now be referenced to the negative edge of the $\overline{WE}$ signal. The only other timing constraints for a write-type-cycle is that both the $\overline{CAS}$ and $\overline{WE}$ signals remain in the logic 0 state for a sufficient time to accomplish the permanent storage of the data into the selected cell.

INPUT/OUTPUT LEVELS

All of the inputs to the MCM4027A are TTL-compatible, featuring high impedance and low capacitance (5 to 7 pF). The three-state data output buffer is TTL-compatible and has sufficient current sink capability (3.2 mA) to drive two TTL loads. The output buffer also has a separate V_{CC} pin so that it can be powered from the same supply as the logic being employed.

REFRESH

In order to maintain valid data, each of the 64 internal rows of the MCM4027A must be refreshed once every 2 ms. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. Any read, write, or read-modify-write cycle will refresh an entire internally selected row. However, if a write or read-modify-write cycle is used to perform a refresh cycle the chip must be deselected to prevent writing data into the selected cell. The memory can also be refreshed by employing only the $\overline{RAS}$ cycle. This refresh mode will not shorten the refresh cycle time; however, the system standby power can be reduced by approximately 30%.

If the $\overline{RAS}$ only refresh cycles are employed for an extended length of time, the output buffer may eventually lose data and assume the high impedance state. Applying $\overline{CAS}$ to the chip will restore activity of the output buffer.

POWER DISSIPATION

Since the MCM4027A is a dynamic RAM, its power drain will be extremely small during the time the chip is unselected.

The power increases when the chip is selected and most of this increase is encountered on the address strobe edge. The circuitry of the MCM4027A is largely dynamic so power is not drawn during the whole time the strobe is active. Thus the dynamic power is a function of the operating frequency rather than the active duty cycle.

In a memory system, the $\overline{CAS}$ signal must be supplied to all the memory chips to ensure that the outputs of the unselected chips are switched to the high impedance state. Those chips that do not receive a $\overline{RAS}$ signal will not dissipate any power on the $\overline{CAS}$ edge except for that required to turn off the chip outputs. Thus, in order to ensure minimum system power, the $\overline{RAS}$ signal should be decoded so that only the chips to be selected receive a $\overline{RAS}$ signal. If the $\overline{RAS}$ signal is decoded, then the chip select input of all the chips can be set to a logic 0 state.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = Ground.)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	Vdc	2
	V_{CC}	V_{SS}	5.0	V_{DD}	Vdc	3
	V_{SS}	0	0	0	Vdc	2
	V_{BB}	-4.5	-5.0	-5.5	Vdc	2
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	5.0	7.0	Vdc	2, 4
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.2	5.0	7.0	Vdc	2, 4
Logic 0 Voltage, all inputs	V_{IL}	-1.0	0	0.8	Vdc	2, 4

DC CHARACTERISTICS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.) Notes 1, 5

Characteristic	Symbol	Min	Typ	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}			35	mA	6
V_{CC} Power Supply Current	I_{CC}				mA	7
Average V_{BB} Power Supply Current	I_{BB}			250	µA	
Standby V_{DD} Power Supply Current	I_{DD2}			2	mA	9
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}			25	mA	6
Input Leakage Current (any input)	$I_{I(L)}$			10	µA	8
Output Leakage Current	$I_{O(L)}$			10	µA	9, 10
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4			Vdc	
Output Logic 0 Voltage @ I_{out} = 3.2 mA	V_{OL}			0.4	Vdc	

NOTES 1 through 11:

1. T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}$(min). Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all ac parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH}(min) specification is not guaranteed in this mode.
4. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5 v).
5. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
6. Current is proportional to cycle rate. I_{DD1}(max) is measured at the cycle rate specified by t_{RC}(min).
7. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
8. All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at +10 volts.
9. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
10. $0 \text{ V} \leq V_{Out} \leq +10 \text{ V}$.
11. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

EFFECTIVE CAPACITANCE (Full operating voltage and temperature range, periodically sampled rather than 100% tested) Note 11

Characteristic		Symbol	Max	Unit
Input Capacitance	(A0-A5), D_{in}, $\overline{CS}$	$C_{in(EFF)}$	5.0	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		10.0	
Output Capacitance		$C_{out(EFF)}$	7.0	pF

ABSOLUTE MAXIMUM RATINGS (See Notes 1 and 2)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}*	V_{in}, V_{out}	-0.5 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Output Current (Short Circuit)	I_{out}	50	mAdc

* (V_{ss} - V_{BB} > 4.5 V)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS ARE EXCEEDED. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability. V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

AC OPERATING CONDITIONS AND CHARACTERISTICS
(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.) Notes 1, 5, 12, 18

Parameter	Symbol	MCM4027AC1		MCM4027AC2		MCM4027AC3		MCM4027AC4		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	320		320		375		375		ns	13
Read Write Cycle Time	t_{RWC}	320		320		375		375		ns	13
Page Mode Cycle Time	t_{PC}	160		170		225		285		ns	13
Access Time From Row Address Strobe	t_{RAC}		120		150		200		250	ns	14, 16
Access Time From Column Address Strobe	t_{CAC}		80		100		135		165	ns	15, 16
Output Buffer and Turn-Off Delay	t_{OFF}		35		40		50		60	ns	
Row Address Strobe Precharge Time	t_{RP}	100		100		120		120		ns	
Row Address Strobe Pulse Width	t_{RAS}	120	10,000	150	10,000	200	10,000	250	10,000	ns	
Row Address Strobe Hold Time	t_{RSH}	80		100		135		165		ns	
Column Address Strobe Pulse Width	t_{CAS}	80		100		135		165		ns	
Column Address Strobe Hold Time	t_{CSH}	120		150		200		250		ns	
Row to Column Strobe Lead Time	t_{RCD}	15	40	20	50	25	65	35	85	ns	17
Row Address Setup Time	t_{ASR}	0		0		0		0		ns	
Row Address Hold Time	t_{RAH}	15		20		25		35		ns	
Column Address Setup Time	t_{ASC}	-5		-10		-10		-10		ns	
Column Address Hold Time	t_{CAH}	40		45		55		75		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	80		95		120		160		ns	
Chip Select Setup Time	t_{CSC}	0		-10		-10		-10		ns	
Chip Select Hold Time	t_{CH}	40		45		55		75		ns	
Chip Select Hold Time Referenced to $\overline{RAS}$	t_{CHR}	80		95		120		160		ns	
Transition Time Rise and Fall	t_T	3	35	3	35	3	50	3	50	ns	18
Read Command Setup Time	t_{RCS}	0		0		0		0		ns	
Read Command Hold Time	t_{RCH}	0		0		0		0		ns	
Write Command Hold Time	t_{WCH}	40		45		55		75		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	80		95		120		160		ns	
Write Command Pulse Width	t_{WP}	40		45		55		75		ns	
Write Command to Row Strobe Lead Time	t_{RWL}	50		50		70		85		ns	
Write Command to Column Strobe Lead Time	t_{CWL}	50		50		70		85		ns	
Data in Setup Time	t_{DS}	0		0		0		0		ns	19
Data in Hold Time	t_{DH}	40		45		55		75		ns	19
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	80		95		120		160		ns	
Column to Row Strobe Precharge Time	t_{CRP}	0		0		0		0		ns	
Column Precharge Time	t_{CP}	60		60		80		110		ns	
Refresh Period	t_{RFSH}		2		2		2		2	ms	
Write Command Setup Time	t_{WCS}	0		0		0		0		ns	
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	60		60		80		90		ns	20
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	100		110		145		175		ns	20
Data Out Hold Time	t_{DOH}	10		10		10		10		μs	

NOTES 12 through 20:

12. AC measurements assume t_T = 5 ns.

13. The specifications for t_{RC}(min) and t_{RWC}(min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.

14. Assumes that $t_{RCD} \leq t_{RCD}$(max).

15. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

16. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

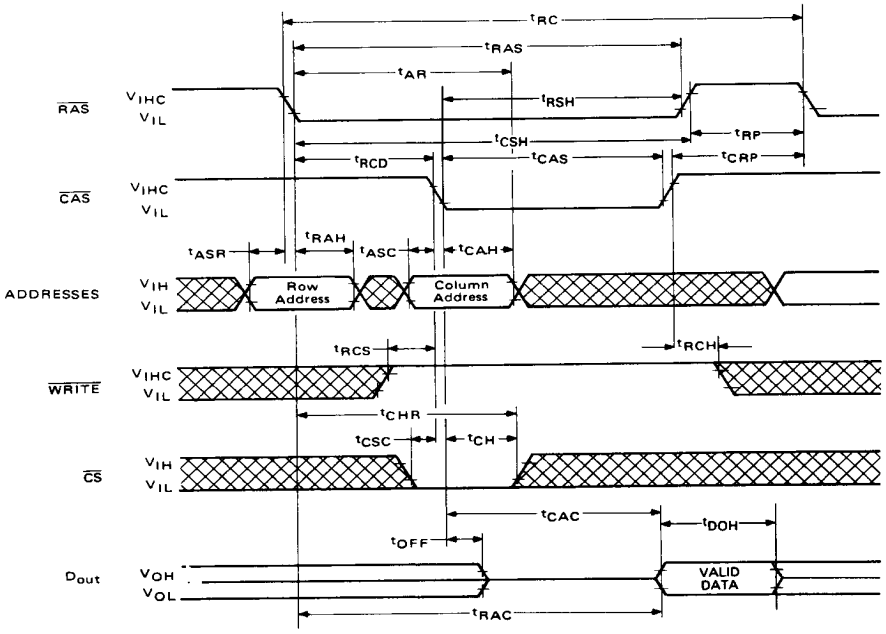
17. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

18. V_{IHC}(min) or V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

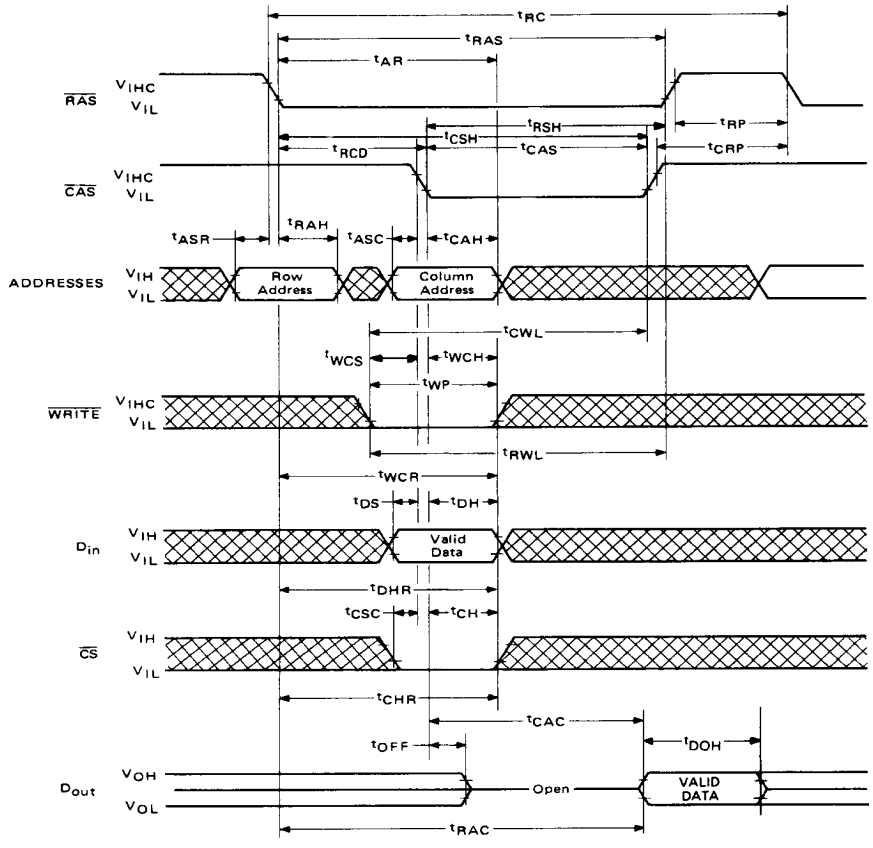
19. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify write cycles.

20. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characterisitcs only: If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

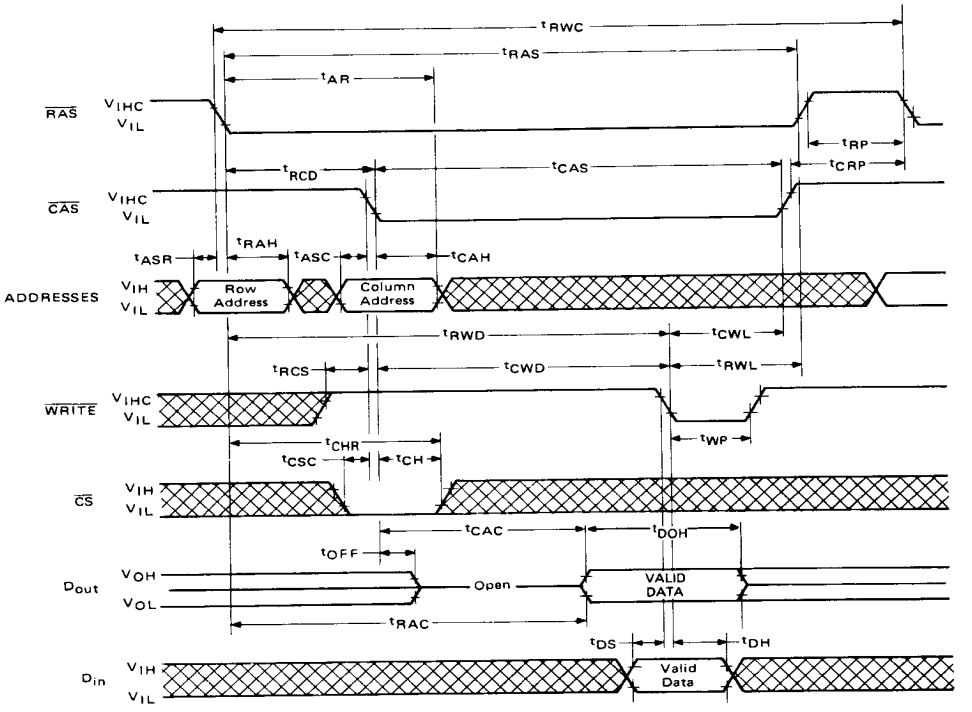
READ CYCLE TIMING



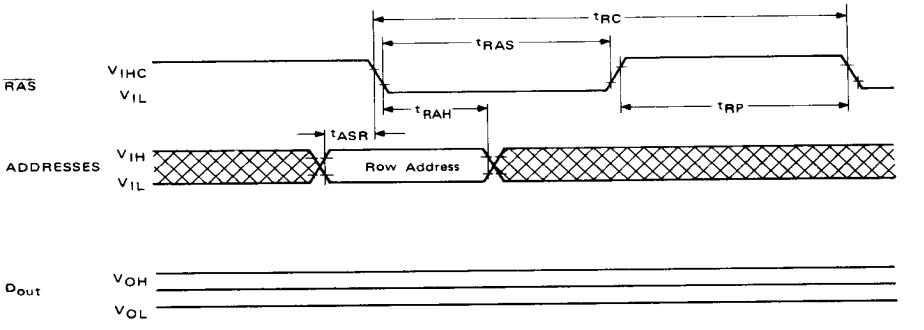
WRITE CYCLE TIMING



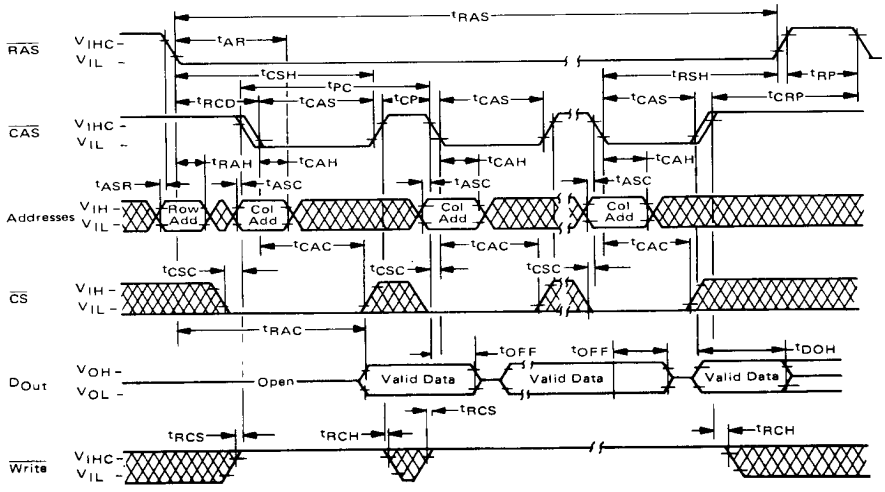
READ-MODIFY-WRITE TIMING



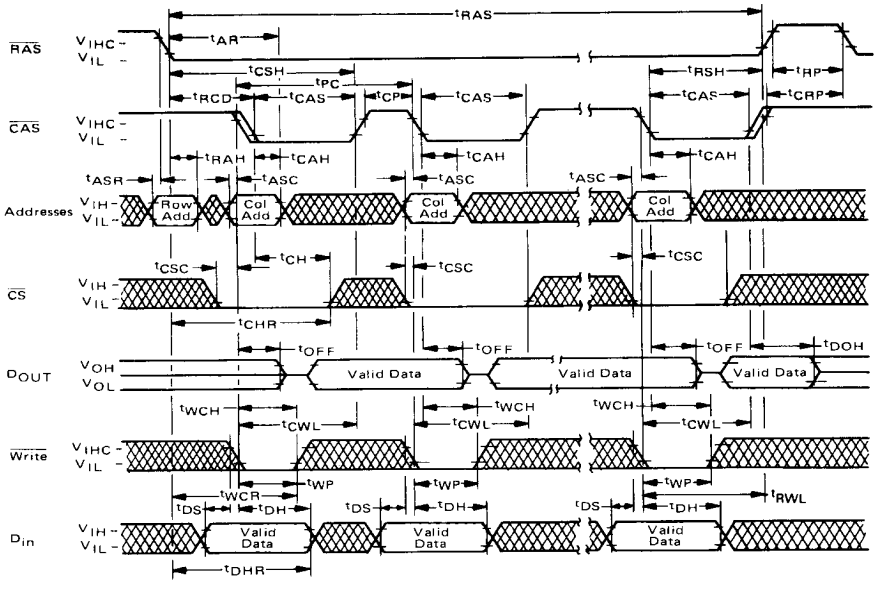
RAS ONLY REFRESH TIMING



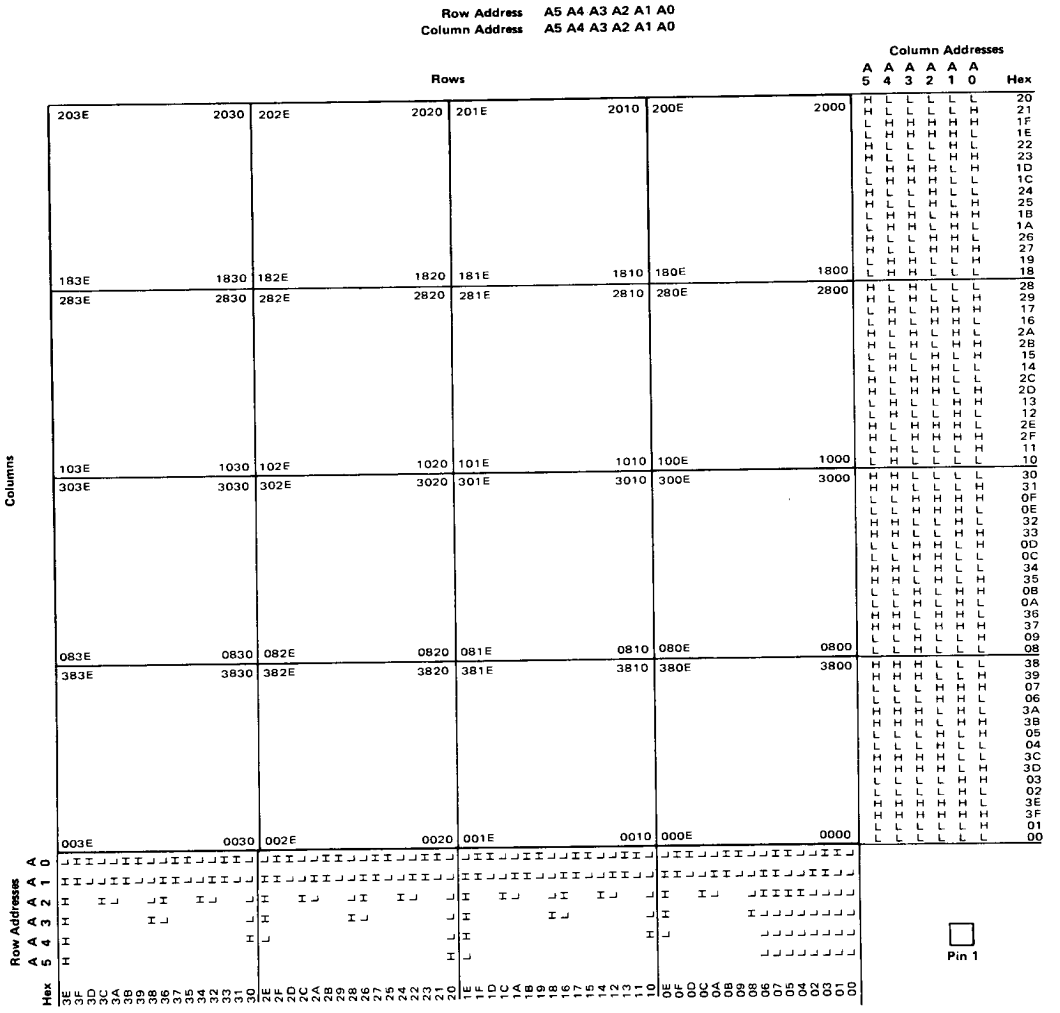
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



DRAM



MCM4027A BIT ADDRESS MAP