

High Speed PWM Controller

FEATURES

- Complementary Outputs
- Practical Operation Switching Frequencies to 1MHz
- 50ns Propagation Delay to Output
- High Current Dual Totem Pole Outputs (1.5A Peak)
- Wide Bandwidth Error Amplifier
- Fully Latched Logic with Double Pulse Suppression
- Pulse-by-Pulse Current Limiting
- Soft Start / Max. Duty Cycle Control
- Under-Voltage Lockout with Hysteresis
- Low Start Up Current (1.1 mA)
- Trimmed Bandgap Reference (5.1V \pm 1%)

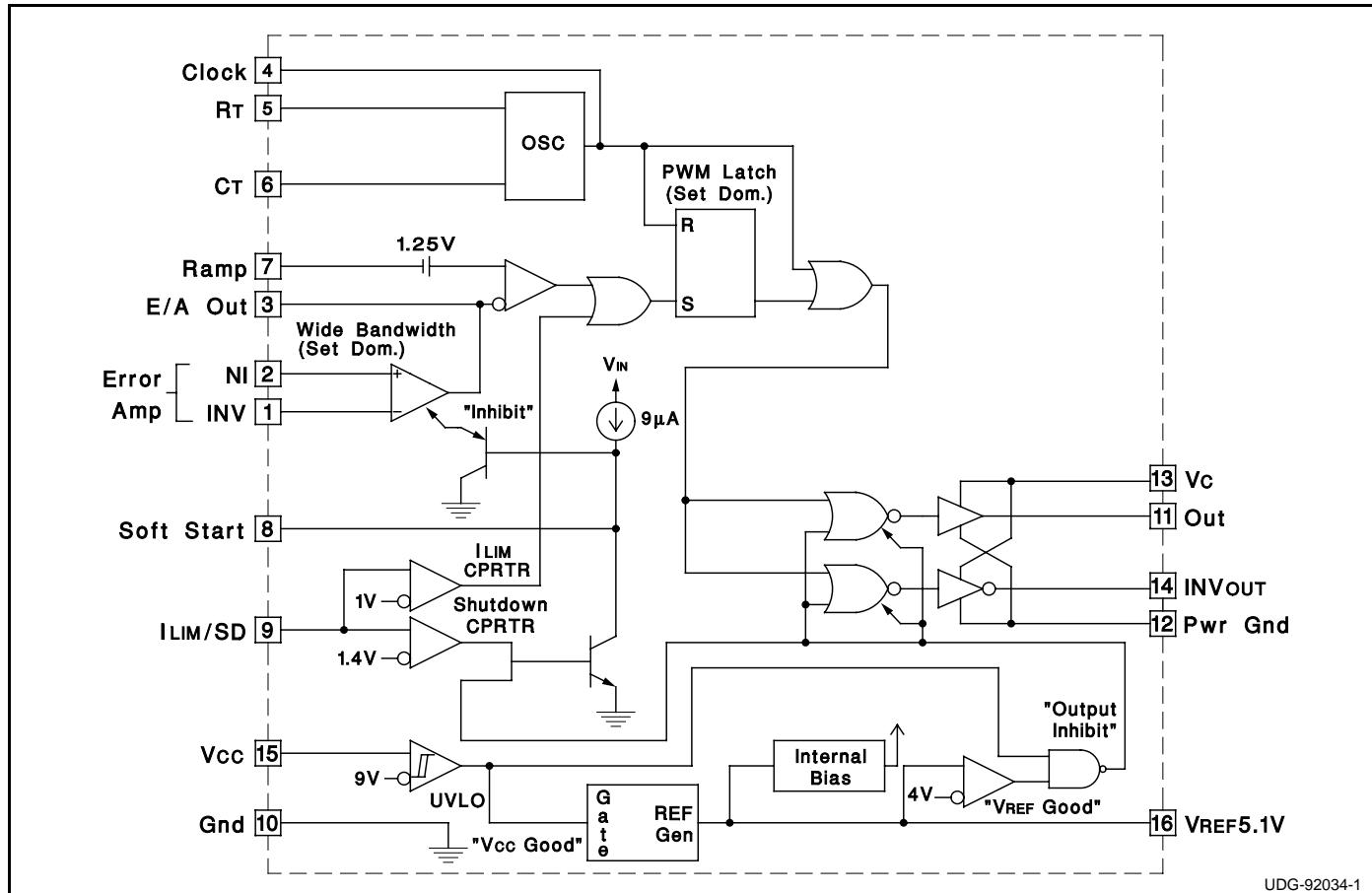
DESCRIPTION

The UC1824 family of PWM control ICs is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current-mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as a maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under-voltage lockout, the outputs are high impedance.

These devices feature totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The on state is designed as a high level.

BLOCK DIAGRAM

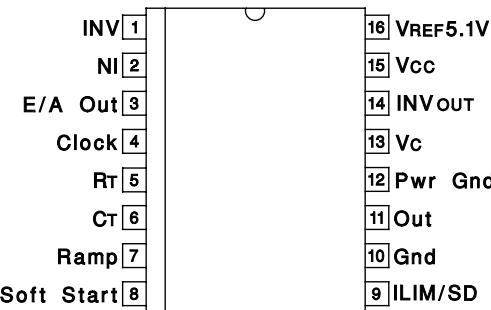
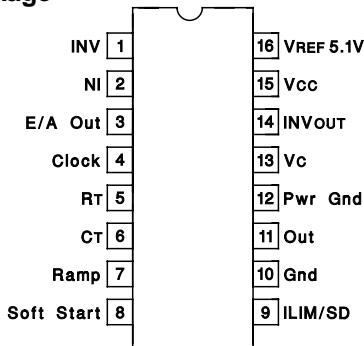
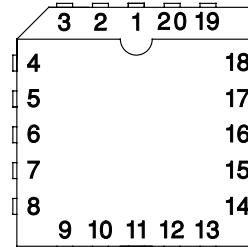


ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Pins 13, 15)	30V
Output Current, Source or Sink (Pins 11, 14)	
DC.....	0.5A
Pulse (0.5μs)	2.0A
Analog Inputs (Pins 1, 2, 7)	-0.3V to 7V
(Pin 8, 9)	-0.3V to 6V
Clock Output Current (Pin 4)	-5mA
Error Amplifier Output Current (Pin 3)	5mA
Soft Start Sink Current (Pin 8)	20mA
Oscillator Charging Current (Pin 5)	-5mA
Power Dissipation	1W
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note 1: All voltages are with respect to GND (Pin 10); all currents are positive into, negative out of part; pin numbers refer to DIL-16 package.

Note 3: Consult Unitrode Integrated Circuit Databook for thermal limitations and considerations of package.

SOIC-16 (Top View)
DW Package**CONNECTION DIAGRAMS****DIL-16 (Top View)**
J Or N Package**PLCC-20 & LCC-20**
(Top View)
Q & L Packages

PACKAGE PIN FUNCTION	
FUNCTION	PIN
N/C	1
INV	2
NI	3
E/A Out	4
Clock	5
N/C	6
RT	7
CT	8
Ramp	9
Soft Start	10
N/C	11
ILIM/SD	12
Gnd	13
Out	14
Pwr Gnd	15
N/C	16
Vc	17
INVOUT	18
Vcc	19
VREF 5.1V	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for , RT = 3.65k, CT = 1nF, VCC = 15V, -55°C<TA<125°C for the UC1824, -40°C<TA<85°C for the UC2824, and 0°C<TA<70°C for the UC3824, TA=TJ.

PARAMETERS	TEST CONDITIONS	UC1824			UC3824			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section								
Output Voltage	TJ = 25°C, IO = 1mA	5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	10V < Vcc < 30V		2	20		2	20	mV
Load Regulation	1mA < IO < 10mA		5	20		5	20	mV
Temperature Stability*	TMIN < TA < TMAX		0.2	0.4		0.2	0.4	mV/°C
Total Output Variation*	Line, Load, Temperature	5.00		5.20	4.95		5.25	V
Output Noise Voltage*	10Hz < f < 10kHz		50			50		μV
Long Term Stability*	TJ = 125°C, 1000hrs.		5	25		5	25	mV
Short Circuit Current	VREF = 0V	-15	-50	-100	-15	-50	-100	mA
Oscillator Section								
Initial Accuracy*	TJ = 25°C	360	400	440	360	400	440	kHz
Voltage Stability*	10V < Vcc < 30V		0.2	2		0.2	2	%
Temperature Stability*	TMIN < TA < TMAX		5			5		%
Total Variation*	Line, Temperature	340		460	340		460	kHz

**ELECTRICAL CHARACTERISTICS
(cont.)**

Unless otherwise stated, these specifications apply for , $R_T = 3.65k$, $C_T = 1nF$, $V_{CC} = 15V$, $-55^{\circ}C < T_A < 125^{\circ}C$ for the UC1824, $-40^{\circ}C < T_A < 85^{\circ}C$ for the UC2824, and $0^{\circ}C < T_A < 70^{\circ}C$ for the UC3824, $T_A = T_J$.

PARAMETERS	TEST CONDITIONS	UC1824			UC3824			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
Oscillator Section (cont.)									
Clock Out High		3.9	4.5		3.9	4.5		V	
Clock Out Low			2.3	2.9		2.3	2.9	V	
Ramp Peak*		2.6	2.8	3.0	2.6	2.8	3.0	V	
Ramp Valley*		0.7	1.0	1.25	0.7	1.0	1.25	V	
Ramp Valley to Peak*		1.6	1.8	2.0	1.6	1.8	2.0	V	
Error Amplifier Section									
Input Offset Voltage				10			15	mV	
Input Bias Current			0.6	3		0.6	3	μA	
Input Offset Current			0.1	1		0.1	1	μA	
Open Loop Gain	$1V < V_O < 4V$	60	95		60	95		dB	
CMRR	$1.5V < V_{CM} < 5.5V$	75	95		75	95		dB	
PSRR	$10V < V_{CC} < 30V$	85	110		85	110		dB	
Output Sink Current	$V_{PIN\ 3} = 1V$	1	2.5		1	2.5		mA	
Output Source Current	$V_{PIN\ 3} = 4V$	-0.5	-1.3		-0.5	-1.3		mA	
Output High Voltage	$I_{PIN\ 3} = -0.5mA$	4.0	4.7	5.0	4.0	4.7	5.0	V	
Output Low Voltage	$I_{PIN\ 3} = 1mA$	0	0.5	1.0	0	0.5	1.0	V	
Unity Gain Bandwidth*		3	5.5		3	5.5		MHz	
Slew Rate*		6	12		6	12		V/ μs	
PWM Comparator Section									
Pin 7 Bias Current	$V_{PIN\ 7} = 0V$			-1	-5		-1	μA	
Duty Cycle Range		0		80	0		85	%	
Pin 3 Zero DC Threshold	$V_{PIN\ 7} = 0V$	1.1	1.25		1.1	1.25		V	
Delay to Output*			50	80		50	80	ns	
Soft-Start Section									
Charge Current	$V_{PIN\ 8} = 0.5V$	3	9	20	3	9	20	μA	
Discharge Current	$V_{PIN\ 8} = 1V$	1			1			mA	
Current Limit / Shutdown Section									
Pin 9 Bias Current	$0 < V_{PIN\ 9} < 4V$			15			10	μA	
Current Limit Threshold		0.9	1.0	1.1	0.9	1.0	1.1	V	
Shutdown Threshold		1.25	1.40	1.55	1.25	1.40	1.55	V	
Delay to Output			50	80		50	80	ns	
Output Section									
Output Low Level	$I_{OUT} = 20mA$			0.25	0.40		0.25	0.40	V
	$I_{OUT} = 200mA$			1.2	2.2		1.2	2.2	V
Output High Level	$I_{OUT} = -20mA$	13.0	13.5		13.0	13.5			V
	$I_{OUT} = -200mA$	12.0	13.0		12.0	13.0			V
Collector Leakage	$V_C = 30V$		100	500		10	500	μA	
Rise/Fall Time*	$CL = 1nF$		30	60		30	60	ns	
Under-Voltage Lockout Section									
Start Threshold		8.8	9.2	9.6	8.8	9.2	9.6	V	
UVLO Hysteresis		0.4	0.8	1.2	0.4	0.8	1.2	V	
Supply Current Section									
Start Up Current	$V_{CC} = 8V$		1.1	2.5		1.1	2.5	mA	
ICC	$V_{PIN\ 1}, V_{PIN\ 7}, V_{PIN\ 9} = 0V; V_{PIN\ 2} = 1V$		22	33		22	33	mA	

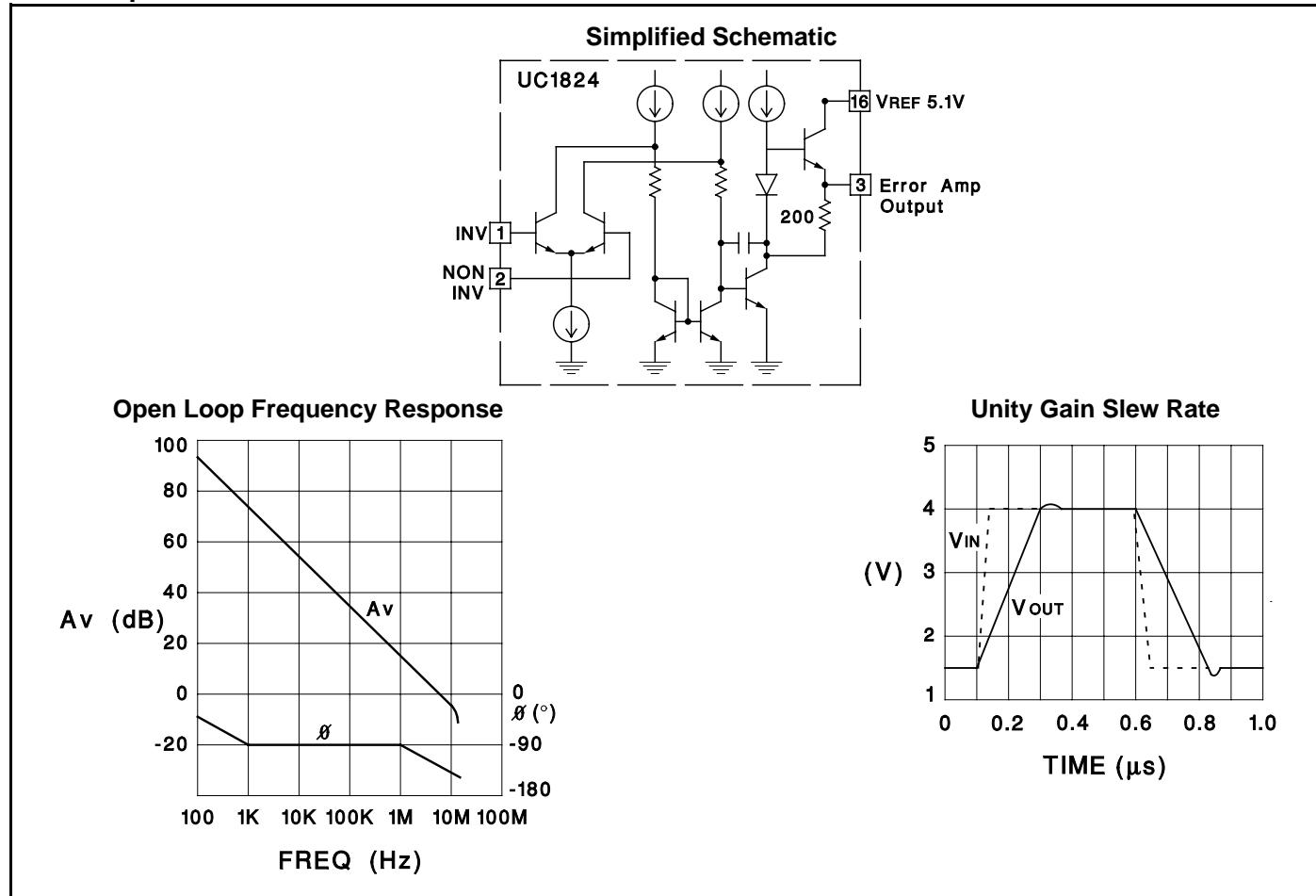
* This parameter not 100% tested in production but guaranteed by design.

UC1824 Printed Circuit Board Layout Considerations

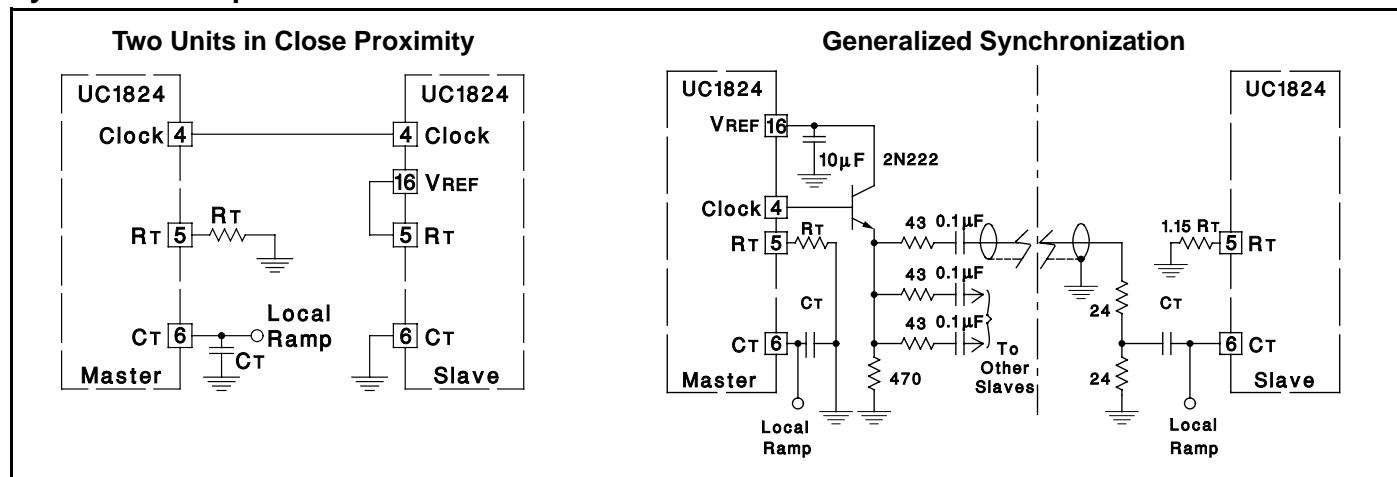
High speed circuits demand careful attention to layout and component placement. To assure proper performance of the UC1824 follow these rules: 1) Use a ground plane. 2) Damp or clamp parasitic inductive kick energy from the gate of driven MOSFETs. Do not allow the output pins to ring below ground. A series gate resistor or a shunt 1 Amp Schottky diode at the output pin will serve this purpose. 3)

Bypass VCC, VC, and VREF. Use 0.1 μ F monolithic ceramic capacitors with low equivalent series inductance. Allow less than 1 cm of total lead length for each capacitor between the bypassed pin and the ground plane. 4) Treat the timing capacitor, CT, like a bypass capacitor.

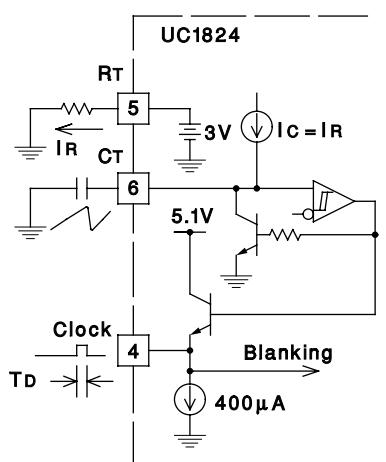
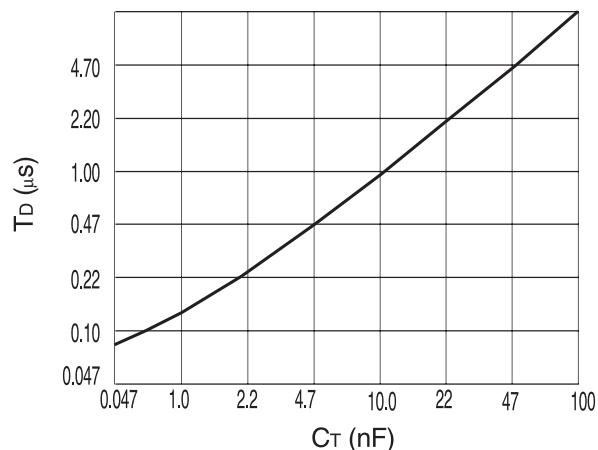
Error Amplifier Circuit



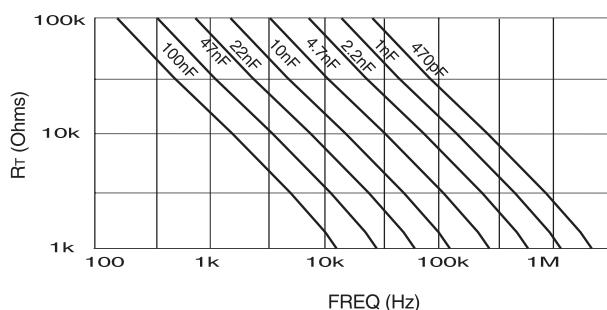
Synchronized Operation



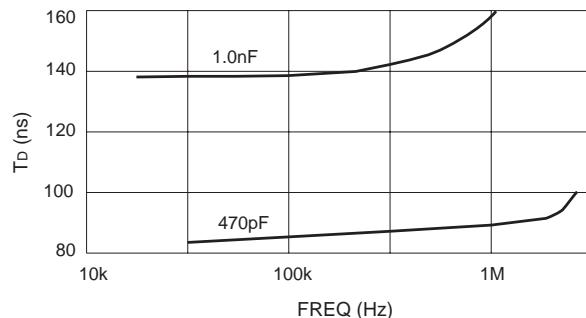
Oscillator Circuit

Primary Output Deadtime vs C_T ($3k \leq R_T \leq 100k$)

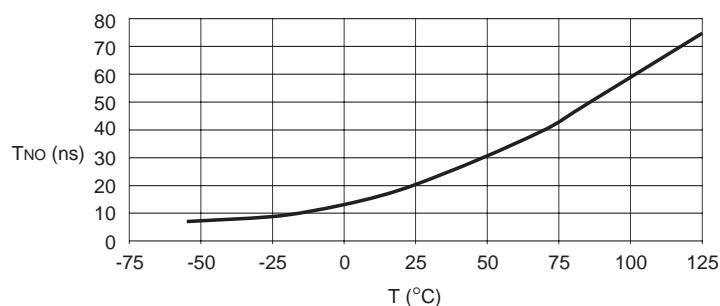
Timing Resistance vs Frequency



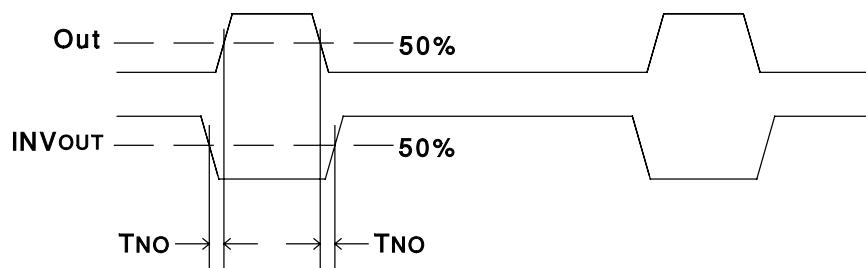
Primary Output Deadtime vs Frequency



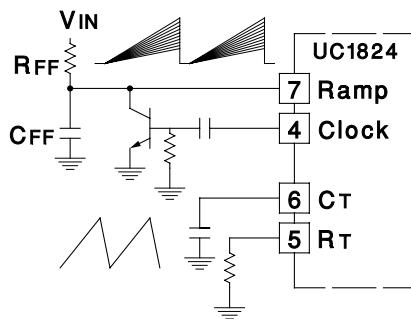
Typical Non-Overlap Time (TNO) Over Temperature



Non-Overlap Time (TNO)

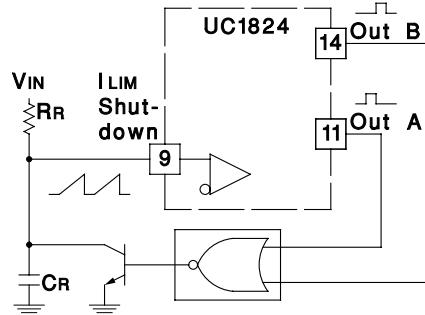


Forward Technique for Off-Line Voltage Mode Application

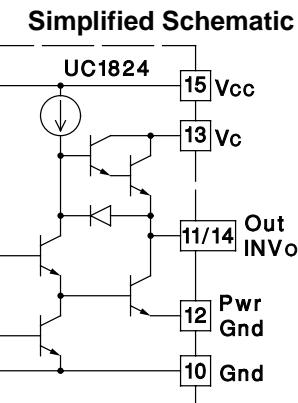


Constant Volt-Second Clamp Circuit

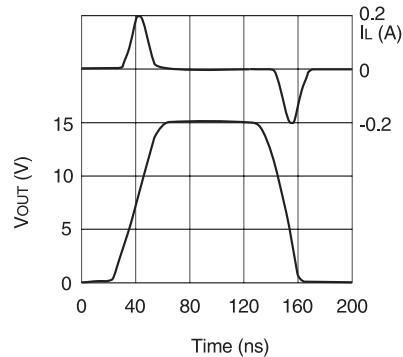
The circuit shown here will achieve a constant volt-second product clamp over varying input voltages. The ramp generator components, R_T and C_R are chosen so that the ramp at Pin 9 crosses the 1V threshold at the same time the desired maximum volt-second product is reached. The delay through the functional nor block must be such that the ramp capacitor can be completely discharged during the minimum deadtime.



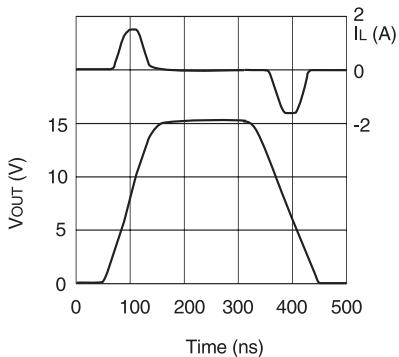
Output Section



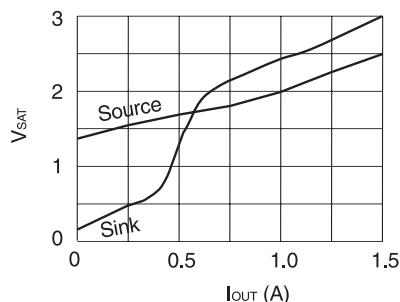
Rise/Fall Time ($C_L=1nF$)



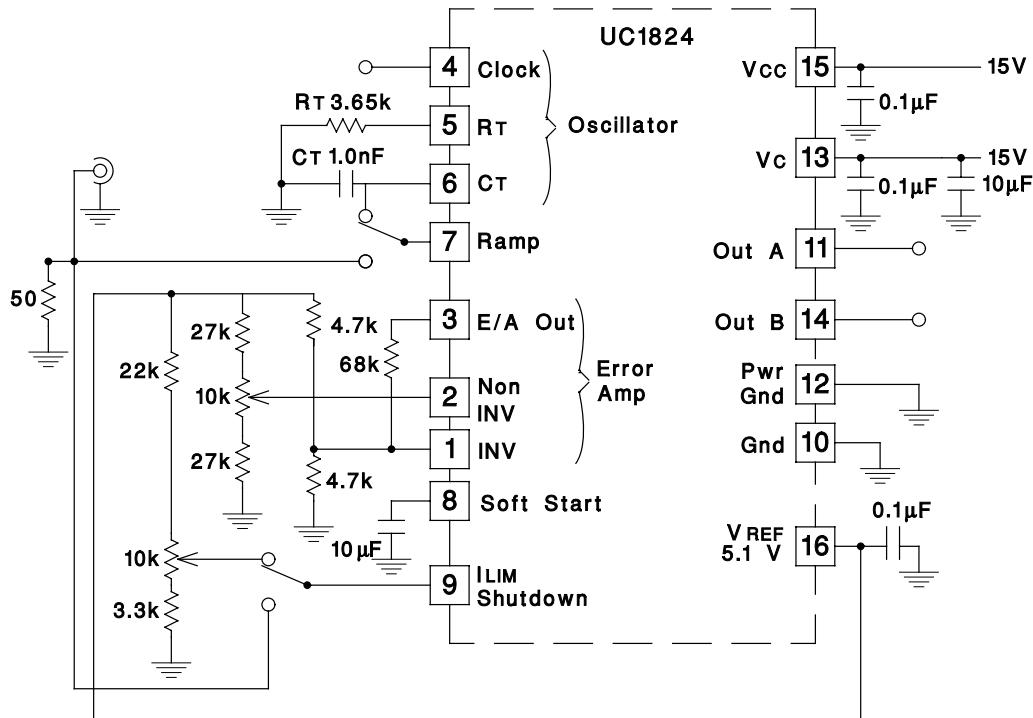
Rise/Fall Time ($C_L=10nF$)



Saturation Curves



Open Loop Laboratory Test Fixture



UDG-92036-2

This test fixture is useful for exercising many of the UC1824's functions and measuring their specifications.

As with any wideband circuit, careful grounding and bypass procedures should be followed. The use of a ground plane is highly recommended.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UC2824DW	ACTIVE	SOIC	DW	16		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2824DWG4	ACTIVE	SOIC	DW	16		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2824DWTR	ACTIVE	SOIC	DW	16		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2824DWTRG4	ACTIVE	SOIC	DW	16		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2824N	ACTIVE	PDIP	N	16		Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2824Q	ACTIVE	PLCC	FN	20		Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC2824QG3	ACTIVE	PLCC	FN	20		Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR
UC3824DW	ACTIVE	SOIC	DW	16		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3824DWG4	ACTIVE	SOIC	DW	16		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3824DWTR	ACTIVE	SOIC	DW	16		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3824DWTRG4	ACTIVE	SOIC	DW	16		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3824N	ACTIVE	PDIP	N	16		Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3824NG4	ACTIVE	PDIP	N	16		Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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