



ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748-5089
<http://www.nteinc.com>

NTE4538B

Integrated Circuit

CMOS, Dual Precision Retriggerable/ Resettable Monostable Multivibrator

Description:

The NTE4538B is a dual, retriggerable, resettable, monostable multivibrator in a 16-Lead DIP type package. It may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X . Linear CMOS techniques allow more precise control of output pulse width.

Features:

- $\pm 1.0\%$ (Typ) Pulsewidth Variation from Part to Part
- $\pm 0.5\%$ (Typ) Pulsewidth Variation over Temperature Range
- New Formula: $T = RC$ (T in Seconds, R in Ohms, C in Farads)
- Pulse Width Range – $10\mu s$ to ∞
- Symmetrical Output Sink and Source Capability
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- Quiescent Current (Standby) = $5nA$ /Package (Typ) at $5V_{DC}$
- $3V_{DC}$ to $18V_{DC}$ Operational Limits
- Triggerable from Positive or Negative Going Edge
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- For Pulse Widths Less Than $10\mu s$, the NTE4525B is Recommended

Absolute Maximum Ratings: (Voltages referenced to V_{SS} , Note 1)

DC Supply Voltage, V_{DD}	–0.5 to +18.0V
Input Voltage (All Inputs), V_{in}	–0.5 to V_{DD} to +0.5V
DC Current Drain (Per Pin), I	10mA
Operating Temperature Range, T_A	–55° to +125°C
Storage Temperature Range, T_{stg}	–65° to +150°C

Note 1. This device contains circuitry to protect the input against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Electrical Characteristics: (Note 2)

Parameter	Symbol	V _{DD} Vdc	-55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
	V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level (V _O = 4.5 or 0.5Vdc) (V _O = 9.0 or 1.0Vdc) (V _O = 13.5 or 1.5Vdc)	V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
	V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current (V _{OH} = 2.5Vdc) (V _{OH} = 4.6Vdc) (V _{OH} = 9.5Vdc) (V _{OH} = 13.5Vdc) (V _{OL} = 0.4Vdc) (V _{OL} = 0.5Vdc) (V _{OL} = 1.5Vdc)	Source I _{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
			–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
	Sink I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current, Pin2 or Pin14	I _{in}	15	–	±0.02	–	±0.00001	±0.05	–	±0.5	μAdc
Input Current, Other Inputs	I _{in}	15	–	±0.1	–	±0.00001	±0.1	–	±0.1	μAdc
Input Capacitance, Pin2 or Pin14	C _{in}	–	–	–	–	25	–	–	–	pF
Input Capacitance, Other Inputs (V _{IN} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I _{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	μAdc
		15	–	15	–	0.015	15	–	600	μAdc
Quiescent Current, Active State (Q1 = Logic 1) (Q2 = Logic 0)	I _{DD}	5.0	–	5.0	–	35	–	–	150	μAdc
		10	–	10	–	80	–	–	300	μAdc
		15	–	15	–	1255	–	–	600	μAdc
Total Supply Current at an External Load Capacitance (C _L) and at External Timing Network (R _X , C _X) (Note 3)	I _T	5 10 15	$I_T = (3.5 \times 10^{-2}) R_X C_X f + 4 C_X f + 1 \times 10^{-5} C_L f$ $I_T = (8 \times 10^{-2}) R_X C_X f + 9 C_X f + 2 \times 10^{-5} C_L f$ $I_T = (1.25 \times 10^{-1}) R_X C_X f + 12 C_X f + 3 \times 10^{-5} C_L f$ where: I _T in μA (one monostable switching only). C _X in μF, C _L in pF, R _X in k ohms, and f in Hz is the input frequency.							

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. Noise immunity specified for worst-case input combination.

Noise margin for both "1" and "0" = 1.0Vdc min @ V_{DD} = 5Vdc
 2.0Vdc min @ V_{DD} = 10Vdc
 2.5Vdc min @ V_{DD} = 15Vdc

Switching Characteristics: ($C_L = 50\text{pF}$, $T_A = +25^\circ\text{C}$, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time $t_{TLH} = (1.35\text{ns/pf}) C_L + 33\text{ns}$ $t_{TLH} = (0.60\text{ns/pf}) C_L + 20\text{ns}$ $t_{TLH} = (0.40\text{ns/pf}) C_L + 20\text{ns}$	t_{TLH}	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Output Fall Time $t_{THL} = (1.35\text{ns/pf}) C_L + 33\text{ns}$ $t_{THL} = (0.60\text{ns/pf}) C_L + 20\text{ns}$ $t_{THL} = (0.40\text{ns/pf}) C_L + 20\text{ns}$	t_{THL}	5.0	–	100	200	ns
		10	–	50	100	ns
		15	–	40	80	ns
Propagation Delay Time, A or B to Q or $\overline{Q}$ $t_{PLH}, t_{PHL} = (0.90\text{ns/pF}) C_L + 255\text{ns}$ $t_{PLH}, t_{PHL} = (0.36\text{ns/pF}) C_L + 132\text{ns}$ $t_{PLH}, t_{PHL} = (0.26\text{ns/pF}) C_L + 97\text{ns}$	$t_{PLH},$ t_{PHL}	5.0	–	300	600	ns
		10	–	150	300	ns
		15	–	100	220	ns
Propagation Delay Time, C_D to Q or $\overline{Q}$ $t_{PLH}, t_{PHL} = (0.90\text{ns/pF}) C_L + 205\text{ns}$ $t_{PLH}, t_{PHL} = (0.36\text{ns/pF}) C_L + 107\text{ns}$ $t_{PLH}, t_{PHL} = (0.26\text{ns/pF}) C_L + 82\text{ns}$	$t_{PLH},$ t_{PHL}	5.0	–	250	500	ns
		10	–	125	250	ns
		15	–	95	190	ns
Minimum Input Pulse Width, A, B or C_D	$t_{WH},$ t_{WL}	5.0	–	35	70	ns
		10	–	30	60	ns
		15	–	25	50	ns
Minimum Retrigger Time	t_{rr}	5.0	0	–	–	ns
		10	0	–	–	ns
		15	0	–	–	ns
Output Pulse Width – Q or $\overline{Q}$ $C_X = 0.002\mu\text{F}$, $R_X = 10\text{k}\Omega$ $C_X = 0.1\mu\text{F}$, $R_X = 100\text{k}\Omega$ $C_X = 10\mu\text{F}$, $R_X = 100\text{k}\Omega$	T	5.0	210	222	234	μs
		10	212	224	236	μs
		15	214	226	238	μs
		5.0	9.3	9.86	10.4	ms
		10	9.5	10.0	10.5	ms
		15	9.6	10.14	10.7	ms
		5.0	0.915	0.965	1.015	s
		10	0.93	0.98	1.03	s
		15	0.94	0.99	1.04	s
Pulse Width Match Between Circuits in the Same Package $C_X = 0.1\mu\text{F}$, $R_X = 100\text{k}\Omega$		5.0	–	± 1	–	%
		10	–	± 1	–	%
		15	–	± 1	–	%

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at $+25^\circ\text{C}$.

Operating Conditions:

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
External Timing Resistance	R_X	–	5.0	–	Note 4	k Ω
External Timing Capacitance	C_X	–	0	–	No Limit	pF

Note 4. The maximum usable resistance R_X is a function of the leakage of the capacitor C_X , leakage of the NTE4538B, and leakage due to board layout and surface resistance.

