

POWER MANAGEMENT**Description**

The SC1211VX is a high speed, Combi-Sense™, dual output driver designed to drive high-side and low-side MOSFETs in a synchronous Buck converter. These drivers combined with Combi-Sense PWM controllers, such as Semtech SC2643VX or SC2643, provide a cost effective multi-phase voltage regulator for advanced microprocessors

The Combi-Sense™ is a technique to sense the inductor current for peak current mode control of voltage regulator without using sensing resistor. It provides the following advantages:

- No costly precision sensing resistor
- Lossless current sensing
- High level noise free signal
- Fast response
- Suitable for wide range of duty cycle
- Only two small signal components (third optional)

The detailed explanation of the technique can be found in the Applications Information section.

A 30ns max propagation delay from input transition to the gate of the power FET's guarantees operation at high switching frequencies. Internal overlap protection circuit prevents shoot-through from Vin to PGND in the main and synchronous MOSFETs. The adaptive overlap protection circuit ensures the bottom FET does not turn on until the top FET source has reached 1V, to prevent cross-conduction.

8.5V gate drive provides optimum enhancement of MOSFETs at minimum driver and MOSFET switching loss. High current drive capability allows fast switching, thus reducing switching losses at high (up to 1.5MHz) frequencies without causing thermal stress on the driver.

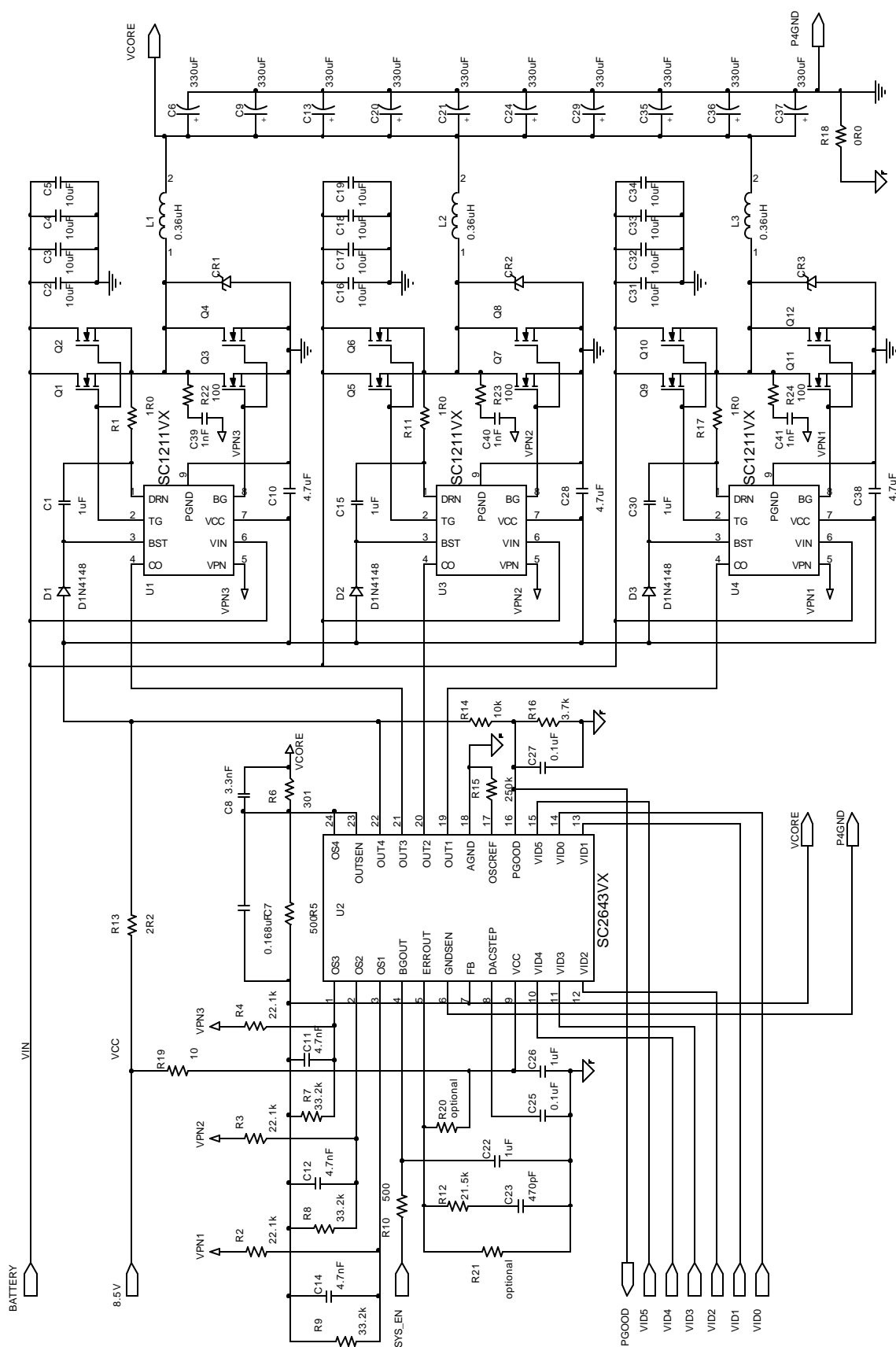
Under-voltage-lockout and over-temperature shutdown features are included for proper and safe operation. Timed latches and improved robustness are built into the housekeeping functions such as the Under Voltage Lockout and adaptive Shoot-through protection circuitry to prevent false triggering and to assure safe operation. The SC1211VX is offered in a Power SOIC-8L package.

Features

- ◆ High efficiency
- ◆ +8.5V optimum gate drive voltage
- ◆ High peak drive current
- ◆ Adaptive non-overlapping gate drives provide shoot-through protection
- ◆ Support Combi-Sense™ and VID-on-fly operations
- ◆ Fast rise and fall times (15ns typical with 3000pf load)
- ◆ Ultra-low (<30ns) propagation delay (BG going low)
- ◆ Floating top gate drive
- ◆ Crowbar function for over voltage protection
- ◆ High frequency (to 1.5 MHz) operation allows use of small inductors and low cost ceramic capacitors
- ◆ Under-voltage-lockout
- ◆ Low quiescent current

Applications

- ◆ Intel Pentium™ processor power supplies
- ◆ AMD Athlon™ and K8™ processor power supplies
- ◆ High efficiency portable and notebook computers
- ◆ Battery powered applications
- ◆ High current low voltage DC-DC converters

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Typical Application Circuit


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Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Conditions	Maximum	Units
V _{CC} Supply Voltage	V _{CC}		11	V
VIN to PGND	V _{IN}		30	V
BST to DRN	V _{BST-DRN}		11	V
BST to PGND	V _{BST-PGND}		40	V
BST to PGND Pulse	V _{BST_PULSE}	t _{PULSE} < 100ns	45	V
DRN to PGND	V _{DRN-PGND}		-2 to 30	V
DRN to PGND Pulse	V _{DRN_PULSE}	t _{PULSE} < 200ns	-5 to 35	V
VPN to PGND	V _{PN}		30	V
PWM Input	CO		-0.3 to 8.5	V
Continuous Power Dissipation	P _D	T _A = 25°C, T _J = 125°C	2.56	W
Thermal Resistance Junction to Case	θ _{JC}		8	°C/W
Operating Junction Temperature Range	T _J		0 to +125	°C
Storage Temperature Range	T _{STG}		-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T _{LEAD}		300	°C

Electrical Characteristics

Unless specified: T_A = 25°C; V_{CC} = 8.5V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V _{CC}		4.2	8.5	9.0	V
Quiescent Current, Operating	I _{q_op}			3.0		mA
Under Voltage Lockout						
Start Threshold	V _{CC_START}			4	4.3	V
Hysteresis	V _{hys_UVLO}			160		mV

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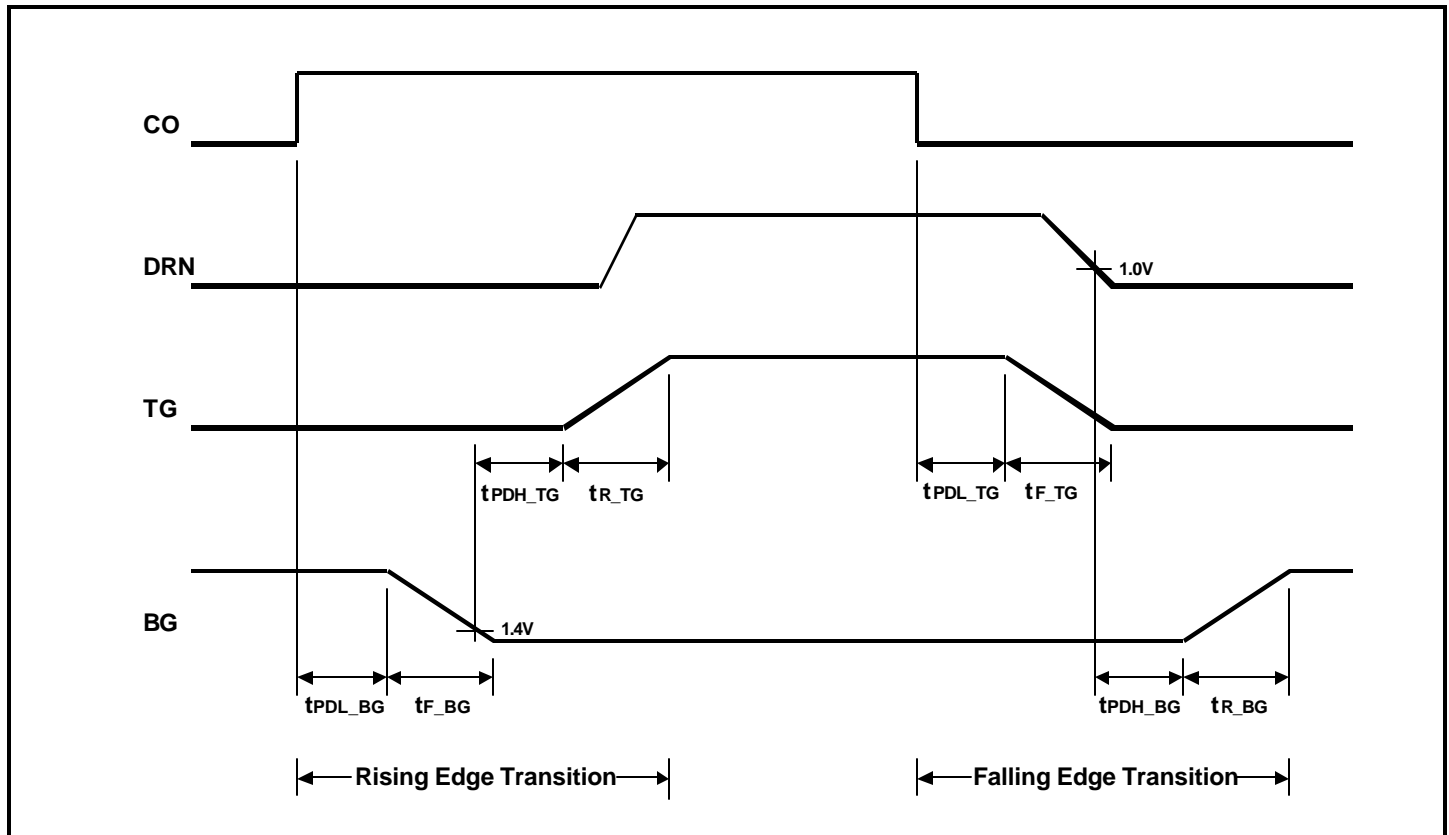
Electrical Characteristics (Cont.)

Unless specified: $T_A = 25^{\circ}\text{C}$; $V_{CC} = 8.5\text{V}$

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CO						
Logic High Input Voltage	V_{CO_H}		2.0			V
Logic Low Input Voltage	V_{CO_L}				0.8	V
Thermal Shutdown						
Over Temperature Trip Point	T_{OTP}			155		$^{\circ}\text{C}$
Hysteresis	T_{HYST}			10		$^{\circ}\text{C}$
High Side Driver (TG)						
Output Impedance	R_{SRC_TG}	$V_{BST} - V_{DRN} = 8.5\text{V}$		1.5	3.0	Ω
	R_{SINK_TG}			1.0	2.0	
Rise Time	t_{R_TG}	$CL = 3\text{nF}$, $V_{BST} - V_{DRN} = 8.5\text{V}$		15		ns
Fall Time	t_{F_TG}	$CL = 3\text{nF}$, $V_{BST} - V_{DRN} = 8.5\text{V}$		10		ns
Propagation Delay, TG Going High	t_{PDH_TG}	$V_{BST} - V_{DRN} = 8.5\text{V}$		37		ns
Propagation Delay, TG Going Low	t_{PDL_TG}	$V_{BST} - V_{DRN} = 8.5\text{V}$		30		ns
Low-Side Driver (BG)						
Output Resistance	R_{SRC_BG}	$V_{BST} - V_{DRN} = 8.5\text{V}$		1.5	3.0	Ω
	R_{SINK_BG}			1.5	3.0	
Rise Time	t_{R_BG}	$CL = 3\text{nF}$, $V_{BST} - V_{DRN} = 8.5\text{V}$		10		ns
Fall Time	t_{F_BG}	$CL = 3\text{nF}$, $V_{BST} - V_{DRN} = 8.5\text{V}$		10		ns
Propagation Delay, BG Going High	t_{PDH_BG}	$V_{BST} - V_{DRN} = 8.5\text{V}$		20		ns
Propagation Delay, BG Going Low	t_{PDL_BG}	$V_{BST} - V_{DRN} = 8.5\text{V}$		27		ns
Under-Voltage-Lockout Time Delay						
V_{CC} ramping up	t_{PDH_UVLO}			2		μs
V_{CC} ramping down	t_{PDL_UVLO}			2		μs

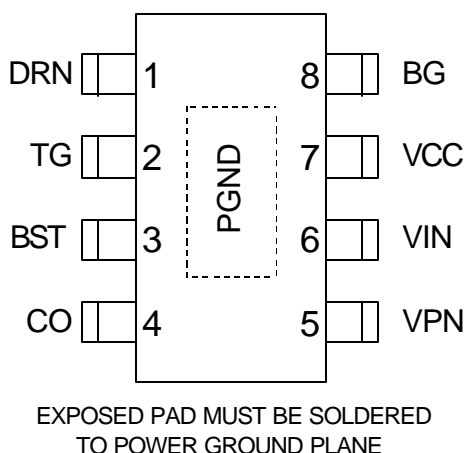
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Timing Diagrams



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Pin Configuration



Ordering Information

Device ⁽¹⁾	Package	Temp Range (T _J)
SC1211VXSTR	EDP SO-8	0° to 125°C

Note:

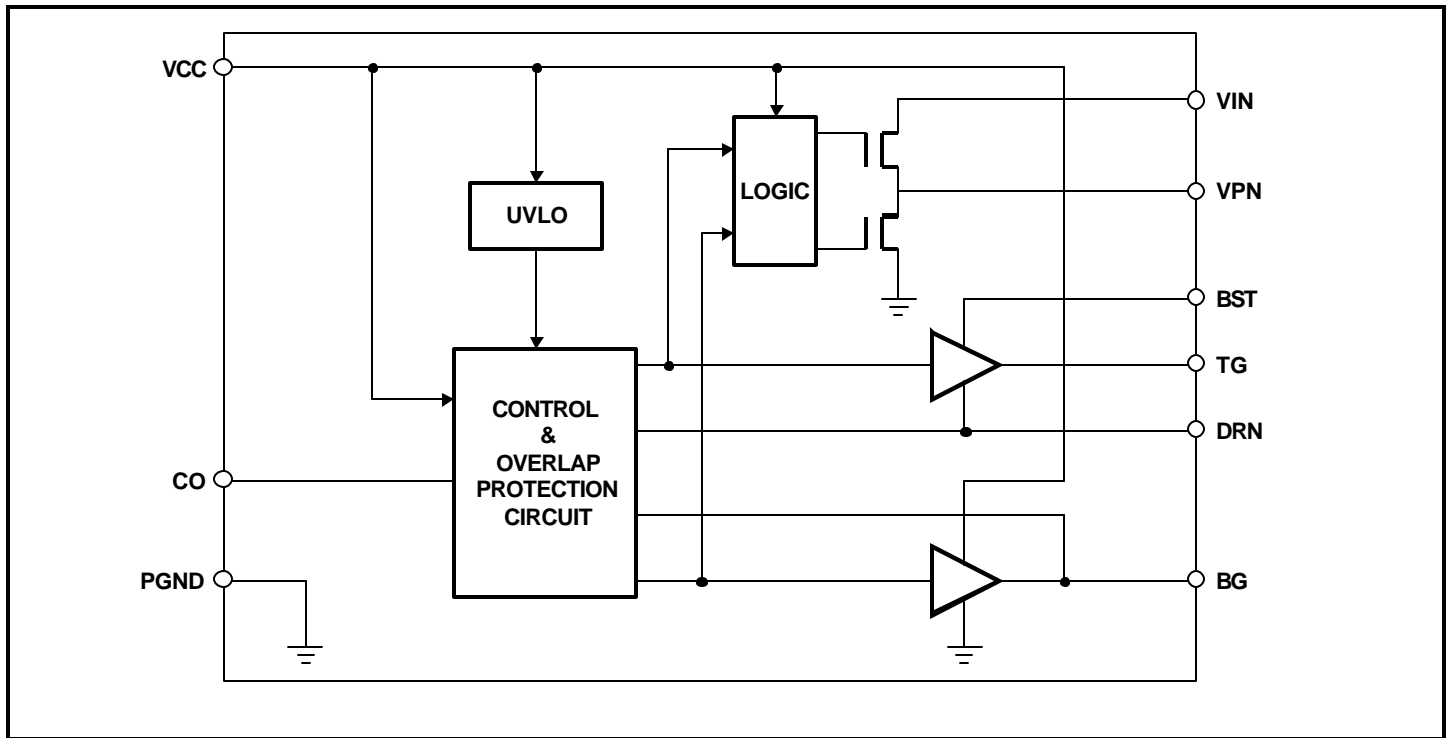
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	DRN	The power phase node (or switching node) of the synchronous Buck converter. This pin can be subjected to a negative spike up to -V _{cc} relative to PGND without affecting operation.
2	TG	Output gate drive for the switching (top) MOSFET.
3	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically 1μF (ceramic).
4	CO	Logic level PWM input signal to the SC1211VX supplied by external controller. An internal 50kohm resistor is connected from this pin to PGND.
5	VPN	Virtual Phase Node. Connect an RC between this pin and the output sense point of the converter to enable Combi-Sense™ operation. See the Typical Application Circuit.
6	VIN	Sensing input for internal Combi-Sense™ circuitry. Connect as close as possible to the Drain of the top MOSFET.
7	VCC	Supply power for the SC1211VX. Connect to 8.5V supply for optimum operation. A 1.0uF-4.7uF Capacitor must be connected from this pin to PGND as close as possible.
8	BG	Output gate drive for the synchronous (bottom) MOSFET.
PAD	PGND	Ground. Keep this pin close to the synchronous MOSFET source.

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Block Diagram



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Applications Information

THEORY OF OPERATION

The SC1211VX is a high speed, Combi-Sense™, dual output driver designed to drive top and bottom MOSFETs in a synchronous Buck converter. It features adaptive delay for shoot-through protection and VID-on-Fly operation; 8.5V optimum gate drive voltage; and Virtual Phase Node for Combi-Sense™ solution. These drivers combined with PWM controller SC2643VX form a multi-phase voltage regulator for advanced microprocessors. A three-phase voltage regulator with 19V input 60A output is shown in the Typical Application Circuit section.

Startup and UVLO

To startup the driver, a supply voltage applied to VCC pin of the SC1211VX. The top and bottom gates are held low until VCC exceeds UVLO threshold of the driver, typically 4.2V. Then the top gate remains low and the bottom gate is pulled high to turn on the bottom FET. Once VIN exceeds UVLO threshold of the PWM controller, typically 7.5V, the soft-start begins and the PWM signal takes fully control of the gate transitions.

Gate Transition and Shoot through Protection

Refer to the Timing Diagrams section, the rising edge of the PWM input initiates the bottom FET turn-off and the top FET turn-on. After a short propagation delay (t_{PDL_BG}), the bottom gate begins to fall (t_{F_BG}). An adaptive circuit in the SC1211VX monitors the bottom gate voltage to drop below 1.4V. Then after a preset delay time (t_{PDH_TG}) is expired, the top gate turns on. The delay time is set to be 20ns typically. This prevents the top FET from turning on until the bottom FET is off. During the transition, the inductor current is freewheeling through the body diode of either bottom FET or top FET, upon the direction of the inductor current. The phase node could be low (ground) or high (VIN).

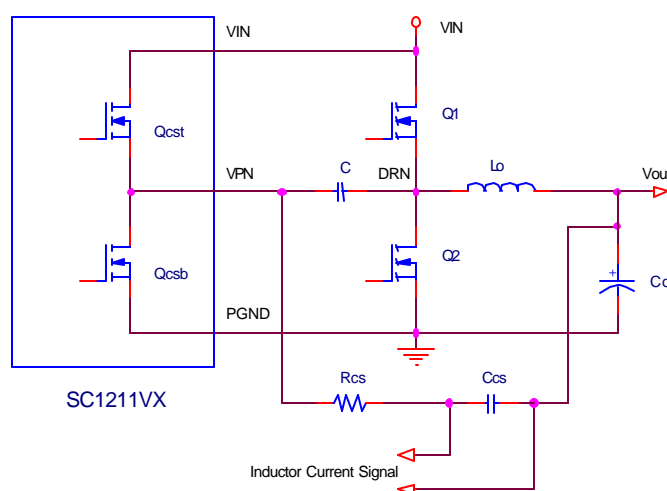
The falling edge of the PWM input controls the top FET turn-off and the bottom FET turn-on. After a short propagation delay (t_{PDL_TG}), the top gate begins to fall (t_{F_TG}). As the inductor current is commutated from the top FET to the body diode of the bottom FET, the phase node begins to fall. The adaptive circuit in the SC1211VX detects the phase node voltage. It holds the bottom FET off until the phase node voltage has dropped below 1.0V. This prevents the top and bottom FETs from conducting simultaneously or shoot-through.

VID-on-Fly Operation

Certain new processors have required to changing the VID dynamically during the operation, or referred as VID-on-Fly operation. A VID-on-Fly can occur under light load or heavy load conditions. At light load, it could force the converter to sink current. Upon turn-off of the top FET, the reversed inductor current has to be freewheeling through the body diode of the top FET instead of the bottom FET. As a result, the phase node voltage remains high. The SC1211VX incorporates the ability by pulling the bottom gate to high internally, which over rides the adaptive circuit and turns the bottom FET on. The delay time from the PWM falling edge to the bottom gate turn-on is set at 200ns typically.

Virtual Phase Node for Combi-Sense™

Peak-Current-Mode control is widely employed in multi-phase voltage regulators. It features phase current balance, fast transient response, and over current protection, etc. These are essential to low-voltage high-current regulators designed for advanced microprocessors. Usually, a costly current sensing resistor is required to obtain the output inductor current information for the peak current control. The Combi-Sense™ technique featured by the SC1211VX is an approach to sense inductor current without using sensing resistor.



The above circuit shows the concept of Combi-Sense™ technique. An internal totem pole (Qcst, Qcsb) generates a VPN (Virtual Phase Node) signal. This VPN follows the DRN (or the Power Phase Node) with the same timing. A RC network (Rcs and Ccs) is connected between

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Applications Information (Cont.)

VPN and Vout. During Q1 turn-on, Qcst turns on as well. The voltage drop across Q1 and Lo charges Ccs. During Q2 turn-on, Qcsb turns on as well. The voltage drop across Q2 and Lo discharges Ccs. Both voltage drops are proportional to the inductor current and a resistance equal to FET's Rdson plus ESR of the inductor. If the time constant Rcs x Ccs is close to the Lo/Ro of the inductor, where Ro is given by

$$R_o = R_{inductor} + R_{dson_hs} * D + R_{dson_ls} * (1 - D)$$

the signal developed across Ccs will be proportional to the inductor current, where Ro is the equivalent current sensing resistance. In the above equation, Rinductor is ESR of the inductor, Rdson_hs and Rdson_ls are the top and bottom FET's Rdson, and D is the duty cycle of the converter.

Since a perfect timing match down to the nanosecond is impossible, the VPN totem pole is held in tri-state during the commutations of DRN in the SC1211VX. This avoids errors and offset on the current detection which can be significant since the timing mismatch is multiplied by the input voltage. An optional capacitor between VPN and DRN allows these two nodes to be AC coupled during the tri-state window, hence yields a perfect timing match. Refer to Semtech SC2643VX Combi-Sense™ Current Mode Controller about the details of the Combi-Sense technique.

Optimized Gate Drive Voltage

The supply voltage of the SC1211VX ranges from 4.2V to 9.0V. It provides supply power for the logic circuitry, the bottom drive, and the top drive (through an external bootstrap circuit). It is recommended to select the supply voltage at 8.5V. The manufacture data and bench tested results show that, for low Rdson FETs run at applied load current, the optimum gate drive voltage is around 8.5V, where the total power losses of power FETs, including conduction loss and switching loss, are minimized.

In portable and notebook applications, the 8.5V supply voltage could be built up from a charge pump, or from a fly-back winding on a +5V out or +3.3V out switcher. The required loading capability of the 8.5V supply is less than 30mA for each SC1211VX driver, dependent on the

switching frequency and the FET's gate charge.

Thermal Shut Down

The SC1211VX will shut down by pulling both driver outputs low if its junction temperature, Tj, exceeds 155°C.

COMPONENT SELECTION

Switching Frequency, Inductor and MOSFETs

The SC1211VX is capable of providing up to 3.5A peak drive current, and operating up to 1.5MHz PWM frequency without causing thermal stress on the driver. The selection of switching frequency, together with inductor and FETs is a trade-off between the cost, size, and thermal management of a multi-phase voltage regulator. In modern microprocessor applications, these parameters could be in the range of:

Switching Frequency	100kHz to 500kHz per phase
Inductor Value	0.2uH to 2uH
FETs	4m-ohm to 20m-ohm Rdson 20nC to 100nC total gate charge

Bootstrap Circuit

The SC1211VX uses an external bootstrap circuit to provide a voltage for the top FET drive. This voltage, referring to the Phase Node, is held up by a bootstrap capacitor. The capacitor value can be calculated based on the total gate charge of the top FET, QTOP, and an allowed voltage ripple on the capacitor, ΔVBST, in one PWM cycle:

$$C_{BST} > Q_{TOP} / \Delta V_{BST}$$

Typically, it is recommended to use a 1uF ceramic capacitor with 25V rating and a commonly available diode 1N4148 for the bootstrap circuit. In addition, a small resistor (one ohm) has to be added in between DRN of the SC1211VX and the Phase Node. The resistor is used to alleviate the stress of the SC1211VX from exposing to the negative spike at the Phase node. A negative spike could occur at the Phase Node during the top FET turn-off due to parasitic inductance in the switching loop. The spike could be minimized with a careful PCB layout. In those applications with TO-220 package FETs, it is recommended to use a clamping diode on the DRN pin to

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Applications Information (Cont.)

mitigate the impact of the excessive phase node negative spike.

Filters for Supply Power

For VCC pin of the SC1211VX, it is recommended to use a 1 μ F to 4.7 μ F, 25V rating ceramic capacitor for decoupling.

LAYOUT GUIDELINES

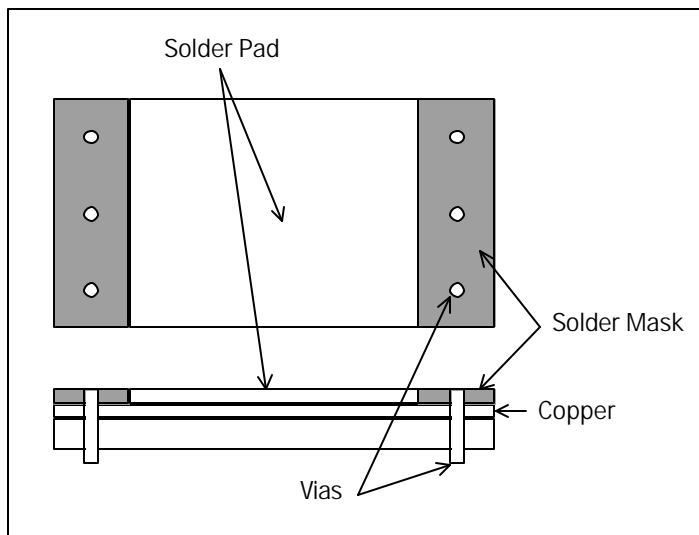
The switching regulator is a high di/dt power circuit. Its Printed Circuit Board (PCB) layout is critical. A good layout can achieve an optimum circuit performance while minimized the component stress, resulting in better system reliability. For a multi-phase voltage regulator, the SC1211VX driver, FETs, inductor, and supply decoupling capacitors in each phase have to be considered as a whole during PCB layout. Refer to Semtech SC2643VX/SC1211VX EVB Layout Guideline.

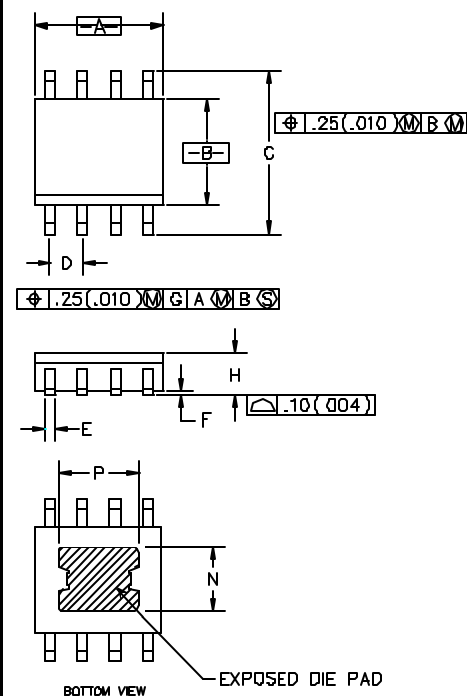
For the SC1211VX driver, the following guidelines are typically recommended during PCB layout:

1. Place the SC1211VX close to the FETs for shortest gate drive traces and ground return paths.
2. Connect the bypass capacitor as close as possible to pin VCC and PGND for decoupling.
3. Locate the components of the bootstrap circuit close to the SC1211VX.

SOLDERING CONSIDERATION

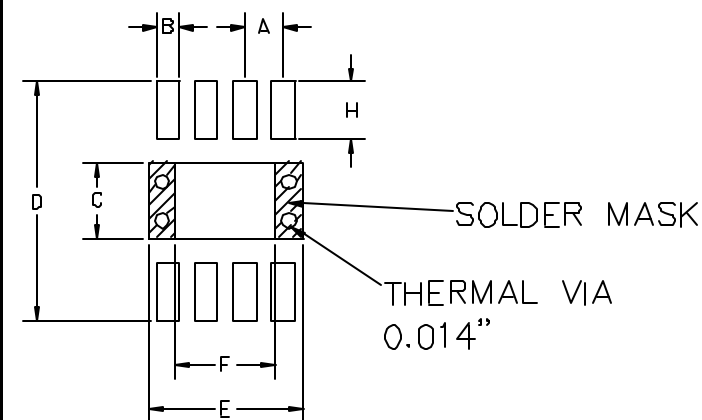
The exposed die pad of the SC1211VX is used for ground return and thermal release of the driver. The pad must be soldered to the ground plane that is further connected to the system ground in the inner layer through multiple vias. For better electrical and thermal performance, it is recommended to use all copper available under the driver as the ground plane, and place the vias as close as possible to the solder pad. Meanwhile, the vias have to be masked out to prevent solder leakage during reflow. The layout arrangement is detailed in the following figure, which also can be found in the "Land Pattern – Power SOIC-8"



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Outline Drawing - Power SOIC-8L


DIM ^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.189	.195	4.80	4.95	2
B	.152	.157	3.86	4.00	3
C	.230	.244	5.84	6.20	
D	.050	BSC	1.27	BSC	
E	.014	.020	0.35	0.51	
F	.001	.005	.025	.127	
H	.056	.066	1.42	1.68	
J	.010	.016	0.25	0.41	
K	.007	.010	0.19	0.25	
L	0°	8°	0°	8°	
M	.016	.035	0.41	0.89	
N	.091	.099	2.31	2.51	4
P	.116	.124	2.95	3.15	4

- ④ END USER SHOULD VERIFY ACTUAL SIZE OF EXPOSED THERMAL DIE PAD FOR SPECIFIC DEVICE APPLICATION.
- ③ DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25 mm (.010") PER SIDE.
- ② DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15 mm (.010") PER SIDE.
- ① CONTROLLING DIMENSION : MILLIMETER

Land Pattern - Power SOIC-8


DIM ^N	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.050	BSC	1.27	BSC	
B	.025	.030	.64	.76	
C	.095	.010	2.41	2.54	
D	.310	.320	7.87	8.13	
E	.200	.210	5.08	5.33	
F	.130	.135	3.30	3.43	
H	.070	.075	1.78	1.91	

Contact Information

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