

74F08

Quad 2-Input AND Gate

General Description

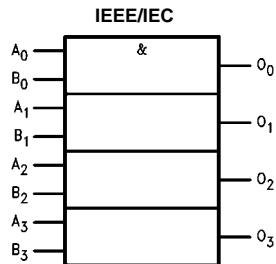
This device contains four independent gates, each of which performs the logic AND function.

Ordering Code:

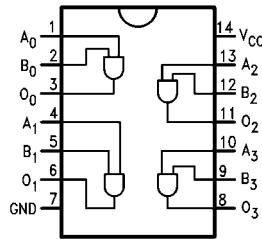
Order Number	Package Number	Package Description
74F08SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74F08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F08PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_n, B_n O_n	Inputs Outputs	1.0/1.0 50/33.3	$20\ \mu A/0.6\ mA$ $-1\ mA/20\ mA$

Absolute Maximum Ratings(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with $V_{CC} = 0V$)	
Standard Output	-0.5V to V_{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

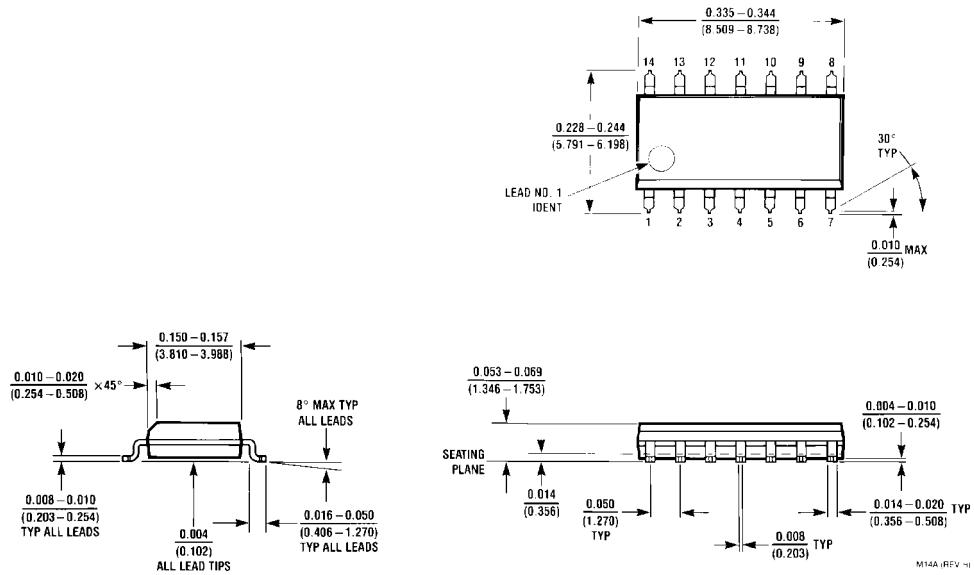
Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

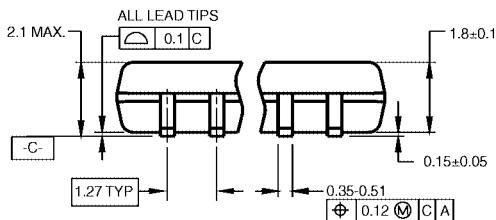
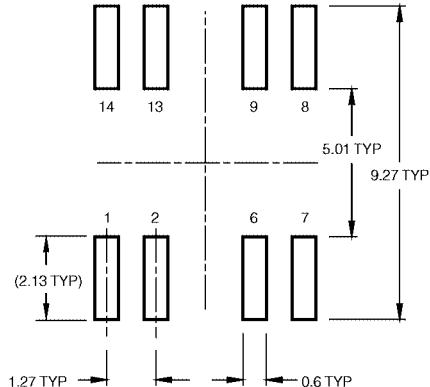
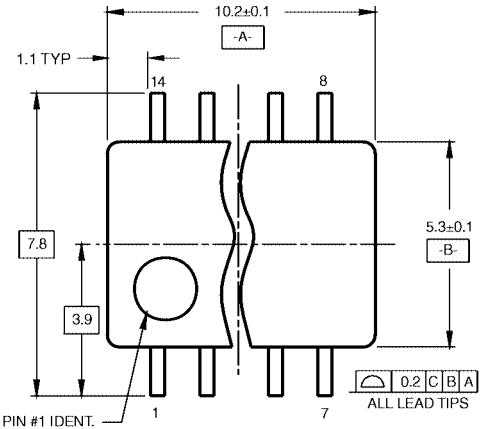
Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5		V	Min	$I_{OH} = -1$ mA
		5% V_{CC}	2.7				$I_{OH} = -1$ mA
V_{OL}	Output LOW Voltage	10% V_{CC}		0.5	V	Min	$I_{OL} = 20$ mA
I_{IH}	Input HIGH Current			5.0	μ A	Max	$V_{IN} = 2.7$ V
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μ A	Max	$V_{IN} = 7.0$ V
I_{CEX}	Output HIGH Leakage Current			50	μ A	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9$ μ A All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current			3.75	μ A	0.0	$V_{OD} = 150$ mV All Other Pins Grounded
I_{IL}	Input LOW Current			-0.6	mA	Max	$V_{IN} = 0.5$ V
I_{OS}	Output Short-Circuit Current	-60		-150	mA	Max	$V_{OUT} = 0$ V
I_{CCH}	Power Supply Current		5.5	8.3	mA	Max	$V_O = \text{HIGH}$
I_{CCL}	Power Supply Current		8.6	12.9	mA	Max	$V_O = \text{LOW}$

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ\text{C}$			$T_A = -55^\circ\text{C} \text{ to } +125^\circ\text{C}$		$T_A = 0^\circ\text{C} \text{ to } +70^\circ\text{C}$		Units
		Min	Typ	Max	$V_{CC} = +5.0\text{V}$	$C_L = 50$ pF	$V_{CC} = +5.0\text{V}$	$C_L = 50$ pF	
t_{PLH}	Propagation Delay A_n, B_n to O_n	3.0	4.2	5.6	2.5	7.5	3.0	6.6	ns
t_{PHL}		2.5	4.0	5.3	2.0	7.5	2.5	6.3	

Physical Dimensions inches (millimeters) unless otherwise noted

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

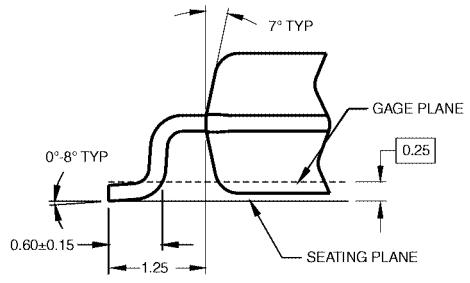
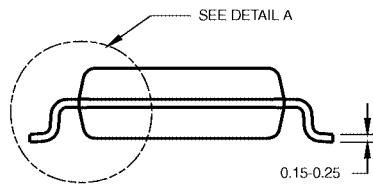
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

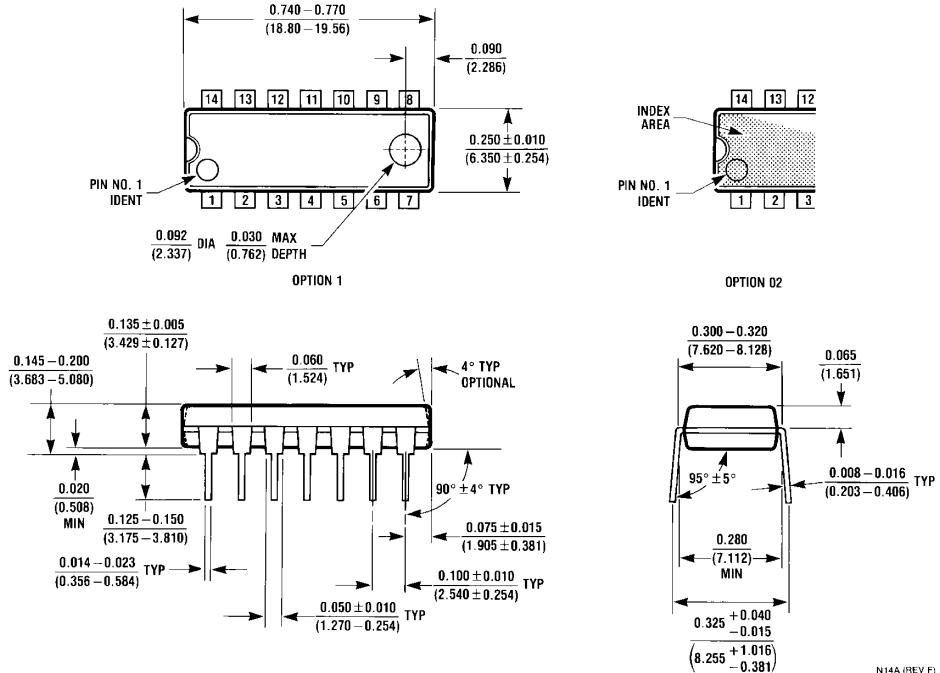
M14DRevB1



14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions

inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A

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