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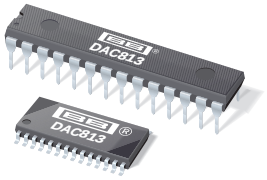


DAC813

Microprocessor-Compatible 12-BIT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- ±1/2LSB NONLINEARITY OVER TEMPERATURE
- GUARANTEED MONOTONIC OVER TEMPERATURE
- LOW POWER: 270mW typ
- DIGITAL INTERFACE DOUBLE BUFFERED: 12 AND 8 + 4 BITS
- SPECIFIED AT ±12V AND ±15V POWER SUPPLIES
- RESET FUNCTION TO BIPOLAR ZERO
- 0.3" WIDE DIP AND SO PACKAGES

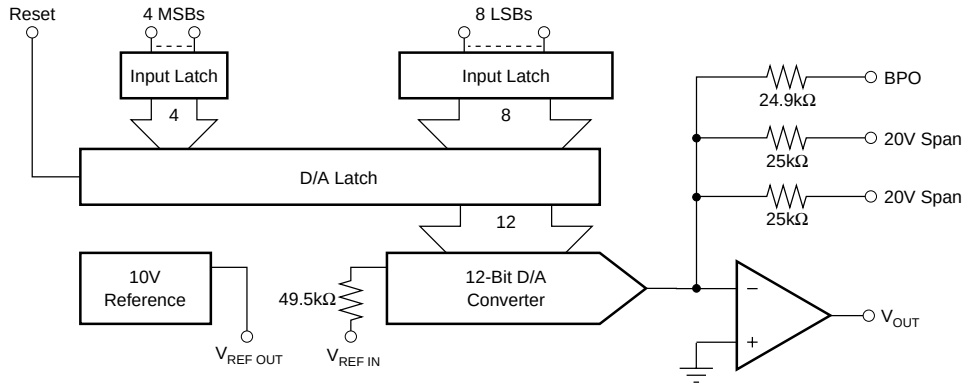
DESCRIPTION

The DAC813 is a complete monolithic 12-bit digital-to-analog converter with a flexible digital interface. It includes a precision +10V reference, interface control logic, double-buffered latch and a 12-bit D/A converter with voltage output operational amplifier. Fast current switches and laser-trimmed thin-film resistors provide a highly accurate, fast D/A converter.

Digital interfacing is facilitated by a double buffered latch. The input latch consists of one 8-bit byte and one 4-bit nibble to allow interfacing to 8-bit (right justified format) or 16-bit data buses. Input gating logic is designed so that the last nibble or byte to be loaded can be loaded simultaneously with the transfer of data to the D/A latch saving computer instructions.

A reset control allows the DAC813 D/A latch to asynchronously reset the D/A output to bipolar zero, a feature useful for power-up reset, recalibration, or for system re-initialization upon system failure.

The DAC813 is specified to ±1/2LSB maximum linearity error (J, A grades) and ±1/4LSB (K grade). It is packaged in 28-pin 0.3" wide plastic DIP and 28-lead plastic SOIC



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SPECIFICATIONS

At T_A = +25°C, $\pm V_{CC}$ = ±12V or ±15V and load on V_{OUT} = 5kΩ || 500pF to common, unless otherwise noted.

PARAMETER	CONDITIONS	DAC813JP, JU, AU			DAC813KP, KU			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS								
Resolution				12			*	Bits
Codes[1]			USB, BOB			*		
Digital Inputs Over Temperature Range[2]								
V_{IH}[3]		+2		+5.5	*		*	VDC
V_{IL}		0		+0.8	*		*	VDC
DATA Bits, $\overline{WR}$, $\overline{Reset}$, $\overline{LDAC}$, $\overline{LMSB}$, $\overline{LLSB}$				±10			*	µA
I_{IH}	V_{IN} = +2.7V			±10			*	µA
I_{IL}	V_{IN} = +0.4V							
ACCURACY								
Linearity Error			±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error			±1/2	±3/4		±1/4	±1/2	LSB
Gain Error[4]			±0.05	±0.2		*	*	%
Unipolar Offset Error[5]			±0.01	±0.02		*	*	% of FSR[7]
Bipolar Zero Error[6]			±0.02	±0.2		*	*	% of FSR
Monotonicity			Guaranteed			*		
Power Supply Sensitivity: $+V_{CC}$	20V Range		5	10		*	*	ppm of FSR/%
$-V_{CC}$			1	10		*	*	ppm of FSR/%
DRIFT	Over Specification							
Gain	Temperature Range		±5	±30		*	±15	ppm/°C
Unipolar Offset			±1	±3		*	±3	ppm of FSR/°C
Bipolar Zero			±3	±10		*	±5	ppm of FSR/°C
Linearity Error Over Temperature Range			±1/2	±3/4		±1/4	±1/2	LSB
Monotonicity Over Temperature Range			Guaranteed			*		
SETTLING TIME[8] (To Within ±0.01% of FSR of Final Value; 5kΩ || 500pF load)								
For Full Scale Range Change	20V Range		4.5	6		*	*	µs
	10V Range		3.3	5		*	*	µs
For 1LSB Change at Major Carry[9]			2			*		µs
Slew Rate			10			*		V/µs
ANALOG OUTPUT								
Voltage Range: Unipolar	$\pm V_{CC}$ > ±11.4V		0 to +10			*		V
Bipolar	$\pm V_{CC}$ > ±11.4V		±5, ±10			*		V
Output Current		±5			*			mA
Output Impedance	At DC		0.2			*		Ω
Short Circuit to Common Duration			Indefinite			*		
REFERENCE VOLTAGE								
Voltage		+9.95	+10	+10.05	*	*	*	V
Source Current Available for External Loads		5			*			mA
Impedance			2			*		Ω
Temperature Coefficient			±5	±25		*	*	ppm/°C
Short Circuit to Common Duration			Indefinite			*		
POWER SUPPLY REQUIREMENTS								
Voltage: $+V_{CC}$		+11.4	+15	+16.5	*	*	*	VDC
$-V_{CC}$		–11.4	–15	–16.5	*	*	*	VDC
Current: $+V_{CC}$ + V_L	No Load		13	15		*	*	mA
$-V_{CC}$	No Load		–5	–7		*	*	mA
Potential at DCOM with Respect to ACOM[10]		–3		+3	*		*	V
Power Dissipation			270	330		*	*	mW
TEMPERATURE RANGE								
Specification: J, K		0		+70	*		*	°C
A		–40		+85	*		*	°C
Operating: J, K		–40		+85	*		*	°C
A		–55		+125	*		*	°C
Storage: J, K		–60		+100	*		*	°C
A		–65		+150	*		*	°C

* Same as specification for DAC813AU, JP, JU.

NOTES: (1) USB = Unipolar Straight Binary; BOB = Bipolar Offset Binary. (2) TTL and 5V CMOS compatible. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY in the OPERATION section. (4) Specified with 500Ω Pin 6 to 7. Adjustable to zero with external trim potentiometer. (5) Error at input code 000_{HEX} for unipolar mode, FSR = 10V. (6) Error at input code 800_{HEX} for bipolar range. Specified with 100Ω Pin 6 to 4 and with 500Ω pin 6 to 7. See page 9 for zero adjustment procedure. (7) FSR means Full Scale Range and is 20V for the ±10V range. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$. (10) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	$+V_L$	Positive supply pin for logic circuits. Connect to $+V_{CC}$.
2, 3	20V Range	Connect Pin 2 or Pin 3 to Pin 9 (V_{OUT}) for a 20V FSR. Connect both to Pin 9 for a 10V FSR.
4	BPO	Bipolar offset. Connect to Pin 6 ($V_{REF\ OUT}$) through 100Ω resistor or 200Ω potentiometer for bipolar operation.
5	ACOM	Analog common, $\pm V_{CC}$ supply return.
6	$V_{REF\ OUT}$	+10V reference output referred to ACOM.
7	$V_{REF\ IN}$	Connected to $V_{REF\ OUT}$ through a 1kΩ gain adjustment potentiometer or a 500Ω resistor.
8	$+V_{CC}$	Analog supply input, nominally +12V to +15V referred to ACOM.
9	V_{OUT}	D/A converter voltage output.
10	$-V_{CC}$	Analog supply input, nominally –12V or –15V referred to ACOM.
11	$\overline{WR}$	Master enable for $\overline{LDAC}$, $\overline{LLSB}$, and $\overline{LMSB}$. Must be low for data transfer to any latch.
12	$\overline{LDAC}$	Load DAC. Must be low with $\overline{WR}$ for data transfer to the D/A latch and simultaneous update of the D/A converter.
13	$\overline{Reset}$	When low, resets the D/A latch such that a Bipolar Zero output is produced. This control overrides all other data input operations.
14	$\overline{LMSB}$	Enable for 4-bit input latch of D_8-D_{11} data inputs. NOTE: This logic path is slower than the $\overline{WR}$ path.
15	$\overline{LLSB}$	Enable for 8-bit input latch of D_0-D_7 data inputs. NOTE: This logic path is slower than the $\overline{WR}$ path.
16	DCOM	Digital common.
17	D0	Data Bit 1, LSB.
18	D1	Data Bit 2.
19	D2	Data Bit 3.
20	D3	Data Bit 4.
21	D4	Data Bit 5.
22	D5	Data Bit 6.
23	D6	Data Bit 7.
24	D7	Data Bit 8.
25	D8	Data Bit 9.
26	D9	Data Bit 10.
27	D10	Data Bit 11.
28	D11	Data Bit 12, MSB, positive true.

ABSOLUTE MAXIMUM RATINGS(1)

$+V_{CC}$ to ACOM	0 to +18V
$-V_{CC}$ to ACOM	0 to –18V
$+V_{CC}$ to $-V_{CC}$	0 to +36V
DCOM with respect to ACOM	±4V
Digital Inputs (Pins 11–15, 17–28) to DCOM	–0.5V to $+V_{CC}$
External Voltage Applied to BPO Span Resistor	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to ACOM
V_{OUT}	Indefinite Short to ACOM
Power Dissipation	750mW
Lead Temperature (soldering, 10s)	+300°C
Max Junction Temperature	+165°C
Thermal Resistance, $\theta_{J\text{-}A}$: Plastic DIP and SOIC	130°C/W
Ceramic DIP	85°C/W

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

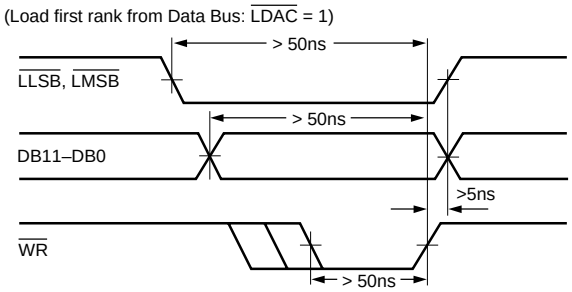
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE	LINEARITY ERROR, MAX AT +25°C (LSB)	GAIN DRIFT (ppm/°C)
DAC813JP	28-Pin Plastic DIP	246	0°C to +70°C	±1/2	±30
DAC813JU	28-Lead Plastic SOIC	217	0°C to +70°C	±1/2	±30
DAC813KP	28-Pin Plastic DIP	246	0°C to +70°C	±1/4	±15
DAC813KU	28-Lead Plastic SOIC	217	0°C to +70°C	±1/4	±15
DAC813AU	28-Lead Plastic SOIC	217	–40°C to +85°C	±1/2	±30

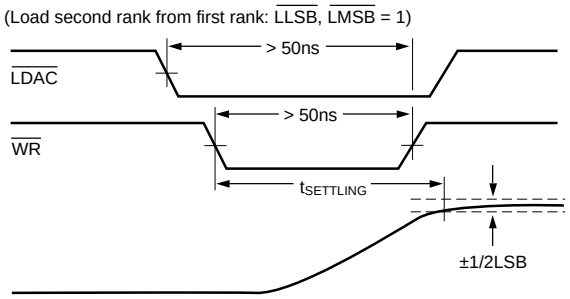
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

MINIMUM TIMING DIAGRAMS

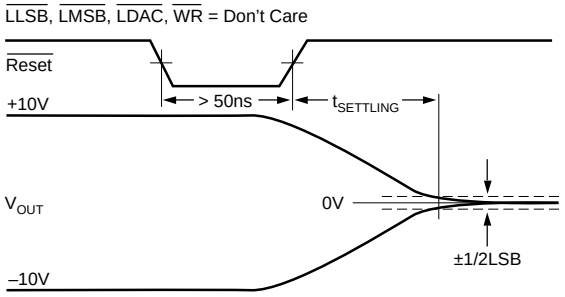
WRITE CYCLE #1



WRITE CYCLE #2



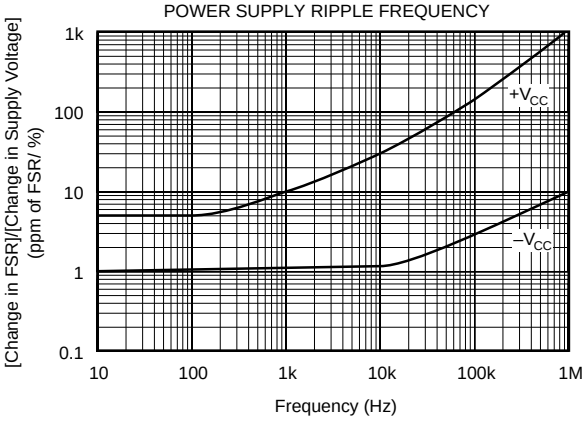
RESET COMMAND (Bipolar Mode)



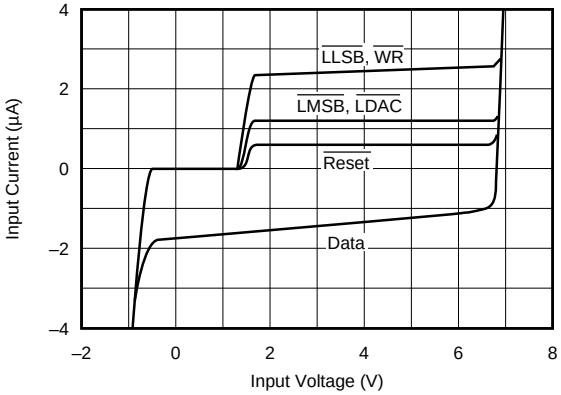
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.

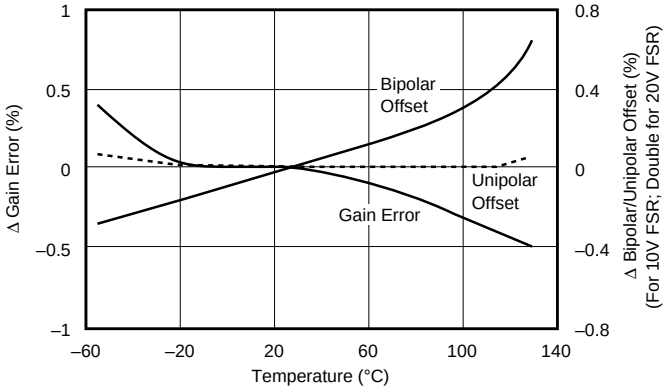
POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY



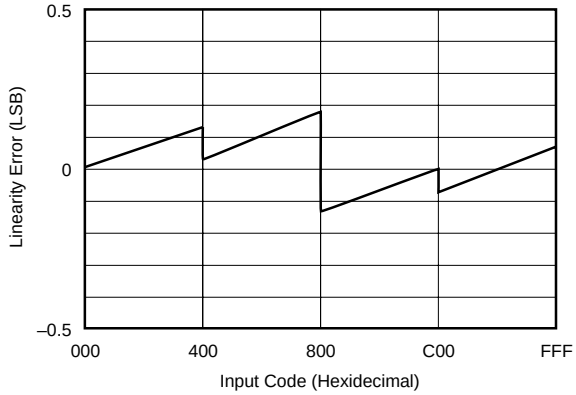
DIGITAL INPUT CURRENT
vs INPUT VOLTAGE



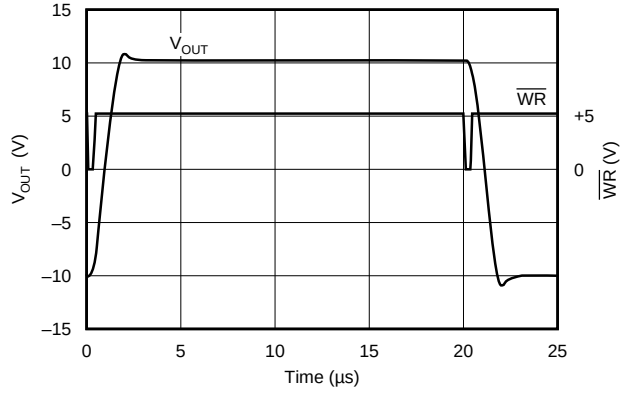
CHANGE OF GAIN AND OFFSET ERROR
vs TEMPERATURE



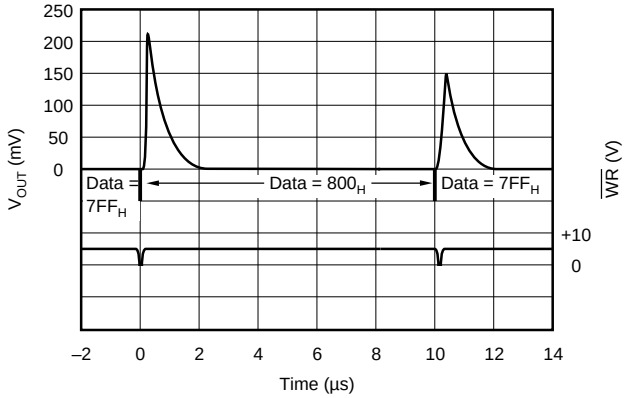
INTEGRAL LINEARITY ERROR



± FULL SCALE OUTPUT SWING

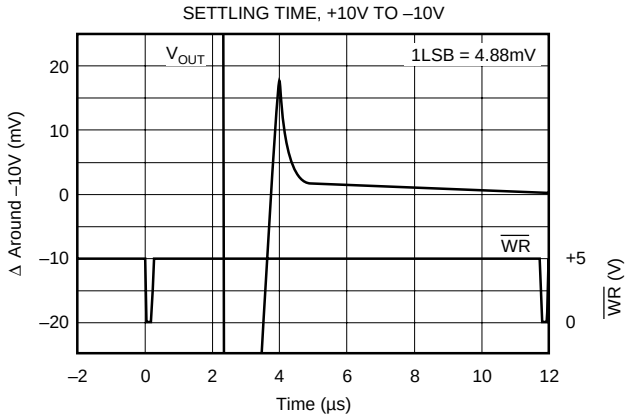


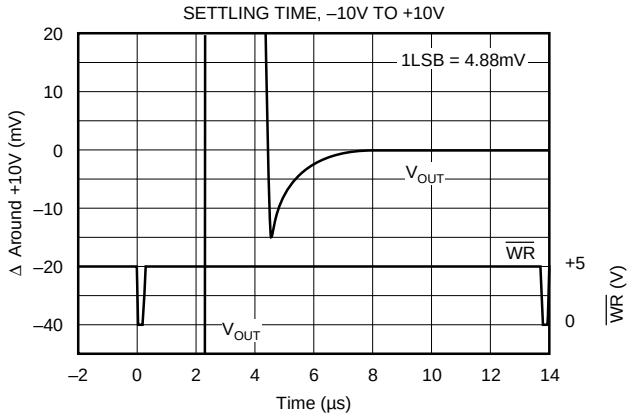
MAJOR CARRY GLITCH



TYPICAL PERFORMANCE CURVES (CONT)

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.





DISCUSSION OF SPECIFICATIONS

INPUT CODES

The DAC813 accepts positive-true binary input codes. DAC813 may be connected by the user for any one of the following codes: USB (Unipolar Straight Binary), BOB (Bipolar Offset Binary) or, using an external inverter on the MSB line, BTC (Binary Two's Complement). See Table I.

DIGITAL INPUT	ANALOG OUTPUT		
MSB to LSB	USB Unipolar Straight Binary	BOB Bipolar Offset Binary	BTC* Binary Two's Complement
FFF_{HEX}	+ Full Scale	+ Full Scale	Zero – 1LSB
800_{HEX}	+ 1/2 Full Scale	Zero	– Full Scale
$7FF_{HEX}$	+ 1/2 Full Scale – 1LSB	Zero – 1LSB	+ Full Scale
000_{HEX}	Zero	– Full Scale	Zero
* Invert MSB of BOB code with external inverter to obtain BTC code.			

TABLE I. Digital Input Codes.

LINEARITY ERROR

Linearity error as used in D/A converter specifications by Burr-Brown is the deviation of the analog output from a straight line drawn between the end points (inputs all "1s" and all "0s"). The DAC813 linearity error is specified at ±1/4LSB (max) at +25°C K grades, and ±1/2LSB (max) for J grades.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of 1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the input changes from one state to the next. Monotonicity requires that DLE be less than 1LSB over the temperature range of interest.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital inputs. All grades of DAC813 are monotonic over their specification temperature range.

DRIFT

Gain Drift is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/°C).

Unipolar Offset Drift is measured with a data input of 000_{HEX}. The D/A is configured for unipolar output. Unipolar Offset Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

Bipolar Zero Drift is measured with a data input of 800_{HEX}. The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/°C).

SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle within an error band around its final value after a change in input. Three settling times are specified to ±0.012% of Full Scale Range (FSR): two for maximum full scale range changes of 20V and 10V, and one for a 1LSB change. The 1LSB change is measured at the major carry ($7FF_{HEX}$ to 800_{HEX} and 800_{HEX} to $7FF_{HEX}$), the input transition at which worst-case settling time occurs.

REFERENCE SUPPLY

DAC813 contains an on-chip +10V reference. This voltage (pin 6) has a tolerance of ±50mV. $V_{REF\ OUT}$ must be connected to $V_{REF\ IN}$ through a gain adjust resistor with a nominal value of 500Ω. The connection can be made through an optional 1kΩ trim resistor to provide adjustment to zero

gain error. The reference output may be used to drive external loads, sourcing at least 5mA. This current should be constant, otherwise the gain of the converter will vary.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a ppm of FSR output change per percent of change in either $+V_{CC}$ or $-V_{CC}$ about the nominal voltages expressed in ppm of FSR/%. The first performance curve on page 5 shows typical power supply rejection versus power supply ripple frequency.

OPERATION

DAC813 is a complete single IC chip 12-bit D/A converter. The chip contains a 12-bit D/A converter, voltage reference, output amplifier, and microcomputer-compatible input logic as shown in Figure 1.

INTERFACE LOGIC

Input latches hold data temporarily while a complete 12-bit word is assembled before loading into the D/A latch. This double-buffered organization prevents the generation of spurious analog output values. Each latch is independently addressable.

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for the control signals is presented in Table II.

$\overline{WR}$	$\overline{LLSB}$	$\overline{LMSB}$	$\overline{LDAC}$	$\overline{RESET}$	OPERATION
1	X	X	X	1	No operation
X	X	X	X	0	D/A latch set to 800_{HEX}
0	1	0	1	1	Enables 4 MSBs input latch
0	0	1	1	1	Enables 8 LSBs input latch
0	1	1	0	1	Loads D/A latch from input latches
0	0	0	0	1	Makes all latches transparent
"X" = Don't Care					

TABLE II. DAC813 Interface Logic Truth Table.

CAUTION: DAC813 was designed to use $\overline{WR}$ as the fast strobe. $\overline{WR}$ has a much faster logic path than $\overline{EN}_X$ (or $\overline{LDAC}$). Therefore, if one permanently wires $\overline{WR}$ to DCOM and uses only $\overline{EN}_X$ to strobe data into the latches, the DATA HOLD time will be long, approximately 15ns to 30ns, and this time will vary considerably in this range from unit to unit. DATA HOLD time using $\overline{WR}$ is 5ns max.

LOGIC INPUT COMPATIBILITY

The DAC813 digital inputs are TTL, 5V CMOS compatible over the operating range of $+V_{CC}$. The input switching threshold remains at the TTL threshold over the supply range. An equivalent circuit of a digital input is shown in Figure 2.

The logic input current over temperature is low enough to permit driving the DAC813 directly from the outputs of 5V CMOS devices.

Open DATA input lines will float to 7V or more. Although this will not harm the DAC813, current spikes will occur in the input lines when a logic 0 is asserted and, in addition,

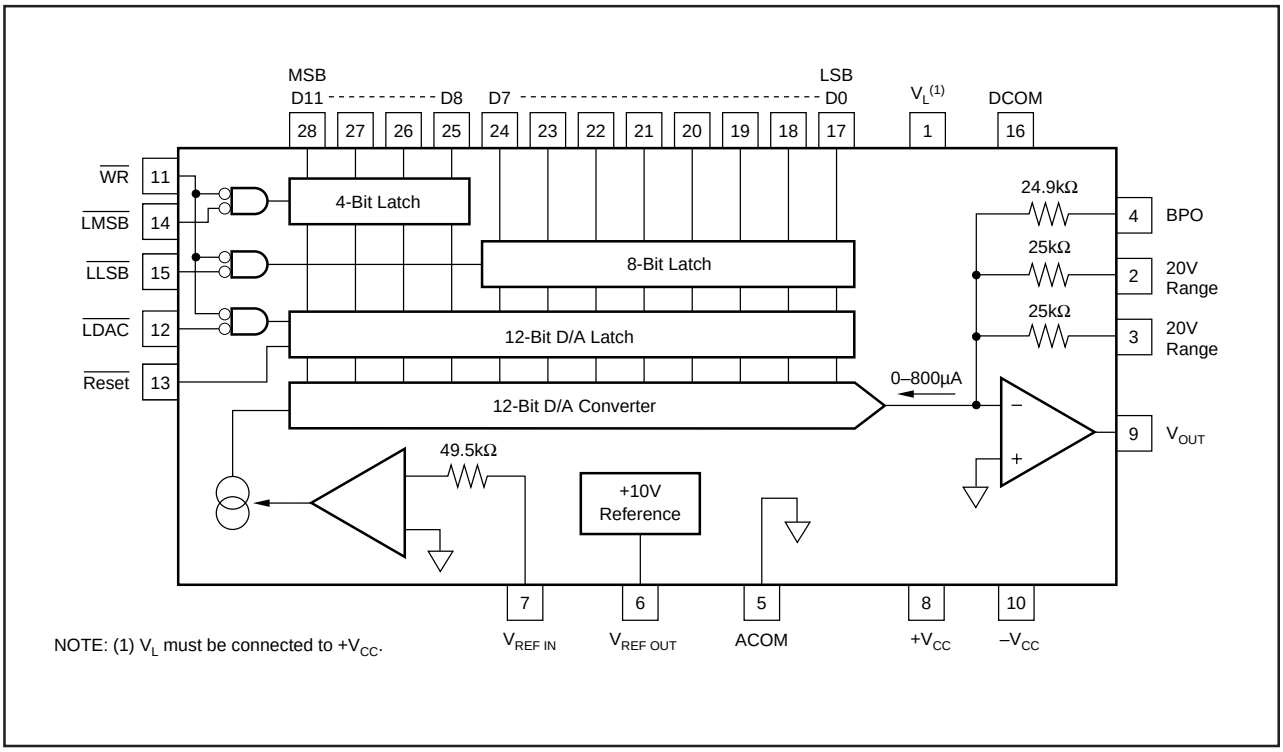


FIGURE 1. DAC813 Block Diagram.

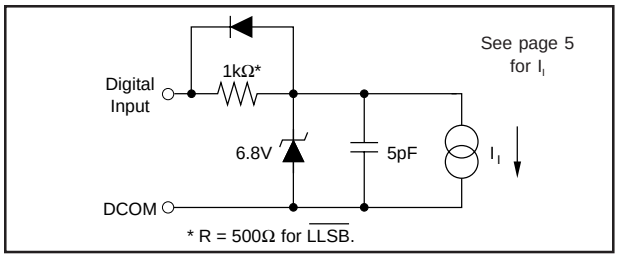


FIGURE 2. Equivalent Input Circuit for Digital Inputs.

the speed of the interface will be slower. A digital output driving a DATA input line of the DAC813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

RESET FUNCTION

When asserted low (<0.8V), $\overline{\text{RESET}}$ (Pin 13) forces the D/A latch to 800_{HEX} regardless of any other input logic condition. If the analog output is connected for bipolar operation (either ±10V or ±5V), the output will be reset to Bipolar Zero (0V). If the analog output is connected for unipolar operation (0 to +10V), the output will be reset to half-scale (+5V).

If $\overline{\text{RESET}}$ is not used, it should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available $\overline{\text{Reset}}$ can be connected to $+V_{CC}$ through a 100kΩ to 1MΩ resistor to limit the input current.

GAIN AND OFFSET ADJUSTMENTS

Figures 3 and 4 illustrate the relationship of offset and gain adjustments to unipolar and bipolar D/A converter output.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the offset potentiometer for minus full scale voltage. Example: If the full scale range is connected for 20V, the maximum negative output voltage is –10V. See Table III for corresponding codes.

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for positive full scale voltages.

DIGITAL INPUT	ANALOG OUTPUT		
MSB to LSB	0 to +10V	±5V	±10V
FFF_{HEX}	+9.9976V	+4.9976V	+9.9951V
800_{HEX}	+5.0000V	0.0000V	0.0000V
$7FF_{HEX}$	+4.9976V	–0.0024V	–0.0049V
000_{HEX}	0.0000V	–5.0000V	–10.0000V
1LSB	2.44mV	2.44mV	4.88mV

TABLE III. Digital Input/Analog Output.

INSTALLATION

POWER SUPPLY CONNECTIONS

Note that the lid of the ceramic packaged DAC813 is connected to $-V_{CC}$. Take care to avoid accidental short circuits in tightly spaced installations.

Power supply decoupling capacitors should be added as shown in Figure 5. Optimum settling performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$ and at least a 0.01µF ceramic capacitor at $+V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well. The 0.01µF capacitors should be located close to the DAC813.

Pin 1 supplies internal logic and **must** be connected to $+V_{CC}$.

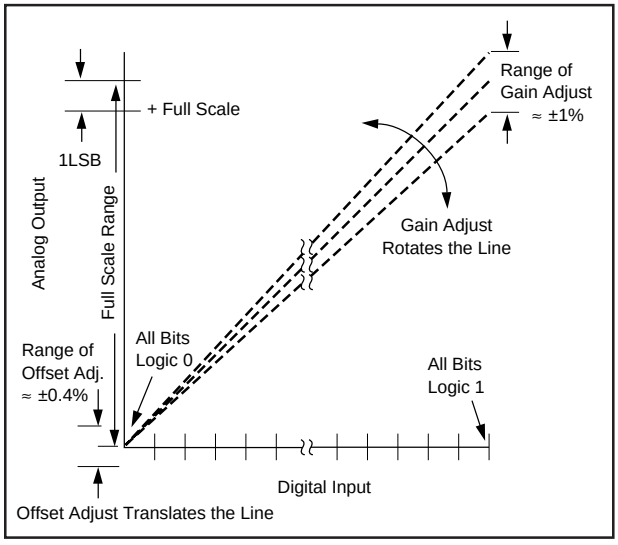


FIGURE 3. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

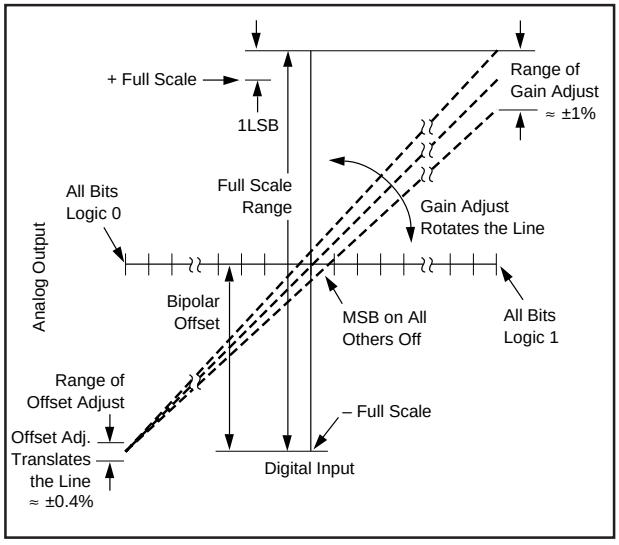


FIGURE 4. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

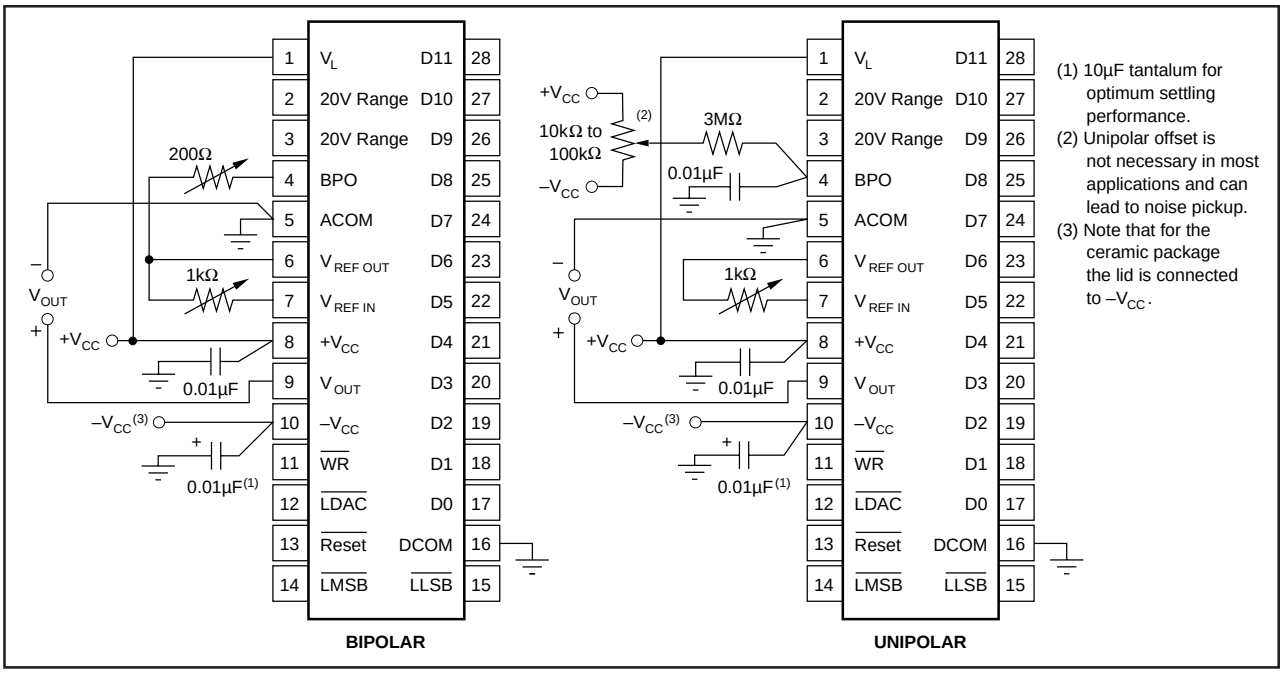


FIGURE 5. Power Supply, Gain, and Offset Connections.

DAC813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both Analog Common (ACOM, Pin 5) and Digital Common (DCOM, Pin 16) be connected directly to a ground plane under the package. If a ground plane is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is also important to connect the load directly to the ACOM pin. Refer to Figure 5.

The change in current in the Analog Common pin (ACOM, Pin 5) due to an input data word change from 000_{HEX} to FFF_{HEX} is only 800µA.

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC813 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. Refer to Figure 6.

The internal feedback resistors (25kΩ) and the bipolar offset resistor (24.9kΩ) are trimmed to an absolute tolerance of less than ±2%. Therefore, one can change the range by adding a series resistor in various feedback circuit configurations. For example, a 600Ω resistor in series with the 20V range terminal can be used to obtain a 20.48V (±10.24V) range (5mV LSB). A 7.98kΩ resistor in series with the 10V range connection (20V ranges in parallel) gives a 16.384V (±8.192V) bipolar range (4mV LSB). Gain drift will be affected by the mismatch of the temperature coefficient of the external resistor with the internal D/A resistors.

APPLICATIONS

MICROCOMPUTER BUS INTERFACING

The DAC813 interface logic allows easy interface to microcomputer bus structures. The control signal is derived from external device select logic and the I/O Write or Memory Write (depending upon the system design) signals from the microcomputer.

The latch enable lines $\overline{LMSB}$, $\overline{LLSB}$, and $\overline{LDAC}$ determine which of the latches are selected. It is permissible to enable two or more latches simultaneously, as shown in some of the following examples.

The double-buffered latch permits data to be loaded into the input latches of several DAC813s and later strobed into the D/A latch of all D/As, simultaneously updating all analog outputs. All the interface schemes shown below use a base address decoder. If blocks of memory are used, the base address decoder can be simplified or eliminated altogether.

8-BIT INTERFACE

The control logic of DAC813 permits interfacing to right-justified data formats, illustrated in Figure 7. When a 12-bit D/A converter is loaded from an 8-bit bus, two bytes of data are required. Figure 8 illustrates an addressing scheme for right-justified data. The base address is decoded from the high-order address bits. A0 and A1 address the appropriate latches. Note that adjacent addresses are used. $X10_{HEX}$ loads the 8 LSBs and $X01_{HEX}$ loads the 4 MSBs and simultaneously transfers input latch data to the D/A latch. Addresses $X00_{HEX}$ and $X11_{HEX}$ are not used.

INTERFACING MULTIPLE DAC813s IN 8-BIT SYSTEMS

Many applications, such as automatic test systems, require that the outputs of several D/A converters be updated simultaneously. The interface shown in Figure 9 uses a 74LSB138 decoder to decode a set of eight adjacent addresses to load the input latches of four DAC813s. The example uses a right-justified data format.

A ninth address using A3 causes all DAC813s to be updated simultaneously. If a certain DAC813 is always loaded last (for instance, D/A #4), A3 is not needed, saving 8 address spaces for other uses. Incorporate A3 into the base address decoder, remove the inverter, connect the common $\overline{LDAC}$ line to $\overline{LLSB}$ of D/A #4, and connect D1 of the 74LS138 to +5V.

12- AND 16-BIT MICROCOMPUTER INTERFACE

For this application the input latch enable lines, $\overline{LMSB}$ and $\overline{LLSB}$, are tied low, causing the latches to be transparent. The D/A latch, and therefore DAC813, is selected by the address decoder and strobed by $\overline{WR}$.

Be sure and read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.

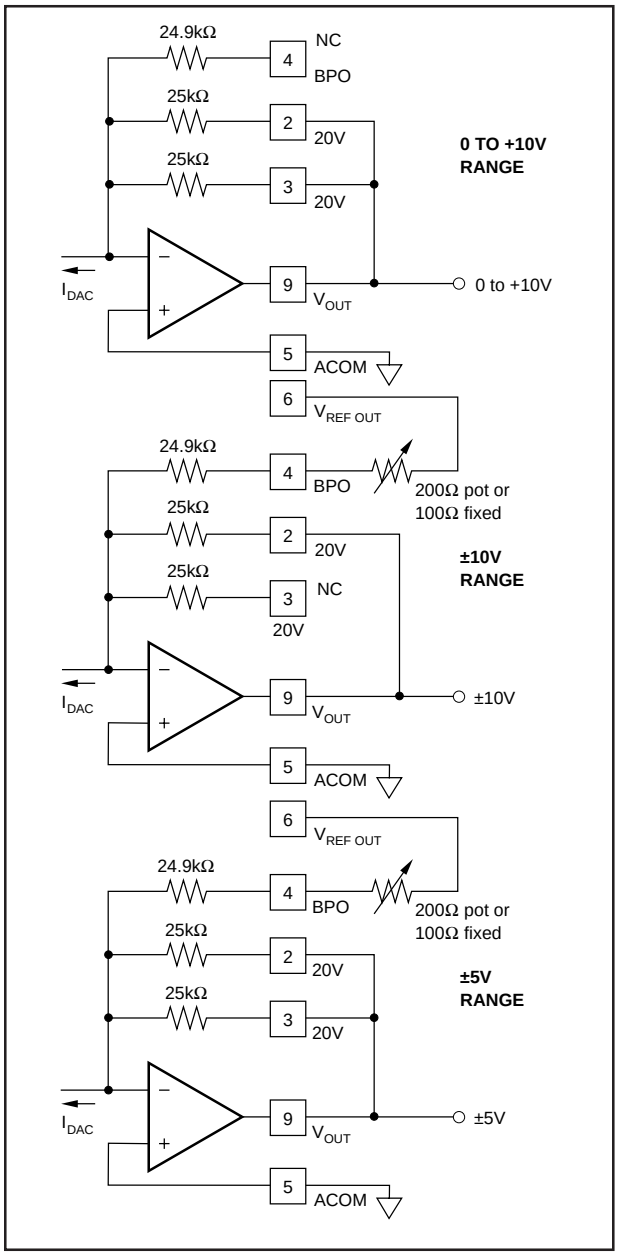


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

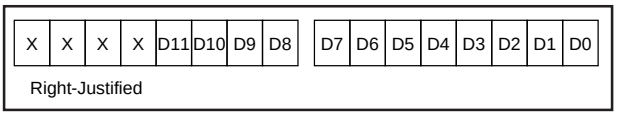


FIGURE 7. 12-Bit Data Format for 8-Bit Systems.

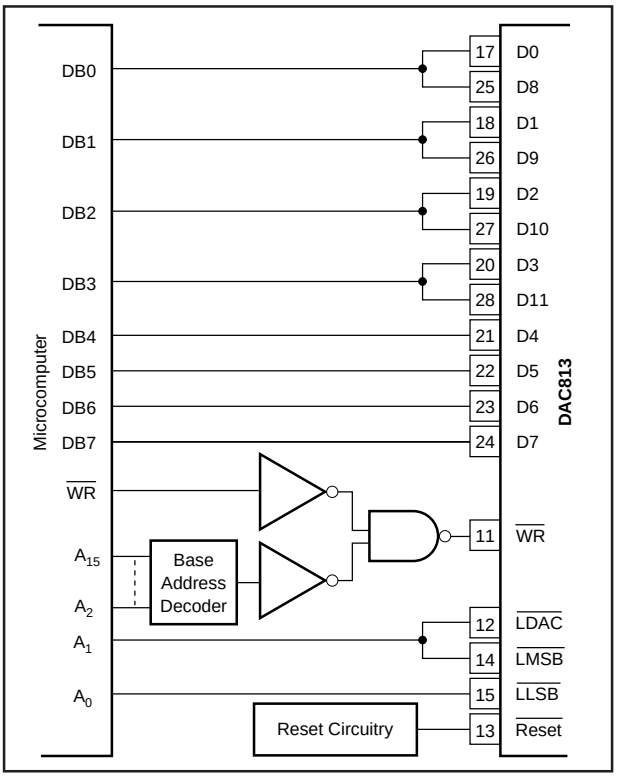
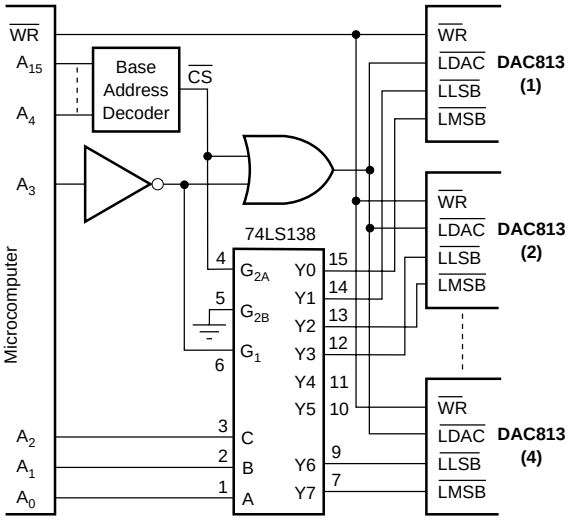


FIGURE 8. Right-Justified Data Bus Interface.



ADDRESS BUS A3	A2	A1	A0	OPERATION
0	0	0	0	Load 8 LSB – D/A #1
0	0	0	1	Load 4 MSB – D/A #1
0	0	1	0	Load 8 LSB – D/A #2
0	0	1	1	Load 4 MSB – D/A #2
0	1	0	0	Load 8 LSB – D/A #3
0	1	0	1	Load 4 MSB – D/A #3
0	1	1	0	Load 8 LSB – D/A #4
0	1	1	1	Load 4 MSB – D/A #4
1	X	X	X	Load D/A Latch—All D/A

FIGURE 9. Interfacing Multiple DAC813s to an 8-Bit Bus.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC813AU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC813AU	Samples
DAC813AU/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC813AU	Samples
DAC813AU/1KG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC813AU	Samples
DAC813AUG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC813AU	Samples
DAC813JP	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	DAC813JP	
DAC813JPG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	DAC813JP	
DAC813JU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC813JU	Samples
DAC813JU/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC813JU	Samples
DAC813JUG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC813JU	Samples
DAC813KP	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	DAC813KP	
DAC813KPG4	NRND	PDIP	NT	28	13	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	DAC813KP	
DAC813KU	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC813KU	Samples
DAC813KUG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 70	DAC813KU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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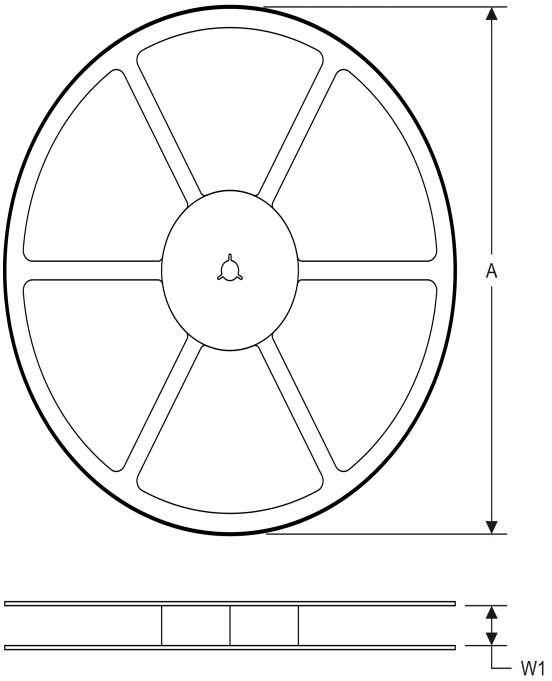
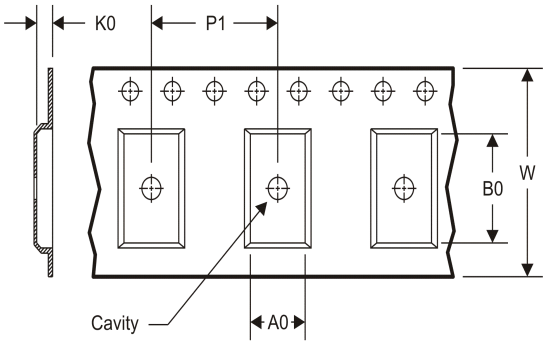
REEL DIMENSIONS



TAPE DIMENSIONS



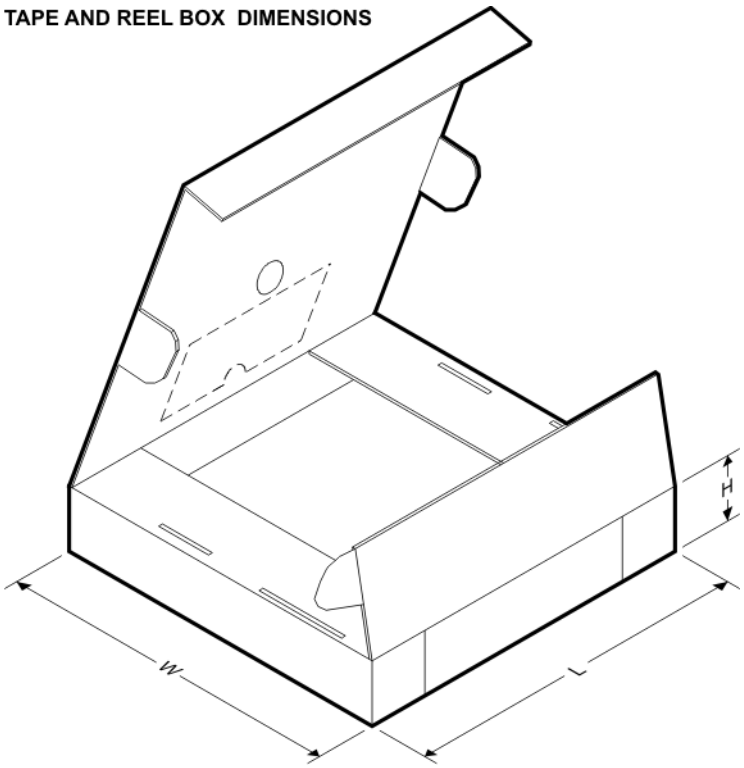
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC813AU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
DAC813JU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC813AU/1K	SOIC	DW	28	1000	367.0	367.0	55.0
DAC813JU/1K	SOIC	DW	28	1000	367.0	367.0	55.0

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