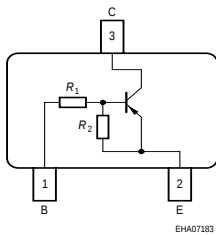


PNP Silicon Digital Transistor

- Built in bias resistor ($R_1 = 1\text{ k}\Omega$, $R_2 = 10\text{ k}\Omega$)
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101



Type	Marking	Pin Configuration			Package
BCR573	XHs	1=B	2=E	3=C	SOT23

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}	50	V
Collector-base voltage	V_{CBO}	50	
Input forward voltage	$V_{i(fwd)}$	12	
Input reverse voltage	$V_{i(rev)}$	5	
Collector current	I_C	500	mA
Total power dissipation- $T_S \leq 79\text{ }^\circ\text{C}$	P_{tot}	330	mW
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-65 ... 150	

Thermal Resistance

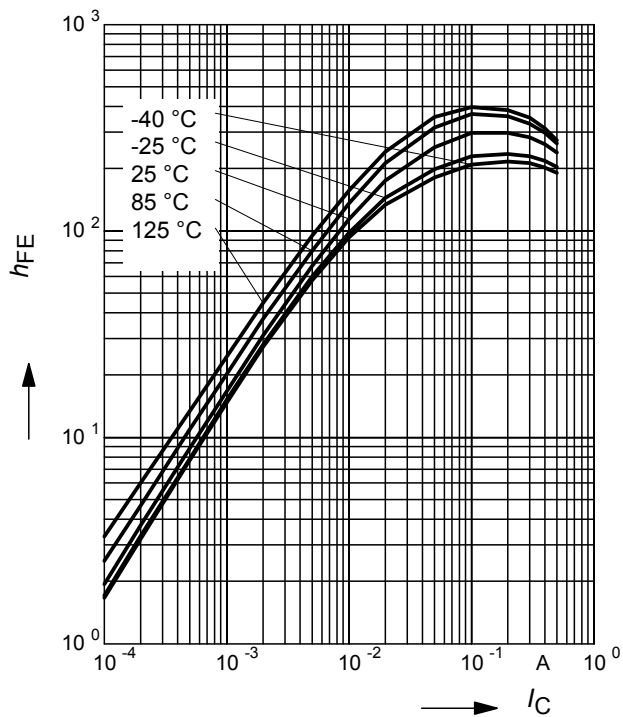
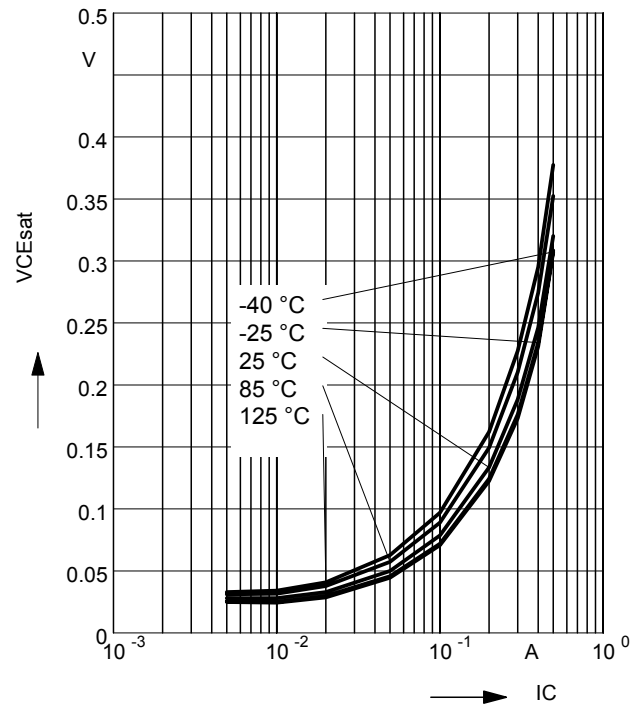
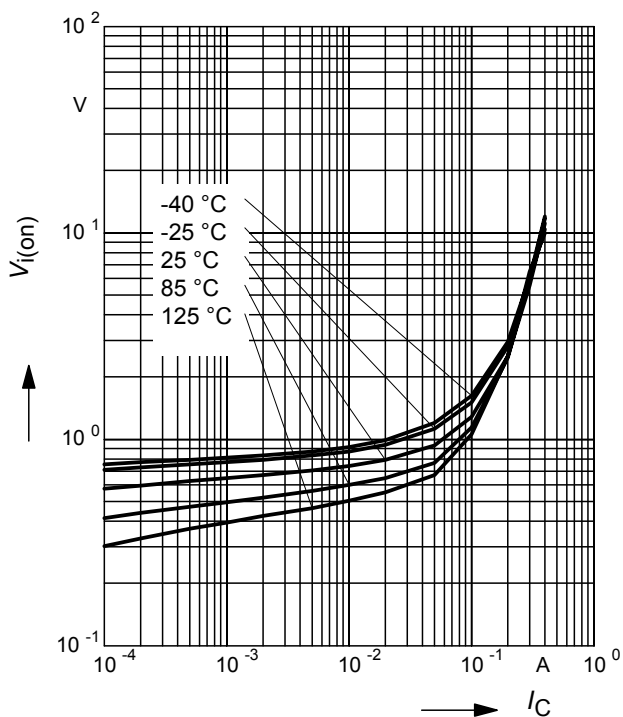
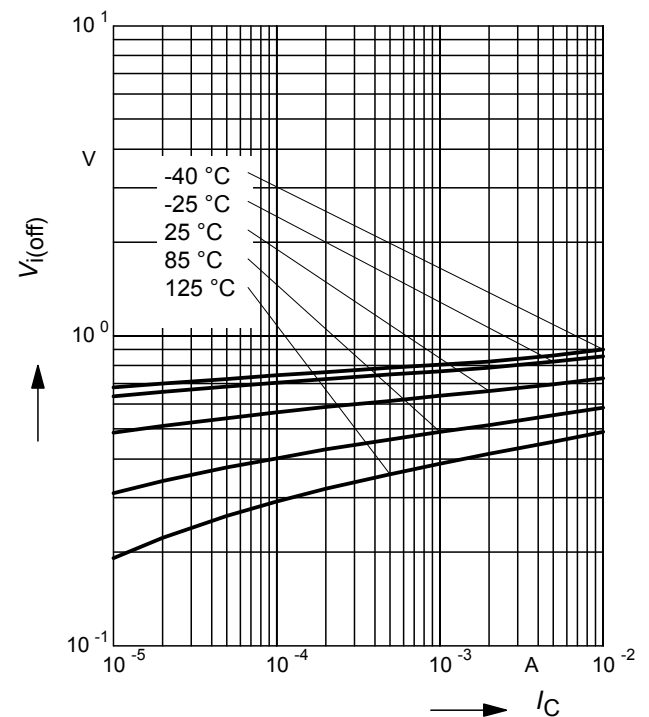
Parameter	Symbol	Value	Unit
Junction - soldering point ¹⁾	R_{thJS}	≤ 215	K/W

¹⁾For calculation of R_{thJA} please refer to Application Note AN077 (Thermal Resistance Calculation)

Electrical Characteristics at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Collector-emitter breakdown voltage $I_C = 100\ \mu\text{A}$, $I_B = 0$	$V_{(\text{BR})\text{CEO}}$	50	-	-	V
Collector-base breakdown voltage $I_C = 10\ \mu\text{A}$, $I_E = 0$	$V_{(\text{BR})\text{CBO}}$	50	-	-	
Collector-base cutoff current $V_{\text{CB}} = 50\ \text{V}$, $I_E = 0$	I_{CBO}	-	-	100	nA
Emitter-base cutoff current $V_{\text{EB}} = 5\ \text{V}$, $I_C = 0$	I_{EBO}	-	-	0.72	mA
DC current gain- $I_C = 50\ \text{mA}$, $V_{\text{CE}} = 5\ \text{V}$	h_{FE}	70	-	-	-
Collector-emitter saturation voltage ¹⁾ $I_C = 50\ \text{mA}$, $I_B = 2.5\ \text{mA}$	V_{CEsat}	-	-	0.3	V
Input off voltage $I_C = 100\ \mu\text{A}$, $V_{\text{CE}} = 5\ \text{V}$	$V_{\text{i(off)}}$	0.3	-	1	
Input on voltage $I_C = 10\ \text{mA}$, $V_{\text{CE}} = 0.3\ \text{V}$	$V_{\text{i(on)}}$	0.4	-	1.4	
Input resistor	R_1	0.7	1	1.3	kΩ
Resistor ratio	R_1/R_2	0.09	0.1	0.11	-
AC Characteristics					
Transition frequency $I_C = 50\ \text{mA}$, $V_{\text{CE}} = 5\ \text{V}$, $f = 100\ \text{MHz}$	f_{T}	-	150	-	MHz

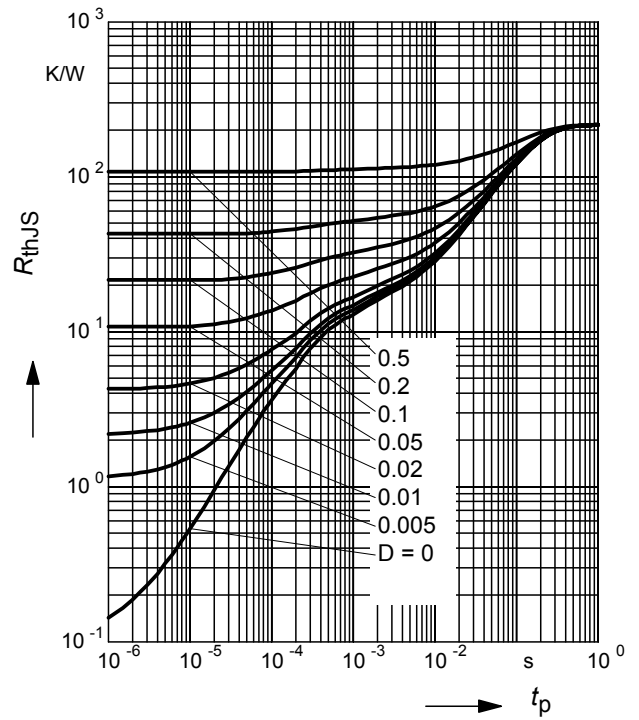
¹⁾Pulse test: $t < 300\ \mu\text{s}$; $D < 2\%$

DC current gain $h_{FE} = f(I_C)$
 $V_{CE} = 5 \text{ V}$ (common emitter configuration)

Collector-emitter saturation voltage
 $V_{CEsat} = f(I_C), h_{FE} = 20$

Input on Voltage $V_{i(on)} = f(I_C)$
 $V_{CE} = 0.3 \text{ V}$ (common emitter configuration)

Input off voltage $V_{i(off)} = f(I_C)$
 $V_{CE} = 5 \text{ V}$ (common emitter configuration)


Total power dissipation $P_{\text{tot}} = f(T_S)$



Permissible Pulse Load $R_{\text{thJS}} = f(t_p)$

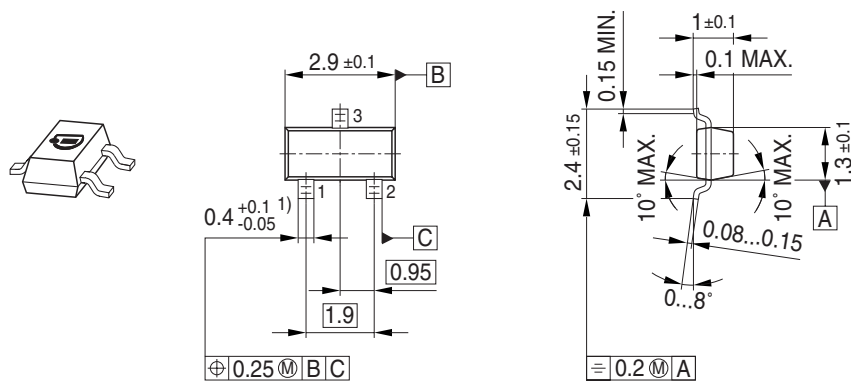


Permissible Pulse Load

$P_{\text{totmax}}/P_{\text{totDC}} = f(t_p)$

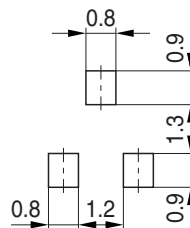


Package Outline

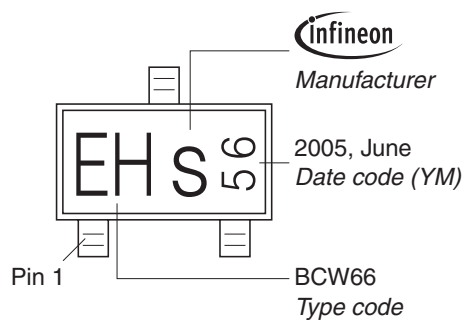


1) Lead width can be 0.6 max. in dambar area

Foot Print

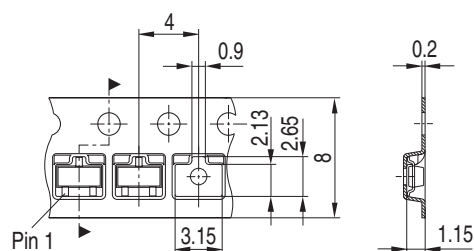


Marking Layout (Example)



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel



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