CYPRESS SEMICONDUCTOR

T-46-23-10

# CY7C194
# CY7C195
# CY7C196

## 65,536 x 4 Static R/W RAM

### Features

- Automatic power-down when deselected
- Output Enable ($\overline{OE}$) feature (7C195 and 7C196)
- CMOS for optimum speed/power
- High speed
  — $t_{AA}$ = 25 ns
- Low active power
  — 880 mW
- Low standby power
  — 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

### Functional Description

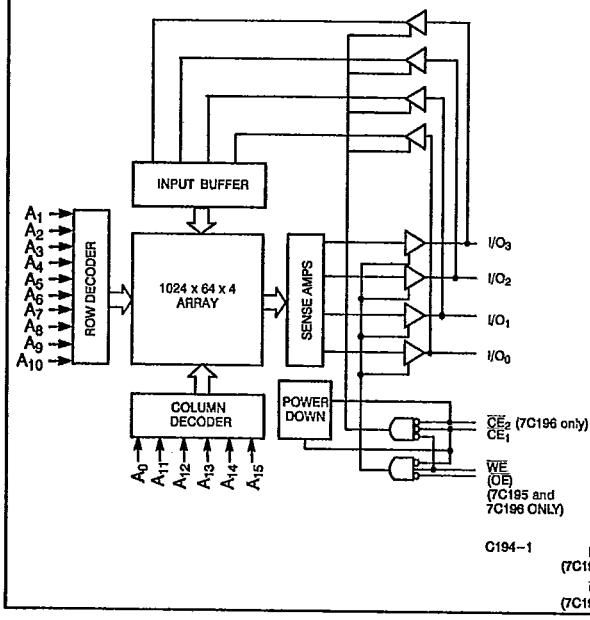
The CY7C194, CY7C195, and CY7C196 are high-performance CMOS static RAMs organized as 65,536 by 4 bits. Easy memory expansion is provided by active LOW chip enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE_1}$, $\overline{CE_2}$ on the CY7C196) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

Writing to the device is accomplished when the chip enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE_1}$, $\overline{CE_2}$ on the CY7C196) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins ($I/O_0$ through $I/O_3$) is written into the memory location, specified on the address pins ($A_0$ through $A_{15}$).

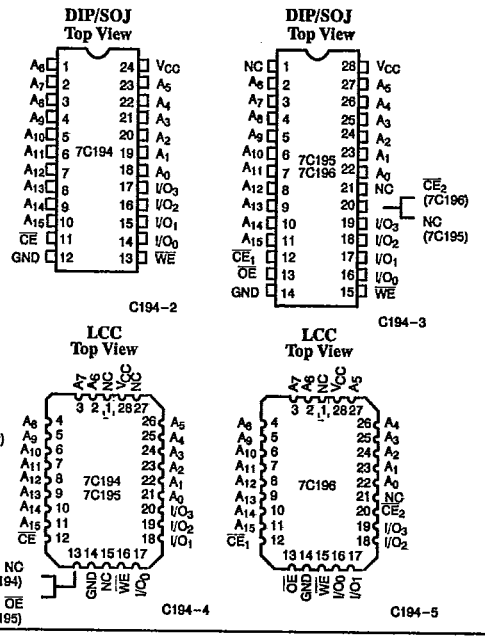
Reading the device is accomplished by taking the chip enable(s) ($\overline{CE}$ on the CY7C194 and CY7C195, $\overline{CE_1}$, $\overline{CE_2}$ on the CY7C196) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

A die coat is used to ensure alpha immunity.

### Logic Block Diagram




### Pin Configurations




### Selection Guide

| | | 7C194–12 7C195–12 7C196–12 | 7C194–15 7C195–15 7C196–15 | 7C194–20 7C195–20 7C196–20 | 7C194–25 7C195–25 7C196–25 | 7C194–35 7C195–35 7C196–35 | 7C194–45 7C195–45 7C196–45 |
|---|---|---|---|---|---|---|---|
| Maximum Access Time (ns) | | 12 | 15 | 20 | 25 | 35 | 45 |
| Maximum Operating Current (mA) | Commercial | 160 | 150 | 140 | 120 | 120 | 120 |
| | Military | | 160 | 150 | 130 | 130 | 130 |
| Maximum Standby Current (mA) | | 40 | 40 | 40 | 35 | 35 | 35 |

Shaded area contains advanced information.

T-46-23-10

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL−STD−883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature[1] | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Military | −55°C to +125°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range[2]

| Parameters | Description | Test Conditions | | 7C194−12 7C195−12 7C196−12 Min. | 7C194−12 7C195−12 7C196−12 Max. | 7C194−15 7C195−15 7C196−15 Min. | 7C194−15 7C195−15 7C196−15 Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = −4.0 mA | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.2 | $V_{CC}$ | 2.2 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | 0.8 | −0.5 | 0.8 | V |
| $I_{IX}$ | Input Load Current | $GND \le V_I \le V_{CC}$ | | −10 | +10 | −10 | +10 | μA |
| $I_{OZ}$ | Output Leakage Current | $GND \le V_O \le V_{CC}$, Output Disabled | | −10 | +10 | −10 | +10 | μA |
| $I_{OS}$ | Output Short Circuit Current[3] | $V_{CC}$ = Max., $V_{OUT}$ = GND | | | −300 | | −300 | mA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, $f = f_{MAX} = 1/t_{RC}$ | Com'l | | 160 | | 150 | mA |
| | | | Mil | | | | 160 | |
| $I_{SB1}$ | Automatic $\overline{CE}$ Power-Down Current —TTL Inputs[4] | Max. $V_{CC}$, $\overline{CE}_{1,2} \ge V_{IH}$, $V_{IN} \ge V_{IH}$ or $V_{IN} \le V_{IL}$, $f = f_{MAX}$ | | | 40 | | 40 | mA |
| $I_{SB2}$ | Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs[4] | Max. $V_{CC}$, $\overline{CE}_{1,2} \ge V_{CC} - 0.3V$, $V_{IN} \ge V_{CC} - 0.3V$ or $V_{IN} \le 0.3V$, $f = 0$ | | | 20 | | 20 | mA |

Shaded area contains advanced information.

**Notes:**

1. $T_A$ is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to $V_{CC}$ on the $\overline{CE}$ input is required to keep the device deselected during $V_{CC}$ power-up, otherwise $I_{SB}$ will exceed values given.

**Electrical Characteristics** Over the Operating Range[2] (continued)

| Parameters | Description | Test Conditions | | 7C194–20 7C195–20 7C196–20 Min. | 7C194–20 7C195–20 7C196–20 Max. | 7C194–25, 35, 45 7C195–25, 35, 45 7C196–25, 35, 45 Min. | 7C194–25, 35, 45 7C195–25, 35, 45 7C196–25, 35, 45 Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = −4.0 mA | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.2 | $V_{CC}$ | 2.2 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | −0.5 | 0.8 | −3.0 | 0.8 | V |
| $I_{IX}$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | −10 | +10 | −10 | +10 | μA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$, Output Disabled | | −10 | +10 | −10 | +10 | μA |
| $I_{OS}$ | Output Short Circuit Current[3] | $V_{CC}$ = Max., $V_{OUT}$ = GND | | | −350 | | −350 | mA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, f = $f_{MAX}$ = $1/t_{RC}$ | Com'l | | 140 | | 120 | mA |
| | | | Mil | | 150 | | 130 | |
| $I_{SB1}$ | Automatic $\overline{CE}$ Power-Down Current —TTL Inputs[4] | Max. $V_{CC}$, $\overline{CE}_{1,2}$ ≥ $V_{IH}$, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | | | 40 | | 35 | mA |
| $I_{SB2}$ | Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs[4] | Max. $V_{CC}$, $\overline{CE}_{1,2}$ ≥ $V_{CC}$ − 0.3V, $V_{IN}$ ≥ $V_{CC}$ − 0.3V or $V_{IN}$ ≤ 0.3V, f = 0 | | | 20 | | 20 | mA |

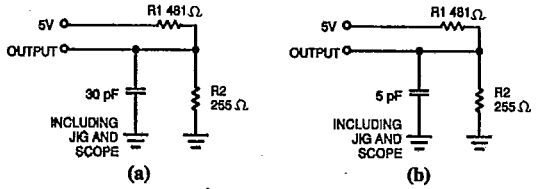
Shaded area contains advanced information.

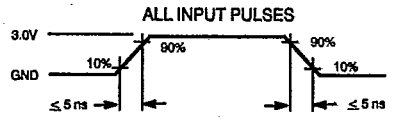
**Capacitance**[5]

| Parameters | Description | Test Conditions | Max. | Units |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

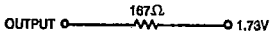
**Note:**
5. Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**




Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics Over the Operating Range[2,6]

| Parameters | Description | | 7C194–12 7C195–12 7C196–12 | | 7C194–15 7C195–15 7C196–15 | | 7C194–20 7C195–20 7C196–20 | | 7C194–25 7C195–25 7C196–25 | | 7C194–35 7C195–35 7C196–35 | | 7C194–45 7C195–45 7C196–45 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | ns |
| $t_{AA}$ | Address to Data Valid | | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | ns |
| $t_{OHA}$ | Output Hold from Address Change | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{ACE1}$, $t_{ACE2}$ | $\overline{CE}$ LOW to Data Valid | | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | 7C195, 7C196 | | 6 | | 8 | | 10 | | 15 | | 20 | | 20 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z | 7C195, 7C196 | 0 | | 0 | | 0 | | 3 | | 3 | | 3 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[8] | 7C195, 7C196 | | 7 | | 8 | | 8 | | 13 | | 15 | | 20 | ns |
| $t_{LZCE1}$, $t_{LZCE2}$ | $\overline{CE}$ LOW to Low Z[7] | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZCE1}$, $t_{HZCE2}$ | $\overline{CE}$ HIGH to High Z[7,8] | | | 7 | | 8 | | 10 | | 13 | | 15 | | 20 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power-Up | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power-Down | | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | ns |
| **WRITE CYCLE[9]** | | | | | | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | | 12 | | 15 | | 20 | | 25 | | 35 | | 45 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | | 9 | | 10 | | 15 | | 20 | | 30 | | 40 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | | 9 | | 10 | | 15 | | 20 | | 25 | | 35 | | ns |
| $t_{HA}$ | Address Hold from Write End | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | | 9 | | 10 | | 15 | | 20 | | 25 | | 30 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | | 7 | | 8 | | 10 | | 15 | | 17 | | 20 | | ns |
| $t_{HD}$ | Data Hold from Write End | | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z[7] | | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[7,8] | | | 7 | | 7 | | 10 | 0 | 13 | 0 | 15 | 0 | 20 | ns |

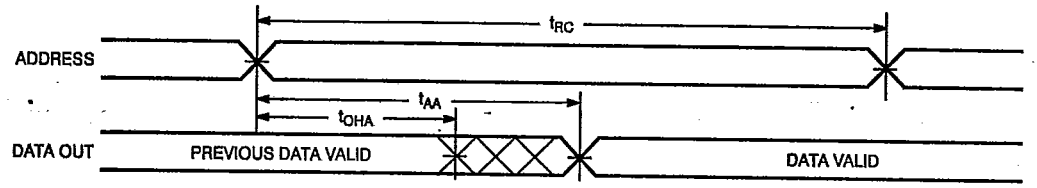
**Notes:**

6. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified $I_{OL}/I_{OH}$ and 30 pF load capacitance.
7. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$ and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
8. $t_{HZOE}$, $t_{HZCE}$, and $t_{HZWE}$ are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
9. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, $\overline{CE}_2$ LOW, and $\overline{WE}$ LOW. All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

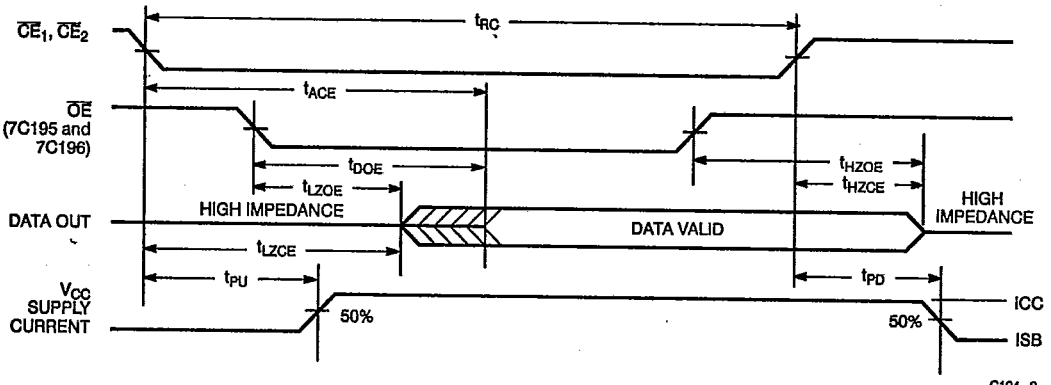
## Switching Waveforms

T-46-23-10

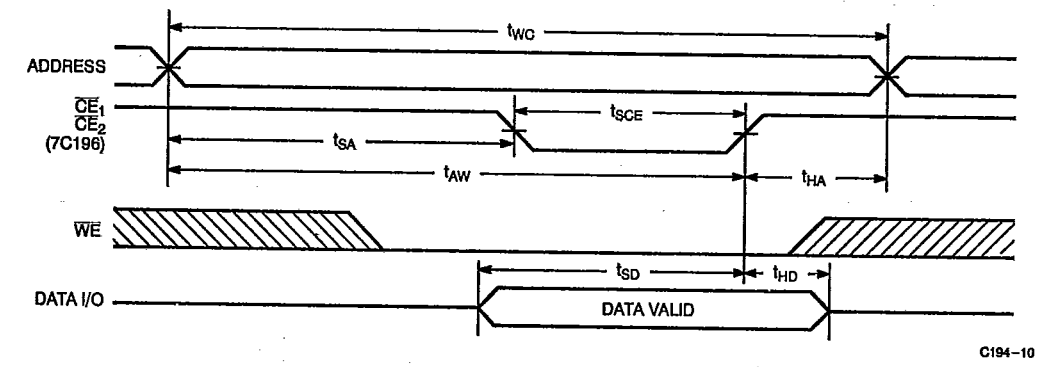
**Read Cycle No. 1**[10, 11]




**Read Cycle No. 2**[10, 12]




**Write Cycle No. 1 ($\overline{CE}$ Controlled)**[9, 13, 14]

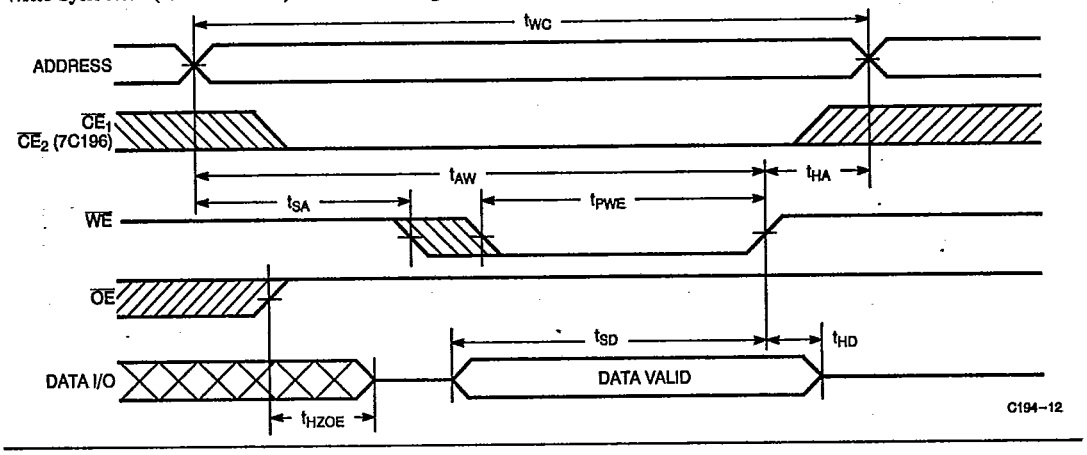



Notes:
10. $\overline{WE}$ is HIGH for read cycle.
11. Device is continuously selected: $\overline{CE}_1 = V_{IL}$, $\overline{CE}_2 = V_{IL}$ (7C196), and $\overline{OE} = V_{IL}$ (7C195 and 7C196).
12. Address valid prior to or coincident with $\overline{CE}_1$ and $\overline{CE}_2$ transition LOW.
13. Data I/O will be high impedance if $\overline{OE} = V_{IH}$ (7C195 and 7C196).
14. If any $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of $t_{HZWE}$ and $t_{SD}$.

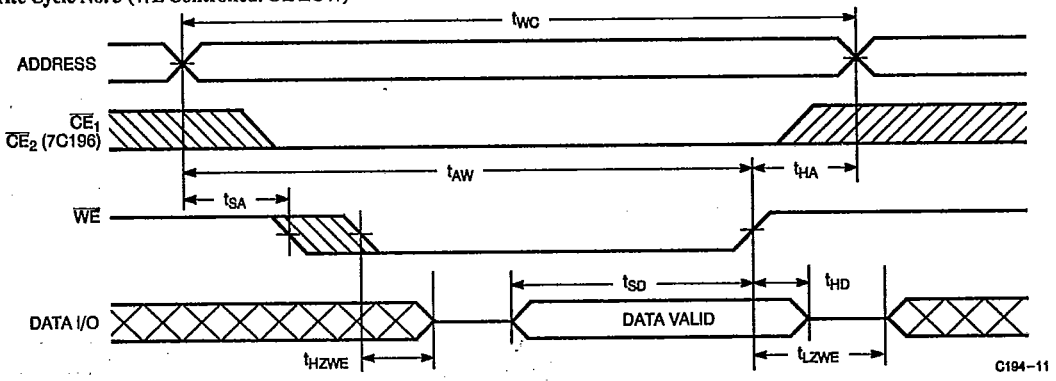
## Switching Waveforms (continued)

T-46-23-10

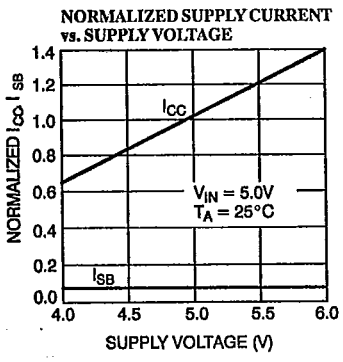
**Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write for 7C195 and 7C196 only)[9, 13, 14]**

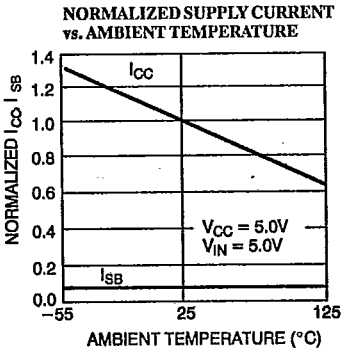


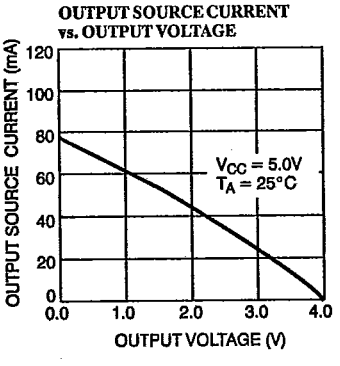

**Write Cycle No. 3 ($\overline{WE}$ Controlled. $\overline{OE}$ LOW)[14, 15]**




## Typical DC and AC Characteristics

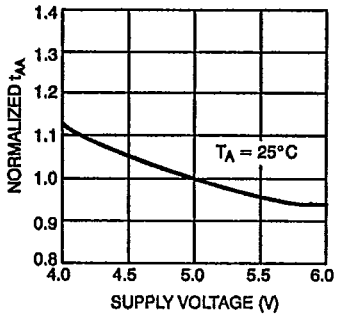


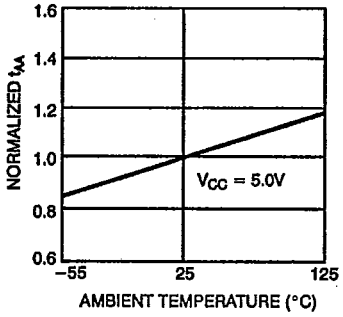



## Typical DC and AC Characteristics (continued)

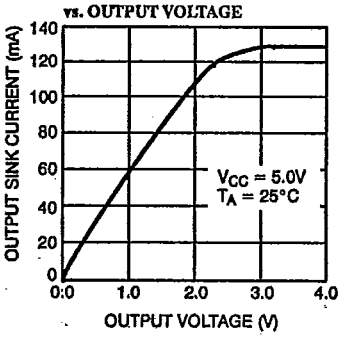
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



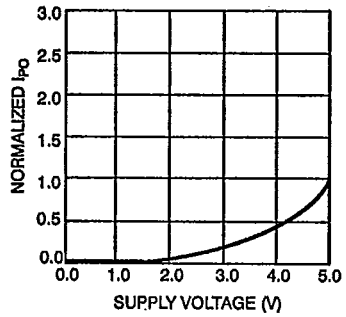

NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



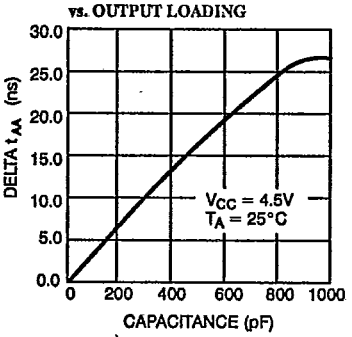

OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



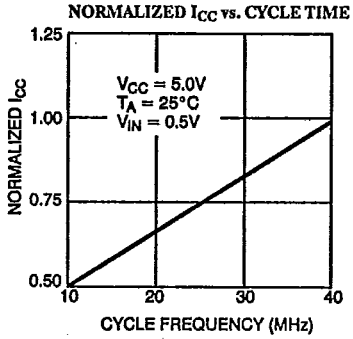

TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE




TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING




NORMALIZED $I_{CC}$ vs. CYCLE TIME




### 7C194 Truth Table

| $\overline{CE}$ | $\overline{WE}$ | Data I/O | Mode | Power |
|---|---|---|---|---|
| H | X | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| L | H | Data Out | Read | Active ($I_{CC}$) |
| L | L | Data In | Write | Active ($I_{CC}$) |

### 7C195 Truth Table

| $\overline{CE_1}$ | $\overline{WE}$ | $\overline{OE}$ | Data I/O | Mode | Power |
|---|---|---|---|---|---|
| H | X | X | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| L | H | L | Data Out | Read | Active ($I_{CC}$) |
| L | L | X | Data In | Write | Active ($I_{CC}$) |
| L | H | H | High Z | Deselect | Active ($I_{CC}$) |

### 7C196 Truth Table

| $\overline{CE_1}$ | $\overline{CE_2}$ | $\overline{WE}$ | $\overline{OE}$ | Data I/O | Mode | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| X | H | X | X | | | |
| L | L | H | L | Data Out | Read | Active ($I_{CC}$) |
| L | L | L | X | Data In | Write | Active ($I_{CC}$) |
| L | L | H | H | High Z | Deselect | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|---|---|---|---|
| 12 | CY7C194–12DC | D14 | Commercial |
| | CY7C194–12LC | L54 | |
| | CY7C194–12PC | P13 | |
| | CY7C194–12VC | V13 | |
| 15 | CY7C194–15DC | D14 | Commercial |
| | CY7C194–15LC | L54 | |
| | CY7C194–15PC | P13 | |
| | CY7C194–15VC | V13 | |
| | CY7C194–15DMB | D14 | Military |
| | CY7C194–15KMB | K73 | |
| | CY7C194–15LMB | L54 | |
| 20 | CY7C194–20DC | D14 | Commercial |
| | CY7C194–20LC | L54 | |
| | CY7C194–20PC | P13 | |
| | CY7C194–20VC | V13 | |
| | CY7C194–20DMB | D14 | Military |
| | CY7C194–20KMB | K73 | |
| | CY7C194–20LMB | L54 | |
| 25 | CY7C194–25DC | D14 | Commercial |
| | CY7C194–25LC | L54 | |
| | CY7C194–25PC | P13 | |
| | CY7C194–25VC | V13 | |
| | CY7C194–25DMB | D14 | Military |
| | CY7C194–25KMB | K73 | |
| | CY7C194–25LMB | L54 | |
| 35 | CY7C194–35DC | D14 | Commercial |
| | CY7C194–35LC | L54 | |
| | CY7C194–35PC | P13 | |
| | CY7C194–35VC | V13 | |
| | CY7C194–35DMB | D14 | Military |
| | CY7C194–35KMB | K73 | |
| | CY7C194–35LMB | L54 | |
| 45 | CY7C194–45DC | D14 | Commercial |
| | CY7C194–45LC | L54 | |
| | CY7C194–45PC | P13 | |
| | CY7C194–45VC | V13 | |
| | CY7C194–45DMB | D14 | Military |
| | CY7C194–45KMB | K73 | |
| | CY7C194–45LMB | L54 | |

Shaded area contains advanced information.

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|---|---|---|---|
| 12 | CY7C195–12DC | D22 | Commercial |
| | CY7C195–12LC | L54 | |
| | CY7C195–12PC | P21 | |
| | CY7C195–12VC | V21 | |
| 15 | CY7C195–15DC | D22 | Commercial |
| | CY7C195–15LC | L54 | |
| | CY7C195–15PC | P21 | |
| | CY7C195–15VC | V21 | |
| | CY7C195–15DMB | D22 | Military |
| | CY7C195–15KMB | K74 | |
| | CY7C195–15LMB | L54 | |
| 20 | CY7C195–20DC | D22 | Commercial |
| | CY7C195–25LC | L54 | |
| | CY7C195–20PC | P21 | |
| | CY7C195–20VC | V21 | |
| | CY7C195–20DMB | D22 | Military |
| | CY7C195–20KMB | K74 | |
| | CY7C195–20LMB | L54 | |
| 25 | CY7C195–25DC | D22 | Commercial |
| | CY7C195–25LC | L54 | |
| | CY7C195–25PC | P21 | |
| | CY7C195–25VC | V21 | |
| | CY7C195–25DMB | D22 | Military |
| | CY7C195–25KMB | K74 | |
| | CY7C195–25LMB | L54 | |
| 35 | CY7C195–35DC | D22 | Commercial |
| | CY7C195–35LC | L54 | |
| | CY7C195–35PC | P21 | |
| | CY7C195–35VC | V21 | |
| | CY7C195–35DMB | D22 | Military |
| | CY7C195–35KMB | K74 | |
| | CY7C195–35LMB | L54 | |
| 45 | CY7C195–45DC | D22 | Commercial |
| | CY7C195–45LC | L54 | |
| | CY7C195–45PC | P21 | |
| | CY7C195–45VC | V21 | |
| | CY7C195–45DMB | D22 | Military |
| | CY7C195–45KMB | K74 | |
| | CY7C195–45LMB | L54 | |

Shaded area contains advanced information.

## Ordering Information (continued)

| Speed (ns) | Ordering Code | Package Type | Operating Range |
|---|---|---|---|
| 12 | CY7C196–12DC | D22 | Commercial |
| | CY7C196–12LC | L54 | |
| | CY7C196–12PC | P21 | |
| | CY7C196–12VC | V21 | |
| 15 | CY7C196–15DC | D22 | Commercial |
| | CY7C196–15LC | L54 | |
| | CY7C196–15PC | P21 | |
| | CY7C196–15VC | V21 | |
| | CY7C196–15DMB | D22 | Military |
| | CY7C196–15KMB | K74 | |
| | CY7C196–15LMB | L54 | |
| 20 | CY7C196–20DC | D22 | Commercial |
| | CY7C196–20LC | L54 | |
| | CY7C196–20PC | P21 | |
| | CY7C196–20VC | V21 | |
| | CY7C196–20DMB | D22 | Military |
| | CY7C196–20KMB | K74 | |
| | CY7C196–20LMB | L54 | |
| 25 | CY7C196–25DC | D22 | Commercial |
| | CY7C196–25LC | L54 | |
| | CY7C196–25PC | P21 | |
| | CY7C196–25VC | V21 | |
| | CY7C196–25DMB | D22 | Military |
| | CY7C196–25KMB | K74 | |
| | CY7C196–25LMB | L54 | |
| 35 | CY7C196–35DC | D22 | Commercial |
| | CY7C196–35LC | L54 | |
| | CY7C196–35PC | P21 | |
| | CY7C196–35VC | V21 | |
| | CY7C196–35DMB | D22 | Military |
| | CY7C196–35KMB | K74 | |
| | CY7C196–35LMB | L54 | |
| 45 | CY7C196–45DC | D22 | Commercial |
| | CY7C196–45LC | L54 | |
| | CY7C196–45PC | P21 | |
| | CY7C196–45VC | V21 | |
| | CY7C196–45DMB | D22 | Military |
| | CY7C196–45KMB | K74 | |
| | CY7C196–45LMB | L54 | |

Shaded area contains advanced information.

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

### DC Characteristics

| Parameters | Subgroups |
|---|---|
| $V_{OH}$ | 1, 2, 3 |
| $V_{OL}$ | 1, 2, 3 |
| $V_{IH}$ | 1, 2, 3 |
| $V_{IL}$ Max. | 1, 2, 3 |
| $I_{IX}$ | 1, 2, 3 |
| $I_{OZ}$ | 1, 2, 3 |
| $I_{OS}$ | 1, 2, 3 |
| $I_{CC}$ | 1, 2, 3 |
| $I_{SB1}$ | 1, 2, 3 |
| $I_{SB2}$ | 1, 2, 3 |

### Switching Characteristics

| Parameters | Subgroups |
|---|---|
| **READ CYCLE** | |
| $t_{RC}$ | 7, 8, 9, 10, 11 |
| $t_{AA}$ | 7, 8, 9, 10, 11 |
| $t_{OHA}$ | 7, 8, 9, 10, 11 |
| $t_{ACE}$, $_{ACE2}$ | 7, 8, 9, 10, 11 |
| $t_{DOE}$[16] | 7, 8, 9, 10, 11 |
| **WRITE CYCLE** | |
| $t_{WC}$ | 7, 8, 9, 10, 11 |
| $t_{SCE}$ | 7, 8, 9, 10, 11 |
| $t_{AW}$ | 7, 8, 9, 10, 11 |
| $t_{HA}$ | 7, 8, 9, 10, 11 |
| $t_{SA}$ | 7, 8, 9, 10, 11 |
| $t_{PWE}$ | 7, 8, 9, 10, 11 |
| $t_{SD}$ | 7, 8, 9, 10, 11 |
| $t_{HD}$ | 7, 8, 9, 10, 11 |

**Note:**
16. 7C195 and 7C196 only.

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