

LOW VOLTAGE 0.5Ω MAX DUAL SPDT SWITCH, SINGLE ENABLE WITH BREAK BEFORE MAKE FEATURE

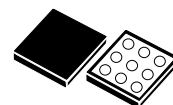
PRELIMINARY DATA

- HIGH SPEED:
 $t_{PD} = 0.3ns$ (TYP.) at $V_{CC} = 3.0V$
 $t_{PD} = 0.4ns$ (TYP.) at $V_{CC} = 2.3V$
- ULTRA LOW POWER DISSIPATION:
 $I_{CC} = 0.2\mu A$ (MAX.) at $T_A = 85^\circ C$
- LOW "ON" RESISTANCE $V_I = 0V$:
 $R_{ON} = 0.4\Omega$ (MAX. $T_A = 25^\circ C$) at $V_{CC} = 4.2V$
 $R_{ON} = 0.5\Omega$ (MAX. $T_A = 25^\circ C$) at $V_{CC} = 3.0V$
 $R_{ON} = 0.6\Omega$ (MAX. $T_A = 25^\circ C$) at $V_{CC} = 2.3V$
- WIDE OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 1.4V to 4.3V SINGLE SUPPLY
- 4.3V TOLERANT AND 1.8V COMPATIBLE THRESHOLD ON DIGITAL CONTROL INPUT at $V_{CC} = 2.3$ to 4.3V
- LATCH-UP PERFORMANCE EXCEEDS 300mA (JESD 17)
- ESD PERFORM. (ANALOG CHAN. vs GND):
HBM > 4KV (MIL STD 883 method 3015)

DESCRIPTION

The STG3685 is an high-speed CMOS DUAL ANALOG S.P.D.T. (Single Pole Dual Throw) SWITCH or DUAL 2:1 Multiplexer/Demultiplexer Bus Switch fabricated in silicon gate C²MOS technology. It is designed to operate from 1.4V to 4.3V, making this device ideal for portable applications.

It offers very low ON-Resistance (<0.5Ω) at $V_{CC}=3.0V$. The IN input is provided to control the switches. The switches nS1 are ON (they are



Flip-Chip

Table 1: Order Codes

PACKAGE	T & R
Flip-Chip9	STG3685BJR

connected to common Ports Dn) when the IN input is held high and OFF (high impedance state exists between the two ports) when IN is held low; the switches nS2 are ON (they are connected to common Ports Dn) when the IN input is held low and OFF (high impedance state exists between the two ports) when IN is held high. Additional key features are fast switching speed, Break Before Make Delay Time and Ultra Low Power Consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage. It's available in the commercial temperature range Flip-chip package with Epoxy Protection.

Figure 1: Pin Connection (Top Through View) And Schematic Circuit

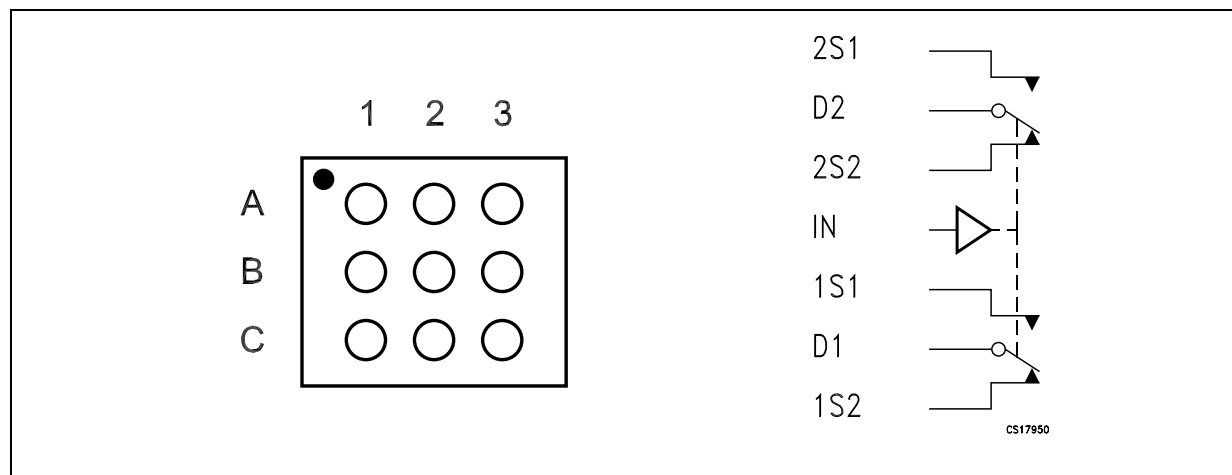


Figure 2: Input Equivalent Circuit

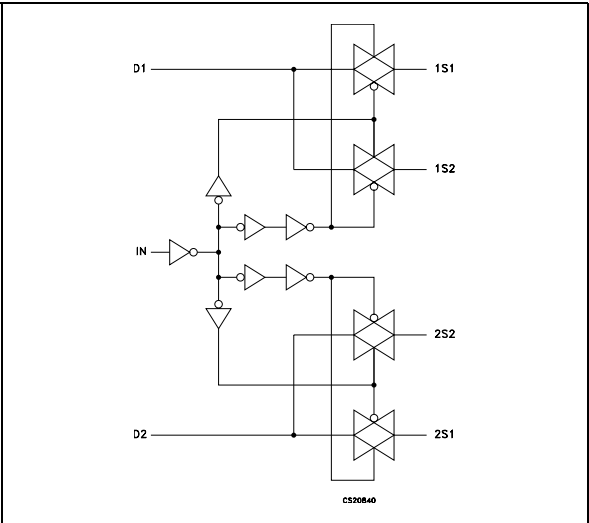


Table 2: Pin Description

PIN N°	SYMBOL	NAME AND FUNCTION
B2	IN	Control
A3, A1 C3, C1	2S1, 1S1 2S2, 1S2	Independent Channels
B3, B1	D2, D1	Common Channels
C2	GND	Ground (0V)
A2	V _{CC}	Positive Supply Voltage

Table 3: Truth Table

IN	SWITCH S1	SWITCH S2
H	ON	OFF(*)
L	OFF(*)	ON

(*) High Impedance

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to 4.6	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _{IC}	DC Control Input Voltage	-0.5 to 4.6	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IKC}	DC Input Diode Current on control pin (V _{IN} < 0V)	– 50	mA
I _{IK}	DC Input Diode Current (V _{IN} < 0V)	± 50	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 300	mA
I _{OP}	DC Output Current Peak (pulse at 1ms, 10% duty cycle)	± 500	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 100	mA
P _D	Power Dissipation at T _a =70°C (1)	TBD	mW
T _{stg}	Storage Temperature	-65 to 150	°C
T _L	Lead Temperature (10 sec)	260	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(1) Derate above 70°C: by 18.5mW/°C.

Table 5: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V _{CC}	Supply Voltage (note 1)		1.4 to 4.3	V
V _I	Input Voltage		0 to V _{CC}	V
V _{IC}	Control Input Voltage		0 to 4.3	V
V _O	Output Voltage		0 to V _{CC}	V
T _{op}	Operating Temperature		-55 to 125	°C
dt/dv	Input Rise and Fall Time Control Input	V _{CC} = 1.4V to 2.7V	0 to 20	ns/V
		V _{CC} = 3.0V to 3.6V	0 to 10	

1) Truth Table guaranteed: 1.2V to 4.3V.

Table 6: DC Specifications

Symbol	Parameter	Test Conditions		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	1.65-1.95		0.65V _{CC}			0.65V _{CC}		0.65V _{CC}		V
		2.3-2.5		1.4			1.4		1.4		
		2.7-3.0		1.4			1.4		1.4		
		3.3		1.5			1.5		1.5		
		3.6		1.6			1.6		1.6		
		4.3		1.6			1.6		1.6		
V _{IL}	Low Level Input Voltage	1.65-1.95				0.40		0.40		0.40	V
		2.3-2.5				0.50		0.50		0.50	
		2.7-3.6				0.50		0.50		0.50	
		3.3				0.50		0.50		0.50	
		3.6				0.50		0.50		0.50	
		4.3				0.50		0.50		0.50	
R _{ON}	Switch ON Resistance (See Fig. 12)	4.3	V _S =0V to V _{CC} I _S =100mA		250	400		500			mΩ
		3.0			300	500		600			
		2.7			300	500		600			
		2.3			350	600		800			
		1.8			550	2000		4000			
		1.4			1200	2500		5000			
R _{FLAT}	ON Resistance FLATNESS (1)	4.3	V _S =0 to V _{CC} I _S =100mA								Ω
		3.0									
		2.7			0.07	0.15		0.15			
		2.3									
		1.65									
I _{OFF}	OFF State Leakage Current (nSn), (Dn)	4.3	V _S =0.3 or 4V			±10		± 100			nA
I _{IN}	Input Leakage Current	0 - 4.3	V _{IN} =0 to 4.3V			±0.1		± 1			μA
I _{CCL}	Quiescent Supply Current	1.65-4.3	V _{IN} =V _{CC} or GND			±0.05		±0.2		±1	μA
I _{CCH}	Quiescent Supply Current	4.2	V _{IN} =1.65V		415	500					μA
			V _{IN} =1.8V		360	400					
			V _{IN} =2.6V		120	150					

Note 1: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Table 7: AC Electrical Characteristics ($C_L = 35\text{pF}$, $R_L = 50\Omega$, $t_r = t_f \leq 5\text{ns}$)

Symbol	Parameter	Test Condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
t _{PLH} , t _{PHL}	Propagation Delay	1.65-1.95			0.45							ns
		2.3-2.7			0.40							
		3.0-3.6			0.30							
		3.6-4.3			0.30							
t _{ON}	TURN-ON time	1.65-1.95	V _S =0.8V		70							ns
		2.3-2.7	V _S =1.5V		32	50		60				
		3.0-3.6			32	50		60				
		3.6-4.3			30	50		60				
t _{OFF}	TURN-OFF time	1.65-1.95	V _S =0.8V		45							ns
		2.3-2.7	V _S =1.5V		25	30		40				
		3.0-3.6			15	30		40				
		3.6-4.3			15	30		40				
t _D	Break Before Make Time Delay	1.65-1.95	C _L =35pF R _L = 50Ω V _S =1.5V									ns
		2.3-2.7		2	15							
		3.0-3.6		2	15							
		3.6-4.3		2	15							
Q	Charge injection	1.65-1.95	C _L = 100pF									pC
		2.3-2.7	R _L = 1MΩ		200							
		3.0-3.6	V _{GEN} = 0V		200							
		3.6-4.3	R _{GEN} = 0Ω		200							

Table 8: Analog Switch Characteristics ($C_L = 5\text{pF}$, $R_L = 50\Omega$, $T_A = 25^\circ\text{C}$)

Symbol	Parameter	Test Condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
OIRR	Off Isolation (1)	1.65-4.3	V _S = 1V _{RMS} f= 100KHz		-64						dB	
Xtalk	Crosstalk	1.65-4.3	V _S = 1V _{RMS} f= 100KHz		-32						dB	
THD	Total Harmonic Distortion	2.3-4.3	R _L = 600Ω V _I = 2V _{PP} f = 20Hz to 20kHz		0.03						%	
BW	-3dB Bandwidth	1.65-4.3	R _L = 50Ω		50						MHz	
C _{IN}	Control Pin Input Capacitance				10						pF	
C _{Sn}	Sn Port Capacitance	3.3	f = 1MHz		35							
C _D	D Port Capacitance when Switch is Enabled	3.3	f = 1MHz		91							

Note 1: Off Isolation = $20\text{Log}_{10}(V_D/V_S)$, V_D = output. V_S = input at off switch.

Figure 3: On Resistance

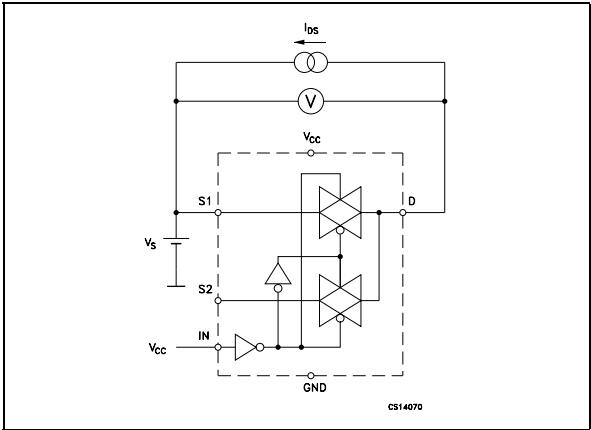


Figure 6: Bandwidth

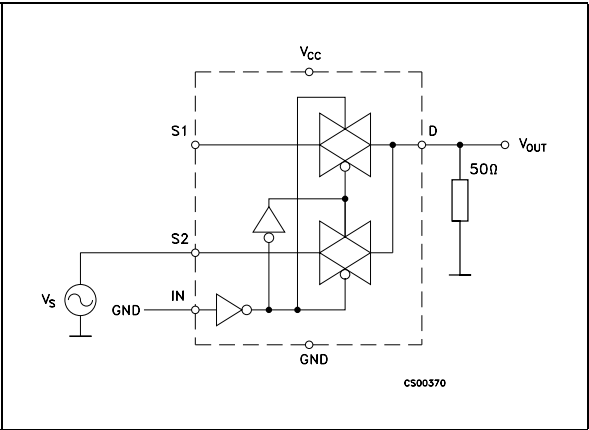


Figure 4: Off Leakage

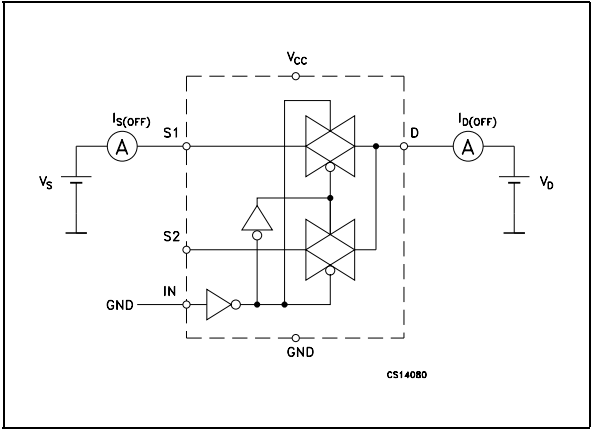


Figure 7: Channel To Channel Crosstalk

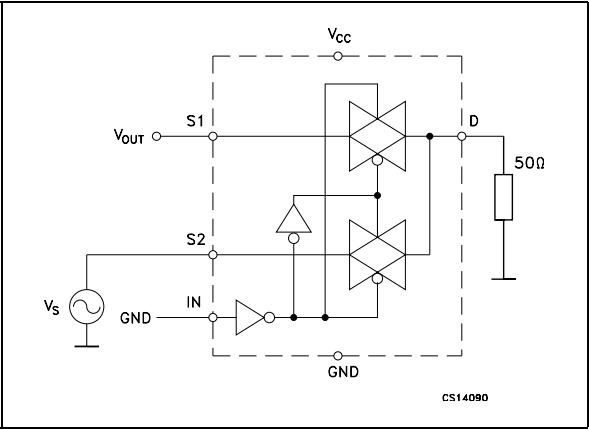


Figure 5: Off Isolation

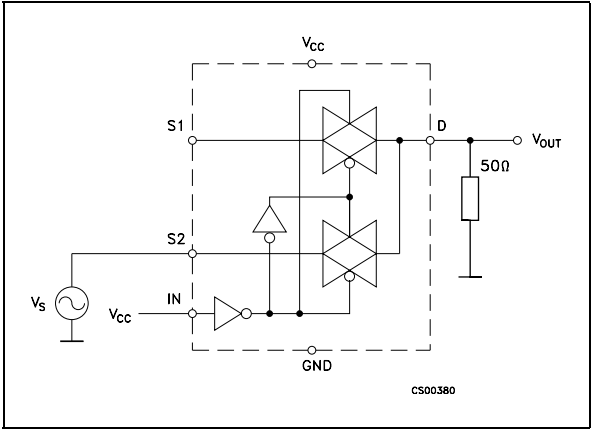
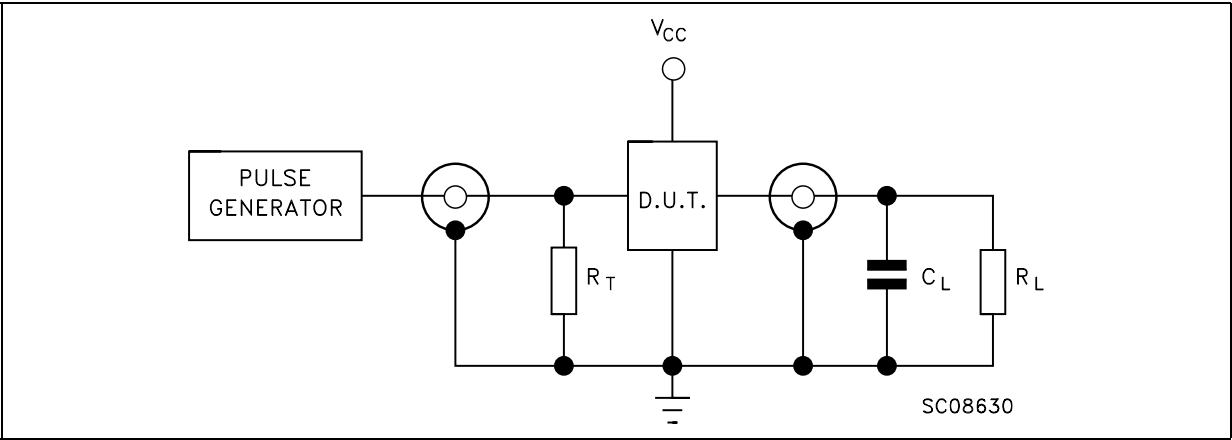


Figure 8: Test Circuit



$C_L = 5/35\text{pF}$ or equivalent (includes jig and probe capacitance)
 $R_L = 50\Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 9: Break Before Make Time Delay

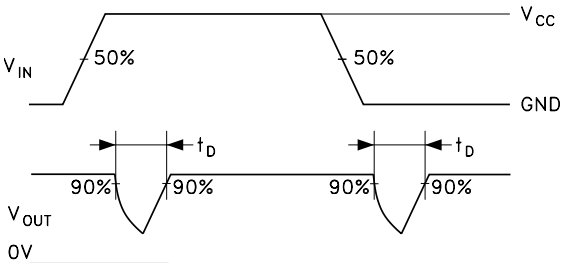
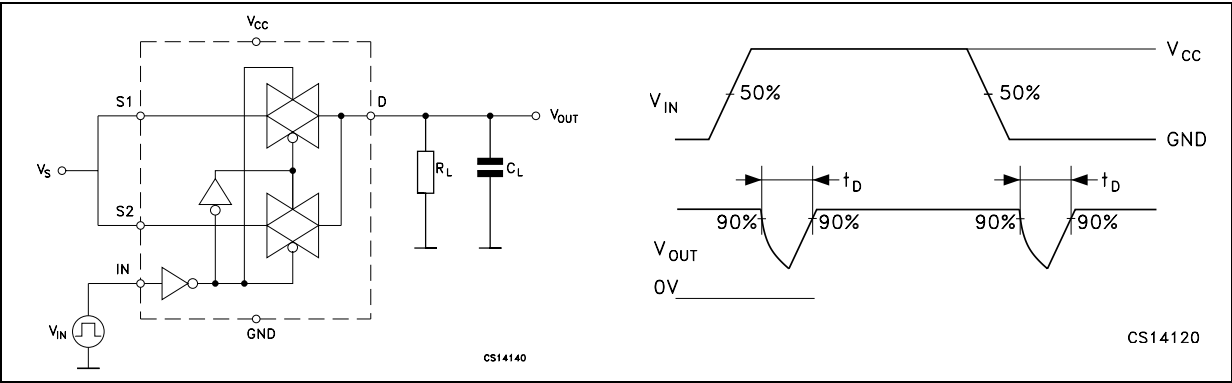


Figure 10: Charge Injection ($V_{GEN} = 0\text{V}$, $R_{GEN} = 0\Omega$, $R_L = 1\text{M}\Omega$, $C_L = 100\text{pF}$)

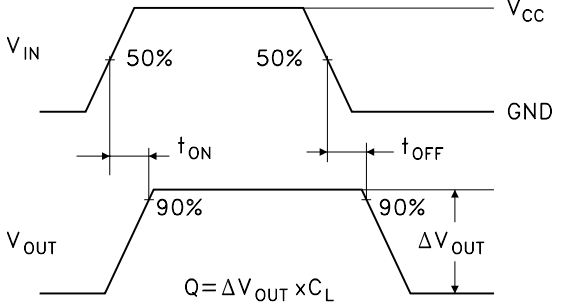
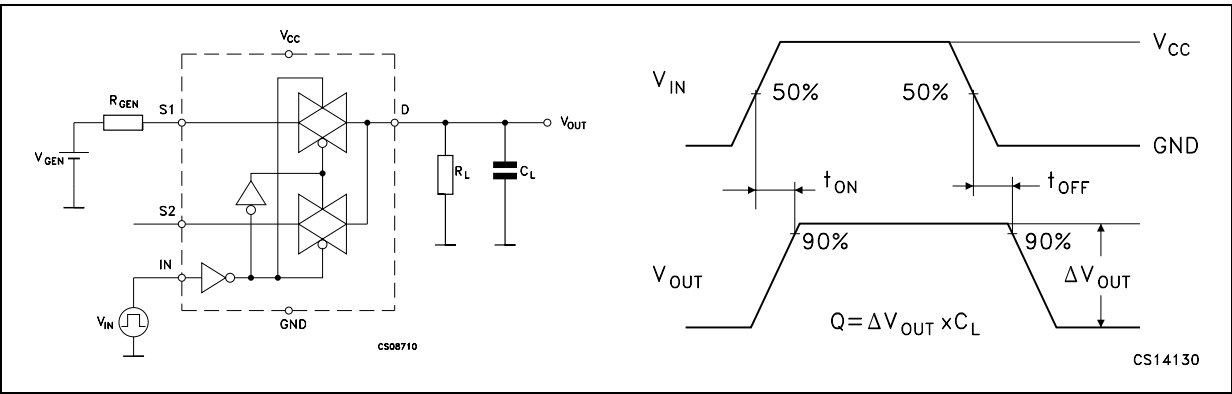
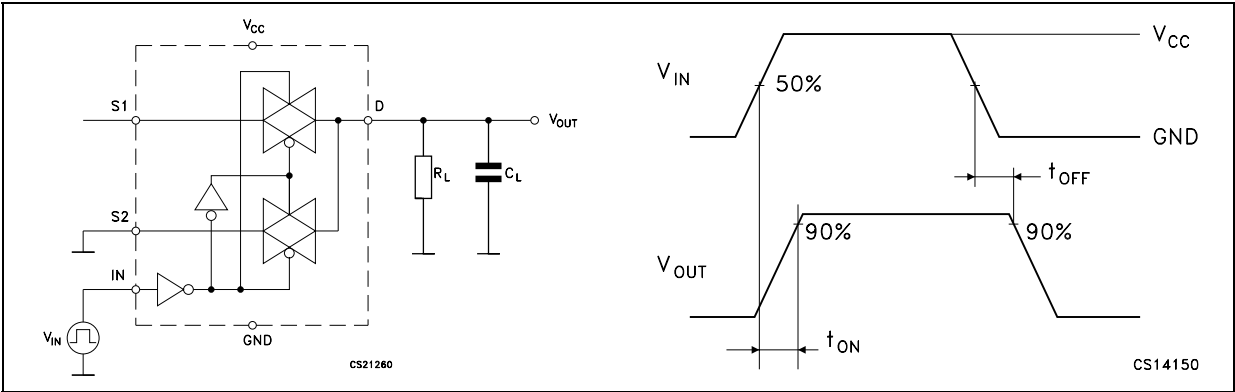
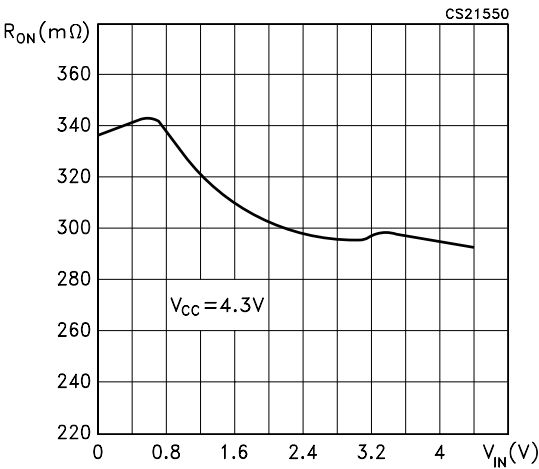


Figure 11: Turn On, Turn Off Delay Time



TYPICAL CHARACTERISTICS

Figure 12: Switch-On R_{ON} vs V_{IN}



Flip-Chip9 MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.59	1.64	1.69	62.6	64.6	66.5
B	1.42	1.47	1.52	55.9	57.9	59.8
C			0.80			31.5
D	0.295	0.32	0.345	11.6	12.6	13.6
E		0.5			19.7	
F	0.35	0.40	0.45	13.8	15.7	17.7
G		0.25			9.8	
H	0.061	0.0635	0.066	2.4	2.5	2.6

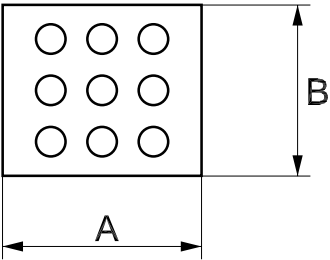
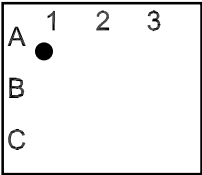
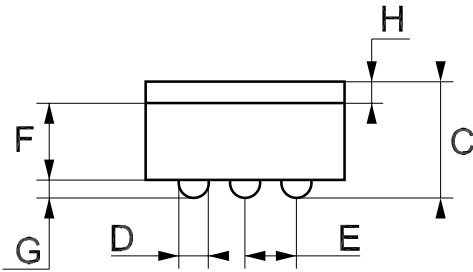


Table 9: Revision History

Date	Revision	Description of Changes
13-Jan-2005	1	First Release.

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