

XtremeDSP™ Development Platform: Spartan-3A DSP 3400A Edition

User Guide

UG498 (v2.2) November 17, 2008





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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
6/2007	0.1	Preliminary version.
7/2007	0.2	Added appendix.
7/2007	0.3	Updated version for final review.
8/2007	1.0	• Updated FMC information. • Updated support information. • Added FPGA pin assignments for DDR2 interface. • Added FPGA pin assignments for USB/System ACE interface.
9/2007	1.1	Added Known Issues section: Limitation of DDR2 clock rate to 133 MHz; Soft Touch connector not compliant with Agilent probes; FMC connector is in violation of some rules of the standard.
10/2007	1.2	• Updated Table 20 (Serial Port FPGA Pin Assignments) and modified layout to reflect change in corporate image. • Updated for XtremeDSP Spartan-3A DSP Development Board Revision D.
10/2007	2.0	Updated for XtremeDSP Spartan-3A DSP Development Board Revision.
1/2008	2.1	Updated with new clock generator configuration.
11/17/08	2.2	• Ported to Xilinx template. • Updated Table 12 (FMC Pin G3 is attached to net 1_CLK0_C2M_N). • Updated to account for PS6 being the power supply used for FMC 2 adjustable voltage.

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About This Guide

The *XtremeDSP™ Development Platform: Spartan-3A DSP 3400A Edition User Guide* provides instructions for designing and accelerating the development of new products. The XtremeDSP Development Platform: Spartan-3A DSP 3400A Edition board is an excellent medium for consumer-oriented wireless and multimedia video applications, where cost-efficient solutions are essential. Throughout the remainder of this guide, the development board may be referred to as both the XtremeDSP Development Platform: Spartan-3A DSP 3400A Edition board and the Spartan-3A DSP 3400A Edition board.

Guide Contents

The User Guide contains the following chapters:

- [Preface, “About this Guide”](#) introduces the organization and purpose of the User Guide and the conventions used in this document.
- [Chapter 1, “Introduction,”](#) identifies the major components, parts, and functionality of the Spartan-3A DSP 3400A Edition board.
- [Chapter 2, “Configuration Options,”](#) provides an overview of the four configuration methods available on the FPGA on the Spartan-3A DSP 3400A Edition board.
- [Chapter 3, “Programming the IDT Clock Chip,”](#) provides step-by-step instructions for using the IDT software to generate a combination of clock frequencies and implement them on the development board.
- [Appendix, “Technical Specifications,”](#) identifies the Spartan-3A DSP 3400A Edition board technical specifications.

Additional Resources

To find additional documentation, see the Xilinx website at:

www.xilinx.com/support/documentation

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support WebCase, see the Xilinx website at:

<http://www.xilinx.com/support>.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
Courier font	Messages, prompts, and program files that the system displays	<code>speed grade: - 100</code>
Courier bold	Literal commands that you enter in a syntactical statement	ngdbuild <i>design_name</i>
<i>Italic font</i>	References to other manuals	See the <i>Development System Reference Guide</i> for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are <i>not</i> connected.
Square brackets []	An optional entry or parameter. However, in bus specifications, such as bus [7:0] , they are required.	ngdbuild [<i>option_name</i>] <i>design_name</i>
Braces { }	A list of items from which you must choose one or more	lowpwr = { on off }
Vertical bar	Separates items in a list of choices	lowpwr = { on off }
Vertical ellipsis . . .	Repetitive material that has been omitted	IOB #1: Name = QOUT' IOB #2: Name = CLKIN' . . .
Horizontal ellipsis ...	Repetitive material that has been omitted	allow block <i>block_name loc1 loc2 ... locn</i> ;

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section “Additional Resources” for details. Refer to “Title Formats” in Chapter 1 for details.

Convention	Meaning or Use	Example
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the <i>Virtex-II Platform FPGA User Guide</i> .
<u>Blue, underlined text</u>	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Introduction

This chapter identifies the major components, parts, and functionality of the Spartan-3A DSP 3400A Edition board.

Spartan-3A DSP 3400A Edition Board Overview

Figure 1-1 displays a block diagram of the Spartan-3A DSP 3400A Edition board.

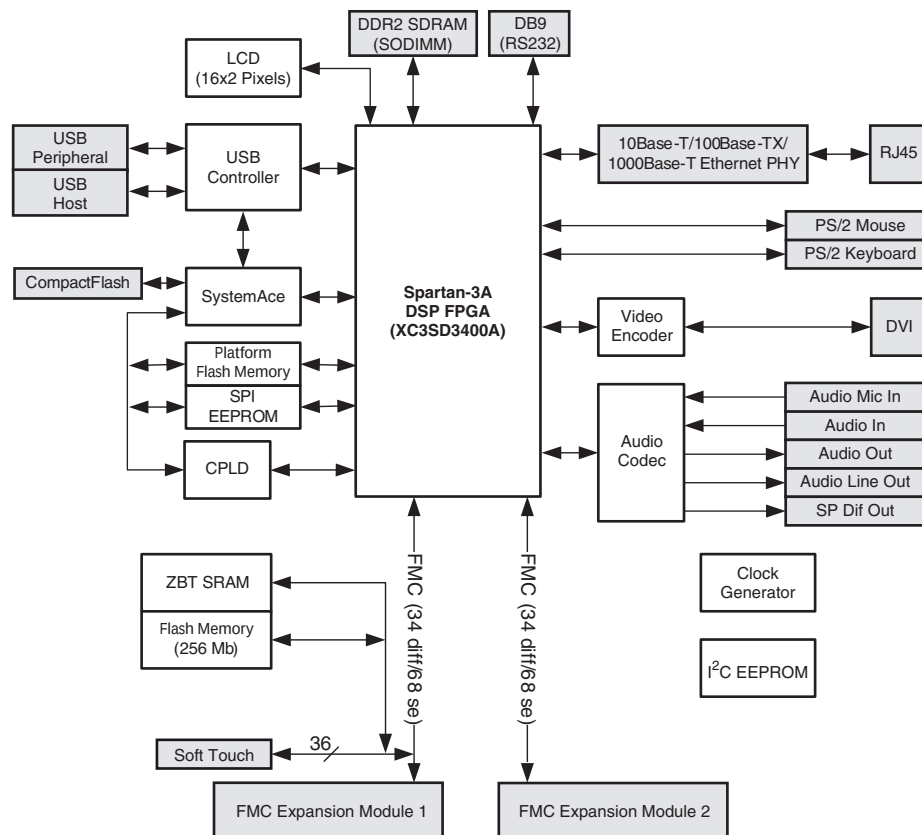


Figure 1-1: Spartan-3A DSP 3400A Edition Board Block Diagram

Spartan-3A DSP 3400A Edition Board Hardware

Board Parts: Top

Figure 1-2 illustrates the parts on the top of the Spartan-3A DSP 3400A Edition board. Each numbered item in the diagram is followed by a numbered description.

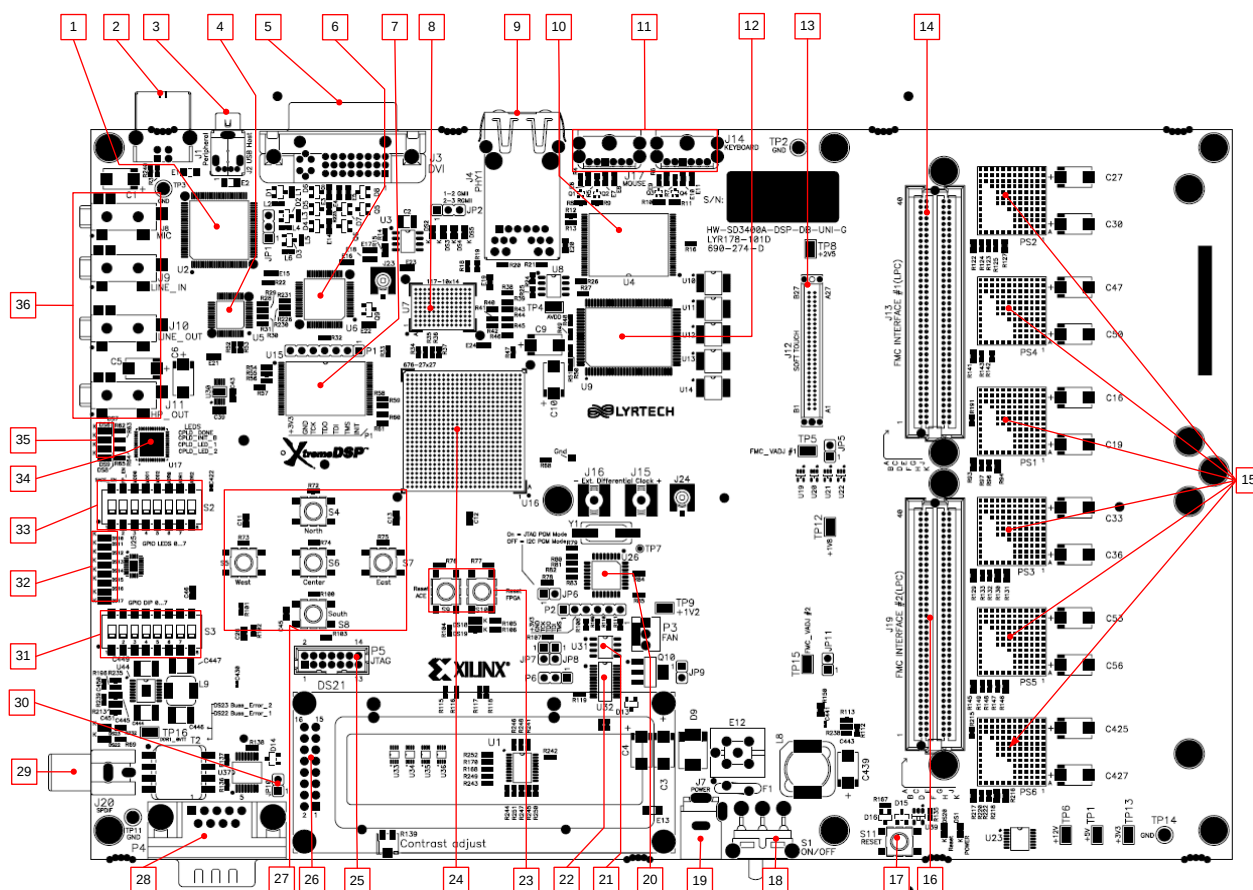


Figure 1-2: Top View of Spartan-3A DSP 3400A Edition Board

Individual Board Parts

1. USB Controller

The Cypress CY7C67300 embedded USB host controller provides high-speed USB connectivity for the board, and supports host and peripheral modes of operation (see “2. USB Peripheral Port” and “3. USB Host Port”). The USB controller also has two Serial Interface Engines (SIE) that can be used independently. SIE1 is connected to the USB host port (“3. USB Host Port”), and SIE2 is connected to the USB peripheral port (“2. USB Peripheral Port”).

The USB controller is equipped with an internal microprocessor to assist in processing USB commands. The firmware for this processor can be stored in its dedicated I²C EEPROM (U41) or downloaded from a host computer through the USB peripheral port (below). Jumper JP1 can be installed (shorting pins 1 and 2) to prevent the USB controller from executing firmware stored in the I²C EEPROM. The FPGA pins used for the USB interface are shared with the System ACE interface, as identified in Table 1-1.

Table 1-1: USB/System ACE Interface Pin Assignments

FPGA Pin	Description	FPGA Pin	Description
AE13	sysace_clk_in (System ACE only)	Y17	sace_usb_d_0
AE23	sace_mpce (System ACE only)	AD21	sace_usb_d_1
AA18	sysace_mpbready (System ACE only)	AA17	sace_usb_d_2
AB18	sysace_mpirq (System ACE only)	AE21	sace_usb_d_3
W17	usb_csn (USB only)	V16	sace_usb_d_4
AA9	usb_int (USB only)	AC20	sace_usb_d_5
AD22	usb_reset (USB only)	AD20	sace_usb_d_6
AC21	sace_usb_oen	U16	sace_usb_d_7
V17	sace_usb_wen	AF20	sace_usb_d_8
AF4	sace_usb_a_0	AE20	sace_usb_d_9
W9	sace_usb_a_1	AC19	sace_usb_d_10
Y9	sace_usb_a_2	AF19	sace_usb_d_11
AE3	sace_usb_a_3	AE19	sace_usb_d_12
AF3	sace_usb_a_4	AD19	sace_usb_d_13
V15	sace_usb_a_5	AC16	sace_usb_d_14
U15	sace_usb_a_6	AB16	sace_usb_d_15

2. USB Peripheral Port

Type B connector, used to connect peripheral USB devices to the Spartan-3A DSP 3400A Edition board.

3. USB Host Port

Type A connector, used to connect a host device to the Spartan-3A DSP 3400A Edition board.

4. AC'97 SoundMAX Codec

Analog Devices AD1981B. The device supports 16-bit stereo audio and sampling rates up to 48 kHz. The sampling rate for recording and playback can also be different.

[Table 1-2](#) defines the pin assignments.

Table 1-2: AC'97 SoundMAX Codec Interface Pin Assignments

FPGA Pin	Description
AC14	CODEC_BIT_CLK
AC15	CODEC_RESET_B
AB6	CODEC_SDATA_IN
AD14	CODEC_SDATA_OUT
W15	CODEC_SYNC

5. DVI Connector

Used to connect an external video monitor (DVI or VGA) to the Spartan-3A DSP 3400A Edition board. [Table 1-3](#) defines the pin assignments.

Note: The VGA monitor can be connected to the development board with a DVI-to-VGA adaptor (sold separately).

Table 1-3: DVI Interface Pin Assignments

FPGA Pin	Description	FPGA Pin	Description
AE7	DVI_D_0	V10	DVI_D_10
AE6	DVI_D_1	U11	DVI_D_11
AC8	DVI_D_2	AD17	DVI_DE
AD7	DVI_D_3	AF25	DVI_GPOI1
AB7	DVI_D_4	AC11	DVI_H
AF5	DVI_D_5	AD15	DVI_RESET_B
AA10	DVI_D_6	AD11	DVI_V
W10	DVI_D_7	AC12	DVI_XCLK_N
Y10	DVI_D_8	AB12	DVI_XCLK_P
V11	DVI_D_9		

6. Display Controller Device

The DVI circuitry uses a Chronitel CH7301C capable of 24-bit color and 1600 × 1200-pixel resolution. The display controller device drives the digital and analog signals to the DVI connector ("[5. DVI Connector](#)"). The display controller device is controlled through the I²C bus.

The DVI connector supports the I²C protocol, allowing the development board to read monitor configuration parameters, which can then be read by the FPGA through the I²C bus. See "[I²C Bus Addressing](#)," [page 42](#) for detailed information.

7. Board Flash PROM

Xilinx XCF32P. This flash PROM is used to program the development board FPGA. The flash PROM can hold up to two distinct configuration images (up to four compressed configuration images) that can be accessed through the configuration DIP switches. Requires that you use the same configuration DIP switches to configure the FPGA from the platform flash PROM. See “33. Configuration DIP Switches” for detailed information.

8. Ethernet PHY

Marvell Alaska 88E1111 PHY device. This PHY supports 10Base-T, 100Base-TX, and 1000Base-T (Gigabit) Ethernet. The PHY is connected to the board's Ethernet connector (“9. Ethernet Port”). The Ethernet PHY is initialized under its default configuration when the development board is turned on or reset. Jumper JP2 selects whether the PHY's default is RGMII mode (pins 2-3) or GMII mode (pins 1-2). Table 1-4 defines the default configuration of the Ethernet PHY, which can be modified through software. Table 1-5 identifies the FPGA pin assignments for building new FPGA files.

Table 1-4: Default Ethernet PHY Configuration

Configuration Pin	Board Connection	Bit 2	Bit 1	Bit 0
CONFIG0	V _{cc} 2.5 V	PHYADR[2] = 1	PHYADR[1] = 1	PHYADR[0] = 1
CONFIG1	Ground	ENA_PAUSE = 0	PHYADR[4] = 0	PHYADR[3] = 0
CONFIG2	V _{cc} 2.5 V	ANEG[3] = 1	ANEG[2] = 1	ANEG[1] = 1
CONFIG3	V _{cc} 2.5 V	ANEG[0] = 1	ENA_XC = 1	DIS_125 = 1
CONFIG4	V _{cc} 2.5 V or LED_DUPLEX	HCWCFG_MODE [2] = 0 or 1	HCWCFG_MODE [1] = 1	HCWCFG_MODE [0] = 1
CONFIG5	V _{cc} 2.5 V	DIS_FC = 1	DIS_SLEEP = 1	HCWCFG_MODE [3] = 1
CONFIG6	LED_RX	SEL_BDT = 0	INT_POL = 1	50/75 ohm = 0 (50 ohm termination)

Table 1-5: Ethernet Interface Pin Assignments

FPGA Pin	Description	FPGA Pin	Description
AB13	PHY_COL	AA14	PHY_RX_CLK
AC10	PHY_CRS	AC13	PHY_RX_ER
AC6	PHY_INT	AE17	PHY_TXCTL_TXEN
AE4	PHY_MDC	W13	PHY_TXC_GTXCLK
AD6	PHY_MDIO	V12	PHY_TXD_0
AE9	PHY_RESET_N	AB9	PHY_TXD_1
AC17	PHY_RXCTL_RXDV	W12	PHY_TXD_2
AF17	PHY_RXD_0	AC9	PHY_TXD_3
AD9	PHY_RXD_1	AA12	PHY_TXD_4

Table 1-5: Ethernet Interface Pin Assignments (Cont'd)

FPGA Pin	Description	FPGA Pin	Description
AD12	PHY_RXD_2	AF9	PHY_TXD_5
AD16	PHY_RXD_3	AE8	PHY_TXD_6
AD10	PHY_RXD_4	AF8	PHY_TXD_7
AC22	PHY_RXD_5	Y14	PHY_TX_CLK
AF22	PHY_RXD_6	V13	PHY_TX_ER
AF15	PHY_RXD_7		

9. Ethernet Port

10Base-T, 100Base-TX, and 1000Base-T (Gigabit) Ethernet port. Connected to the Ethernet PHY (“8. Ethernet PHY”).

10. Flash Memory

Intel StrataFlash embedded memory JS28F256P30B95; provides the development board with 32-MB flash memory. This memory provides non-volatile storage for data, software, or bitstreams. The device is 16-bits wide. This flash memory can also be used to program the FPGA. To use the Flash and ZBT memories, the memory enable pin must be set in the FPGA. Table 1-6 identifies the pin assignment.

Note: The FMC module 1 cannot be used when using ZBT or flash memory. Make sure that the FMC adjustable power supply no. 1 is configured for 3.3V to use the ZBT or flash memory. See FMC expansion connector for information about how to configure the adjustable power supply. The Flash memory shares the same address/data bus as the ZBT synchronous SRAM (“12. ZBT Synchronous SRAM”).

Table 1-6: Memory Enable Pin Assignment

FPGA Pin	Signal	Description
R9	MEM_EN_B	0: memory is accessible 1: memory is not accessible

11. PS/2 Connectors

The Spartan-3A DSP 3400A Edition board is equipped with two PS/2 connectors, one each for a keyboard and mouse. Bi-directional level shifting transistors allow the 1.8-V I/O to interface with the 5-V I/O of the PS/2 connectors, which are powered directly from the 5-V power source of the development board. Connector J17 is used to connect a mouse, and connector J14 is used to connect a keyboard. Table 1-7 identifies the pin assignments.

Note: Be sure that the power load of the connected PS/2 devices does not overload the AC adapter of the development board.

Table 1-7: PS/2 Pin Assignments

FPGA Pin	Description
R17	KEYBOARD_CLK
R18	KEYBOARD_DATA
H21	MOUSE_CLK
J21	MOUSE_DATA

12. ZBT Synchronous SRAM

ISSI IS61NLP25636A-200TQL. The ZBT synchronous SRAM is high-speed, low-latency external memory for the FPGA. The memory is organized as 256K × 36 bits, providing a 32-bit data bus supporting four parity bits. The ZBT synchronous SRAM shares the same data bus as the flash memory (“10. Flash Memory”).

Note: FMC module #1 cannot be used when using ZBT synchronous SRAM. Make sure that FMC #1 adjustable power supply is configured for 3.3V to use the memory. See “14. FMC Expansion Connector #1” for information about configuring the adjustable power supply.

13. Soft Touch Connector

The Soft Touch connector (J12) lets you monitor signals between the FPGA and the FMC expansion connector #1. Table 1-8 defines the pin assignments.

Table 1-8: Soft Touch Connector Pin Assignments

Soft Touch Pin	FPGA Pin	Description
A1	H2	FMC_LA03_P
A2	H1	FMC_LA03_N
A3	NC	GND
A4	J5	FMC_LA14_P
A5	J4	FMC_LA14_N
A6	NC	GND
A7	L4	FMC_LA06_P
A8	L3	FMC_LA06_N
A9	NC	GND
A10	P8	FMC_LA32_P
A11	P9	FMC_LA32_N
A12	NC	GND
A13	U1	FMC_LA28_P
A14	U2	FMC_LA28_N

Table 1-8: Soft Touch Connector Pin Assignments (Cont'd)

Soft Touch Pin	FPGA Pin	Description
A15	NC	GND
A16	M10	FMC_LA21_P
A17	M9	FMC_LA21_N
A18	NC	GND
A19	T5	FMC_LA27_P
A20	U4	FMC_LA27_N
A21	NC	GND
A22	P7	FMC_LA25_P
A23	P6	FMC_LA25_N
A24	NC	GND
A25	U5	FMC_LA31_P
A26	V5	FMC_LA31_N
A27	NC	GND
B1	NC	GND
B2	M8	FMC_LA08_P
B3	M7	FMC_LA08_N
B4	NC	GND
B5	K3	FMC_LA18_P
B6	K2	FMC_LA18_N
B7	NC	GND
B8	K5	FMC_LA10_P
B9	K4	FMC_LA10_N
B10	NC	GND
B11	P4	FMC_LA00_P_CC
B12	P3	FMC_LA00_N_CC
B13	NC	GND
B14	R8	FMC_LA30_P
B15	R7	FMC_LA30_N
B16	NC	GND
B17	K6	FMC_LA24_P
B18	L7	FMC_LA24_N
B19	NC	GND
B20	V1	FMC_LA19_P

Table 1-8: Soft Touch Connector Pin Assignments (Cont'd)

Soft Touch Pin	FPGA Pin	Description
B21	V2	FMC_LA19_N
B22	NC	GND
B23	R5	FMC_LA29_P
B24	R6	FMC_LA29_N
B25	NC	GND
B26	T10	FMC_LA33_P
B27	T9	FMC_LA33_N

14. FMC Expansion Connector #1

Samtec ASP-134603-01. The FMC expansion connector #1 (J13) follows the VITA 57.1 FMC standard and is used in low pin count (LPC) format. It can either be used to accommodate a single width FMC Module or one dual FMC Module when used in conjuncture with FMC expansion connector #2 (J19). See FMC expansion connector for details. To use the Flash and ZBT memories, the memory enable pin needs to be set in the FPGA (see Table 1-6). Table 1-9 defines the FMC Expansion Connector #1 pin assignments.

Note: The Flash memory and ZBT synchronous SRAM cannot be used when using FMC module #1. The FMC connector #1 has its own adjustable power supply to provide the appropriate voltage to the FPGA bank used to communicate with the FMC module. Be sure that the FMC adjustable power supply is configured for the voltage specified by the FMC module. See FMC expansion connector for instructions about how to configure the adjustable power supplies.

Table 1-9: FMC #1 Expansion Connector Pin Assignments (1)

FMC Pin	FPGA Pin	Signal	FMC Pin	FPGA Pin	Signal
C1	NC	GND	D1	M2	PGC2M
C2	NC	DP0C2MP	D2	NC	GND
C3	NC	DP0C2MN	D3	NC	GND
C4	NC	GND	D4	NC	GBTCLK0M2CP
C5	NC	GND	D5	NC	GBTCLK0M2CN
C6	NC	DP0M2CP	D6	NC	GND
C7	NC	DP0M2CN	D7	NC	GND
C8	NC	GND	D8	P1	0_LA01_P_CC
C9	NC	GND	D9	P2	0_LA01_N_CC
C10	L4	0_LA06_P	D10	NC	GND
C11	L3	0_LA06_N	D11	D3	0_LA05_P
C12	NC	GND	D12	E4	0_LA05_N
C13	NC	GND	D13	NC	GND

Table 1-9: FMC #1 Expansion Connector Pin Assignments (1) (Cont'd)

FMC Pin	FPGA Pin	Signal	FMC Pin	FPGA Pin	Signal
C14	K5	0_LA10_P	D14	E3	0_LA09_P
C15	K4	0_LA10_N	D15	F4	0_LA09_N
C16	NC	GND	D16	NC	GND
C17	NC	GND	D17	K7	0_LA13_P
C18	J5	0_LA14_P	D18	J6	0_LA13_N
C19	J4	0_LA14_N	D19	NC	GND
C20	NC	GND	D20	N9	0_LA17_P_CC
C21	NC	GND	D21	P10	0_LA17_N_CC
C22	K3	0_LA18_P	D22	NC	GND
C23	K2	0_LA18_N	D23	N5	0_LA23_P
C24	NC	GND	D24	N4	0_LA23_N
C25	NC	GND	D25	NC	GND
C26	T5	0_LA27_P	D26	N1	0_LA26_P
C27	U4	0_LA27_N	D27	N2	0_LA26_N
C28	NC	GND	D28	NC	GND
C29	NC	GND	D29	A25	TCK
C30	AF23 ⁽¹⁾	SCL	D30	E23	TDI
C31	AE25 ⁽¹⁾	SDA	D31	NC	TDO
C32	NC	GND	D32	NC	3P3VAUX
C33	NC	GND	D33	D4	TMS
C34	NC	GA0 (ground)	D34	NC	TRSTL
C35	NC	12P0V	D35	NC	GA1 (GND)
C36	NC	GND	D36	NC	3P3V
C37	NC	12P0V	D37	NC	GND
C38	NC	GND	D38	NC	3P3V
C39	NC	3P3V	D39	NC	GND
C40	NC	GND	D40	NC	3P3V

1. I²C bus connected to FPGA through I²C mux (U1). Mux needs to be configured for the proper channel

Table 1-10: FMC #1 Expansion Connector Pin Assignments (2)

FMC Pin	FPGA Pin	Signal	FMC Pin	FPGA Pin	Signal
G1	NC	GND	H1	NC	VREFAM2C
G2	T3	0_CLK0_C2M_P	H2	G1	PRSNTM2CL
G3	T4	0_CLK0_C2M_N	H3	NC	GND
G4	NC	GND	H4	N6	0_CLK0_M2C_P
G5	NC	GND	H5	N7	0_CLK0_M2C_N
G6	P4	0_LA00_P_CC	H6	NC	GND
G7	P3	0_LA00_N_CC	H7	F5	0_LA02_P
G8	NC	GND	H8	G4	0_LA02_N
G9	H2	0_LA03_P	H9	NC	GND
G10	H1	0_LA03_N	H10	B2	0_LA04_P
G11	NC	GND	H11	B1	0_LA04_N
G12	M8	0_LA08_P	H12	NC	GND
G13	M7	0_LA08_N	H13	E1	0_LA07_P
G14	NC	GND	H14	F2	0_LA07_N
G15	J7	0_LA12_P	H15	NC	GND
G16	H6	0_LA12_N	H16	J8	0_LA11_P
G17	NC	GND	H17	J9	0_LA11_N
G18	K9	0_LA16_P	H18	NC	GND
G19	K8	0_LA16_N	H19	G3	0_LA15_P
G20	NC	GND	H20	F3	0_LA15_N
G21	M4	0_LA20_P	H21	NC	GND
G22	M3	0_LA20_N	H22	V1	0_LA19_P
G23	NC	GND	H23	V2	0_LA19_N
G24	G6	0_LA22_P	H24	NC	GND
G25	H7	0_LA22_N	H25	M10	0_LA21_P
G26	NC	GND	H26	M9	0_LA21_N
G27	P7	0_LA25_P	H27	NC	GND
G28	P6	0_LA25_N	H28	K6	0_LA24_P
G29	NC	GND	H29	L7	0_LA24_N
G30	R5	0_LA29_P	H30	NC	GND
G31	R6	0_LA29_N	H31	U1	0_LA28_P
G32	NC	GND	H32	U2	0_LA28_N
G33	U5	0_LA31_P	H33	NC	GND

Table 1-10: FMC #1 Expansion Connector Pin Assignments (2) (Cont'd)

FMC Pin	FPGA Pin	Signal	FMC Pin	FPGA Pin	Signal
G34	V5	0_LA31_N	H34	R8	0_LA30_P
G35	NC	GND	H35	R7	0_LA30_N
G36	T10	0_LA33_P	H36	NC	GND
G37	T9	0_LA33_N	H37	P8	0_LA32_P
G38	NC	GND	H38	P9	0_LA32_N
G39	NC	VADJ	H39	NC	GND
G40	NC	GND	H40	NC	VADJ

15. Power Supply Devices

The power supply circuitry of the Spartan-3A DSP 3400A Edition board generates 0.9V, 1.2V, 1.8V, 2.5V, 3.3V, and 12V, as well as two adjustable voltages to power the components of the board. The 1.2V (PS3), 1.8V (PS5), 2.5V (PS2), 3.3V (PS4), FMC #1 adjustable (PS1) and FMC #2 adjustable (PS6) supplies are driven by Linear Technology LTM4601 switching power regulators. The regulators are driven by a 620-kHz clock, making them run synchronously and reducing noise caused by beat frequencies. The clocks sent to each regulator are out of phase to reduce reflected noise at the input.

The adjustable devices are user configurable through the FPGA and are used for the VCCIO of the FPGA banks connected to the FMC expansion connectors. When no FMC expansion module is present, the output voltage of PS1 should be set to 3.3V with the I²C bus interface to configure the digital potentiometer (U23). See [“I²C Bus Addressing”](#) for detailed information.

[Figure 1-3](#) illustrates the power supply architecture and maximum current handling by each supply. The typical operating currents are significantly below the maximum capacity. The power supply delivered with the Spartan-3A DSP 3400A Edition board is generally suitable for most applications.

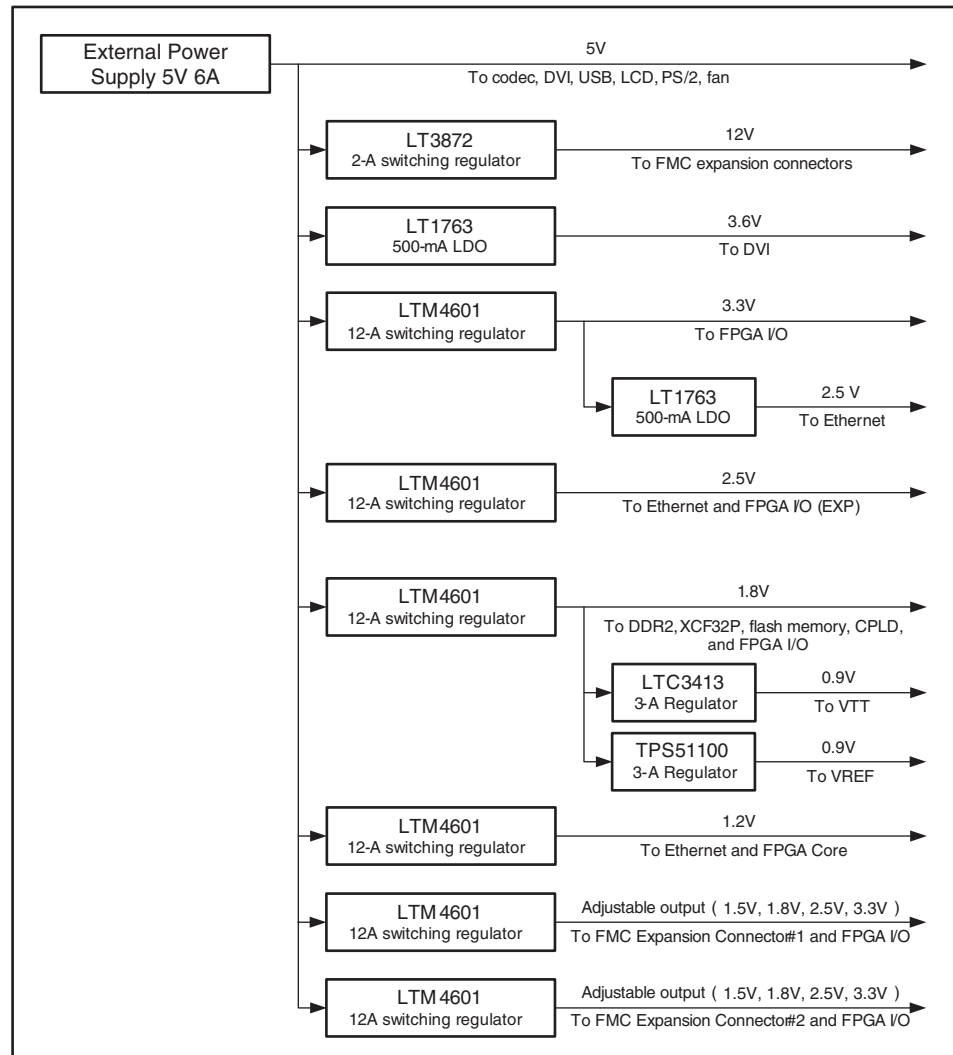


Figure 1-3: Spartan-3A DSP 3400A Edition Board Power Supply

16. FMC Expansion Connector #2

Samtec ASP-134603-01. The FMC expansion connector #2 (J19) follows the VITA 57.1 FMC standard and is used in low pin count (LPC) format. It can either be used to accommodate a single width FMC Module or one dual FMC Module when used in conjuncture with FMC expansion connector #1 (J13). See [“FMC Expansion Connectors”](#) for detailed information.

Note: The FMC connector #2 has its own adjustable power supply to provide the appropriate voltage to the FPGA bank used to communicate with the FMC module. Make sure that the FMC adjustable power supply is configured for the voltage specified by the FMC module. See [“FMC Expansion Connectors”](#) for instructions about how to properly configure the adjustable power supplies.

Table 1-11: FMC #2 Expansion Connector Pin Assignments (1)

FMC Pin	FPGA Pin	Signal	FMC Pin	FPGA Pin	Signal
C1	NC	GND	D1	M2	PGC2M
C2	NC	DP0C2MP	D2	NC	GND
C3	NC	DP0C2MN	D3	NC	GND
C4	NC	GND	D4	NC	GBTCLK0M2CP
C5	NC	GND	D5	NC	GBTCLK0M2CN
C6	NC	DP0M2CP	D6	NC	GND
C7	NC	DP0M2CN	D7	NC	GND
C8	NC	GND	D8	K14	1_LA01_P_CC
C9	NC	GND	D9	J14	1_LA01_N_CC
C10	D22	1_LA06_P	D10	NC	GND
C11	C22	1_LA06_N	D11	C21	1_LA05_P
C12	NC	GND	D12	B21	1_LA05_N
C13	NC	GND	D13	NC	GND
C14	D17	1_LA10_P	D14	B7	1_LA09_P
C15	C16	1_LA10_N	D15	C7	1_LA09_N
C16	NC	GND	D16	NC	GND
C17	NC	GND	D17	E14	1_LA13_P
C18	C5	1_LA14_P	D18	F14	1_LA13_N
C19	D6	1_LA14_N	D19	NC	GND
C20	NC	GND	D20	F13	1_LA17_P_CC
C21	NC	GND	D21	G13	1_LA17_N_CC
C22	B19	1_LA18_P	D22	NC	GND
C23	A19	1_LA18_N	D23	B15	1_LA23_P
C24	NC	GND	D24	A15	1_LA23_N
C25	NC	GND	D25	NC	GND
C26	G10	1_LA27_P	D26	A9	1_LA26_P
C27	H10	1_LA27_N	D27	B9	1_LA26_N
C28	NC	GND	D28	NC	GND
C29	NC	GND	D29	A25	TCK
C30	AF23*	SCL	D30	E23	TDI
C31	AE25*	SDA	D31	NC	TDO
C32	NC	GND	D32	NC	3P3VAUX
C33	NC	GND	D33	D4	TMS

Table 1-11: FMC #2 Expansion Connector Pin Assignments (1) (Cont'd)

FMC Pin	FPGA Pin	Signal	FMC Pin	FPGA Pin	Signal
C34	NC	GA0 (3P3V)	D34	NC	TRSTL
C35	NC	12P0V	D35	NC	GA1 (GND)
C36	NC	GND	D36	NC	3P3V
C37	NC	12P0V	D37	NC	GND
C38	NC	GND	D38	NC	3P3V
C39	NC	3P3V	D39	NC	GND
C40	NC	GND	D40	NC	3P3V

Table 1-12: FMC #2 Expansion Connector Pin Assignments (2)

FMC Pin	FPGA Pin	Signal	FMC Pin	FPGA Pin	Signal
G1	NC	GND	H1	NC	VREFAM2C
G2	A12	1_CLK0_C2M_P	H2	A13	PRSNM2CL
G3	B12	1_CLK0_C2M_P	H3	NC	GND
G4	NC	GND	H4	B13	1_CLK0_M2C_P
G5	NC	GND	H5	C13	1_CLK0_M2C_N
G6	B14	1_LA00_P_CC	H6	NC	GND
G7	A14	1_LA00_N_CC	H7	D23	1_LA02_P
G8	NC	GND	H8	C23	1_LA02_N
G9	B23	1_LA03_P	H9	NC	GND
G10	A22	1_LA03_N	H10	D20	1_LA04_P
G11	NC	GND	H11	C20	1_LA04_N
G12	E21	1_LA08_P	H12	NC	GND
G13	D21	1_LA08_N	H13	C17	1_LA07_P
G14	NC	GND	H14	B17	1_LA07_N
G15	C10	1_LA12_P	H15	NC	GND
G16	D10	1_LA12_N	H16	D18	1_LA11_P
G17	NC	GND	H17	C18	1_LA11_N
G18	G12	1_LA16_P	H18	NC	GND
G19	H12	1_LA16_N	H19	G20	1_LA15_P
G20	NC	GND	H20	F20	1_LA15_N
G21	F17	1_LA20_P	H21	NC	GND
G22	E17	1_LA20_N	H22	G15	1_LA19_P
G23	NC	GND	H23	H15	1_LA19_N

Table 1-12: FMC #2 Expansion Connector Pin Assignments (2) (Cont'd)

FMC Pin	FPGA Pin	Signal	FMC Pin	FPGA Pin	Signal
G24	E10	1_LA22_P	H24	NC	GND
G25	D9	1_LA22_N	H25	D16	1_LA21_P
G26	NC	GND	H26	C15	1_LA21_N
G27	A8	1_LA25_P	H27	NC	GND
G28	B8	1_LA25_N	H28	H17	1_LA24_P
G29	NC	GND	H29	G17	1_LA24_N
G30	J12	1_LA29_P	H30	NC	GND
G31	K12	1_LA29_N	H31	J16	1_LA28_P
G32	NC	GND	H32	K16	1_LA28_N
G33	C8	1_LA31_P	H33	NC	GND
G34	D8	1_LA31_N	H34	J11	1_LA30_P
G35	NC	GND	H35	K11	1_LA30_N
G36	B6	1_LA33_P	H36	NC	GND
G37	C6	1_LA33_N	H37	A4	1_LA32_P
G38	NC	GND	H38	B4	1_LA32_N
G39	NC	VADJ	H39	NC	GND
G40	NC	GND	H40	NC	VADJ

17. General Reset Button

An active-low button used as a system or user reset.

Table 1-13: Reset Connection Pin Assignment

Button	FPGA Pin	Description
S11	Y16	PORESET

18. Power Switch

Lets you turn the Spartan-3A DSP 3400A Edition board on and off by controlling the 5V supply of the board.

19. Power Connector

Center positive, 2.1-mm × 5.5-mm barrel-type plug. Used to connect the supplied AC adaptor with an output of 5V DC.

20. Clock Generator

IDT IDT5V9885PFGI. Used to generate different clocks on the Spartan-3A DSP 3400A Edition board. [Table 1-14](#) summarizes the default settings of output clocks. The clock generator can be programmed through the I²C interface (see [“I²C Bus Addressing,”](#) [page 42](#)) or through a JTAG interface using connector P2 (see [Chapter 3](#), [“Programming the IDT Clock Chip”](#) for information).

Table 1-14: Clock Generator Default Settings

Clock Generator Output	FPGA Pin (if Connected to FPGA)	Default Frequency	Clock Usage
1	NA	25 MHz	Ethernet PHY clock
2	NA	14.31818 MHz	Audio codec clock
3	NA	12 MHz	USB clock
4_P	NA	31.25 MHz	System ACE clock
4_N	AE13	31.25 MHz	FPGA clock
5_P	AA13	125 MHz	FPGA LVDS differential clock P
5_N	Y13	125 MHz	FPGA LVDS differential clock N
6	AF13	27 MHz	FPGA clock

21. 64-Kb I²C EEPROM

The I²C EEPROM 24LC64 can be used to store non-volatile data, for example, an Ethernet MAC address. The EEPROM is accessible through the I²C bus (see [“I²C Bus Addressing”](#)). The EEPROM write-protect is disabled on the board. I²C bus pull-up resistors are provided on the board.

The I²C bus is extended to the FMC expansion connector so that the board can access additional I²C devices and share the I²C controller in the FPGA.

Table 1-15: I²C FPGA Pin Assignments

I ² C Signal	FPGA Pin	Description
IIC_SCLK	AF23 ⁽¹⁾	I ² C clock
IIC_SDAT	AE25 ⁽¹⁾	I ² C data

1. I²C bus connected to FPGA through I²C MUX (U1). MUX needs to be configured for the proper channel.

22. I²C Fan Controller and Temperature/voltage Monitor

Onboard temperature and voltage monitoring and control are handled by an Analog Devices ADT7476A device. This device is controlled through I²C ([“I²C Bus Addressing”](#)) and do the following:

- ♦ Measure the voltage of the 5-V, 3.3-V, 1.8-V, and 1.0-V supplies
- ♦ Measure the FPGA temperature through the DXP/DXN pins on the FPGA
- ♦ Measure ambient temperature
- ♦ Read power good status signals from the 2.5-V linear regulators

- ◆ Provide PWM control of the fan speed
- ◆ Provide fan tachometer readings
- ◆ Generate interrupts/alarms based on readings

Connector P3 is a keyed three-pin fan header similar to the ones in computers. It is designed to support a 5V DC fan. To bypass the fan controller device and operate the fan at full speed, you can use connector JP9.

Under high-power operating conditions, a heat sink and/or fan for the FPGA can be accommodated on the board (for example, Calgreg Electronics Smart-CLIP family of heat sink/fan assemblies). The Spartan-3A DSP 3400A Edition board does not come with a heat sink and/or fan.

Table 1-16: FPGA Fan Controller Interface

Signal	FPGA Pin	Description
FAN_ALERT	T17	Interrupt to signal out-of-limit conditions.

23. Program and Reset Buttons

Button S10 forces the FPGA to be reprogrammed; button S9 forces the System ACE to reset.

24. FPGA

XC3SD3400A-4FGG676C Xilinx Spartan-3A DSP FPGA. The board supports configuration in several modes: JTAG, master serial, slave serial, master SelectMAP, slave SelectMAP, byte-wide peripheral interface (BPI) up, BPI down, and SPI modes. See [Chapter 2, “Configuration Options.”](#)

The FPGA is also equipped with four I/O banks. [Table 1-17](#) defines the I/O voltage applied to each bank.

Table 1-17: FPGA I/O Bank Voltage Rail

FPGA Bank	I/O Voltage Rail
0	FMC expansion connector #2 adjustable (1.5V, 1.8V, 2.5V, or 3.3V)
1	1.8V
2	3.3V
3	FMC expansion connector #1 adjustable (1.5V, 1.8V, 2.5V, or 3.3V)

25. JTAG Header

The JTAG header (P5) allows programming devices and troubleshooting the FPGA. The JTAG port supports the Xilinx Parallel Cable III, Parallel Cable IV, or Platform USB cable products. (Third-party configuration products may also be available.) The JTAG chain can also be extended to the FMC expansion module when it is present. See [Chapter 2, “Configuration Options.”](#)

26. LCD

Hantronix HDM16216L-2-L30S, 16-character × 2-line resolution LCD to display text information. The data interface to the LCD is connected to the FPGA and supports only the 4-bit mode. Onboard level shifters are used to shift the voltage level between the FPGA and the LCD. The LCD is equipped with a connector that allows the LCD to be removed from the development board to gain access to the components below. Turning the potentiometer located below the LCD with a screwdriver allows you to adjust the image contrast of the LCD. The LCD is equipped with a backlight that can be turned off by removing jumper JP10.

Table 1-18: FPGA LCD Interface

Signal	FPGA Pin
LCD_DB_4	G21
LCD_DB_5	R19
LCD_DB_6	D25
LCD_DB_7	D24
LCD_E	J20
LCD_RS	H20
LCD_RW	J19

27. User-defined Buttons

The functions of the five user-defined buttons are determined by the designer; all the buttons are directly connected to the FPGA.

Table 1-19: User-defined Button FPGA Pin Assignments

Button No.	FPGA Pin	Description
S4	N25	GPIO_SW_NORTH
S5	N26	GPIO_SW_WEST
S6	Y26	GPIO_SW_CENTER
S7	N23	GPIO_SW_EAST
S8	P21	GPIO_SW_SOUTH

28. RS232 Serial Port

This DB9 male connector allows the FPGA to communicate serial data to another device. The port is wired as a host device (DCE) and configured to operate at up to 115200 bauds. For this reason, a null modem cable is normally required to connect the board to the serial port on a computer. An interface device is used to shift the voltage level between FPGA and RS232 signals.

Note: The FPGA is only connected to the TX and RX data pins of the serial port. As such, other RS232 signals such as hardware flow-control signals are not used. For this reason, flow control should be disabled when communicating with a computer.

Table 1-20: Serial Port FPGA Pin Assignments

DB9 Pin	FPGA Pin	Description
2	V14	TX
3	AA20	RX

29. SPDIF Output Connectors

The SPDIF connector J20 is used to output digital audio output.

30. Configuration Jumpers

Ten configuration jumpers are present on the Spartan-3A DSP 3400A Edition board.

[Table 1-21](#) defines how to use the configuration jumpers.

Table 1-21: Configuration Jumpers

Jumper	Function	On	Off
JP1	Prevents the USB controller from running the firmware in the I ² C EEPROM.	1-2: Does not run the firmware from I ² C EEPROM	Runs the firmware from the I ² C EEPROM (default).
JP2	Ethernet modes	1-2: GMII (default) 2-3: RGMII	N/A
JP5	FMC #1 I/O bank voltage selection	Voltage present a FPGA and at FMC Connector J13 (default)	No voltage present a FPGA and at FMC Connector J13
JP6	Clock generator programming mode	JTAG programming (default)	I ² C programming
JP7/ JP8	System ACE failsafe mode	Failsafe mode enabled when both jumpers are populated	Failsafe mode disabled when both jumpers are unpopulated
JP9	Fan controller bypass	Fan controller bypassed	Fan controller is not bypassed (default)
JP10	LCD backlight control	Backlight is on (default)	Backlight is off
JP11	FMC #2 I/O bank voltage selection	Voltage present a FPGA and at FMC Connector J19 (default)	No voltage present a FPGA and at FMC Connector J19

31. User-defined DIP Switches

Eight general-purpose, active-high DIP switches (S3) are connected to the user I/O pins of the FPGA.

Table 1-22: User-defined DIP Switch FPGA Pin Assignments

Switch No.	FPGA Pin	Description
1	R26	FPGA_DIP_SW0
2	R25	FPGA_DIP_SW1
3	T23	FPGA_DIP_SW2
4	R24	FPGA_DIP_SW3
5	T18	FPGA_DIP_SW4
6	R22	FPGA_DIP_SW5
7	R21	FPGA_DIP_SW6
8	R20	FPGA_DIP_SW7

32. User-defined LEDs

Eight general-purpose, active-high LEDs (DS10-DS17) are connected to the user I/O pins of the FPGA.

Table 1-23: User-defined LED FPGA Pin Assignments

LED No.	FPGA Pin	Description
1 (DS10)	W23	GPIO_LED_0
2 (DS11)	V22	GPIO_LED_1
3 (DS12)	V25	GPIO_LED_2
4 (DS13)	V24	GPIO_LED_3
5 (DS14)	V23	GPIO_LED_4
6 (DS15)	U23	GPIO_LED_5
7 (DS16)	U22	GPIO_LED_6
8 (DS17)	T24	GPIO_LED_7
BUS_ERROR_1 (DS22)	C26	BUS ERROR LED 1
BUS_ERROR_2 (DS23)	Y24	BUS ERROR LED 2

33. Configuration DIP Switches

Eight configuration DIP switches (S2) allow you to configure the System ACE configuration address and the FPGA configuration mode, as well as to enable the fallback configuration of the board's System ACE configuration.

Table 1-24: Configuration DIP Switch Functions

Switch No.	Function	On Position	Off Position
8	System ACE Config address [2]	0	1
7	System ACE Config address [1]	0	1
6	System ACE Config address [0]	0	1
5	Config Mode [2] (see Table 1-25)		
0	1		
4	Config Mode [1] (see Table 1-25)		
0	1		
3	Config Mode [0] (see Table 1-25)		
0	1		
2	Board flash memory fallback	0 (Disabled)	1 (Enabled)
1	System ACE configuration When the System ACE configuration is enabled, the System ACE controller (on the bottom of the board) configures the FPGA from the CompactFlash card reader (on the bottom of the board) whenever a CompactFlash card is inserted in the reader or the Reset ACE button is depressed.	0 (Disabled)	1 (Enabled)

Table 1-25: Configuration Modes

Configuration Mode	Configuration Source	Mode [2]	Mode [1]	Mode [0]
MASTER SERIAL	CONFIG FROM XCF32P FLASH	0	0	0
MASTER SPI	CONFIG FROM SPI EEPROM	0	0	1
MASTER BPI-UP	NOT SUPPORTED	0	1	0
MASTER BPI-DOWN	NOT SUPPORTED	0	1	1
MASTER SELECTMAP	CONFIG FROM XCF32P FLASH	1	0	0
JTAG	CONFIG FROM SYSTEMACE	1	0	1

Table 1-25: Configuration Modes (Cont'd)

Configuration Mode	Configuration Source	Mode [2]	Mode [1]	Mode [0]
SLAVE SELECTMAP	CONFIG FROM XCF32P FLASH	1	1	0
SLAVE SERIAL	CONFIG FROM XCF32P FLASH	1	1	1

34. CPLD

Xilinx XC2C64A CoolRunner-II. This device is designed for high-performance and low-power applications. The CPLD is used to configure the Spartan-3A DSP 3400A Edition board and to provide statuses through the status LEDs (below).

35. Status LEDs

The status LEDs are driven by the CPLD to provide statuses on the Spartan-3A DSP 3400A Edition board.

Table 1-26: Status LED Signals

LED	Signal	Description
DS6	DONE	Status of the FPGA DONE signal
DS7	INIT	Status of the FPGA INIT signal
DS8	EXTRA_LED_2	Not used
DS9	EXTRA_LED_1	Not used

36. Audio Input Output Connectors

Microphone, line in, line out, and headphones connectors. All connectors are stereo with the exception of the microphone connector.

Table 1-27: Audio Connectors

Connector	Function
J8	Microphone - In
J9	Analog line - In
J10	Analog line - Out
J11	Headphones - Out
J20	S/PDIF - Out (see no. 29)

Board Parts: Bottom

Figure 1-4 displays the parts on the bottom of the Spartan-3A DSP 3400A Edition board. Each numbered item in the diagram is followed by a numbered description.

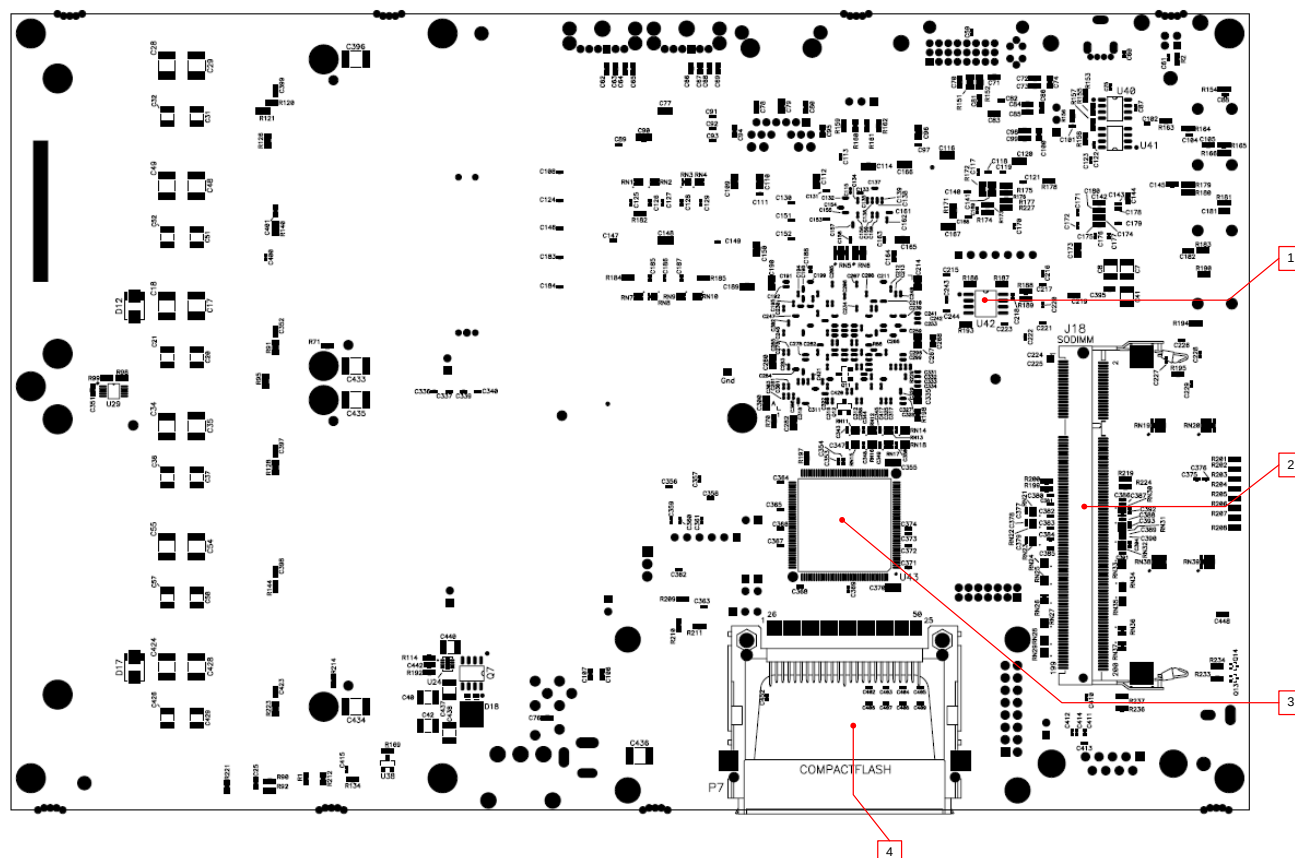


Figure 1-4: Bottom View of Spartan-3A DSP 3400A Edition Board

1. SPI EEPROM

ST Microelectronics M25P16 16-Mb SPI EEPROM. The device can be used to configure the FPGA or to hold user data. See [Chapter 2, “Configuration Options”](#) for detailed information.

2. DDR2 SDRAM

The Spartan-3A DSP 3400A Edition board is equipped with a single-rank, unregistered 512-MB DDR2 SDRAM. The DDR2 SDRAM is usually a Micron MT8HTF6464HY-53E or similar. Serial presence detection (SPD) through an I²C interface to the memory is also supported by the FPGA. See DDR2 memory for details. [Table 1-28](#) identifies the FPGA pin assignments used for the DDR2 interface.

Notes:

- Only half the available memory of the DDR2 SDRAM (that is, 256 MB) is available because of certain limitations.
- The Spartan-3A DSP 3400A Edition board is only tested for DDR2 SDRAM operation at a data rate of 266 MHz (133 MHz clock rate). Using faster data rates is possible, but they are untested and not guaranteed.

Table 1-28: FPGA DDR2 Interface Pin Assignments

FPGA Pin	Description	FPGA Pin	Description
AA25	DDR2_A_0	N24	DDR2_0_DQ_0
AA22	DDR2_A_1	M26	DDR2_0_DQ_1
AB26	DDR2_A_2	M25	DDR2_0_DQ_2
Y21	DDR2_A_3	P23	DDR2_0_DQ_3
AC24	DDR2_A_4	N21	DDR2_0_DQ_4
AA24	DDR2_A_5	P22	DDR2_0_DQ_5
AD26	DDR2_A_6	P20	DDR2_0_DQ_6
AE26	DDR2_A_7	P26	DDR2_0_DQ_7
AB23	DDR2_A_8	M20	DDR2_0_DQ_8
AC25	DDR2_A_9	L24	DDR2_0_DQ_9
W21	DDR2_A_10	J25	DDR2_0_DQ_10
AD25	DDR2_A_11	J26	DDR2_0_DQ_11
AC23	DDR2_A_12	N17	DDR2_0_DQ_12
V19	DDR2_A_13	N20	DDR2_0_DQ_13
V21	DDR2_0_BA_0	M23	DDR2_0_DQ_14
AA23	DDR2_0_BA_1	M21	DDR2_0_DQ_15
AC26	DDR2_0_BA_2	G24	DDR2_0_DQ_16
U20	DDR2_0_CAS_B	G23	DDR2_0_DQ_17
U18	DDR2_0_CK0_N	K22	DDR2_0_DQ_18
U19	DDR2_0_CK0_P	M19	DDR2_0_DQ_19
D26	DDR2_0_CK1_N	F24	DDR2_0_DQ_20
E26	DDR2_0_CK1_P	K23	DDR2_0_DQ_21
P25	DDR2_0_DM_0	K21	DDR2_0_DQ_22
N18	DDR2_0_DM_1	L22	DDR2_0_DQ_23
M22	DDR2_0_DM_2	F23	DDR2_0_DQ_24
M18	DDR2_0_DM_3	E24	DDR2_0_DQ_25
N19	DDR2_0_DQS0_N	K20	DDR2_0_DQ_26
P18	DDR2_0_DQS0_P	L20	DDR2_0_DQ_27
K26	DDR2_0_DQS1_N	G22	DDR2_0_DQ_28
K25	DDR2_0_DQS1_P	F25	DDR2_0_DQ_29
J22	DDR2_0_DQS2_N	K18	DDR2_0_DQ_30
J23	DDR2_0_DQS2_P	K19	DDR2_0_DQ_31
L17	DDR2_0_DQS3_N	C25	DDR2_LOOP_OUT

Table 1-28: **FPGA DDR2 Interface Pin Assignments (Cont'd)**

FPGA Pin	Description	FPGA Pin	Description
L18	DDR2_0_DQS3_P	H24	DDR2_LOOP_IN
Y22	DDR2_0_ODT_0	W20	DDR2_0_S0
U21	DDR2_0_ODT_1	V18	DDR2_0_S1
Y20	DDR2_0_RAS_B	T20	DDR2_0_WE_B
Y23	DDR2_0_CKE_0	Y25	DDR2_0_CKE_1

3. System ACE Controller

The Xilinx System ACE controller allows a type I CompactFlash card to program the FPGA through the JTAG port. The System ACE controller supports up to eight configuration images on a single CompactFlash card. The configuration address DIP switches (332 on the top of the board) allow you to select what configuration image to use.

System ACE error and status LEDs indicate the operational state of the System ACE controller:

- ◆ The DS19 LED blinks green to indicate that no CompactFlash card is present.
- ◆ The DS19 LED lights green to indicate an error during configuration.
- ◆ The DS18 LED blinks green to indicate an ongoing configuration operation.
- ◆ The DS18 LED lights green to indicate a successful download.

Every time that a CompactFlash card is inserted in the CompactFlash reader, a configuration operation is initiated. Pressing the System ACE reset button (S9) reprograms the FPGA.

The FPGA pins used for the USB interface are shared with the System ACE interface. See the FPGA pin assignments on Table 1.

Note: Configuration with the System ACE controller is enabled with the configuration DIP switches.

The board also features a System ACE failsafe mode. Under this mode, if the System ACE controller detects a failed configuration attempt, it automatically restarts under a predefined configuration image. The failsafe mode is enabled by inserting two jumpers across JP7 and JP8 (horizontally or vertically).

Caution: Exercise caution when handling a CompactFlash card in the vicinity of the board, as contact between the card's metallic parts and board components could create short-circuits.

The System ACE MPU port is connected to the FPGA. This connection allows the FPGA to use the System ACE controller to reconfigure the system or access the CompactFlash card as a generic FAT file system. The data bus for the System ACE MPU port is shared with the USB controller.

4. CompactFlash Reader

The CompactFlash reader is used as an interface point between the Spartan-3A DSP 3400A Edition board and a CompactFlash card. The CompactFlash card used is generally a Lexar Media 512-MB module.

FMC Expansion Connectors

The FMC expansion connectors (J13 and J19) follow the VITA 57.1 FMC standard (standard to be released at a later date) and are used in low-pin-count (LPC) format. The Spartan-3A DSP 3400A Edition board was designed with a preliminary version of the standard.

When an FMC mezzanine module is intended to be used, the FPGA should access the FMC mezzanine module's I²C EEPROM to read the board information. This information allows the FPGA to set the appropriate I/O voltages to the FPGA I/Os connected to the FMC expansion connector. The way the board information will be stored in the FMC mezzanine I²C EEPROM is not defined at this time. A work group is currently developing the Vita-57.2 standard. The standard should be released soon.

To set the appropriate voltage on the FMC connector, an I²C digital pot must be set to a specific value. The value should be written to the volatile register of the digital pot. This register is located at address 0x00 for FMC connector #1 and to address 0x01 for FMC connector #2. To write to the volatile section of the digital pot make sure that address 0x08 is set to 0x80.

Use the following steps to configure the digital pot to the appropriate voltages:

Vout = 1.5V

1. Configure register 0x8 to value 0x80
2. Configure register 0x0 (FMC #1) or 0x1 (FMC #2) to value 0x8A

Vout = 1.8V

1. Configure register 0x8 to value 0x80
2. Configure register 0x0 (FMC #1) or 0x1 (FMC #2) to value 0x57

Vout = 2.5V

1. Configure register 0x8 to value 0x80
2. Configure register 0x0 (FMC #1) or 0x1 (FMC #2) to value 0x1E

Vout = 3.3V

1. Configure register 0x8 to value 0x80
2. Configure register 0x0 (FMC #1) or 0x1 (FMC #2) to value 0x00

DDR2 Memory

DDR2 Memory Expansion

The SODIMM connector lets you install DDR2 SODIMM modules with more memory because higher order addresses and chip select signals are also routed from the SODIMM connector to the FPGA. However, a permanent limitation is that only the first 32 bits of data are routed to the FPGA, as shown in [Table 1-28](#).

DDR2 Clock Signal

Two matched-length pairs of DDR2 clock signals are broadcast from the FPGA to the SODIMM connector. The FPGA design is responsible for driving the two clock pairs at a low skew. The delay on the clock traces is designed to match the delay of the other DDR2 control signals.

DDR2 Signaling

All DDR2 control signals are terminated through 47- Ω resistors to a 0.9-V VTT reference voltage. The DDR2 interface of the FPGA supports SSTL18 signaling and all the DDR2 signals are controlled impedances. The DDR2 data, mask, and strobe signals are of matched length within byte groups. On die termination (ODT) is available and better performance can be achieved when used by the memory controller.

MIG Compatibility

MIG can be used to generate a compatible design for the Spartan-3A DSP 3400A Edition board.

I²C Bus Addressing

The Spartan-3A DSP 3400A Edition board uses an I²C bus to interface different devices to the FPGA. Because of the large amount of devices having similar slave address, an I²C MUX (Philips PCA9544APW) is used to separate those devices from one to the other. [Table 1-29](#) defines the various slave addresses accessible by the FPGA through the I²C MUX output.

Note: To change the I²C MUX output you need to perform a write access to the I²C MUX (slave address 0xE4) with the following data: 0x04 for MUX 0, 0x05 for MUX 1, 0x06 for MUX 2 and 0x07 for MUX3. See the I²C MUX [data sheet](#) for detailed information.

Table 1-29: I²C Slave Device Addresses

I ² C MUX	Device	Slave Address	A7	A6	A5	A4	A3	A2	A1	A0
MUX 0	Fan controller	0x58	0	1	0	1	1	0	0	R/W
	I ² C EEPROM	0xA8	1	0	1	0	1	0	0	R/W
	I ² C MUX	0xE4	1	1	1	0	0	1	0	R/W
MUX 1	DDR2 SODIM EEPROM	0xA0	1	0	1	0	0	0	0	R/W
	Clock generator	0xD4	1	1	0	1	0	1	0	R/W
	I ² C MUX	0xE4	1	1	1	0	0	1	0	R/W
MUX 2	FMC #1 I ² C EEPROM	0xA0	1	0	1	0	0	0	0	R/W
	FMC #1 optional	0xX0/0xX8	X	X	X	X	X	0	0	R/W
	FMC #2 I ² C EEPROM	0xA2	1	0	1	0	0	0	0	R/W
	FMC #2 optional	0xX2/0xXA	X	X	X	X	X	0	1	R/W
	Digital pot (adj. power supply)	0xA4	1	0	1	0	0	1	0	R/W
	I ² C MUX	0xE4	1	1	1	0	0	1	0	R/W

Table 1-29: I²C Slave Device Addresses (Cont'd)

I ² C MUX	Device	Slave Address	A7	A6	A5	A4	A3	A2	A1	A0
MUX 3	DVI Monitor E-DDC	0x60	0	1	1	0	0	0	0	R/W
	DVI Monitor E-DDC	0x62	0	1	1	0	0	0	1	R/W
	DVI Monitor E-DDC/CI	0x6E	0	1	1	0	1	1	1	R/W
	DVI Monitor E-DDC	0xA0	1	0	1	0	0	0	0	R/W
	DVI Monitor DDC Display Dependent Devices	0xFF	1	1	1	1	X	X	X	R/W
	Video Encoder	0xEC	1	1	1	0	1	1	0	R/W
	I ² C MUX	0xE4	1	1	1	0	0	1	0	R/W

Configuration Options

This chapter provides an overview of the four ways the FPGA on the Spartan-3A DSP 3400A Edition board can be configured:

- Xilinx download cable (JTAG)
- System ACE controller (JTAG)
- Board flash memory
- SPI flash memory

JTAG Configuration

The FPGA, the board flash memory, and the CPLD can all be configured through the JTAG port of the Spartan-3A DSP 3400A Edition board, as illustrated in [Figure 2-1](#).

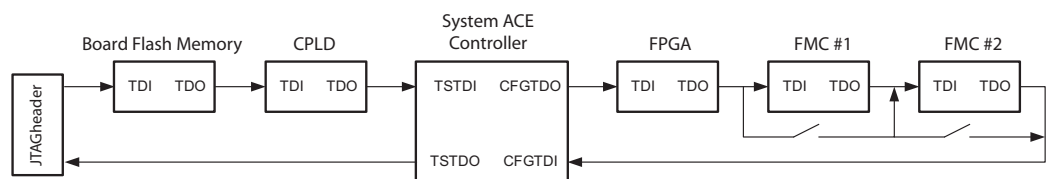


Figure 2-1: Spartan-3A DSP 3400A Edition Board JTAG Chain

JTAG Chain

The JTAG chain starts at the JTAG header (see [25. JTAG Header](#)) and goes through

- the System ACE controller
- the board flash memory
- the FPGA
- the CPLD
- the FMC expansion connector

The chain bypasses the FMC expansion connector if no expansion module is present. Jumper JP4 must not be populated for appropriate JTAG operation.

The JTAG chain can be used to program the FPGA and to access the FPGA for hardware and software troubleshooting. The JTAG header's connection to the JTAG chain allows a host computer to transfer bitstreams to the FPGA using iMPACT from Xilinx. The JTAG header also allows such troubleshooting tools as ChipScope Pro to access the FPGA.

System ACE Controller Configuration

The System ACE controller can program the FPGA through the JTAG port. By inserting a CompactFlash card in the CompactFlash reader (see [“33. Configuration DIP Switches,” page 36](#)), configuration information can be stored and programmed on the FPGA.

The System ACE controller supports up to eight configuration images that can be selected using the three configuration address DIP switches (see [“Spartan-3A DSP 3400A Edition Board Hardware,” page 16](#)). Under the control of the FPGA, the System ACE controller can be instructed use any of the eight configuration images.

The configuration mode should be set to 101 (ACE_CFGADDR0_IN (OFF), ACE_CFGADDR1_IN (ON), ACE_CFGADDR2_IN (OFF) and ACE_CFG_EN should be OFF to use System ACE configuration. See [“33. Configuration DIP Switches,” page 36](#) for information.

When set correctly, the System ACE controller programs the FPGA on power-up if a CompactFlash card is present or whenever a CompactFlash card is inserted. Pressing the System ACE reset button also causes the System ACE controller to program the FPGA if a CompactFlash card is present.

Board Flash Memory Configuration

The board flash memory can also be used to program the FPGA. This memory can hold up to two configuration images (or up to four with compression), selectable with the two least significant bits of the configuration address DIP switches. See [“Spartan-3A DSP 3400A Edition Board Hardware,” page 16](#) for information.

The board is designed so the board flash memory can download bitstreams under master serial, slave serial, master SelectMAP (parallel), or slave SelectMAP (parallel) modes. Using iMPACT to program the memory, you can select which of the four modes to use in programming the FPGA. The configuration mode DIP switches on the board must match the programming method used by the memory. See [“33. Configuration DIP Switches,” page 36](#) for information.

When correctly configured, the board flash memory programs the FPGA when the Spartan-3A DSP 3400A Edition board is turned on or whenever the program button is depressed. See [“23. Program and Reset Buttons,” page 32](#) for information.

SPI Flash Memory Configuration

Data stored in the SPI flash memory can be used to program the FPGA. The configuration mode DIP switches must be set to 0 0 1 to configure the FPGA from the SPI flash memory. See [“33. Configuration DIP Switches,” page 36](#) for information.

When correctly configured, the FPGA is programmed when the XtremeDSP Spartan-3A DSP Development Board is turned on or whenever the program button is depressed.

Programming the IDT Clock Chip

The XtremeDSP Development Platform - Spartan-3A DSP 3400A Edition evaluation board features an Integrated Device Technology (IDT) 3.3V EEPROM Programmable Clock Generator that is pre-programmed at the factory. In the event the chip programming is changed, the instructions in this appendix show how to return the clock chip to its factory default settings using the following equipment:

- Xilinx download cable
- JTAG flying wires

Downloading to the Spartan-3A DSP 3400A Edition Board

1. Connect a Xilinx download cable to the board using flying leads connected to jumper P2.

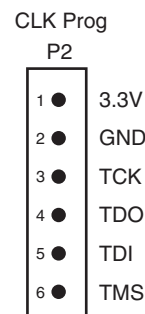


Figure 3-1: P2 IDT5V9885 JTAG Connector

2. From the Windows Start menu, choose iMPACT to open the main iMPACT window.
3. Click Boundary Scan; then right-click Add Xilinx Device.
4. Locate the SVF file (*s3adsp_clock_setup.svf*) as illustrated in [Figure 3-2](#) and click Open.

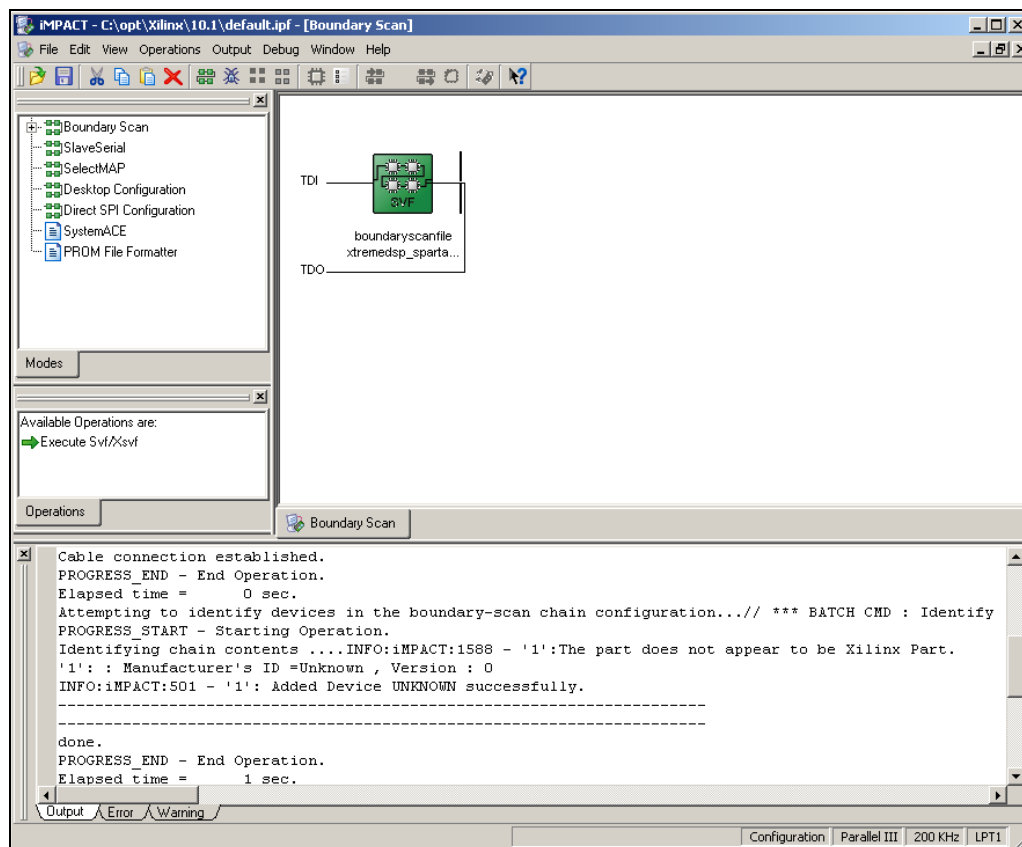


Figure 3-2: Programming the IDT5V9885 on the Spartan-3A DSP 3400A Edition Board Using iMPACT

5. Right-click the device and select Execute XSUF/SVF.
6. To finish programming the chip, cycle the power by turning off the board power switch.
7. After turning the board back on, verify that the clock frequencies are correct.

Technical Specifications

This appendix identifies the XtremeDSP Spartan-3A DSP Development Board technical specifications, which are subject to change without notice.

General Specifications

- **Mass:** 359.1 g
- **Length:** 254.0 mm
- **Width:** 165.1 mm
- **Height:** 40 mm (feet included)
- **Feet:** 15 mm
- **Operating temperature range:** 0°C to 70°C (non-condensing)
- **Storage temperature range:** -55°C to 150°C (non-condensing)

Maximum Power Consumption

The maximum power consumption is 6.84 W.

- The power consumption specifications were calculated with a production test bitstream
- The power consumptions outlined above can vary according to the FPGA load

FPGA

- **Model:** Xilinx Spartan-3A DSP, XC3SD3400A-4FGG676C
- **DSP Performance:** 32 GMACS
- **Maximum DSP frequency:** 250 MHz
- **Block RAM:** 2,268 Kb
- **Logic cells:** 53,712
- **Speed:** 213 × 622+ Mbps LVDS pairs

